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*Article*

# Optimization of Line-Tunneling Type L-Shaped Tunnel Field-Effect-Transistor for Steep Subthreshold Slope

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**Abstract:** Recently L-shaped tunneling field-effect-transistor (LTFET) has been introduced to overcome the thermal subthreshold limit of conventional metal-oxide-semiconductor field-effect-transistors (MOSFET). In this work, shortcoming of LTFET was investigated. It was found that corner effect present in LTFET effectively degrades its subthreshold slope. To get rid of corner effect a new type of device with dual material gates is presented. The new device termed as DG-LTFET gets rid of the corner effect and results in a significantly improved subthreshold slope of less than 10 mV/dec, and an improved ON/OFF current ratio over LTFET. In this work DG-LTFET was evaluated for different device parameters, and bench-marked against LTFET. This work presents an optimum configuration of DG-LTFET in terms of device dimensions and doping levels, to get the best subthreshold, ON current and ambipolar performance from the DG-LTFET.

**Keywords:** Band-to-band tunneling, L-shaped tunnel field-effect-transistor, double-gate tunnel field-effect-transistor, corner-effect.

## 1. Introduction

Tunnel field-effect-transistors (TFET) are being actively pursued as a potential replacement to conventional complementary metal-oxide-semiconductor (CMOS) technology [1]. TFETs offer sub-thermal subthreshold slope (SS) but suffer from limited ON current $I_{ON}$ performance [2]. To overcome the limit, recently different types of line tunneling type TFETs have been introduced including L-shaped TFET [3] (LTFET), U-shaped [4] (UTFET), and Z-shaped [5] TFET (ZTFET). Among them, only LTFET has been experimentally demonstrated [3].

It was found using device simulations that 2-dimenasional (2D) corner effect [6] present in LTFET degrades its subthreshold performance. In order to remove SS degradation due to the kink effect induced by the source corner, the fully depleted rounded corner with gradual doping profile was used [6]. LTFET still achieves sub-thermal SS but as shown in this work there is room for significant improvement in the subthreshold performance of LTFET. To achieve this improvement, a new device based on the original LTFET is introduced in this work. The new device uses a dual-gate (DG) structure, and is termed as DG-LTFET. The two gates (gate1 and gate2) have different workfunctions and different heights. DG-LTFET was thoroughly evaluated for different device parameters including the source region height, gate1 and gate2 heights, gate1 and gate2 workfunctions, channel thickness, and drain doping levels. Optimum dimensions and drain doping level were determined for the DG-LTFET. Section 2 briefly discusses the corner-effect problem of LTFET. Section 3 introduces DG-LTFET, and compares its results with LTFET. Section 4 presents conclusion.

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## 2. LTFET: Corner Effect

Fig. 1 shows a schematic for LTFET. The $p^+$ ($10^{20}$ $cm^{-3}$) doped source region overlaps the gate with the $n^-$ ($10^{12}$ $cm^{-3}$) channel sandwiched in between them. This sandwiched channel region is termed as $R_{nonoffset}$. Also, there is a part of the channel termed as $R_{offset}$ in which there is an offset present between the source and the gate as indicted in Fig. 1. The following parameters were used for all devices considered in this work unless otherwise specified. Source height ($H_s$) = 40 nm, oxide thickness ($t_{ox}$) = 2 nm, length of $R_{nonoffset}$ ($T_j$) = 5 nm, channel length ($L_{ch}$) = 50 nm, height of $R_{offset}$ ($H_{offset}$) = 10 nm, height of $R_{nonoffset}$ ($H_{nonoffset}$) = $H_s$, gate height ($H_{g1}$) = $H_s$ + ($H_{offset}$ - $t_{ox}$) = 48 nm, dielectric permittivity $\varepsilon_{ox}$ = 25, metal gate workfunction $W_{rk_LTFET}$ = 4.72 eV, and drain doping ($N_d$) = $10^{20}$ $cm^{-3}$.

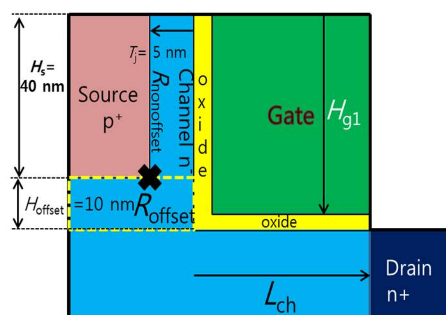


**Figure 1.** Schematic of LTFET.

Sentaurus technology-computer-aided-design tool (TCAD) was used as the simulator [7]. The following models were used in the simulation: dynamic nonlocal band-to-band-tunneling (BTBT) model, fermi statistics, and constant mobility model. Dynamic nonlocal BTBT model calculates BTBT in both lateral and 1-dimensional (1D) directions. Crystal orientation is assumed to be <100> in all devices. A constant electron effective tunneling mass of 0.19 $m_o$ was used in all simulations [8]. All simulation were done at drain source bias $V_{ds}$ = 0.1 V unless otherwise specified.

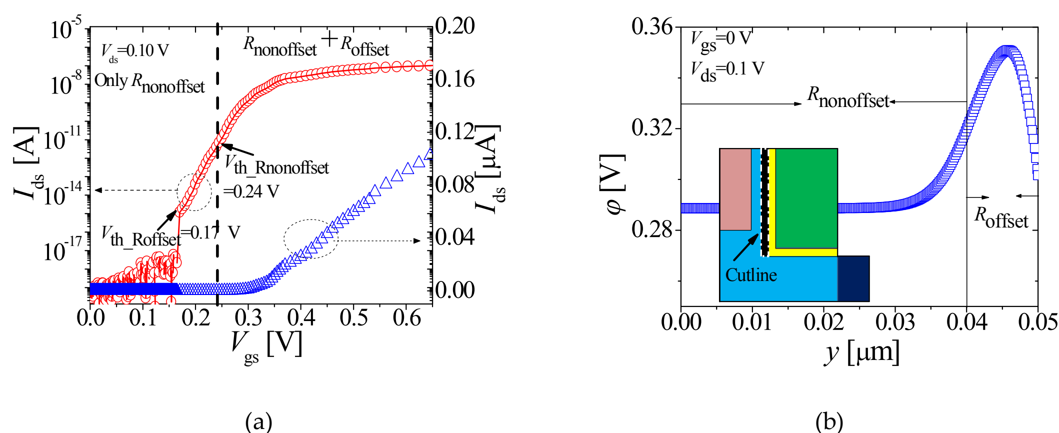


**Figure 2.** (a). $I_{ds}$-$V_{gs}$ transfer characteristics of LTFET. Indicated are $V_{th_Rnonoffset}$ = 0.24 V, and $V_{th_Roffset}$ = 0.17 V. (b) Potential along the cutline shown in the inset at $V_{gs}$ = 0 V. Potential is higher in $R_{offset}$.

For analysis to follow, drain-source current ($I_{ds}$) versus gate-source bias ($V_{gs}$) characteristics of the LTFET are shown in Fig. 2(a). There is a direct overlap between gate and source in $R_{nonoffset}$, and the electric field in $R_{nonoffset}$ is in 1D direction. However, in $R_{offset}$, electric field from the gate converges around the sharp source corner marked by an **X** in Fig. 1. This increases the potential in $R_{offset}$ as compared to $R_{nonoffset}$ for any given bias (until potential saturates due to electron inversion). Fig. 2(b) shows the surface potential at $V_{gs}$ = 0 V. It can be seen that because the electric field

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converges around the sharp source corner [6], the potential in $R_{offset}$ has increased. Since the potential is higher in $R_{offset}$ as compared to $R_{nonoffset}$, the threshold voltage for BTBT in $R_{offset}$ ($V_{th_Roffset}$) is lower than the threshold voltage for BTBT in $R_{nonoffset}$ ($V_{th_Rnonoffset}$).

Figs. 3(a) and (b) show the tunneling rate ($G_{tun}$) contour plot and $G_{tun}$, respectively at $V_{gs}$ = 0.21 V which is the bias needed to generate $I_{ds}$ = $10^{-13}$ A (from Fig. 2(a)). It is obvious from Fig. 3 that the BTBT only takes place in $R_{offset}$ whereas $R_{nonoffset}$ is completely switched off. Fig. 4(a) shows $G_{tun}$ at several $V_{gs}$ values. From Fig. 4(a) $V_{th_Roffset}$ and $V_{th_Rnonoffset}$ can be found to be around $V_{gs}$ = 0.17 and 0.24 V, respectively. Fig. 4(b) shows $G_{tun}$ contour plot at $V_{gs}$ = $V_{th_Rnonoffset}$ = 0.24 V. It can be noticed from Fig. 4(a) that $G_{tun}$ in $R_{nonoffset}$ just after it turns on, is always higher and has much larger BTBT area (in $y$ direction) as compared to $R_{offset}$. Thus whenever $R_{nonoffset}$ turns on, it dominates over $R_{offset}$. The reason why $G_{tun}$ is higher in $R_{nonoffset}$ is simply because the BTBT paths in $R_{offset}$ are laterally oriented or 2D from source to the surface in $R_{offset}$, whereas the BTBT paths in $R_{nonoffset}$ are 1D. The 2D BTBT paths being naturally longer than the 1D paths result in lower $G_{tun}$ in $R_{offset}$.

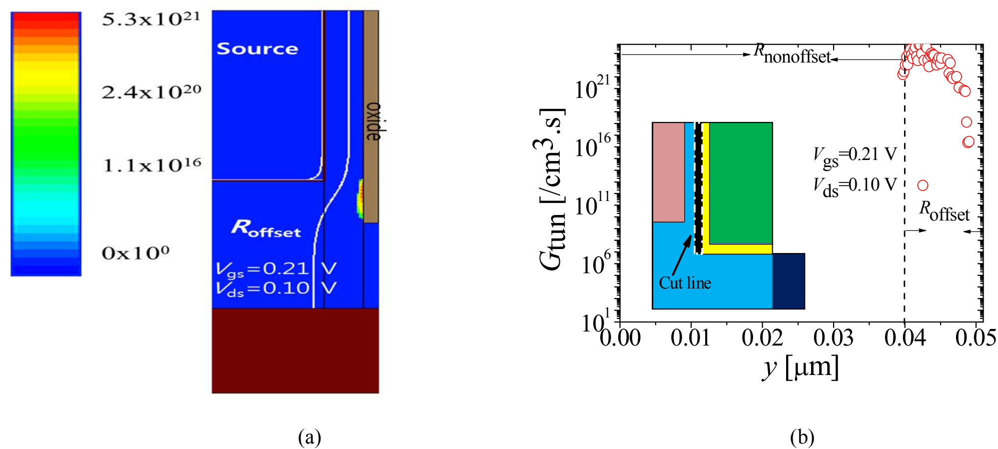


**Figure 3.** (a) $G_{tun}$ contour plot at $V_{gs}$ = 0.21 V, which is the bias needed to generate $I_{ds}$ = $10^{-13}$ A and (b) $G_{tun}$ extracted from Fig. 3(a).

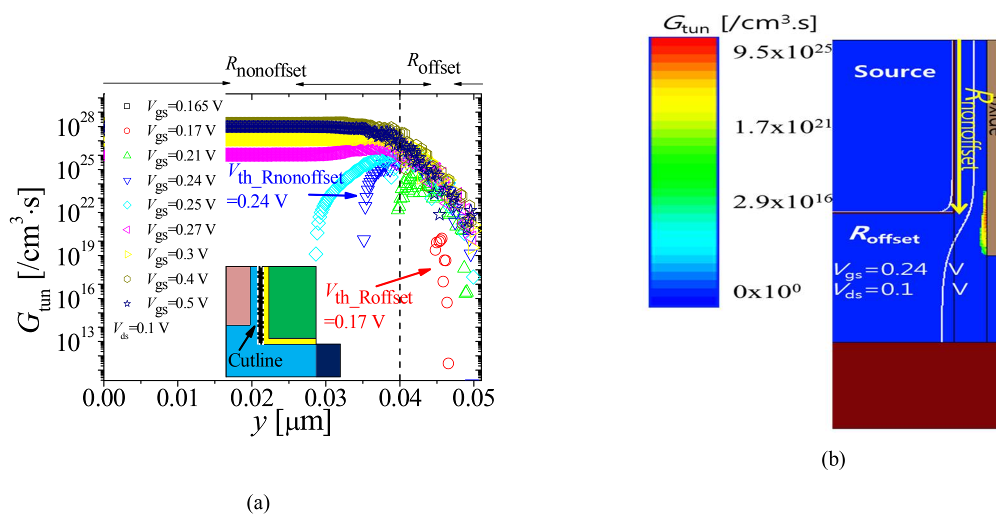


**Figure 4**. (a) $G_{tun}$ at different $V_{gs}$. Indicated in Fig. 4(a) are $V_{th_Rnonoffset}$ = 0.24 V, and $V_{th_Roffset}$ = 0.17 V and (b) $G_{tun}$ contour plot at $V_{gs}$ = $V_{th_Rnonoverlap}$ = 0.24 V. In Fig. 4(b), yellow arrow indicates the height of $R_{nonoffset}$.

From Fig. 4(a), it can be observed that for a large part of the subthreshold region ($V_{gs}$ < 0.24 V) only $R_{offset}$ with the longer 2D BTBT paths and lower $G_{tun}$ is contributing to the BTBT current and the more efficient $R_{nonoffset}$ makes no contribution to the current. In other words, LTFET underperforms in the subthreshold region. If $R_{nonoffset}$ could be forced to turn on at a lower bias than $R_{offset}$ that is the

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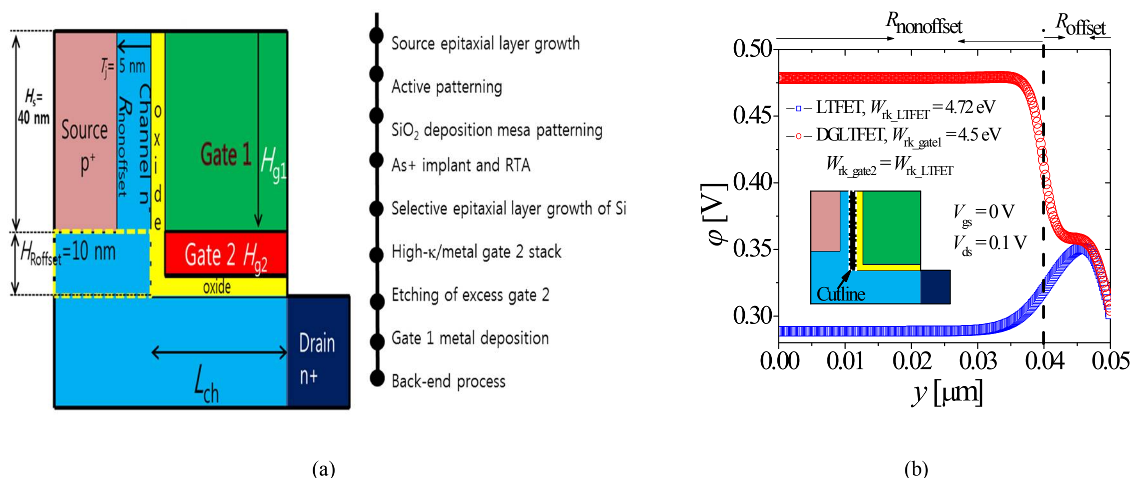
85 condition $V_{th_Rnonoffset}$ < $V_{th_Roffset}$, $R_{nonoffset}$ will turn on in the subthreshold region, and with the
86 condition, $G_{tun}$ in $R_{nonoffset}$ > $G_{tun}$ in $R_{offset}$, demonstrated in Fig. 4(a), a significant improvement in SS
87 could be expected.

## 88 3. DG-LTFET

### 89 *3.1. DG-LTFET: Basic Device Physics*

90 In order to achieve the condition $V_{th_Rnonoffset}$ < $V_{th_Roffset}$, DG-LTFET is presented in Fig. 5(a).
91 DG-LTFET uses dual material gates denoted by gate1 and gate2, each with a different workfunction
92 ($W_{rk_gate1/2}$) and height ($H_{g1/2}$). $H_{g1}$ = $H_{nonoffset}$ = $H_s$ = 40 nm, $H_{offset}$ = 10 nm, $H_{g2}$ = $H_{nonoffset}$ - $H_{g1}$ + ($H_{offset}$ -
93 $t_{ox}$) = 8 nm, and $T_j$ = 5 nm. $W_{rk_gate1}$ is always lower than $W_{rk_gate2}$. $W_{rk_gate2}$ is fixed at $W_{rk_LTFET}$ = 4.72 eV
94 for all DG-LTFET considered in this work. DGLTFET process-flow is indicated in Fig. 5(a). The
95 process-flow is based on LTFET process-flow [3]. DGLTFET process-flow follows LTFET
96 process-flow until the metal-organic chemical vapor deposition of gate 2 (similar to gate deposition
97 in LTFET). After this two additional steps are required. The device is masked to protect the gate
98 oxide and channel areas, and gate 2 is selectively etched according to desired height. Metal of Gate
99 1 is then deposited in the recess created by gate 2-etching. Similar dual-material gate structures
100 have been extensively reported in the literature including [9-11].

101 Lower $W_{rk_gate1}$ results in an increased flatband voltage ($V_{fb}$) [12] in $R_{nonoffset}$ as compared to $R_{offset}$.
102 Fig. 5(b) shows $V_{fb}$ of DG-LTFET (red symbols) with $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$. Also $V_{fb}$
103 of LTFET (blue symbols) is shown for reference. Expectedly DG-LTFET potential increases in
104 $R_{nonoffset}$. The potential does not change abruptly from gate1 to gate2 because of the presence of 2D
105 effects around the source corner. Electric field from bottom of gate2 converges around the source
106 corner. Around the middle of $R_{offset}$, equilibrium is established between the two gates and
107 DG-LTFET potential overlaps LTFET potential since $W_{rk_gate2}$ = $W_{rk_LTFET}$. With $W_{rk_gate1}$ < $W_{rk_gate2}$, the
108 increased potential in $R_{nonoffset}$ reduces $V_{th_Rnonoffset}$. If $W_{rk_gate1/2}$ are appropriately tuned with $W_{rk_gate1}$ <
109 $W_{rk_gate2}$, the condition $V_{th_Rnonoffset}$ < $V_{th_Roffset}$ = 0.17 V could be achieved. Because $W_{rk_gate2}$ = $W_{rk_LTFET}$ =
110 4.72 eV, $V_{th_Roffset}$ (in DG-LTFET) is equal to $V_{th_Roffset}$ (in LTFET).




(a) (b)

**Figure 5.** (a) Schematic of DG-LTFET with process-flow indicated alongside and (b) $V_{fb}$ of DG-LTFET (red symbols) compared with that of LTFET (blue symbols). In DG-LTFET, $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$ = 4.72 eV were used.

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112 Figs. 6(a), (b), and (c) show $I_{ds}$-$V_{gs}$ characteristics at different $W_{rk_gate1}$, SS, and $I_{ON}/I_{OFF}$ of
113 DG-LTFET with constant $W_{rk_gate2} = W_{rk_LTFET} = 4.72$ eV for all DG-LTFET, respectively. Also the $I_{ds}$-$V_{gs}$
114 characteristics of LTFET (black squares) are shown for reference. $I_{ON}$ is extracted at $V_{gs} = 0.7$ V, and
115 $I_{OFF}$ is defined as $I_{ds} = 10^{-17}$ A. With $W_{rk_gate1} = 4.675$ eV (red circles), the $V_{th_Rnonoffset}$ is reduced to 0.189
116 V. Compared with LTFET, $R_{nonoffset}$ now turns on earlier in the subthreshold region, along with $R_{offset}$.
117 Since BTBT is more efficient in $R_{nonoffset}$ (Fig. 4(a)) as compared to $R_{offset}$, $I_{ds}$ increases more rapidly
118 within the subthreshold region. Hence, just at the transition point, where $R_{nonoffset}$ turns on ($V_{gs}$ ~
119 0.189) a kink appears in the $I_{ds}$-$V_{gs}$ curve. With $W_{rk_gate1} = 4.65$ eV (green triangles), $V_{th_Rnonoffset}$ is
120 reduced to $V_{gs} = 0.167$ V and the condition $V_{th_Rnonoffset} < V_{th_Roffset}$ is achieved and DG-LTFET exhibits a
121 remarkable SS with values less than 10 mV/dec as seen in Fig. 6(b). With $W_{rk_gate1} = 4.625$ eV (blue
122 stars), $V_{th_Rnonoffset}$ reduces further to 0.1448 V which is < $V_{th_Roffset}$. If $V_{th_Rnonoffset} < V_{th_Roffset}$ is established
123 than any increase in $V_{th_Roffset} – V_{th_Rnonoffset}$ simply shifts the $I_{ds}$-$V_{gs}$ to the left without any change in SS
124 as shown by the blue stars ($W_{rk_gate1} = 4.625$ eV) and orange diamonds ($W_{rk_gate1} = 4.5$ eV) in Figs. 6(a)
125 and (b), respectively. An improvement of ~16 % is observed in $I_{ON}/I_{OFF}$ of DG-LTFET (with $W_{rk_gate1} =$
126 4.625 eV) over LTFET.

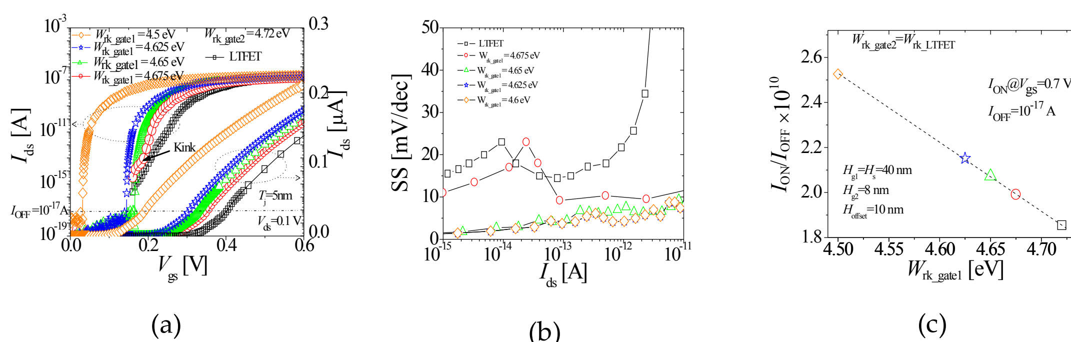


**Figure 6.** (a). $I_{ds}$-$V_{gs}$ characteristics of DG-LTFET with different $W_{rk_gate1}$s and fixed $W_{rk_gate2} = W_{rk_LTFET}$. Also shown is $I_{ds}$-$V_{gs}$ characteristics of LTFET (black squares). (b) SS extracted from $I_{ds}$-$V_{gs}$ characteristics in Fig. 6(a). (c) $I_{ON}/I_{OFF}$ ratio extracted from $I_{ds}$-$V_{gs}$ characteristics in Fig. 8(a). Red circles: $W_{rk_gate1} = 4.675$ eV, Green triangles: $W_{rk_gate1} = 4.65$ eV, Blue stars: $W_{rk_gate1} = 4.625$ eV, Orange diamonds: $W_{rk_gate1} = 4.5$ eV.

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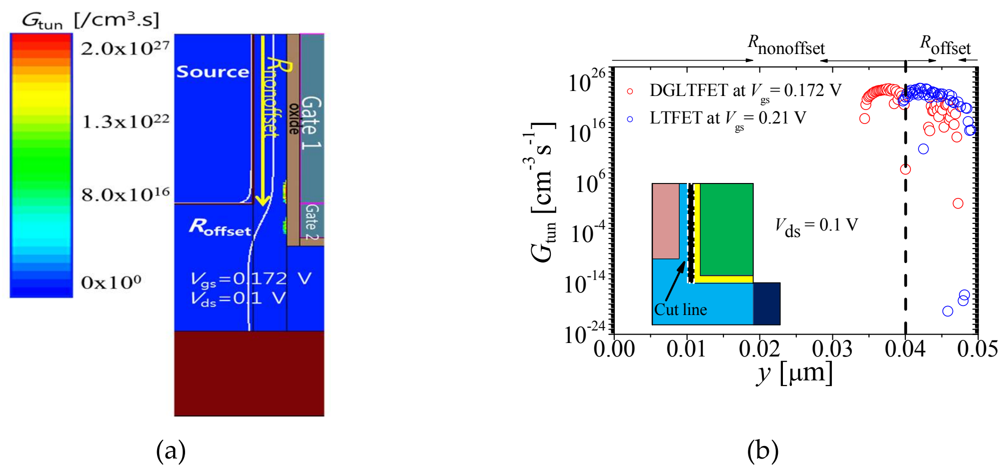


(a) (b)

**Figure 7.** (a) $G_{tun}$ contour plot of DG-LTFET with $W_{rk_gate1}$ = 4.65 eV at $V_{gs}$ = 0.172 V, which is needed to generate $I_{ds}$ = $10^{-13}$ A and (b) $G_{tun}$ extracted from Fig. 7(a) (red symbols). Also $G_{tun}$ (blue symbols) of LTFET at a $V_{gs}$ bias needed to generate $I_{ds}$ = $10^{-13}$ A are shown for reference. In Fig. 7(a), yellow arrow indicates the height of $R_{nonoffset}$.

Fig. 7(a) shows $G_{tun}$ contour plot of DG-LTFET at a $V_{gs}$ (= 0.172 V) bias needed to achieve an equivalent $I_{ds}$ of $10^{-13}$ A in DG-LTFET with $W_{rk_gate1}$ = 4.65 eV. Fig. 7(b) shows contour plot extracted from Fig. 7(a). For reference Fig. 7(b) also shows $G_{tun}$ needed to generate an equivalent amount of $I_{ds}$ in LTFET (at a $V_{gs}$ bias of 0.21 V, Fig. 3(b)). As can be seen in Fig. 7(b), LTFET needs contribution only from $R_{offset}$, but to generate the same amount of $I_{ds}$, DG-LTFET depends heavily on $R_{nonoffset}$ with some contribution from $R_{offset}$. Because $G_{tun}$ in $R_{nonoffset}$ is more efficient (Fig. 4(a)), as the $V_{gs}$ bias increases, $G_{tun}$ increases exponentially in a much larger area in $R_{nonoffset}$ which results in the DG-LTFET exhibiting a much steeper subthreshold swing, while the LTFET continues to depend only on the inefficient BTBT in $R_{offset}$ until around $V_{th_Rnonoffset}$ = 0.24 V.

### 3.2. Device Optimization

To optimize device performance, impact of variations in key parameters including $H_{g1/2}$, $H_s/T_j$, and $N_d$ was investigated. To investigate the impact of $H_{g1/2}$ values, $I_{ds}$-$V_{gs}$ characteristics for DG-LTFET at different $H_{g1}$ and $H_{g2}$ = $H_{nonoffset}$ - $H_{g1}$ + ($H_{offset}$ - $t_{ox}$) with fixed $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$, $H_s$ = $H_{nonoffset}$ = 40 nm, $H_{offset}$ = 10 nm, and $T_j$ = 5 nm is presented in Fig. 8. It can be seen that $I_{ds}$ is independent of $H_{g1/2}$.

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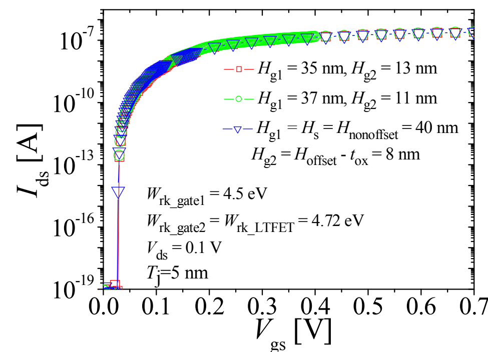


**Figure 8.** $I_{ds}$-$V_{gs}$ characteristics for several $H_{g1/2}$s with $W_{rk_gate1/2}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$. Red squares, green circles, and blue triangles: $H_{g1}$ = 35, 37, and 40 nm, respectively.

Next, to investigate the effect of $T_j$ on device performance, $I_{ds}$-$V_{gs}$ characteristics, SS, and $I_{ON}/I_{OFF}$ of DG-LTFET are presented for different $T_j$ with fixed $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$, $H_{g1}$ = $H_{nonoffset}$ = 40 nm, $H_{offset}$ = 10 nm. and $H_{g2}$ = $H_{nonoffset}$ - $H_{g1}$ + ($H_{offset}$ - $t_{ox}$) = 8 nm in Fig. 9(a), (b) and (c), respectively. It was found that the increasing $T_j$ results in a degradation of $I_{ON}/I_{OFF}$ ratio. It is simply because of the increase in BTBT path length with the increase in $T_j$. $T_j$ of 5 nm was found to be optimum in this work as any further reduction will bring significant quantum confinement effect into play which is well known to degrade device performance [4-5], [13-15].

Next, the impact of varying $H_s$ is investigated. $I_{ds}$-$V_{gs}$ characteristics of DG-LTFET for several $H_s$ with fixed $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$, $H_{g1}$ = $H_s$ = $H_{nonoffset}$, $H_{g2}$ = $H_{nonoffset}$ - $H_{g1}$ + ($H_{offset}$ - $t_{ox}$) = 8 nm, and $T_j$ = 5 nm is presented in Fig. 10. By maintaining $H_{g1}$ = $H_s$, $H_{offset}$ =10 nm, and $H_{g2}$ = 8 nm, the electric field vector distribution within DG-LTFET remains the same as $H_s$ is varied, and BTBT area simply scales with $H_s$. An increase (decrease) in BTBT area with $H_s$ simply results in an increased (decreased) $I_{ON}/I_{OFF}$ ratio as shown in Fig. 10(b) with no change in SS as evident from Fig. 10(a).

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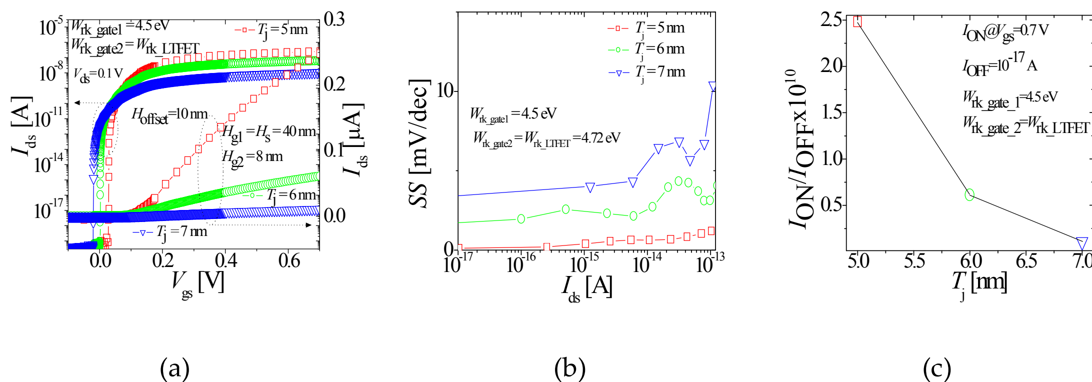
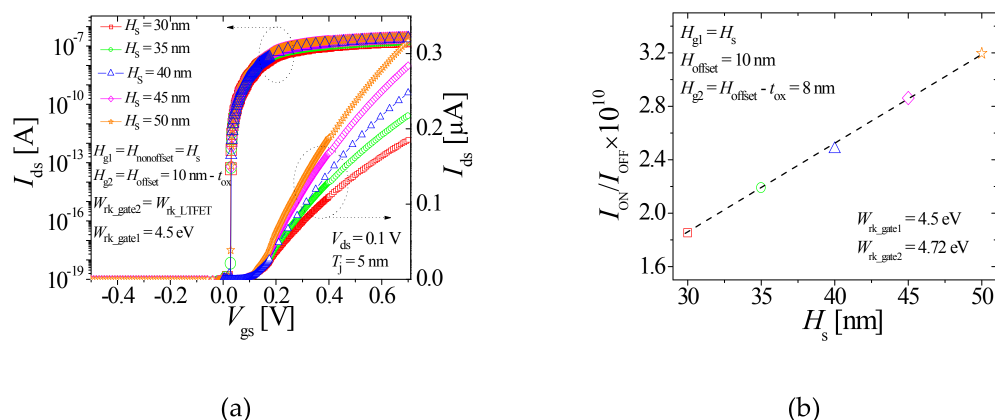



(a) (b) (c)

**Figure 9.** $I_{ds}$-$V_{gs}$ characteristics of DG-LTFET with different $T_j$ and fixed $W_{rk_gate1}$ = 4.5 eV, $W_{rk_gate2}$ = $W_{rk_LTFET}$ and $H_{g1}$ = $H_s$ = $H_{nonoffset}$ = 40 nm, $H_{g2}$ = $H_{offset}$ (10 nm) - $t_{ox}$ = 8 nm. (b) SS of $I_{ds}$-$V_{gs}$ shown in Fig. 8(a). (c) $I_{ON}/I_{OFF}$ ratio of $I_{ds}$-$V_{gs}$ characteristics shown in Fig. 8(a). Red squares, green circles, and blue triangles: $T_j$ = 5, 6 and 7 nm, respectively.




(a) (b)

**Figure 10.** $I_{ds}$-$V_{gs}$ characteristics of DG-LTFET with different $H_s$, fixed $W_{rk_gate1}$ = 4.5 eV, $W_{rk_gate2}$ = $W_{rk_LTFET}$, and $H_{g1}$ = $H_s$ = $H_{nonoffset}$, $H_{g2}$ = $H_{offset}$ (= 10 nm) - $t_{ox}$ = 8 nm. (b) $I_{ON}/I_{OFF}$ ratio of $I_{ds}$-$V_{gs}$ characteristics shown in Fig. 10(a). Red squares, green circles, blue triangles, magenta diamonds, and orange stars: $H_s$ = 30, 35, 40, 45, and 50 nm, respectively.

Finally, ambipolar current of DG-LTFET is discussed. Ambipolar $I_{ds}$ of TFET depends on drain-channel junction. In DG-LTFET, drain-channel junction is controlled by gate2 with $W_{rk_gate2}$ = $W_{rk_LTFET}$. With the same workfunction, the electrostatics of drain-channel junction in DG-LTFET is exactly the same as that in LTFET. Fig. 11(a) shows ambipolar $I_{ds}$ of DG-LTFET compared with LTFET. Any change in $W_{rk_gate1}$ in DG-LTFET does not affect the drain-channel junction. Same argument applies for any other design parameter variation in DG-LTFET including $H_s$, $H_{g1/2}$, $T_j$, that is, as long as electrostatics of drain-channel junction remains unaffected, DG-LTFET will exhibit equivalent ambipolar $I_{ds}$ as LTFET. Further, impact of $N_d$ on ambipolar $I_{ds}$ was considered. Different $N_d$ values were considered for a DG-LTFET with $W_{rk_gate1}$ = 4.5 eV and $W_{rk_gate2}$ = $W_{rk_LTFET}$, $H_{g1}$ = $H_{nonoffset}$ = 40 nm, $H_{g2}$ = $H_{offset}$ − $t_{ox}$ = 8 nm, and $T_j$ = 5 nm and the results are shown in Fig. 11(b). Drain doping level of $10^{18}$ cm$^{-3}$ was found to suppress ambipolar $I_{ds}$ appreciably without affecting the $I_{ON}$.

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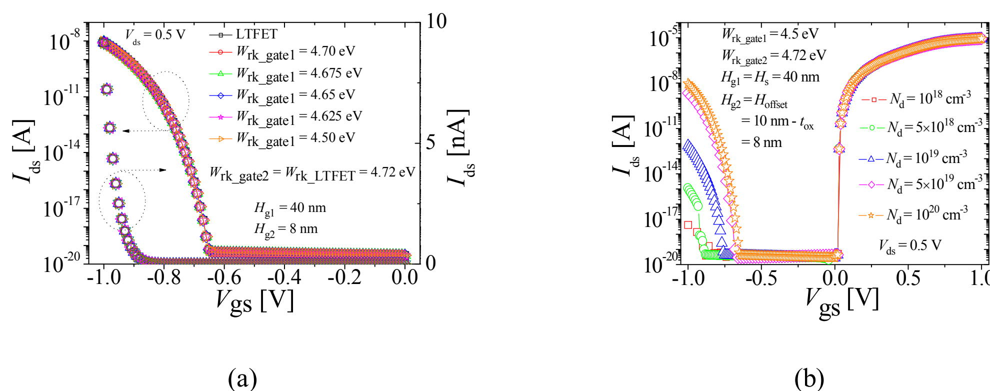


**Figure 11.** (a) $I_{ds}$-$V_{gs}$ characteristics of DG-LTFET at $V_{ds}$ = 0.5 V with different $W_{rk_gate1}$ and $W_{rk_gate2}$ = $W_{rk_LTFET}$, $H_{g1}$ = $H_{offset}$ = 10 nm, $H_{g2}$ = 8 nm, $T_j$ = 5 nm and $N_d$ = $10^{20}$ cm$^{-3}$. Red circles, green triangles, blue diamonds, magenta stars, and orange right triangles: $W_{rk_gate1}$ = 4.7, 4.675, 4.65, 4.625, and 4.5 eV. (b) DG-LTFET $I_{ds}$ with different $N_d$. $N_d$ = $10^{18}$ cm$^{-3}$ demonstrates almost negligible ambipolar $I_{ds}$. Red squares, green circles, blue triangles, magenta diamonds, and orange stars: $N_d$ = $10^{18}$, $5{\times}10^{18}$, $10^{19}$, $5{\times}10^{19}$, and $10^{20}$ cm$^{-3}$.

## 5. Conclusions

Device physics of LTFET were investigated. It was found that a large part of subthreshold region is dominated by the parasitic, lateral, and 2D BTBT from source to $R_{offset}$ with lower $G_{tun}$. The more efficient 1D BTBT from source to $R_{nonoffset}$, which has higher $G_{tun}$, takes place at a higher bias in the subthreshold region because of $V_{th_Rnonoffset} > V_{th_Roffset}$. The device does not utilize its channel fully during the subthreshold region due to $V_{th_Rnonoffset} > V_{th_Roffset}$. A new type of device based on LTFET was introduced in this work. The device uses a dual gate-stacked structure which workfunction of upper gate $W_{rk_gate1}$ is below that of lower gate $W_{rk_gate2}$. This makes the potential in $R_{nonoffset}$ increase and thus $V_{th_Rnonoffset}$ reduce. DG-LTFET reverses the threshold condition of LTFET, which it lowers $V_{th_Rnonoffset}$ (< $V_{th_Roffset}$). $R_{nonoffset}$ with higher $G_{tun}$ turns on earlier than $R_{offset}$ in the subthreshold region of DG-LTFET and the device exhibits SS of less than 10 mV/dec. It was found that $W_{rk_gate1}$ in DG-LTFET needs to be sufficiently less than $W_{rk_gate2}$ to achieve the sub 10 mv/dec SS. It was found that $I_{ds}$ and SS are independent of $H_{g1/2}$. DG-LTFET was further evaluated for different device dimensions including $T_j$ and $H_s$, while maintaining the electric field vector distribution equivalent. $I_{ds}$ decreases with an increase in $T_j$ and scales with $H_s$. $N_d$ value of $10^{18}$ cm$^{-3}$ was found to appreciably reduce ambipolar $I_{ds}$. With the results presented in this work DG-LTFET could be considered as a viable potential replacement to conventional MOSFET.

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