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Article

Environmental effects on the electrical characteristics of back-gated WSe_2 field effect transistors

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Abstract: We study the effect of polymer coating, pressure, temperature and light on the electrical characteristics of monolayer WSe_2 back-gated transistors with quasi-ohmic Ni/Au contacts. We prove that the removal of a layer of poly(methyl methacrylate) or a decrease of the pressure change the device conductivity from p to n-type. We demonstrate a gate-tunable Schottky barrier at the contacts and measure a barrier height of ~70 meV in flat-band condition. We report and discuss a temperature-driven change in the mobility and the subthreshold slope which we use to estimate the trap density at the WSe_2/SiO_2 interface. We study the spectral photoresponse of the device, that can be used as a photodetector with a responsivity of ~0.5 AW^{-1} at 700 nm wavelength and 0.37 mW/cm^2 optical power.

Keywords: 2D materials, field effect transistors, PMMA, tungsten diselenide

1. Introduction

The continuous downscaling of the channel length and thickness in modern field effect transistors (FETs) increases the need for atomically layered materials to minimize short channel effects at extreme scaling limits [1,2]. Layered transition metal dichalcogenides (TMDs), owing to their two-dimensional structure, fairly good mobility and absence of dangling bonds, can enable extreme channel length scaling and have recently emerged as promising materials for future electronic and optoelectronic devices [3–7]. These graphene-like materials offer the advantages of sizeable and non-zero bandgap, high on/off ratio and quasi-ideal subthreshold swing, mechanical flexibility, and thermal and chemical stability. As for graphene, their electronic transport properties are strongly influenced by the choice of the metal contacts [8,9], interface traps and impurities [10,11], structural defects and environmental exposure [12–14]. These effects need to be understood and controlled for technological applications.

Molybdenum disulfide (MoS_2) has been one of the most heavily investigated systems from the TMD family to date [15–18]. Similar to MoS_2, tungsten diselenide (WSe_2), whose electrical and optical properties have been less explored [20], is characterized by an indirect bandgap (1.0-1.2 eV) in its bulk form and shows a transition to a direct gap of 1.6 eV when it is thinned to monolayer [21]. A few recent reports on WSe_2 FETs demonstrated relatively high field-effect mobility controllable by temperature and bias voltage [21], an ideal subthreshold slope ~ 60 mV/dec [22] and an *on/off* ratio greater than 10^8. The ambipolar behavior, controllable using different metal contacts like In or Pd [8], which favor electron and hole injection respectively [23,24], makes mono- and few-layer WSe_2 an interesting material for complementary logic applications; indeed, a stable WSe_2 -based CMOS technology has been proved [25].

A great challenge for electronic integration WSe_2 is the achievement of low-resistance ohmic contacts, a task often complicated by the appearance of Schottky barriers due to the occurrence of Fermi level pinning [26,27].

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Accordingly, several studies have aimed at clarifying the role of the contacts, focusing on the carrier transport at the WSe_2/metal interface [23,28].

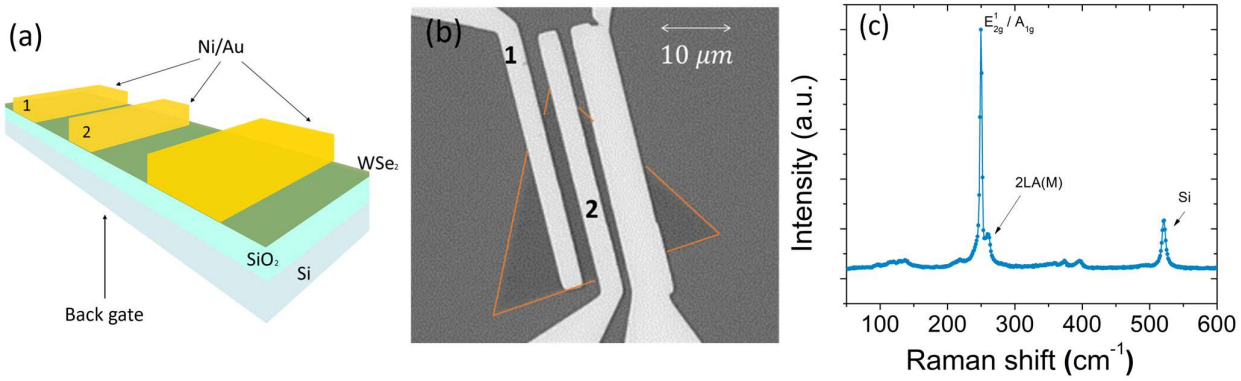
In this paper, we study back-gate monolayer WSe_2 devices with Ni contacts, measuring their electrical characteristics under different conditions, considering for instance the effect of a poly(methyl methacrylate) (PMMA) coating layer, and the dependence on the chamber pressure and the sample temperature. Similar to graphene [29,30], we observe that PMMA strongly influences the electric transport to the extent of modifying the polarity of the device from p-type to n-type conduction when the PMMA layer is removed. We demonstrate that lowering the pressure on air exposed WSe_2- FETs affects their characteristics in a similar way to PMMA, turning the conduction from p- to n-type. Furthermore, from the current-voltage (I-V) characteristics measured at different temperatures, we prove a gate modulation of the Schottky barrier (SB) at contacts.

In addition, we study the temperature dependence of the carrier mobility and the subthreshold slope and show that both undergo a change of behavior with rising temperature. From the subthreshold slope data, we derive the interface trap density. The monolayer WSe_2 device, characterized at several laser wavelengths, achieves a responsivity as high as $\sim 0.5\ AW^{-1}$ at 700 nm, i.e. at photon energy close to the WSe_2 bandgap.

2. Experimental

The WSe_2 flakes were grown by chemical vapor deposition (CVD) at 900°C and pressure of 6 Torr on highly p-doped Si (silicon) substrate covered by 300 nm of SiO_2 (silicon dioxide). The schematic of the back gate FET device and a scanning electron microscope top-view of a WSe_2 monolayer with evaporated Ni/Au $(5/50\ nm)$ contacts are shown in Figure 1 (a) and Figure 1 (b). In the following, the transistor characterization refers to contact 1 and 2, as marked in Figure 1 (a) and (b). The distance between the two contacts, i.e. the channel length, is L~2 μm, while the mean channel width is W~22 μm (Figure 1 (b)).The electrical analyses are performed using a Keithley 4200 SCS (semiconductor characterization system) connected with a Janis ST-500 probe station, equipped with four probes used for the electrical connection to the drain and source Ni/Au terminals and to the Si back-gate of the device.

The Raman spectrum of the WSe_2, displayed in Figure 1 (c), exhibits two peaks around $\sim 250\ cm^{-1}$ and $\sim 260\ cm^{-1}$, corresponding to an overlapping contribution from the in-plane vibrations of W and Se atoms (E^1_{2g}) and out-of-plane vibration of Se atoms (A_{1g}), and to a second order resonant Raman mode $(2\ LA\ (M))$ due to LA phonons at the M point in the Brillouin zone [31,32], respectively. The peak frequency positions are typical of a WSe_2 monolayer of thickness $d \sim 0.7\ nm$ [24,36,37]. The monolayer structure of the flake is further verified by the electrical response to laser light, as reported in Figure 1 (d) and Figure 1 (e).



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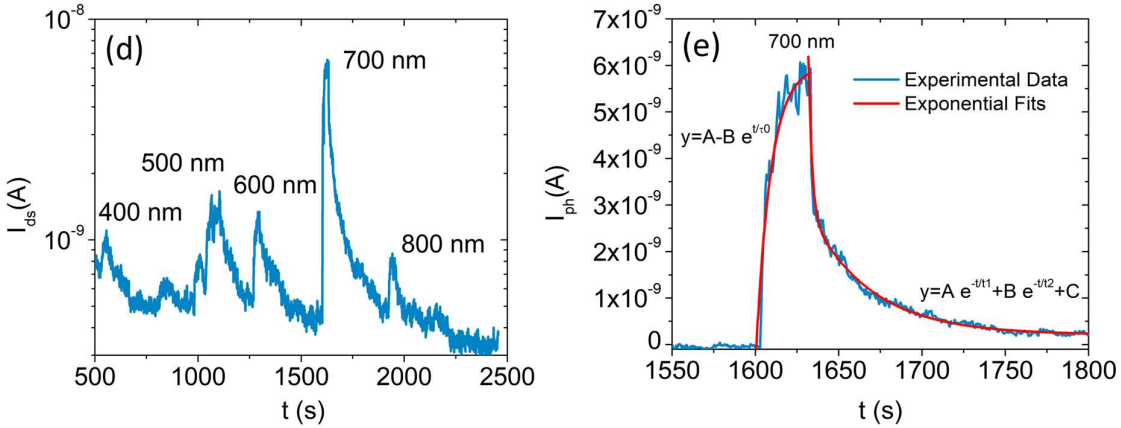

Figure 1. Schematic section (**a**) and optical microscope image (**b**) of WSe_2 back gate FET transistor. (**c**) Raman spectrum of the WSe_2 flake. (**d**) Drain-source current measured under illumination at different wavelengths ($V_{ds} = +5\,V$, $V_{gs} = 0\,V$, $P{\sim}10^{-4}\,mbar$). (**e**) Photocurrent generated by a $30\,s$ laser pulse at the wavelength of $\sim 700\,nm$ and optical power $\sim 0.37\,mW/cm^2$ with exponential fits.

The photocurrent, $I_{ph} = I_{light} - I_{dark}$, in Figure 1 (d-e) shows a higher peak at the wavelength of 700 nm (photon energy 1.7 eV), which is slightly above the bandgap of a WSe_2 monolayer, confirming the Raman spectroscopy assignment of the single-layer nature of the WSe_2 channel.

The different wavelengths are selected filtering a supercontinuous laser source (NKT Photonics, Superk Compact, wavelength ranging from 450 nm to 2400 nm, total output power of $110\,mW$) using pass-band filters with 50 nm bandwidth.

3. Results and discussion

We start presenting the transistor characterization by comparing the device electrical I-V curves with and without a PMMA coating layer. We encapsulated the transistor channel with a layer of PMMA to protect it from residues and adsorbates [35,36]. It has been observed that a PMMA film, or even only residues of it, cause p-type doping of graphene and other 2D channels due to the presence of oxygen. The p-type conduction is either explained considering the charge transfer to oxygen which, acting as electron capture center, suppresses the free electron density, or ascribed to the pinning of the Fermi level close to the maximum of the valence band, which favors the hole conduction [27,37–39]. Here, we report a similar effect for WSe_2 FETs. The PMMA-covered devices show p-type behavior, as can be seen from the $I_{ds} - V_{gs}$ transfer curves of Figure 2 (a) showing high channel current I_{ds} (*on*-state of the FET) at negative gate voltages, V_{gs}. After the removal of the PMMA in acetone, a dramatic change to n-type behavior occurred, with *on*-state at $V_{gs} < 0\,V$, as shown in Figure 2 (b). We remark that a similar effect has been reported in [25], but for exfoliated WSe_2 flakes on an SiO_2/Si substrate covered by F_4PCNQ doped PMMA. The corresponding $I_{ds} - V_{ds}$ output characteristics are reported in Figure 2 (c) and (d). Both of these show a quasi ohmic behavior, for the device in the *on* state; a slightly asymmetric behavior appears when the device is in the *off* state, indicating low-SB at Ni/WSe_2 contacts with possible slightly different heights [28,40].

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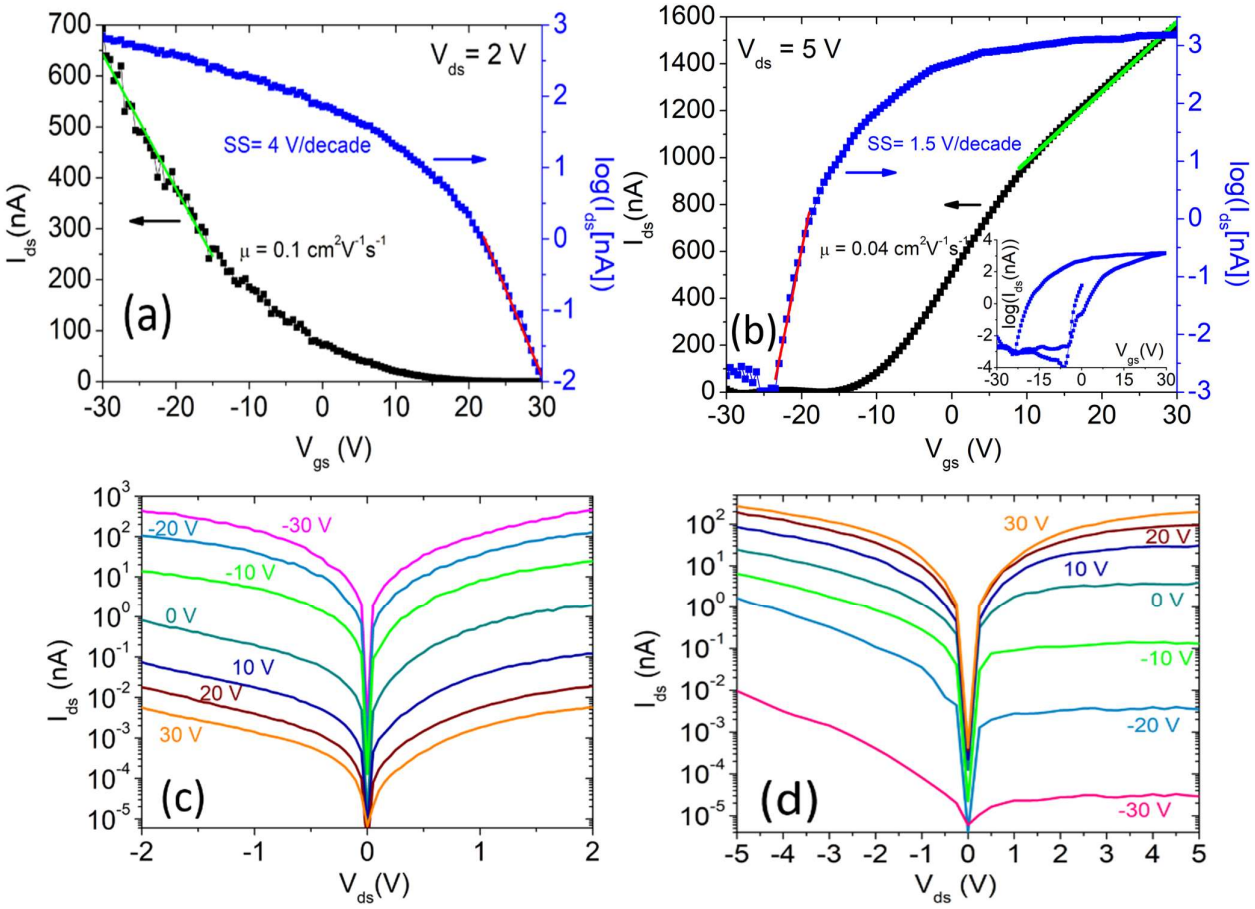

Figure 2. (**a**) Transfer characteristic ($I_{ds} - V_{gs}$ curves) performed at a drain voltage bias $V_{ds} = 2\,V$ for the device covered with PMMA. (**b**) Transfer characteristic performed at a drain voltage bias of 5 V after the removal of PMMA. The inset shows a complete cycle with the gate voltage V_{gs} swept forward and backward. Output characteristics ($I_{ds} - V_{ds}$ curves) at different gate voltages for the device with (**c**) and without (**d**) PMMA. For the uncovered device, the drain bias was increased from $V_{ds} = 2V$ to $V_{ds} = +5V$ to better characterize the above-threshold region. All measurements were performed at $T = 293$ K and $P = 2.3$ mbar.

For increasing V_{gs}, the channel current at constant V_{ds} bias shows an exponential dependence (below threshold region) followed by a linear or power law behavior (above threshold region).

A quadratic behavior is particularly evident in the transfer characteristic of Figure 2 (a), despite the transistor is operated in the triode region. The parabolic dependence of I_{ds} on V_{gs} can be ascribed to a linear gate-voltage dependence of the mobility μ [41,42], that defines the drain current as

$$I_{ds} = \frac{W C_{ox}\,\mu}{L}(V_{gs} - V_{th})V_{ds} \tag{1}$$

with

$$\mu = \mu_B(V_{gs} - V_{th}) \tag{2}$$

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in which μ_B represents the mobility per unit gate voltage and V_{th} is the gate threshold voltage. The V_{gs}-dependent mobility can be explained considering that the increasing carrier density becomes more effective in screening Coulomb scatters or in filling trap states at higher V_{gs}, thus resulting in enhanced mobility.

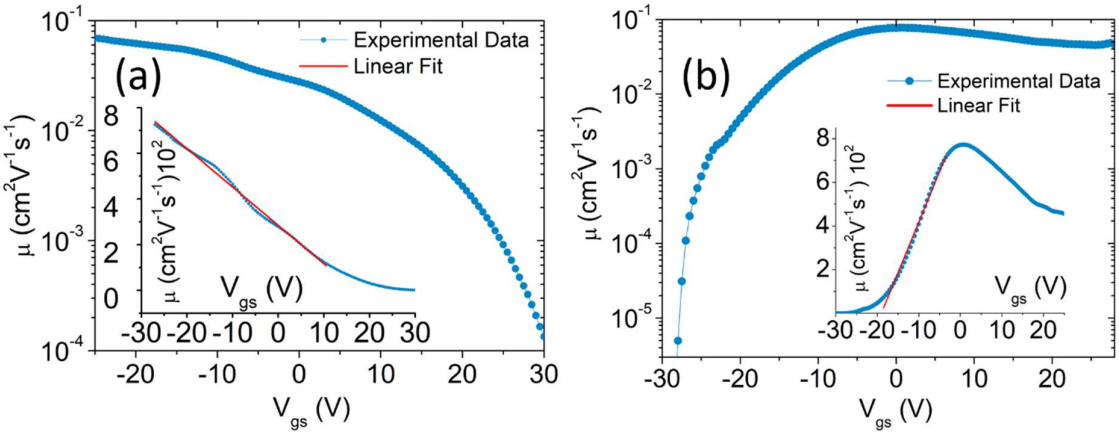

Figure 3. Mobility versus gate voltage on logarithmic scale for the WSe_2 flake covered (**a**) or uncovered (**b**) by PMMA. The inset graphs show the mobility on linear scale.

According to eq. (1) and (2),

$$\mu(V_{gs}) = \frac{L}{W}\frac{1}{C_{ox}}\frac{1}{V_{ds}}\frac{dI_{ds}}{dV_{gs}} \tag{3}$$

Figure 3 (a) and (b) show the $\mu - V_{gs}$ curves on logarithmic and linear (insets) scales obtained from eq. (3) and the data of Figure 2, for the devices with and without PMMA, respectively. These confirm a linear dependence of μ on V_{gs} over a certain range. Remarkably, for the device with removed PMMA, the mobility shows the typical decrease observed in common FETs due to increased scattering suffered by carriers attracted at the channel/dielectric interface at higher gate voltages.

Neglecting the V_{gs} dependence of the mobility, as usually done in literature, μ can be obtained, by fitting a straight line to the transfer characteristic as shown in Figures 2 (a) and 2 (b). By this method, which confirms the previous results, we estimate an electron mobility of $\sim 0.04\ cm^2V^{-1}s^{-1}$ for the n-type transistor without PMMA, consistent with other works with WSe_2 on SiO_2 [41], and a hole mobility of $\sim 0.1\ cm^2V^{-1}s^{-1}$ for the p-type transistor with covering PMMA, thus confirming the higher hole mobility in WSe_2 reported elsewhere [24,27,32,42].

The subthreshold slope $SS = dV_{gs}/dlog(I_{ds})$ is $4\ V/decade$ and $1.5\ V/decade$, for the p-type and n-type transistor, respectively. The different SS results from a different trap density at the WSe_2/dielectric interface, implying a higher trap density when the WSe_2 channel is covered by PMMA, which adds a second interface [43,44]. The trap states manifest also as a hysteresis in the transfer curve, as shown in the inset of Figure 2 (b), due to trapping and detrapping of charge carriers, whose potential adds to that of the back-gate [41,42,45,46].

After the removal of the polymeric film and exposure of the device to air for a few days, we observed a restoration of prevailing p-type behavior due to O_2 and water adsorption on the WSe_2 surface, which could also pin the Fermi level closer to the maximum of the valence band. Then, we studied the effect of dynamic pressure by increasing the vacuum level of the probe station chamber from the atmospheric ($\sim 1\ bar$) value to $P = 10^{-5}$ mbar. As reported in Figure 4 (a), the transistor transfer characteristic changes again from p to n-type. The transition occurred with a gradual decrease of the subthreshold slope and an increase of the *on/off* ratio, as shown in Figure 4 (b). We attribute the polarity change to the desorption of adsorbed O_2 and H_2O.

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The study of the electrical characteristics of the transistor as a function of temperature T is a prerequisite for the practical exploitation of the device. It can be conveniently used to investigate the Schottky barrier at contacts.

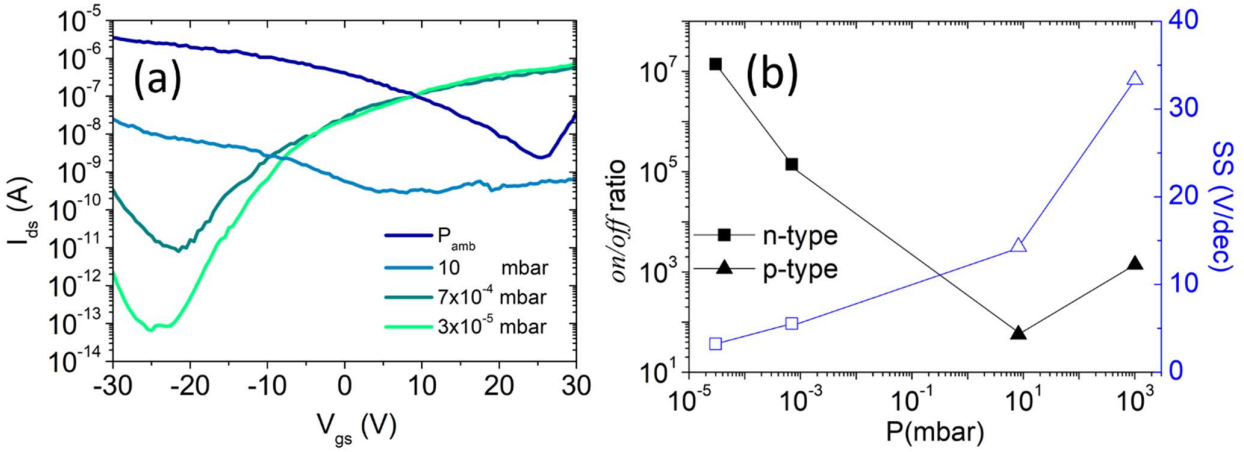

Figure 4. (**a**) Transfer characteristics at different pressures from atmospheric value (blue curve) to $\sim 10^{-5}$ mbar (light green curve) (**b**) Threshold voltage and subthreshold slope as a function of chamber pressure.

We extract the Schottky barrier at the flat-band condition (Figure 5) from a plot of the Schottky barrier height evaluated as a function of V_{gs}. Measuring the $I_{ds} - V_{gs}$ characteristics of the device at several temperatures (Figure 5 (a)) and extracting $I_{ds} - T$ datasets at given gate voltage (examples are marked by the vertical lines in Figure 5(a)), we construct the Arrhenius plot of Figure 5 (b), showing the $ln(I_{ds}/T^{3/2}) - \frac{1}{T}$ curves at a representative subset of V_{gs} values. We assume that the contacts behave as two back-to-back Schottky junctions, where the current is controlled by reverse biased one and is written as

$$I_{ds} \sim T^{3/2}\, exp\left(-\frac{\Phi_B}{kT}\right) \tag{4}$$

where k is the Boltzmann constant , T the absolute temperature and Φ_B the Schottky barrier height [23,47,48]. According to eq. (4), a linear fit of $\ln(I_{ds}/T^{3/2})$ vs $1/T$ for each V_{gs} dataset in Figure 5 (b) yields a Schottky barrier Φ_B. The so-obtained $\Phi_B - V_{gs}$ relationship is displayed in Figure 5 (c) and can be divided into three zones, each one corresponding to a different transport regime, consistent with the behavior of the transfer characteristics of Figure 5 (a).

At low gate voltage the device is set in the *off* state and the transport is due to the thermal excitation of electrons over the barrier, which is gradually lowered by the gate, as sketched in the insets of Figure 5 (c). This corresponds to a steep exponential rise of the current in the transfer characteristic (with $60\ mV/decade$ slope in the ideal case). When the gate voltage is further increased the device reaches the flat band condition ($V_{gs} = V_{FB}$), which sometimes appears in the subthreshold part of the transfer characteristics as a sudden change of slope; for $V_{gs} > V_{FB}$ the device enters the so-called Schottky regime which includes part of the downward bended region of $I_{ds} - V_{ds}$ curves and is characterized by thermionic and thermionic field emission; finally, at higher V_{gs}, tunneling through the thinned Ni/WSe_2 barrier becomes the dominant conduction mechanism and the device reaches the above threshold region with a linear or power-law $I_{ds} - V_{gs}$ dependence.

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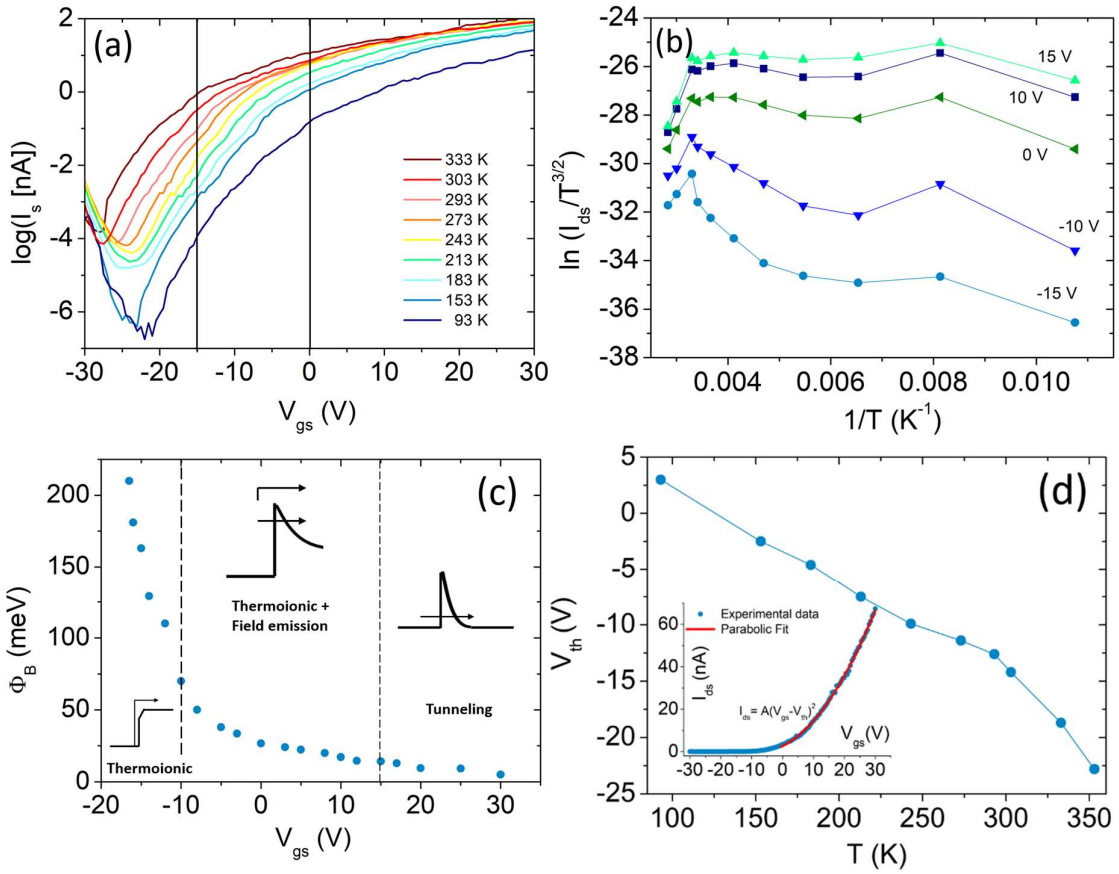

Figure 5. (**a**) Transfer characteristic at different temperatures. (**b**) Arrhenius plot of the current at different temperatures corresponding to a subset of the gate voltages (two of these V_{gs} values are represented by the vertical lines in (**a**)). (**c**) Apparent Schottky barrier as a function of the gate voltage; the insets show the band alignment and the transport regimes at the Ni/WSe2 contacts. (**d**) Threshold voltage V_{th} as a function of the temperature; the inset shows, as an example, the parabolic fit of the $I_{ds} - V_{gs}$ curve at $T = 273\ K$.

The gate voltage that corresponds to V_{FB} is identified by the change of slope in the $\Phi_B - V_{gs}$ plot at lower V_{gs}. The Φ_B corresponding to $V_{gs} = V_{FB}$ is the so-called Schottky barrier height at the flat-band (or simply Schottky barrier). From the plot in Figure 5 (c), its value is $\sim 70\ meV$, confirming the quasi-ohmic Ni-WSe_2 contacts, inferred from the low rectifying output characteristics of Figure 2.

Figure 5 (d) shows the temperature behavior of the threshold voltage V_{th}, which has been extracted assuming a quadratic $I_{ds} - V_{gs}$ law as expressed by eq. (1.1) and (1.2). The decreasing behavior is easily explained considering that the rising temperature accelerates the transition from the Schottky power power-law (above threshold) regime; furthermore, the plot seems to indicate a change of slope above room temperature.

Figure 6 (a) reports the temperature behavior the mobility μ at $V_{gs} = 10\ V$ obtained from the quadratic fit of the $I_{ds} - V_{gs}$ curves.

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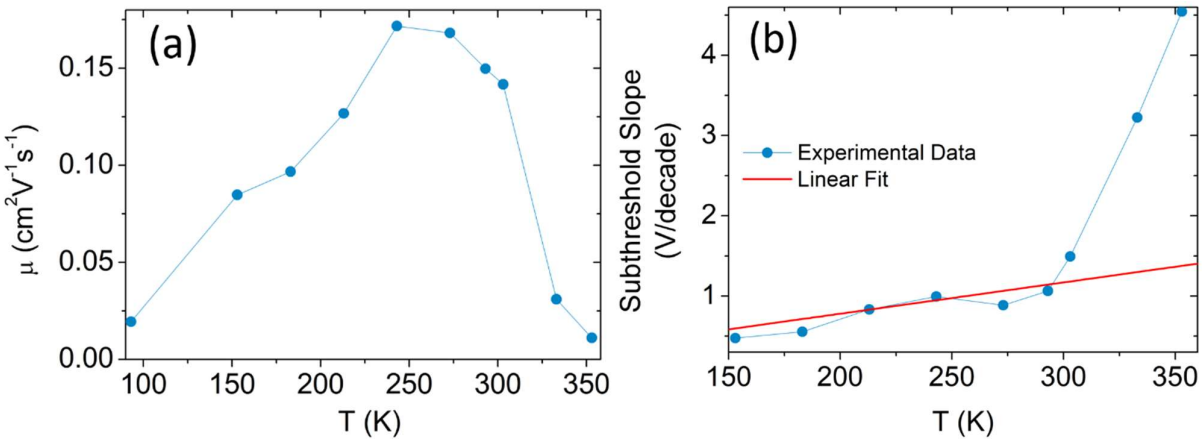

Figure 6. Temperature dependence of (**a**) mobility per unit voltage μ_B and (**b**) subthreshold slope.

The mobility increases for $T < 250\ K$ and decreases for $T > 250\ K$, a behavior typical of semiconductor materials indicating that charged-impurity coulomb scattering dominates at lower temperatures, while phonon scattering becomes the conduction limiting mechanism at high temperature [35].

The subthreshold slope has a dependence on temperature that can be simplified with the following expression

$$SS = n\frac{kT}{q}ln10 \tag{5}$$

where n is the body factor which is related to the interface trap (C_{it}), SiO_2 (C_{SiO2}) and channel depletion layer (C_{dl}) capacitances by

$$n = 1 + \frac{C_{it} + C_{dl}}{C_{ox}} \tag{6}$$

Figure 6 (b) confirms the linear $SS - T$ dependence (eq. 5) but shown an unexpected above room temperature. The deviation from eq. (5) behavior at high temperature is an effect of the low Schottky barrier which becomes ineffective above room temperature ($kT = 26\ meV$), resulting in an increase of the subthreshold current leakage.

Assuming that the WSe_2 monolayer channel is fully depleted, i.e. that $C_{dl} \approx 0$, from the fit of the experimental data with eq. (5), we obtain a $n \approx 48$ and an interface trap density $N_{it} = \frac{C_{it}}{q^2} \approx 1.3 \times 10^{13}\ eV^{-1}cm^{-2}$, which is consistent with previous results reported in the literature [49].

The presence of such a density of trap states justifies the observed hysteretic behavior of the transfer characteristic, inset of Figure 2 (b) [42]. It is also confirmed by the electrical response of the device under illumination.

Figure 1 (e) displays the photocurrent obtained in response to a laser pulse of $30\ s$ at the wavelength of $\sim 700\ nm$, and optical power about $0.37\ mW/cm^2$, and its exponential fits, with rising time $\tau_0 \sim 9\ s$ and a double exponential decay with times $\tau_1 \sim 2\ s$ and $\tau_2 \sim 36\ s$, indicating the presence of faster and slow traps [50] and it is consistent with a photoresponse speed longer than 5 s for quasi-ohmic contacts on similar WSe_2 FETs [50].

We notice that the contact type can play an important role in the response time of WSe2 phototransistors; indeed reduced times have been reported for Schottky contacts [51,52].

Furthermore, we estimate a photoresponsivity (Figure 1 (e))

$$R = \frac{I_{ph}}{W_{opt}} \approx 0.5\frac{A}{W} \tag{7}$$

where W_{opt} is the incident power. This value is in good agreement with the $0.6\ A/W$ at 750 nm previously reported [52]. Such a responsivity is competitive with solid state devices on the market and, despite the ultrathin absorber. It confirms the excellent photoresponse of monolayer WSe2 enhanced by the direct bandgap [53,54].

4. Conclusions

In conclusion, we showed that different environmental conditions can have dramatic effects on the electrical properties of monolayer WSe_2 back-gated transistors. In particular, we demonstrated that the removal of a polymer coating layer, as well as of oxygen and water adsorbates, can change the conduction from p to n-type. From I-V characterization at different temperatures, we extracted the Ni/WSe_2 Schottky barrier height, which we studied as a function of the back-gate voltage. We reported and discussed a change in the temperature behavior of the mobility and the subthreshold slope. Finally, we studied the photoresponse of the device to selected laser wavelengths achieving a responsivity competitive with solid state devices on the market.

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