

Electroplating of Electronic Materials for Applications in Large Area Electronics: A Review

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Abstract

The attributes of electroplating as a low-cost, simple, scalable and manufacturable semiconductor deposition technique for the fabrication of large-area and nanotechnology-based device applications are discussed. These strengths of electrodeposition are buttressed experimentally using techniques such as X-ray diffraction, Ultraviolet-visible spectroscopy, Scanning electron microscopy, Atomic force microscopy, Energy-dispersive X-ray spectroscopy and photoelectrochemical cell studies. Based on the structural, morphological, compositional optical, and electronic properties evaluated results, it is evident that electroplating possesses the capabilities of producing high quality semiconductors usable in producing excellent devices. In this paper we will describe the progress of electroplating technique mainly for the deposition of semiconductor thin film materials, their treatment processes and fabrication of solar cells.

Keywords: Electroplating; Semiconductors; Large area electronics; Characterisation; Solar cells

1 Introduction

Electroplating has been well explored over the years especially for the purification, extraction, protection, coating of semiconductors, metals and metalloids in the industrial sector [1] to achieve inherent properties. The use of electroplating technique in the deposition of semiconductor materials dates back to the 1970s [2–4] with the deposition of semiconductors from the II-VI group. The ascendance of the electrodeposition of semiconductor material led to the growth and fabrication of CdS/CdTe-based solar cell device within a decade afterwards [5]. The fabrication of thin-film solar cells with photovoltaic conversion efficiency of ~10% was the stimulus for an intense global research in the electrodeposited semiconductor compounds. The research also spanned into the electrodeposition of II-VI semiconductor materials such as ZnTe [6], ZnSe [6], ZnS [7], ZnO [8] etc and spread into semiconductor material compounds in the binary (III-V, IV-VI), ternary (CuInSe₂) [9,10], and quaternary (Cu₂ZnSnS₄, CuInGaSe₂) groups [11]. The electroplating of elemental semiconductors and other wide bandgap nitrides has also been captured in the literature. This communication critically appraises the strengths, weaknesses, potentials and the state-of-the-art electroplating technique in the fabrication of large-area electronics and other macro-electronic devices such as photovoltaic (PV) solar panels and display devices.

2 An overview of electrodeposition technique

Electrodeposition is the process of depositing elemental or compound metals or semiconductors on a conducting substrate by passing an electric current through an ionic electrolyte in which metal or semiconductor ions are inherent [12]. The passage of current is required due to the inability of the chemical reaction resulting in the deposition of the solid material on the conducting substrate to proceed on its own as a result of positive free energy change ΔG of the reaction.

Electrodeposition can be categorised based on power supply source, working electrode and electrode configuration (as shown in Figure 1) but the basic deposition mechanism and setup remains similar. The basic deposition mechanism entails the flow of electrons from the power supply to the cathode. The positively charged cations are attracted towards the cathode and negatively charged anions to the anode. The cations or anions are neutralised electrically by gaining electrons (through reduction process) or losing electrons (through oxidation process) and being deposited on the working electrode (WE) respectively [12].

The typical electrodeposition (ED) setup of two-electrode (2E) configuration as shown in Figure 2 (a) consist of deposition container (beaker), deposition electrolyte, magnetic stirrer, hotplate, power supply, a working electrode, a counter electrode and an optional reference electrode (RE) in the case of 3-electrode (3E) configuration (see Figure 2 (b)). The use of potentiostatic power source was due to the effect of deposition voltage on the atomic percentage composition of elements in the electrodeposited layer, which is one of the factors determining the conductivity type [13,14]. Cathodic deposition is mainly utilized due to its ability to produce stoichiometric thin-films with good adherence to the substrate as compared to anodic deposition [15]. Conversely, the galvanostatic electrodeposition is controlled and measured by maintaining constant current density through an electrolytic cell disregarding the changes in the resistance due to the deposited electroplated layer.

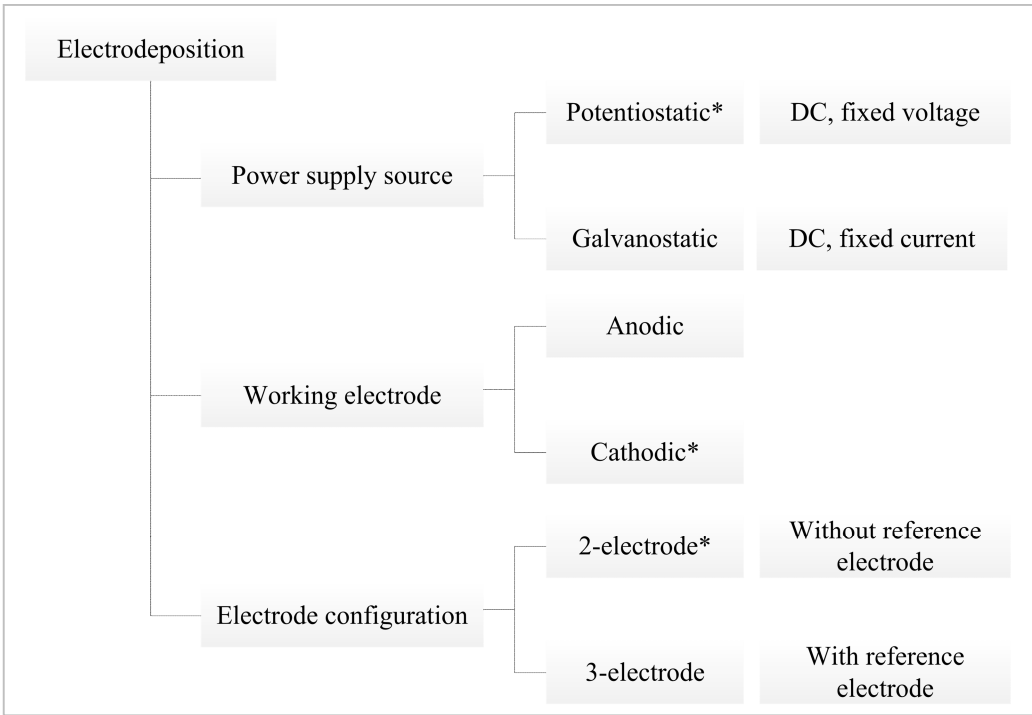


Figure 1: The main categories of electrodeposition technique.

The 2E configuration as shown in Figure 2 (a) was utilised due to its industrial applicability, process simplification and also to eliminate possible Ag^+ and K^+ ions doping [16,17] which may emerge from the Ag/AgCl or saturated calomel electrode (SCE) reference electrodes (see Figure 2 (b)). Taking the electrodeposition of $n\text{-CdS}$ and $n\text{-CdTe}$ layers which are respectively utilised as the main window and absorber layers in this work into perspective,

both K^+ and Ag^+ from group I of the periodic table are considered as *p*-type dopants. Therefore, any leakage of K^+ and Ag^+ into the electrolytic bath may result in compensation leading to the growth of highly resistive material which has a detrimental effect on the efficiency of fabricated solar cells. This has been experimentally shown and reported in the literature [16].

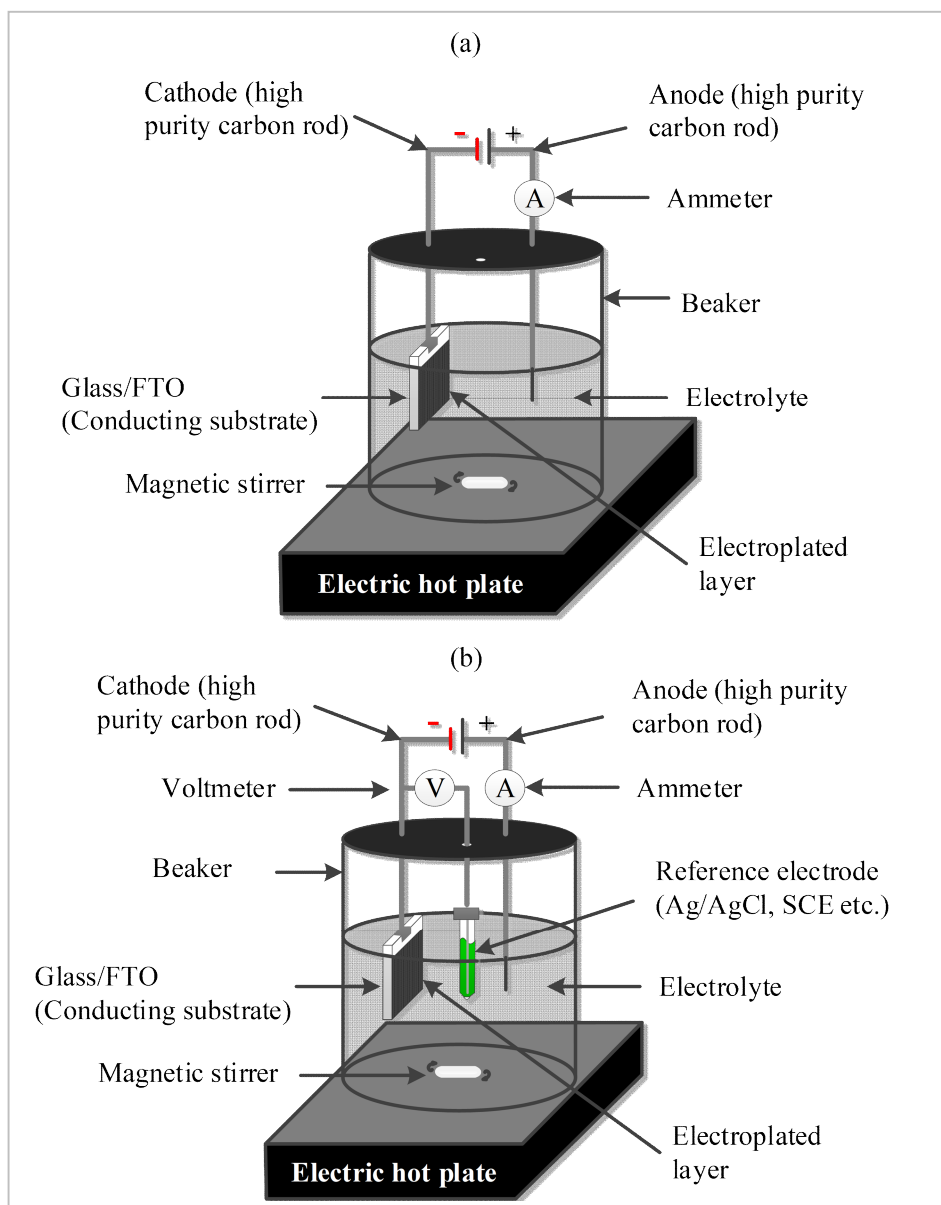


Figure 2: Typical (a) two-electrode and (b) three-electrode electrodeposition set up.

The two-electrode electrodeposition configurations are not without challenges, with the main challenge being the fluctuation or drop in the potential measured across the cathode and the anode during deposition. This is due to the alteration in resistivity of the substrate with

increasing semiconductor layer thickness and the change in the ionic concentration of the electrolyte. Unlike the 3-electrode configuration, the potential difference is measured across the working and the reference electrodes while the measured current is between the working and the counter electrodes. In general, other factors such as the pH of the electrolyte [18], applied deposition potential [13,14], deposition temperature [19], stirring rate [20], deposition current density, duration of deposition and thickness [21], underlying substrate [22], and concentration of ions in the deposition electrolyte [18] affects the electrodeposition process and the properties of the deposited layers. Recent publications have demonstrated the similarities between electrodeposited semiconductors using 3-electrode and 2-electrode electroplating configuration [23,24]. The electrodeposition of both elements and compounds is governed by Faraday's laws of electrodeposition as mathematically depicted in Equation (1).

$$T = \left(\frac{1}{nF} \right) \left(\frac{itM}{\rho A} \right) = \left(\frac{JtM}{nF\rho} \right) \quad (1)$$

where T is the thickness (cm), J is current density (Acm^{-2}), t is the deposition time (s), M is the molecular mass (gmol^{-1}), n is the number of electrons transferred in the chemical reaction for the formation of 1 mole of substance in gcm^{-3} , F is the Faraday's constant (96485 Cmol^{-1}), and ρ is the density (gcm^{-3}). It should be noted that the Faraday's law of electrolysis assumes that all the electronic charges pass through the electrolyte contribute to the deposition of deposited material layer without any consideration of the resistance losses in the system and electronic charge contribution to the decomposition of solvent into its constituent ions [25].

3 Factors influencing electrodeposition

3.1 Solutes, solvents and the deposition Electrolytes

The effects of the incorporated solute and solvent utilised are of importance in electrodeposition. Taking the electrodeposition of CdS into consideration, sodium (Na) based precursor ($\text{Na}_2\text{S}_2\text{O}_3$) has been often utilised [26,27]. Although sodium (Na) ions are not electrodeposited at low cathodic voltages, the incorporation of Na in CdS films is achievable through adsorption, absorption or chemical reactions as a result of increased Na accumulation in the electrolytic bath. It should be noted that Na is a p-type dopant in CdS [28] resulting into increasing electrical resistivity of subsequent CdS layers due to Na accumulation. Further to this, the Na-based precursor ($\text{Na}_2\text{S}_2\text{O}_3$) is also associated with the precipitation of sulphur during the electroplating. Recent understanding has shown that the replacement of

the well-established sulphur precursor with thiourea (NH_2CSNH_2) (which is more associated with chemical bath deposition (CBD) technique) results in the reduction/elimination of sulphur precipitate [29,30].

The choice of solvent to be utilised also possesses as an important factor in electroplating as demonstrated by the deposition of CdTe from ethylene glycol ($\text{C}_2\text{H}_6\text{O}_2$) electrolyte containing cadmium iodide (CdI_2) [31]. Using aqueous solution as solute, Cd-I complexes such as CdI^+ , CdI_2 , CdI_3^- and CdI_4^{2-} are formed in aqueous solution [32,33] debarring the deposition of Cd and the co-deposition of CdTe. it is noteworthy that CdTe from other Cd precursors have been explored and reported in the literature [34,35]. Therefore the choice of solute and solvent for electroplating purposes is a factor to reckon with in addition to a number of other factors inherent in the electrodeposition process to achieve superior qualities of electroplated semiconductor materials. This understanding has been accrued for over two decades of exploration, and careful examination of grown semiconductors at Solar Energy Group within Sheffield Hallam University (SHU), in addition to the literature. A large number of semiconductors explored in SHU is summarised in Table 1.

Table 1: Summary of explored electronic materials to date at authors' research group using electroplating from aqueous solutions.

Material electroplated	E _g (eV)	Precursors used for electroplating	Comments	Ref.
CuInSe ₂	~1.00	CuSO ₄ for Cu ions, In ₂ (SO ₄) ₃ for In ions and H ₂ SeO ₃ for Se ions	Ability to grow both p- and n-type material.	[9]
CdTe	1.45	CdSO ₄ or Cd(NO ₃) ₂ or CdCl ₂ for Cd ions and TeO ₂ for Te ions	Ability to grow both p- and n-type CdTe using Cd-Sulphate, Nitrate and Chloride precursors.	[75,77]
CuInGaSe ₂	1.00-1.70	CuSO ₄ for Cu ions, In ₂ (SO ₄) ₃ for In ions, Ga ₂ (SO ₄) ₃ for Ga ions and H ₂ SeO ₃ for Se ions	Ability to grow both p- and n-type material.	[59]
CdSe	1.90	CdCl ₂ for Cd ions and SeO ₂ for Se ions	<i>Work is in progress</i>	[82]
InSe	1.90	InCl ₃ for In ions and SeO ₂ for Se ions	<i>Work is in progress</i>	[83]
GaSe	2.00	Ga ₂ (SO ₄) ₂ for Ga ions and SeO ₂ for Se ions	<i>Work is in progress</i>	
ZnTe	1.90-2.60	ZnSO ₄ for Zn ions and TeO ₂ for Te ions.	Ability to grow both p- and n-type material.	[84]
CdS	2.42	CdCl ₂ for Cd ions and Na ₂ S ₂ O ₃ , NH ₄ S ₂ O ₃ or NH ₂ CSNH ₂ for S.	Conductivity type is always n-type.	[29,74,85]
CdMnTe	1.57-2.50	CdSO ₄ for Cd ions, MnSO ₄ for Mn ions and TeO ₂ for Te ions	<i>Work is in progress</i>	
ZnSe	2.70	ZnSO ₄ for Zn ions and SeO ₂ for Se ions.	Ability to grow both p- and n-type material.	[86]
ZnO	3.30	Zn(NO ₃) ₂ for Zn ions		[87]
ZnS	3.75	ZnSO ₄ for Zn and (NH ₄) ₂ S ₂ O ₃ for S ions	Ability to grow both p- and n-type material.	[54]
Poly aniline (PAni)	-----	C ₆ H ₅ NH ₂ and H ₂ SO ₄	To use as a pinhole plugging layer.	[88]

3.2 Electrolytic bath pH value

The composition of an electrolytic bath naturally determines the pH of the bath. Basically, the acidity ($\text{pH} < 7.00$) of an electrolyte can be increased by the introduction of an acid. The hydrogen ions (H^+) from the dissociated acid reacts with water in aqueous solution to form hydronium ions (H_3O^+). On the other hand, the alkalinity of a solution increases ($\text{pH} > 7.00$) with the reduction in the H_3O^+ concentration. This is caused by the reaction of dissociated hydroxide ions (OH^-) from introduced alkaline with H^+ ions from water dissociation to form water (H_2O) rather than hydronium ions. It is well documented that elemental and compound deposition responds to this chemical dynamic mainly in wet deposition techniques such as chemical bath deposition (CBD) [36] and electrodeposition techniques [37]. With emphasis on electrodeposition, the effect of pH of the bath and the deposited layers vary from selective deposition/etching of element [38], alteration of the characteristic properties of the deposited layers [39,40], elemental/compound precipitation [41] and increase in the deposition current density [42]. Furthermore, the effect of pH on the dissociation of common solvent such as water is also well documented in the literature [43]. With the notion that increase in acidity of electroplating bath resulting into the increase in the concentration of dissociated ions in the aqueous solution [43]. Due to the increased ionic concentration, the deposition current density increases until it stabilises or continues to increase, depending on the composition of the solution.

3.3 Deposition temperature

It is a known fact that an increase in the temperature of a matter increases the motion of the molecules inside it. As such, the electrolytic bath temperature increases solubility of the solvent, catalyses the reactions, energizes the ions and increases the transport number, which results to an increase in the deposition current density and rate of deposition of constituent element or compound. Further to this, the work performed on electrodeposition depicted that an increase in the crystallinity of as-deposited semiconductor material is achievable at higher growth temperature [3,44]. For electroplated semiconductor materials from aqueous solution, there is a limitation on the growth temperature due to the boiling temperature of water at 100°C under standard temperature and pressure. While the electroplating from other electrolytic bath can go as high as 160°C [31]. Deposition of materials at higher temperature provides energy required for ions/atoms to move around and deposit in a regular crystalline pattern.

3.4 Deposition current density

With regards to Faraday's law of electrodeposition, the deposition current density is directly related to the thickness of the deposited layer. Thus, the deposition current density is dependent on factors effecting the energizing of the inherent ions in the electrolyte such as stirring rate, bath temperature, concentration of constituent [45] and electrical conductivity of the substrate amongst other constraints. While a gradual alteration in the deposition current density is expected depending on the electrical conductivity of the electroplated layers.

With respect to semiconductor materials such as CdTe, literature depicts the effect of current density on the morphological, compositional and the structural properties of the deposited layer [46,47]. Based on the deposition configuration, it can be inferred that the deposition current density of 3-electrode configuration and 2-electrode deposition configuration vary. CdTe with optimal characteristic properties deposited from a 3-electrode deposition is known to lie between $\sim(0.3 \text{ to } 0.6) \text{ mAcm}^{-2}$ [45,48]. While 2-electrode electrodeposition has been documented to produce CdTe layers with optimal characteristic property of $\sim(0.15 \text{ to } 0.18) \text{ mAcm}^{-2}$ [49]. Under potentiostatic mode, Basol 1988, clarified that the deposition current density for CdTe electroplating depends on the tellurium concentration in the electrolyte [45]. The incorporation of excessive Te can alter the composition of the deposited CdTe, conduction type to p-CdTe due to Te-richness [50], and reduced adhesion on the underlying substrate. Reduction in the adhesion of CdTe may also occur due to the deficiency of Te concentration in the electrolytic bath. In either condition (excess or deficiency of Te concentration in the electrolyte), the crystallinity, morphology and adhesion of the ensued CdTe layer suffer.

3.5 Duration of deposition and thickness

Electroplating of materials with main emphasis on semiconductor commences by the nucleation of the most electropositive element on the points on the conducting substrates with the highest electric field. Therefore, it can be categorically stated that the nucleation and nucleation modes of semiconductor material is conductive substrate dependent [1,22,51]. Consequential to the surface roughness of the underlying working electrode such as glass/fluorine doped tin oxide (g/FTO), the highest electric field is experienced at the peaks of the rough surfaces. The nucleation of the electroplated material spreads out through to the lowest valley from the initiation rough surface peaks resulting into columnar nature of the deposited layers [14]. The potency of this mechanism is highly influential at the initial stages of deposition due to unevenness of the deposited layer thickness characterised by pin-holes,

voids, gaps and high dislocation density within the semiconductor material [21]. This characteristic property is detrimental when thin semiconductor layer with thickness of <100 nm is required [21].

4 Strengths and Weaknesses of Electrodeposition

4.1 Strengths of electrodeposition

4.1.1 Electrolytic bath life longevity and Self-purification

At the start of an electrolytic bath, electro-purification of the bath is highly essential to reduce and eliminate the impurity level which is mostly incorporated in the precursors amongst other impurity sources. It should be noted that even with high purity precursor with 99.999% purity carry impurity level of 10 part per million (ppm). The purification is essential due to the effect of impurities even in ppm levels [52] on the characteristic properties of electroplated semiconductor materials. It should be noted that electro-purification of a bath must be performed using similar deposition parameters (such as bath temperature, pH, stirring rate etc.) to the semiconductor deposition. The electro-purification potential utilised should be lower than the deposition potential range of the required elements established using cyclic voltammetry. Based on this characteristic property of electroplating technique, the more layers are deposited, the purer the electrolyte and the electroplated semiconductor gets due to the gradual reduction of background impurities and improved material property. This property does not only increase the purity of the electrolyte and the deposited semiconductor but also increase the longevity of the bath as compared to the batch process of chemical bath deposition (CBD) technique.

To further mitigate other sources of impurities, a fraction of researchers choose 2-electrode over the 3-electrode configuration to avoid possible impurities from the reference electrode. While the usage of Teflon-ware (polypropylene beaker) is necessitated to house the electrolyte due to possible leaching of elemental sodium and other dopant from glass-ware [53] into acidic electrolytes.

4.1.2 Ease of doping - intrinsic and extrinsic

With the effective purification of the electrolyte, intrinsic doping has been demonstrated in the literature for binary [54,55], ternary [56] and quaternary [57,58] semiconductor materials by changing the deposition voltage. Taking an example of a I–III–VI₂ semiconductor materials such as CuInGaSe₂, the stoichiometric semiconductor layer consists of 25% of the

group I element, 25% of the group III elements and 50% of group VI element. Due to the positive reduction potential of Cu ($E_o=0.52$ V), at low deposition voltages, high elemental composition of Cu (group I) is incorporated in the semiconductor resulting into p-type conduction type. But an increase in the cathodic voltage increases the elemental composition of In resulting in an n-type semiconductor material as in the case of CuInSe₂ (see Figure 3 (a)). While at intermediate voltages, the material exhibits insulating or intrinsic properties. This electrical characteristic property as demonstrated in the literature [56–58] signify the ability of growth of p-, i- and n- type materials from the same bath by cathodic voltage variation (see Figure 3). The incorporation of Ga in CuInGaSe₂ [59] increases the bandgap and also make the material p-type. This must be due to the formation of acceptor-like defect in the material (see Figure 3 (b)).

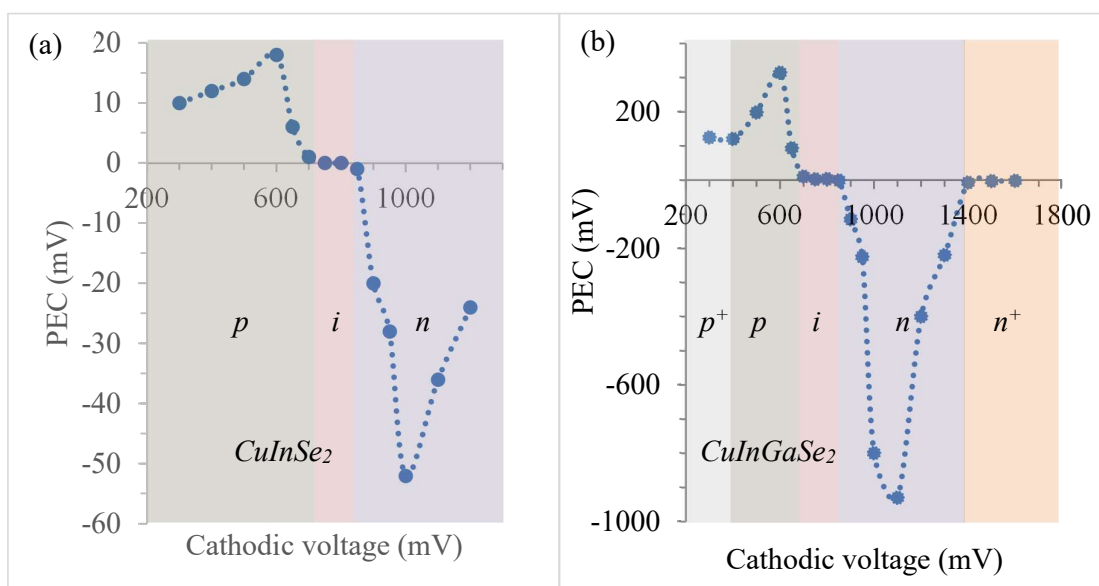


Figure 3: PEC signal for (a) CuInSe₂ and (b) CuInGaSe₂ with increasing cathodic voltages. Note the ability to grow p⁺, p, i, n and n⁺ materials from the same electrolyte, simply by varying the deposition voltage [56–58].

The effect of cathodic voltage on the elemental composition of binary semiconductor has also been demonstrated and documented in the literature [14,50]. The effect of alteration in the growth voltage on the elemental composition of electroplated materials even for as low as 1 mV step has been documented [29] (see Figure 4).

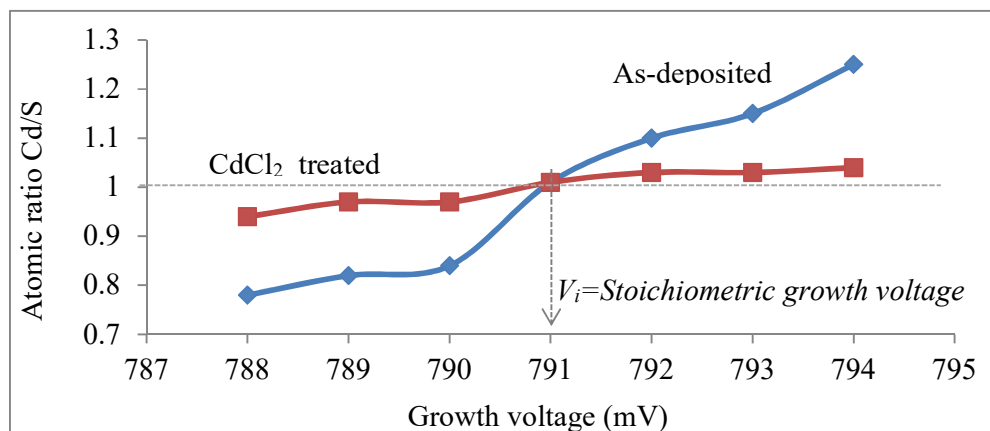


Figure 4: Atomic compositions ratio of Cd to S in as-deposited and CdCl₂ treated CdS thin films at different deposition cathodic voltages.

The ease of intrinsic doping and the effect of extrinsic doping of electroplated semiconductor materials have been well established in the literature [52,60]. Due to the simplicity of ED, doping at parts-per-million (ppm) level is made possible [52,60,61].

4.1.3 Bandgap engineering capability

The Control or alteration of the bandgap of materials (with emphasis on semiconductor) is easily achievable in electrodeposition technique. Typically, this can be achieved by controlling the atomic composition of the elemental component of the semiconductor material. Intrinsically, electrodeposition have the ability to change the composition of growing material by a simple alteration of the cathodic voltage [54,56–58]. An ensuing alteration in the bandgap of grown semiconductor material due to change in the growth cathodic voltage has been documented in the literature [59]. It is well known that an increase in the atomic concentration of Ga in CuInGaSe₂ by increasing the cathodic voltage increases the bandgap of CuInGaSe₂. While a reduction in the cathodic voltage of the CuInGaSe₂ result in the reduction of bandgap due to the richness of Cu [59] (see Figure 5). This ability provides the ease of bandgap engineering of semiconductor material such as CuInGaSe₂ between $\sim(1.00$ to $2.20)$ eV. Extrinsically, this observation has also been documented for electroplated binary semiconductor materials such as CdTe doped with Ga [52] amongst others. With the bandgap of the resulting doped semiconductor directly affected with the incorporated dopant even at parts per million levels [52,60].

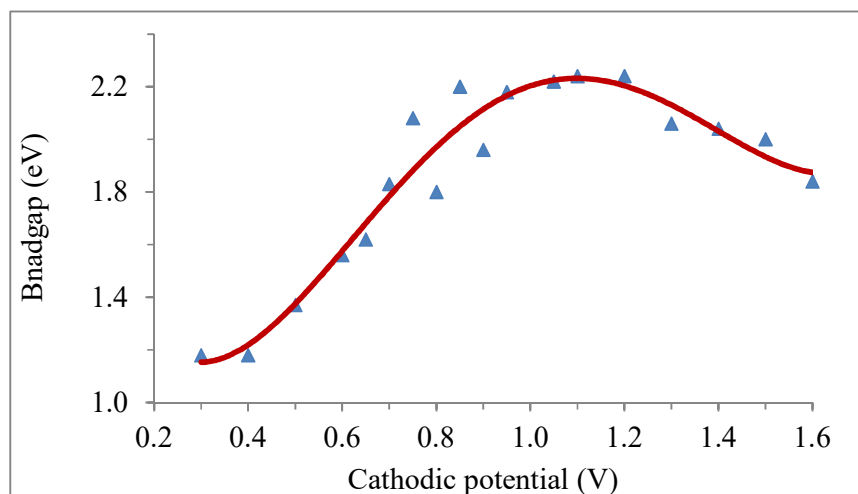


Figure 5: Energy bandgap variation for CuInGaSe₂ as a function of the cathodic voltage.

4.1.4 Low-cost and simplicity

There are over 14 different and well-established techniques to grow thin-film semiconductor materials [62] which can be broadly categorised under physical or chemical deposition. The physical deposition refers to the technologies in which material is released from a source and deposited on a substrate using thermodynamic, electromechanical or mechanical processes [1,63]. While the chemical deposition techniques are accomplished by the utilisation of precursors either in their liquid or gaseous state to produce a chemical reaction on the surface of a substrate, leaving behind chemically deposited thin-film coatings on the substrate. Electrodeposition falls under the chemical deposition techniques which can be carried out in an uncontrolled environment and without a vacuum system. The setup for electroplating which is mainly constituted of computerized potentiostat and hotplate/magnetic stirrer with a cost implication of £5000 as compared to other techniques. As compared to the well-established metallorganic chemical vapor deposition (MOCVD) or close space sublimation (CSS) system with an high initial cost implication of about £1 million. In addition, these systems have limitations as concerning the materials that can be grown. Furthermore, the relatively low heat energy required during growth and post growth treatment makes electroplating a more energy-economic deposition technique as compared to a large number of other techniques. More importantly grown semiconductor layers using cost-effective electroplating technique is comparable to semiconductor layers grown using highly expensive techniques [29,64] and they all require post-deposition treatments [65,66].

4.1.5 Scalability and manufacturability

The scalability and manufacturability of electroplating has been demonstrated on an industrial scale by BP solar in the 1980s and 1990s [67,68]. BP solar manufactured CdTe-based solar cells with solar panel area $\sim 1 \text{ m}^2$ with a conversion efficiency of $\sim 10\%$ [67,68]. As compared to the laboratory scale setup as shown in Figure 2, scaling up requires a larger tank to contain the electrolyte and multi-plate cathode attached to multiple conducting substrates. The use of larger tanks and multi-plate cathode increases the throughput of deposited layers and an added advantage of electroplating on intricate shapes and designs.

4.2 Weaknesses of electrodeposition

One of the main disadvantages of electrodeposition includes the need for a conducting substrate as the working electrode in the electroplating setup. Due to this requirement, using conventional characterisation technique such as Hall Effect to determine the electrical properties of the deposited layers on FTO for example will not be possible due to the underlying conducting layer.

4.2.1 Instability of current density during deposition

The control of the electrodeposition process due to the alteration of current density with increasing deposition layer thickness is a challenge (under potentiostatic condition). The electroplating of materials with electrical conductivity level lower than the primary substrate results in the reduction of current density with direct relationship with the thickness of the deposited material [69]. This observation is common for both 2E and 3E electroplating configurations but the applied voltage can vary slightly in 2E configuration.

4.2.2 Control and regulation of ions within the electrolytic bath

Control and regulation of ions within the electrolytic bath – as a result of depletion in the ionic concentration and the inability to gauge/measure ionic concentration in the electrolyte during layer deposition, replenishing the bath with the appropriate chemical concentration is vague. Thereby reducing reproducibility tendencies.

4.2.3 Formation of solution based complexes

There is a possibility for the formation of complexes within the electrolyte which might be debarring the deposition of element and/or the co-deposition of a compound [32,33]. This is the case of the deposition of CdTe from aqueous solution containing CdI_2 as the Cd-

precursor. Literature shows that due to the formation of Cd-I complexes in aqueous solution, only p-CdTe layers due to Te-richness is possible [32,33]. Unnecessary precipitation remove chemicals from the electrolyte, changing the elemental concentration in the bath.

4.2.4 Extrinsic doping of electrolytic bath by the electrodes

Control of purity throughout the electrolytic bath lifespan – as there has been an observation of increased carbon concentration in deposited semiconductor layers. The incorporation of carbon into the electrolytic bath is due to the deterioration of the anode utilised in the electrolytic cell setup.

4.2.5 Non-uniformity of electrodeposited semiconductor layers

Due to the unevenness of the underlying conducting substrate such as transparent conducting oxide (TCO), the highest electric field is experienced at the peaks of the rough conducting substrate surfaces. Nucleation starts at the peaks and spreads out through to the lowest valley resulting into layers with columnar nature [14].

5 All-electroplated photovoltaic devices

Electrodeposited cadmium telluride (CdTe) and copper indium gallium selenide (CIGS) are amongst the commonly used absorber layers in all-electrodeposited photovoltaic applications [45,70]. The versatility of the technique in the growth of all-electrodeposited configuration has been well documented [13,71–73]. The band diagrams of possible n-p and n-n⁺ large Schottky barrier junctions are shown in Figure 6 fabricated using CdS/CdTe configuration. The full characterisation process of both the CdS and CdTe are documented in the literature [74,75]. The electronic properties of the fabricated photovoltaic cells obtained using current-voltage (I-V) and capacitance-voltage (C-V) techniques are summarised in Table 2.

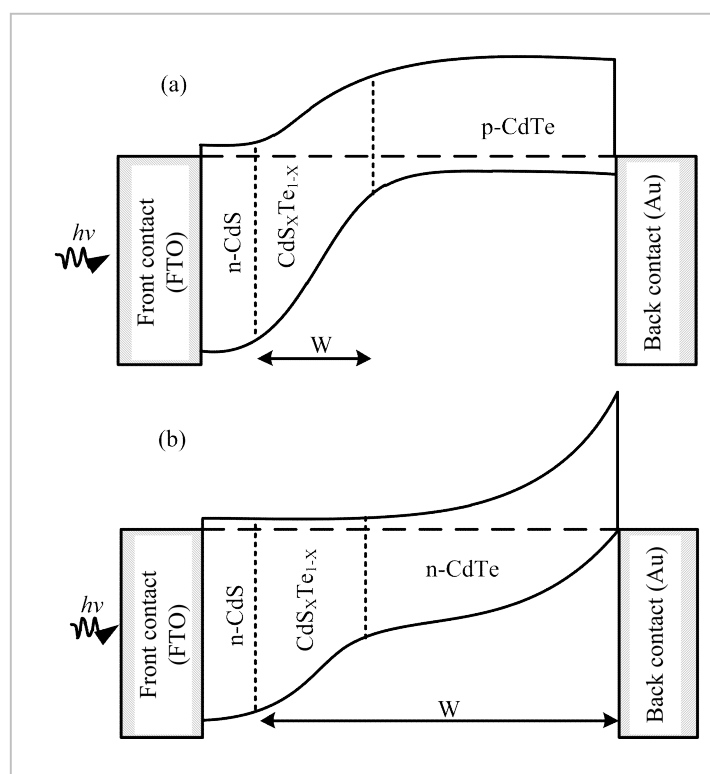


Figure 6: Energy band diagrams representing (a) glass/FTO/n-CdS/p-CdTe/Au and (b) glass/FTO/n-CdS/n-CdTe/Au device configurations.

It is well known that intrinsic CdS is n-type and remains n-type due to the inherent defect as a result of the presence of S vacancies and Cd interstitials in the crystal lattice of the deposited CdS layers [76]. The devices are fabricated by incorporating CdTe deposited at the vicinity of the transition voltage (V_i) from p-type to n-type CdTe or vice versa. Electroplated CdTe can either be p-type (when Te rich) or n-type (when Cd rich) material under as-deposited condition. While a retention or transition of electrical conduction type is possible after cadmium chloride treatment. It is noteworthy that the conversion of the electrical conduction type after post-growth treatment may be attributed to the doping effect as a result of the heat treatment temperature, duration of treatment, initial atomic composition of Cd and Te, the concentration of CdCl₂ utilised in treatment, defect structure present in the starting CdTe layer and the material's initial conductivity type as documented in the literature [75,77,78]. Therefore depending on the final electrical conduction type, the possible device configurations are possible, and the analysis of device results must be performed with extreme care.

Table 2 summarises the results of CdS/CdTe solar cells made with CdTe layers grown in the vicinity of $V_i=1370$ mV. Below the V_i , the CdTe layers are p-type and therefore the devices made are p-n junctions (see Figure 6 (a)). Above the V_i , the CdTe layers are n-type and hence the device structures are n-n +Schottky barrier (see Figure 6 (b)). As shown in Table 2, the devices fabricated with n-CdTe performs better than those made with p-CdTe layers.

Table 2: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for simple CdS/CdTe-based solar cells grown at different growth voltages in the vicinity of $V_i=1370$ mV.

CdTe growth voltage (mV)	1340	1360	1370	1380	1400
I-V under dark condition					
$R_{sh} (\Omega)$	1016	$>10^5$	$>10^5$	$>10^5$	$>10^5$
$R_s (k\Omega)$	0.21	0.80	0.50	1.43	1.50
$\log(RF)$	0.4	3.5	3.9	3.3	3.0
$I_0 (A)$	2.5×10^{-5}	3.9×10^{-9}	1.0×10^{-9}	3.2×10^{-9}	5.0×10^{-9}
n	>2.00	1.95	1.86	1.58	1.86
Φ_b (eV)	>0.52	>0.76	>0.81	>0.77	>0.77
I-V under 1.5 AM illumination condition					
I_{sc} (mA)	0.53	0.62	0.65	0.82	0.57
J_{sc} (mAcm $^{-2}$)	16.88	19.75	20.70	26.11	18.15
V_{oc} (V)	0.23	0.49	0.72	0.60	0.57
Fill factor	0.31	0.46	0.50	0.45	0.48
Efficiency (%)	1.20	4.45	7.50	7.05	4.97
C-V under dark condition					
$\sigma \times 10^{-4} (\Omega.cm)^{-1}$	1.41	/	2.85	/	6.03
N_A or N_D (cm $^{-3}$)	7.74×10^{16}		3.10×10^{14}		9.10×10^{14}
μ (cm $^2V^{-1}s^{-1}$)	0.01		5.74		4.14
C_o (pF)	1630		330		370
W (nm)	187.6		926.7		826.5

CdTe-based devices assuming p-CdTe in CdS/CdTe devices has been documented in the literature [27,79]. But based on recent observations, the incorporation of Cd-rich CdTe absorber layer produce high efficiencies. These effects have been independently observed and reported [80,81] and mainly attributed to the reduced defects in Cd-rich CdTe (*the layers are deposited using physical deposition processes*).

Using mainly n-CdTe absorber layers, few devices incorporating all-electrodeposited from the SHU group have been documented in the literature and summarised in Table 3.

Table 3: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for glass/FTO/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells.

Configuration Properties	g/FTO/n-CdS/n-CdTe/Au (Two-layer device)	g/FTO/n-CdS/n-CdTe/p-CdTe/Au (Three-layer device)	g/FTO/n-CdS/n-CdTe/p-CdTe/Cu-Au (Three-layer device)	Glass/FTO/n-ZnS/n-CdS/n-CdTe/Au (Three-layer device)
I-V under dark condition				
$R_{sh} (\Omega)$	$>10^5$	$>7.2 \times 10^5$	10^6	$>10^5$
$R_s (k\Omega)$	0.50	0.50	0.92	0.47
$\log(RF)$	3.9	4.1	3.5	4.8
$I_o (A)$	1.0×10^{-9}	1.0×10^{-9}	3.16×10^{-9}	1.0×10^{-9}
n	1.86	1.86	1.68	1.60
$\Phi_b (eV)$	>0.81	>0.80	>0.80	>0.82
I-V under 1.5 AM illumination condition				
$I_{sc} (mA)$	0.65	1.06	1.85	1.07
$J_{sc} (mAcm^{-2})$	20.70	33.80	58.9	34.08
$V_{oc} (V)$	0.72	0.73	0.64	0.73
Fill factor	0.50	0.62	0.50	0.57
Efficiency (%)	7.50	15.3	18.5	14.18
C-V under dark condition				
$\sigma \times 10^{-4} (\Omega.cm)^{-1}$	2.85	-----	-----	8.82
$N_D - N_A (cm^{-3})$	3.10×10^{14}	6.67×10^{14}	1.82×10^{14}	7.79×10^{14}
$\mu (cm^2V^{-1}s^{-1})$	5.74	-----	-----	7.07
$C_o (pF)$	330	395	160	280
$W (nm)$	926.7	-----	-----	1092.2

6 Conclusion

This work describes electroplating as a robust material deposition technique with wide applications ranging from surface protection to large-area electronics and nano-technology while focusing on semiconductor deposition. The manuscript also reviews the pros and cons of electroplating technique. The effect of growth parameters such as temperature, pH, stirring rate, precursor, solvent and cathodic voltage, and post-growth heat treatments of the deposited were iterated. The capability of electroplated material to be comparable and possibly superior to semiconductor materials grown using other cash intensive techniques are

also highlighted with experimental evidence. Electroplated materials can be applicable in large area devices such as photovoltaic solar panels and large area display panels in which intricate shapes are required. Bandgap grading, alteration of elemental composition and different conductivity type are also possible intrinsically with a change in the cathodic voltage. Other advantages such as columnar growth of nanorods which are tightly-packed and normal to the substrate could trigger many new applications in the nanotechnology area.

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