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Article

Elimination of Common-Mode Voltage in Dual Two-Level Voltage Source Inverter Fed Open-end Load using a Discontinuous SVM Technique

Nuttawout Buarat[1] and Yuttana Kumsuwan[2,*]

[1, 2] Department of Electrical Engineering, Faculty of Engineering, Chiang Mai University, Chiang Mai, Thailand
[1] nuttawout@hotmail.com
* Correspondence: yt@eng.cmu.ac.th; Tel.: +66-5394-4135 ext. 4140

Abstract: The popular motor drive systems with a single two-level voltage source inverter (VSI) have one main problem that is the occurrence of the common-mode voltage (CMV), which is an effect of the electromagnetic interference, shaft voltage, bearing currents, leakage current. These cause the high stress, increasung temperature and early mechanical failure in machine. To overcome this problem, the technology of the dual two-level VSI fed open-end three-phase ac loads is now available to eliminate the CMV at the ac/induction motor load with the 120-degree modulation technique for controlling each inverter. In this paper, the discontinuous space vector modulation (DSVM) schemes are proposed and applied for the dual two-level VSI fed open-end load. It is based on the 120-degree modulation technique by using only 12 active voltage vectors and the 10 zero voltage vectors from the total 64 voltage vectors along with the different five-segment swicthing sequence designs with centralizing pulse width modulation technqiue in order to not only cancel the CMV in the ac load, but also reduce the switching number/switching loss of the conversion system. Among the various DSVM schemes, their performances are compared in this paper, such as the number of the switching, the step and peak value of the CMV in each inverter, and the quality of the output waveform, etc. The details of the verfication and comparison are carried out by simulation using Matlab/Simulink software.

Keywords: dual two-level voltage source inverter; common-mode voltage; discontinuous space vector modulation schemes; centralizing pulse width modulation; open-end load.

1. Introduction

In view of the two-level voltage source inverter (VSI), it has been incessantly important and extensively available for long-term industrial applications, such as adjustable speed drives, renewable energy conversions, power conditions, and power protections, etc. In spite of its uncomplicated and flexible circuit structure and control algorithms, there runs into some problems itself. One fundamental problem is the induced common-mode voltage (CMV), especially in the loads of motors, resulting in the electromagnetic interference (EMI), shaft voltage, bearing currents, leakage current, and so on, which influence a high stress and temperature in machine, undesirable losses, and finally the early mechanical failure [1].

There are two typical group methods of solving the aforementioned problem. The first one is the hardware solutions, such as the additional *RLC* filter equipment method proposed in [1]. This is difficult to the design of the parasitic elements due to a high order system and it is an inflexible method. Another one is the software solutions, such as pulse-width-modulation (PWM) modification methods reviewed in [2]. Among these methods, they are able to achieve more saving

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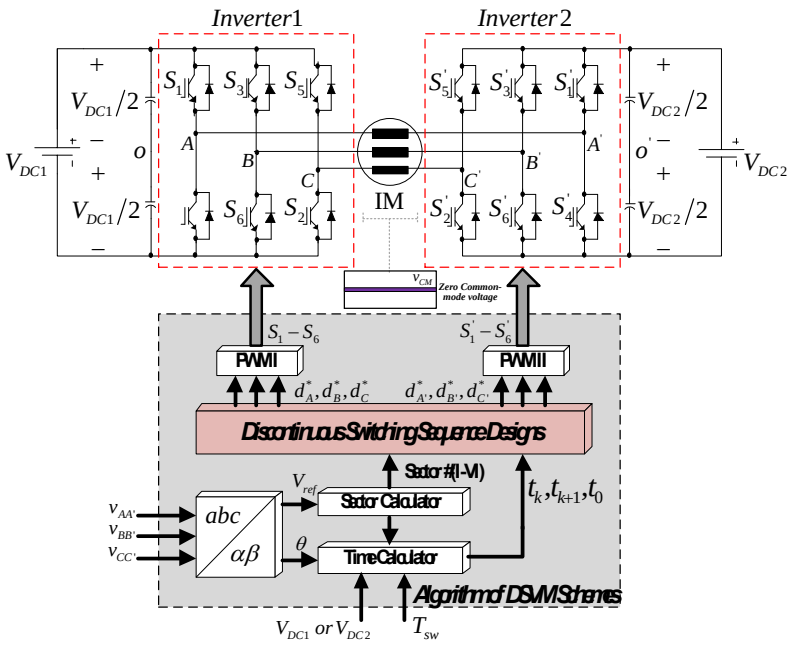

Figure 1. A simplified schematic circuit of the two isolated-dc-supply two-level voltage source inverter (VSI) fed open-end three-phase AC loads with the proposed discontinuous space vector modulation (DSVM) technique.

cost and sizing, and also more flexible procedure in comparison to its counterpart. Although all the hardware and software solutions for the two-level VSI system can suppress the CMV in the loads, they are not able to completely eliminate the CMV anyway. Hence, the CMV still exists and also impacts on the electrical machine load.

Removing the CMV in the desirable loads [3], there are two structures of the dual two-level VSI fed open-end loads. Structure of the single dc source is applied. According to its advantage of only one dc source/front-end rectifier stage consuming, the zero-sequence voltage is however appeared in the load/motor, which leads to the zero-sequence current through the motor creating the distortion and increasing of the root mean square (RMS) value of the output current. Therefore, the two isolated dc source structure is introduced to prevent the zero-sequence component flow through the motor. In [4], a remarkable continuous space vector modulation (CSVM) technique for the dual two-level VSI with two isolated dc supplies fed open-end loads is proposed. However, the number of the switching is very high, as double as compared with the traditional systems [1] and [2].

This paper presents the discontinuous SVM (DSVM) technique for the dual two-level VSI with two isolated dc supplies fed open-end loads, as shown in Figure 1. This is done by using only six active voltage vectors and a zero voltage vector for arrangement in the concept of five-segment switching sequence with centralizing PWM scheme. The major contribution of this paper is to entirely eliminate the CMV at the open-end loads. The other goals are to reduce the switching number, which can reduce the switching loss from [4], and lastly reduce the step and peak value of the CMV of each inverter, which can reduce the CM current as well.

2. Proposed Discontinuous SVM Technique for Dual Two-Level Voltage Source Inverter fed Open-End Load

Referring to Figure 1, the configuration of the power circuit is consisted of two sets of the two-level VSIs driving the open-end three-phase AC loads, where the inverter connected to the dc voltage source V_{DC1} and the anterior terminal of the three-phase loads is called inverter 1 and another one connected to the dc voltage source V_{DC2} and the posterior terminal is namely inverter 2. According to the figure, the following terms of the three-phase output voltages are

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$$\begin{cases} V_{AA'} = V_{AO} - V_{A'O'} \\ V_{BB'} = V_{BO} - V_{B'O'} \\ V_{CC'} = V_{CO} - V_{C'O'} \end{cases}, \tag{1}$$

where V_{AO}, V_{BO}, V_{CO} are the pole voltages for phases *A*, *B*, and *C* of the inverter 1. $V_{A'O'}, V_{B'O'}, V_{C'O'}$ are the pole voltages for phases *A*, *B*, and *C* of the inverter 2. $V_{AA'}, V_{BB'}, V_{CC'}$ are the phase-A, -B, and -C output voltages.

According to (1), the phase output voltages of the open-end loads are generated by the interactive operation between dual two-level VSIs. Therefore, based on the principle of the CMV in the single two-level VSI systems, the CMVs of the dual two-level VSI fed open-end loads can be formulated by

$$\begin{cases} V_{CM1} = \dfrac{v_{AO} + v_{BO} + v_{CO}}{3} \\ V_{CM2} = \dfrac{v_{A'O'} + v_{B'O'} + v_{C'O'}}{3} \\ V_{CM} = \dfrac{v_{AA'} + v_{BB'} + v_{CC'}}{3} = V_{CM1} - V_{CM2} \end{cases}, \tag{2}$$

where V_{CM1}, V_{CM2}, V_{CM} are the CMVs of the inverter 1, inverter 2, and open-end loads, respectively.

From (2), the CMV of the open-end loads is found by the cancellation between the CMVs of inverters 1 and 2. For a given identical CMVs of inverters 1 and 2, the elimination of the CMV at the open-end load can be absolutely satisfied.

On the basis of the two-level SVM scheme, using (1) into $\vec{V}_n = 2/3(v_{AA'} + v_{BB'}e^{j120^\circ} + v_{CC'}e^{j240^\circ})$, there are 64 possible voltage space vectors for the dual two-level VSIs, as shown Figure 2(a). Out of these voltage vectors, the seven medium voltage vectors (see the red lines), which provide the zero for the CMV of the open-end loads, are used in this paper. In addition, as separately shown in Figures 2(b) and 2(c) for inverters 1 and 2, the dual two-level VSIs are operated by shifting phase 120°. After obtaining the desirable seven voltage vectors, they are subsequent to the proposed DSVM switching sequence design using the five-segment concept, as shown in Figure 3. For an example of Sector 1, the inverters 1 and 2 are operated in Sectors I and III, respectively. According to the proposed technique, the number of the switching in three legs for inverters 1 and 2 results in eight, which is reduced by 1/3 from [4]. As expected, the CMVs of inverters 1 and 2 are the same manner as three levels ($-V_{DC}/2$, $-V_{DC}/6$, $V_{DC}/6$), which can be directly cancelled each other.

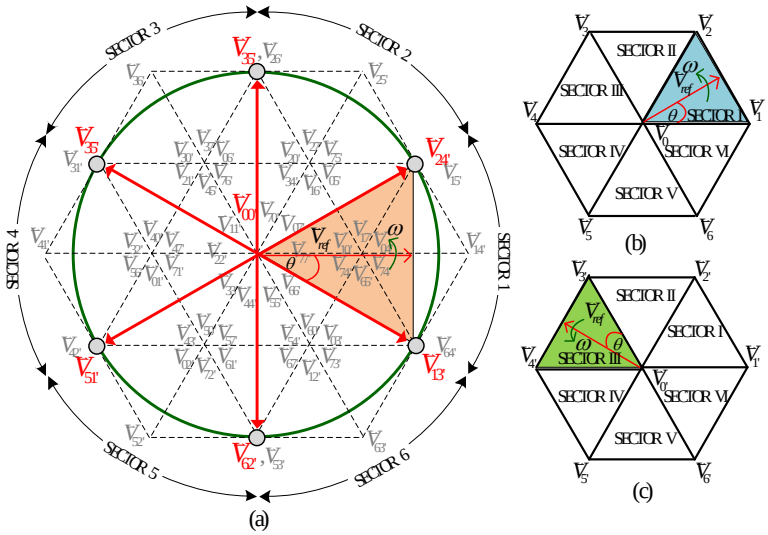

Figure 2. Schematic diagrams of space vector voltage synthesis for (a) dual two-level VSIs, (b) inverter 1, and (c) inverter 2.

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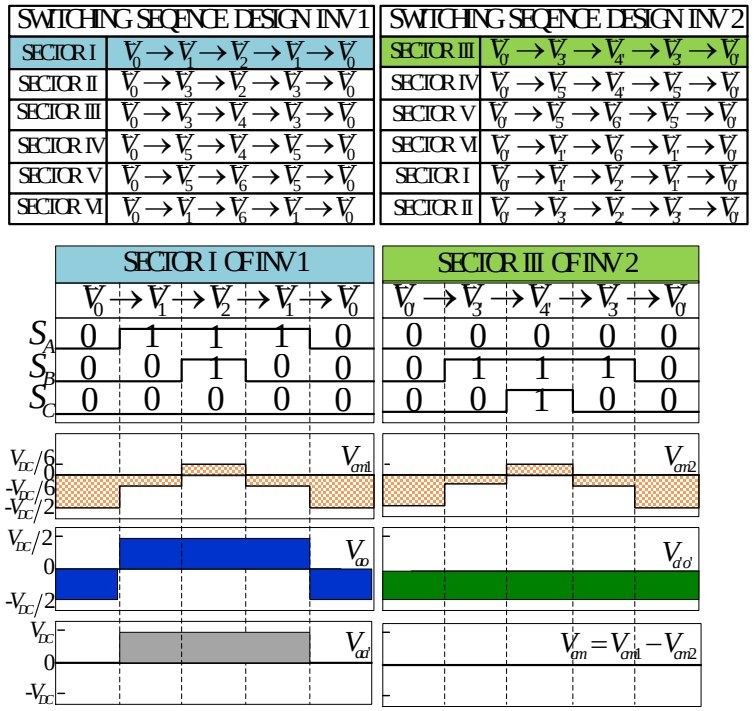

Figure 3. Proposed discontinuous/five-segment switching sequence design with centralizing PWM scheme.

3. Simulation Results and Discussion

The proposed DSVM technique for elimination of the CMV in dual two-level VSI fed open-end AC loads, as shown in Figure 1, is investigated by simulating in Matlab/Simulink environment. In terms of the parameters, the system is carried out by using the open-end three-phase inductive loads R = 20 Ω and L = 20 mH, the two-isolated dc supplies $V_{DC1}=V_{DC2}=325$ V, the fundamental frequency $f_1 = 50$ Hz, the switching frequency $f_{sw} = 3$ kHz, and the modulation index $M_a = 0.8$. Moreover, the superiority of the proposed technique in the reduction of the step and peak value of the CMV in each inverter and the switching loss points of view is demonstrated and also compared with the conventional technique [4].

As shown in Figure 4(a), the duty cycles of inverters 1 and 2 are clamped 120° per fundamental period with a 120° phase-shift between each other, corresponding to the waveforms of the pole voltage of inverters 1 and 2. This leads to no switching of inverters 1 and 2 for 1/3 of cycle, resulting in the switching loss reduction. In addition, the phase-A output voltage has three voltage levels (V_{DC}, 0, $-V_{DC}$) along with symmetrical configuration, which cause accordingly balanced and stable three-phase output currents.

The relative frequency spectrum of the pole voltages of inverters 1 and 2 and the phase-A output voltage are shown in Figure 4(b). Even though the pole voltages of both inverters have 120° angle displacement, the profiles of their frequency spectrum are similar, which can be pointed out by the identical values of their THD_v and peak fundamental components. Besides, the triplen harmonics, such as 3, 6, 9, and so on for low frequency and $60, 60\pm3, 60\pm6,$ and so on for high frequency, are also generated. However, the phase-A output voltage lacks these triplen harmonics due to its formation, $v_{AA'}=v_{AO}-v_{A'O'}$. Therefore, its low-frequency harmonics are cancelled and high-frequency harmonics remain $60\pm1, 60\pm2, 60\pm4, 60\pm5,$ and so on. In comparison to the pole voltage, the THD_v of the phase-A voltage deceases to 77.08% and the peak value of fundamental component increases to be square root three times about 252.2 V, according to theoretical principle of $\hat{V}_{O,1rms} = M_a V_{DC}/\sqrt{2}$.

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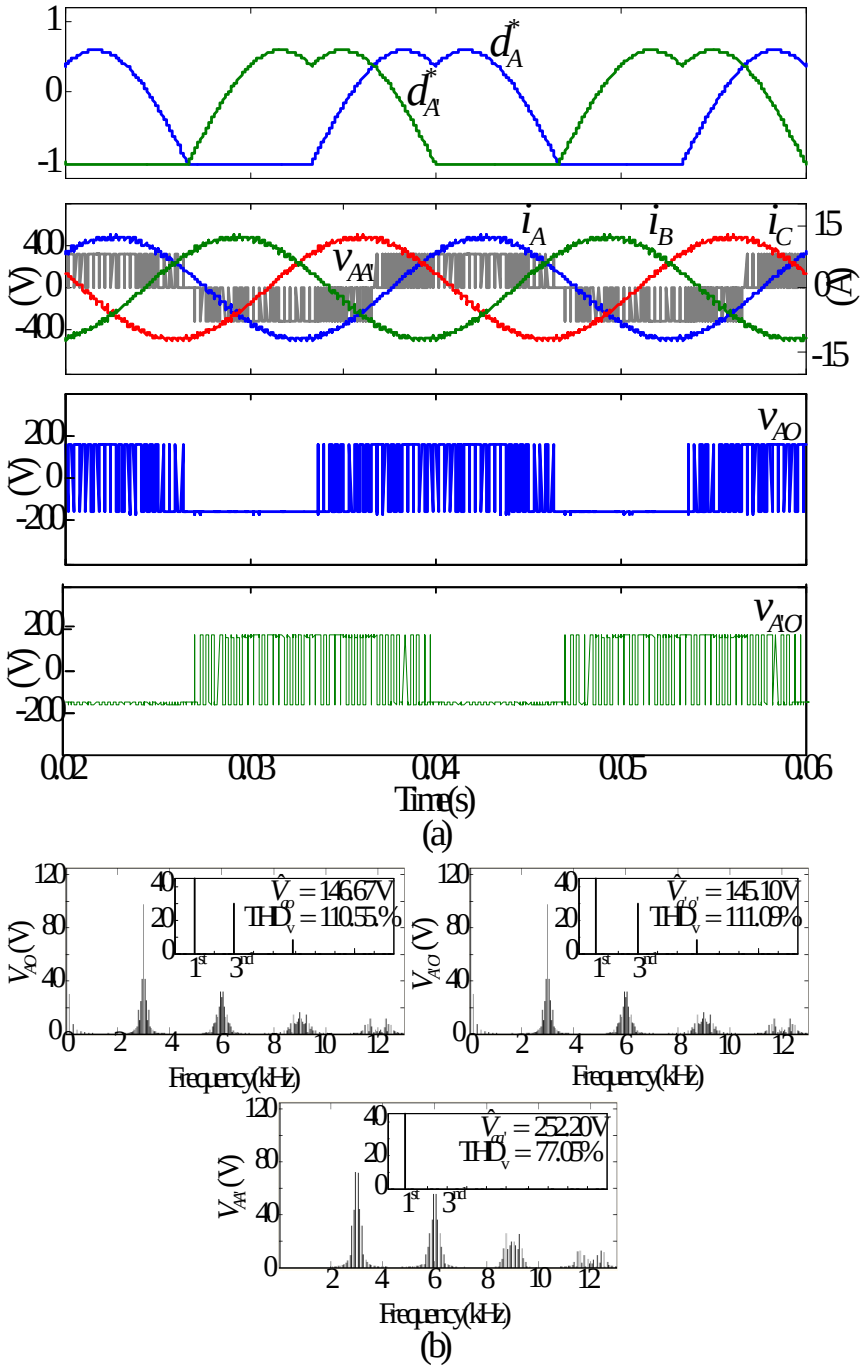

Figure 4. Simulation results of proposed DSVM technique for the dual two-level fed three phase AC loads with $M_a = 0.8$. (a) (top to bottom) Waveforms of duty cycles for inverter 1 d_A^* and inverter 2 $d_{A'}^*$, phase output voltage phase a $v_{AA'}$ and three phase output currents i_A, i_B, i_C, pole voltage of inverter 1 v_{AO} and pole voltage of inverter 2 $v_{A'O'}$. (b) Frequency spectrum harmonic of pole voltage of inverter 1 v_{AO}, pole voltage of inverter 2 $v_{A'O'}$ and phase output voltage $v_{AA'}$.

Figure 5(a) shows the CMVs of inverters 1, 2, and open-end AC loads. Regarding those of inverters 1 and 2, their waveforms and profiles of the frequency spectrum (see Figure 5(b)) are in a same manner. For this reason, the CMVs are eliminated at the AC loads in accordance with (2). It can be noted that the proposed DSVM technique is not only able to reduce the switching loss, but also eliminate the CMVs. For a given the open-end winding motor, it results in solving the problems of shaft voltage, bearing currents, and EMI, which further lead to the improvements of the early mechanical failure and the system efficiency.

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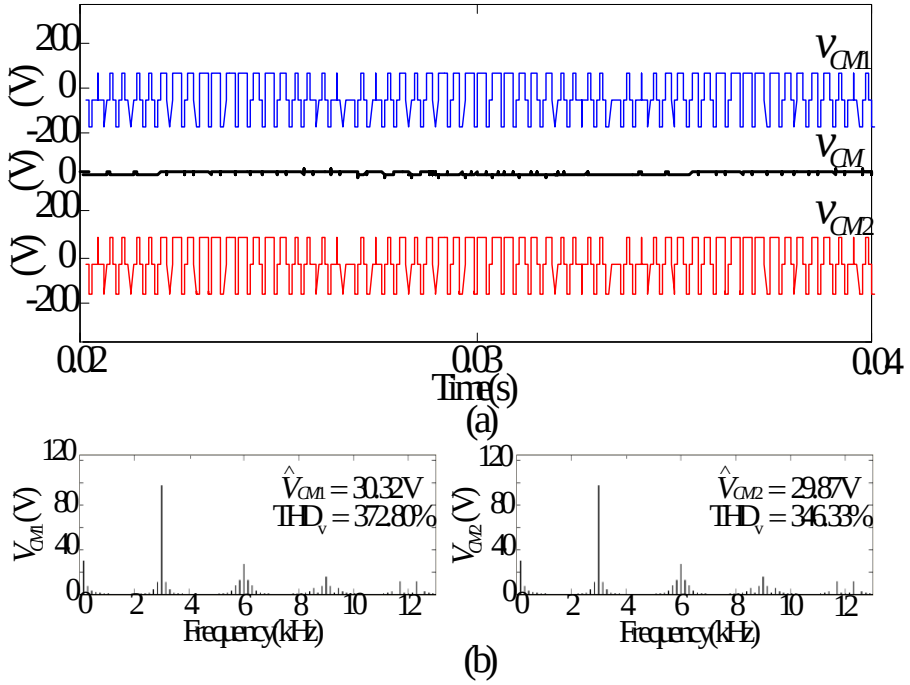

Figure 5. Simulation results of the common mode voltage elimination using the proposed DSVM technique for the Dual two-level fed three phase AC loads with $M_a = 0.8$. (a) Common-mode voltage of inverter1 v_{CM1}, inverter 2 v_{CM2} and common mode voltage at the open-end loads. v_{CM} (b) Frequency spectrum harmonic of common-mode voltage v_{CM1} and v_{CM2}.

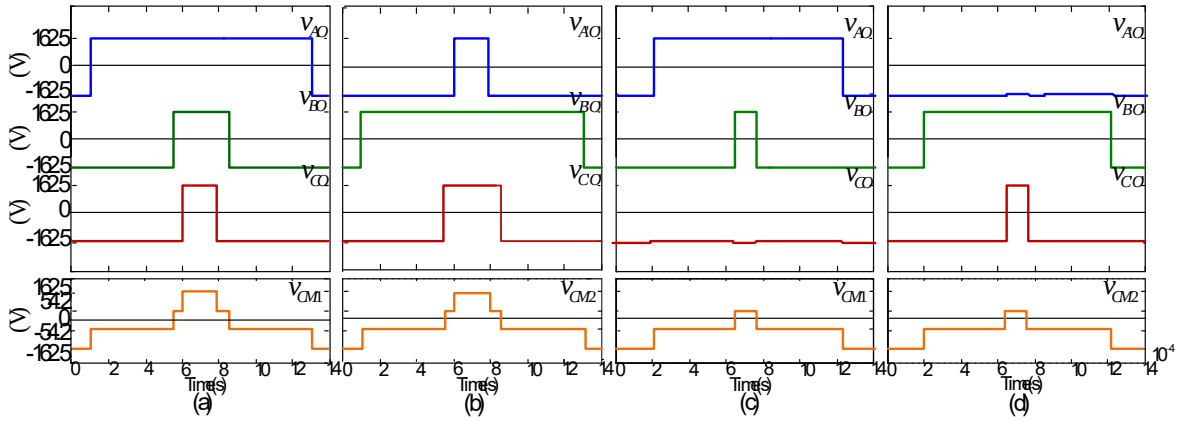

Figure 6. Simulation results during one switching cycle of three-phase pole voltages v_{AO}, v_{BO}, v_{CO} and $v_{A'O'}, v_{B'O'}, v_{C'O'}$, and common-mode voltages v_{CM1} and v_{CM2} for (a) inverter 1 and (b) inverter 2, respectively, with the CSVM method [4], and (c) inverter 1 and (d) inverter 2, respectively, with the proposed DSVM technique.

Figure 6 shows the three-phase pole voltages and the CMVs of both inverters 1 and 2 during one switching cycle for making the comparison between the conventional CSVM [4] (see Figures 6(a) and 6(b)) and proposed DSVM techniques (see Figures 6(c) and 6(d)). Observing the pole voltages, it can be concluded that the switching number of the converters with the proposed DSVM technique is eight in total, which can confirm a 33% switching loss reduction from the conventional CSVM technique. In terms of the CMV in each inverter, the proposed DSVM technique reduces the stepwise and peak from $-V_{DC}/2$, $-V_{DC}/6$, $V_{DC}/6$, and $V_{DC}/2$ to $-V_{DC}/2$, $-V_{DC}/6$, and $V_{DC}/6$.

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Other than the benefits of the CMV elimination at the open-end AC loads and the switching loss reduction, the achieved CMV reduction in each inverter is referred to the mitigation of the RMS value of the CM current.

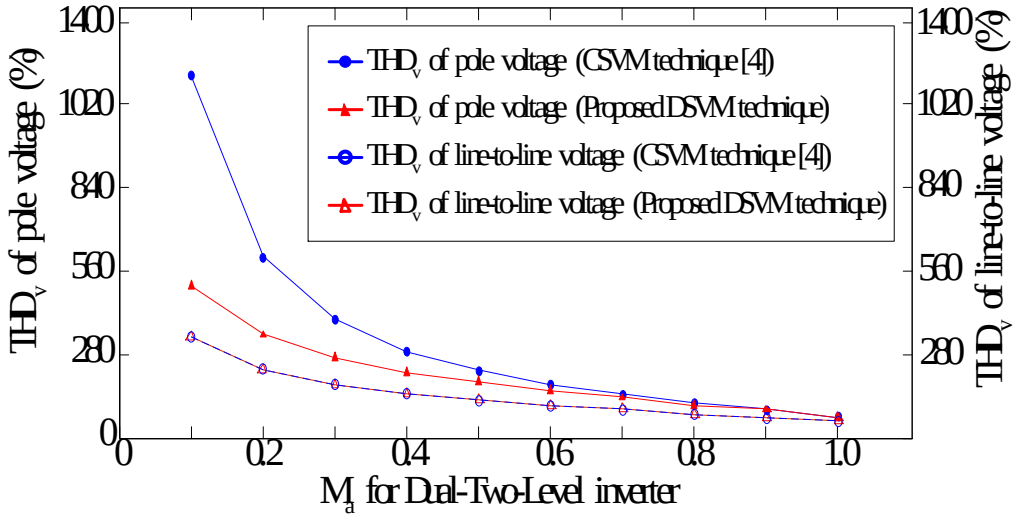

Figure 7. THD_v of pole voltage and phase output voltage versus the variation of the modulation index.

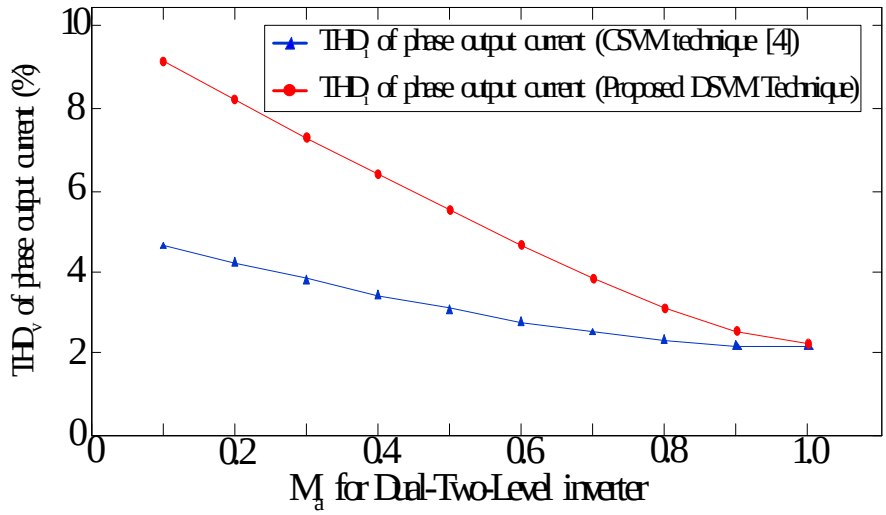

Figure 8. THD_i of phase output current versus the variation of the modulation index.

In order to evaluate the voltage qualities, referring to Figure 7, the THD_v of the pole voltage with the proposed DSVM technique is better than that of the conventional CSVM technique. This can as well confirm the achieved CMV reduction in each inverter of the proposed technique, as given in Figures 6(c) and 6(d). On account of the triplen harmonic cancellation in the phase output voltage at the open-end loads with both conventional and proposed techniques, the THD_v of the phase output voltages for these two technique are very close.

Figure 8 is shown that the proposed DSVM technique provides higher value of the THD_i of the phase output current compared with the conventional CSVM technique due to the inherent feature of the five-segment switching sequence design. Despite of the lower quality of the output current with the proposed technique, it can be recognizable by a compromise between the filter and the switching frequency.

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4. Conclusion

In this paper, the DSVM technique based on five-segment switching sequence design is synthesized to eliminate the CMV of the open-end AC loads/motor for the dual two-level VSIs with two isolated dc sources. Apart from this benefit, it is an effective alternative to the reduction of the switching loss by 33%, and also mitigation of the stepwise and peak value of the CMV in each inverter, when compared to the conventional CSVM technique.

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