1 *Article*

2 # A Single-Stage Asymmetrical Half-Bridge Flyback

3 # Converter with Resonant Operation

4 **Chung-Yi Ting [2], Yi-Chieh Hsu [2], Jing-Yuan Lin [1,*] and Chung-Ping Chen [2]**

5 [1] Department of Electronic and Computer Engineering, National Taiwan University of Science and
6   Technology, Taiwan, ROC; jylin@mail.ntust.edu.tw (J.L.)
7 [2] Graduate Institute of Electronics Engineering, National Taiwan University; d01943002@ntu.edu.tw (C.T.);
8   d02943003@ntu.edu.tw (Y.H.); cpchen@ntu.edu.tw (C.C.)
9 *   Correspondence: jylin@mail.ntust.edu.tw (J.L.); Tel.: x-886-2-27376419

10

11 **Abstract:** This paper proposes a single-stage asymmetrical half-bridge fly-back (AHBF) converter
12 with resonant mode using dual-mode control. The presented converter has an integrated boost
13 converter and asymmetrical half-bridge fly-back converter and operates in resonant mode. The
14 boost-cell always operates in discontinuous conduction mode (DCM) to achieve high power factor.
15 The presented converter operates simultaneously using a variable-frequency-controller (VFC) and
16 pulse-width-modulation (PWM) controller. Unlike the conventional single-stage design, the
17 intermediate bus voltage of this controller can be regulated depending on the main power switch
18 duty ratio. The asymmetrical half-bridge fly-back converter utilizes a variable switching frequency
19 controller to achieve the output voltage regulation. The asymmetrical half-bridge fly-back
20 converter can achieve zero-voltage-switching (ZVS) operation and significantly reduce the
21 switching losses. Detailed analysis and design of this single-stage asymmetrical half-bridge
22 fly-back converter with resonant mode is described. A wide AC input voltage ranging from 90 to
23 264 V_{rms} and output 19 V/ 120 W prototype converter was built to verify the theoretical analysis and
24 performance of the presented converter.

25 **Keywords:** fly-back converter; zero-voltage-switching (ZVS); Variable-frequency-controller (VFC);
26 single-stage

27

28 ## 1. Introduction

29   A conventional power supply was designed with a two-stage scheme that can be divided into
30 two parts. The first stage achieves power-factor-correction (PFC) to reduce the input current
31 harmonics. The second stage is a DC/DC converter that regulates the output voltage. However, the
32 two-stage scheme has several defects, such as high cost and power supply system complexity. In
33 recent years, a single-stage scheme was proposed [1-5] that integrates a boost stage and a DC/DC
34 stage to share a common switch. The boost-cell stage operates in discontinuous conduction mode
35 (DCM) to provide high power factor while the DC/DC stage can be responsible for output voltage
36 regulation. Unfortunately, the single-stage scheme presents major problems in which the
37 intermediate bus voltage cannot be regulated, such as the BIFRED converter, single-stage fly-back
38 converter and single-stage LLC resonant converter [6-10]. When voltage is input for universal
39 applications, the intermediate bus voltage could be as high as 1000 V, causing difficulty in selecting
40 converter components, with voltage stress issues throughout the capacitors and switches. The wide
41 intermediate bus voltage variation will cause output voltage regulation design difficulty and also
42 cause lower conversion efficiency though the DC/DC stage. The single-stage scheme intermediate
43 bus voltage cannot be regulated at light loads and universal input voltage. The
44 zero-voltage-switching (ZVS) fly-back converters have been used widely in industry and are

45 suitable for low-to-medium power applications, such as LED-driver and desktop computer power
46 supplies. Various kinds of ZVS schemes have been proposed, such as the active-clamp network and
47 asymmetrical half-bridge circuit [11,12]. The active-clamp fly-back converter [13] employs the active
48 clamp network to achieve ZVS operation; however, the voltage stresses on the switches are greater
49 than input voltage which will cause high conduction losses in the power switches. The asymmetrical
50 half-bridge fly-back converter (AHBF) with resonant mode [14-17] was developed to achieve ZVS
51 and reduce the voltage stresses on the switches to less than that of the active-clamp fly-back
52 converter, so the power density and conversion efficiency can be effectively increased. Furthermore,
53 it can operate under changed duty cycles or variable switching frequencies for regulated output
54 voltage.

55   This paper proposes a new single-stage asymmetrical half-bridge fly-back converter with
56 resonant mode. The proposed converter integrates a boost converter and an asymmetrical
57 half-bridge fly-back converter with resonant mode using dual-mode control. The converter
58 intermediate bus voltage can be regulated by the pulse-width-modulation control (PWM). The
59 variable-frequency-controller (VFC) can regulate the converter output voltage. Therefore, this
60 proposed converter can operate in universal input voltage and solves the voltage stress issues
61 throughout the capacitors and switches. The proposed converter utilizes the ZVS technique to
62 decrease the switching losses, resulting in high conversion efficiency. The operational principle for
63 the proposed converter is analyzed, a prototype converter with AC input voltage of 90-264 V_{rms} and
64 output voltage/current of 19 V/8 A is built to verify the analytical results.

2. Circuit Description and Principle Operation of Proposed Converter

66   Figure 1 shows the circuit configuration for the single-stage asymmetrical half-bridge fly-back
67 converter with resonant mode. The primary switches Q_1 and Q_2 operate at asymmetrical duty ratio.
68 D_{b1} and D_{b2} are the anti-paralleled power MOSFETs. The primary side diode D_{in} is a braking diode.
69 The L_{boost} is a boost-cell inductor. The resonant inductor L_r, resonant capacitor C_r and magnetizing
70 inductor L_m for are the resonant tank for the asymmetrical half-bridge fly-back converter. The
71 secondary diode D_r is a rectifier diode, the C_{bus} is boost cell output capacitor and C_O is the
72 asymmetrical half-bridge fly-back converter output capacitor.

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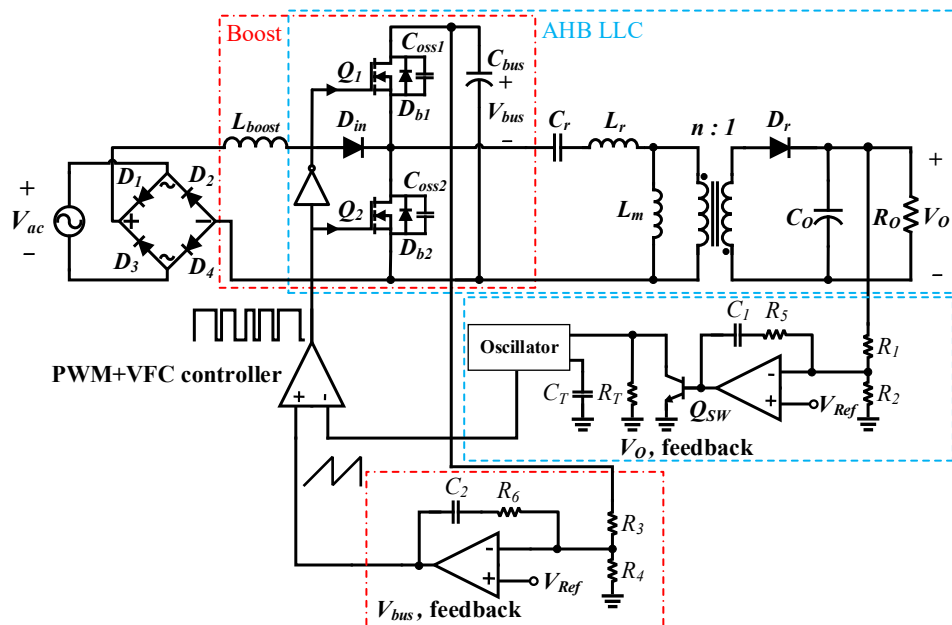
74 **Figure 1.** Schematic of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant
75 mode.

76   The following assumptions were made to analyze the proposed single-stage asymmetrical
77   half-bridge fly-back converter.

78   —   The conduction losses of all switches, diodes and layout traces, and the copper losses of the
79   transformer are neglected.

80   —   The turn ratio of the transformer windings is $n = N_1 / N_2$.

81   —   The resonant inductor L_r is composed of a leakage inductor and external inductor, where

82         $L_r = L_{eakage} + L_{ex}$.

83   —   The conduction times for Q_1 are $(1-D)T_s$ and Q_2 is DT_s, respectively, where D is the duty cycle
84   for Q_2, and T_s denotes the switching period. In addition, the dead time is much smaller than
85   that other of conduction times.

86   —   In the steady state the bus capacitance C_{bus} and output capacitance C_O are large enough so that
87   the bus voltage V_{bus} and output voltage V_O are a constant value.

88   Both the boost-cell stage and asymmetrical half-bridge fly-back converter stage share the
89   common switches Q_1 and Q_2, and furthermore there is bus capacitor C_{bus} between the two stages. The
90   boost-cell stage was presented in [18]. When the switch Q_2 is turned on and the switch Q_1 is turned
91   off, this results in a positive voltage $V_{Lboost} = V_{IN}$ across the inductor L_{boost} causing a linear increase in
92   the inductor current i_{Lboost}. Conversely, when the switch Q_1 is turned on and the switch Q_2 is turned
93   off, the inductor L_{boost} is releases energy to the bus capacitor C_{bus}. Therefore, from the flux-balance of
94   L_{boost} under the steady-state, V_{bus} can be determined as

95
$$\frac{V_{bus}}{V_{IN}} = \frac{1}{2} + \frac{\sqrt{1 + 2 \cdot \frac{D^2 \cdot R_{L,bus}}{L \cdot f_s}}}{2} \tag{1}$$

96   In the DC/DC stage, when the switch Q_1 is turned on, the intermediate bus voltage V_{bus} will
97   charge C_r, L_r and L_m. Conversely, when the switch Q_2 is turned on, the secondary diode D_r conducts
98   and L_m is releases energy to the output load. When the asymmetrical half-bridge fly-back converter
99   operates in resonant mode, the voltage transfer ratio can be expressed as

100
$$M = \frac{nV_O}{V_{bus}} = \frac{(1-D) \cdot \frac{1 - \cos\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right]}{Z_r \cdot \omega_r}}{\frac{1-D}{\omega_r}\left[\frac{1}{n^2 R_o} + \frac{D}{2L_m f_s}\right] \cdot \sin\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right] + \frac{(1-D)^2}{n^2 R_o f_s} + \frac{1 - \cos\left[\omega_r \cdot \left(\frac{D}{f_s}\right)\right]}{Z_r \cdot \omega_r}} \tag{2}$$

101   Where

102
$$\omega_r = \frac{1}{\sqrt{C_r \cdot L_r}} \tag{3}$$

103
$$Z_r = \sqrt{\frac{L_r}{C_r}} \qquad (4)$$

104   From equation (2), the voltage transfer ratio of the asymmetrical half-bridge fly-back converter
105   includes relation between the duty ratio D and switching frequency f_s simultaneously. Figure 2
106   shows the relation between the duty ratio D, switching frequency f_s and voltage transfer ratio. It
107   shows that when the duty-ratio D is decreased from 0.35 to 0.65, to maintain fixed voltage gain, the
108   switching frequency can shift from f_c to f_a correspondingly. However, Figure 2 also shows that when
109   the switching frequency f_s or duty ratio D decreases the voltage gain will be increased. In contrast,
110   when the switching frequency f_s or duty ratio D increase, the voltage gain will be decreased.

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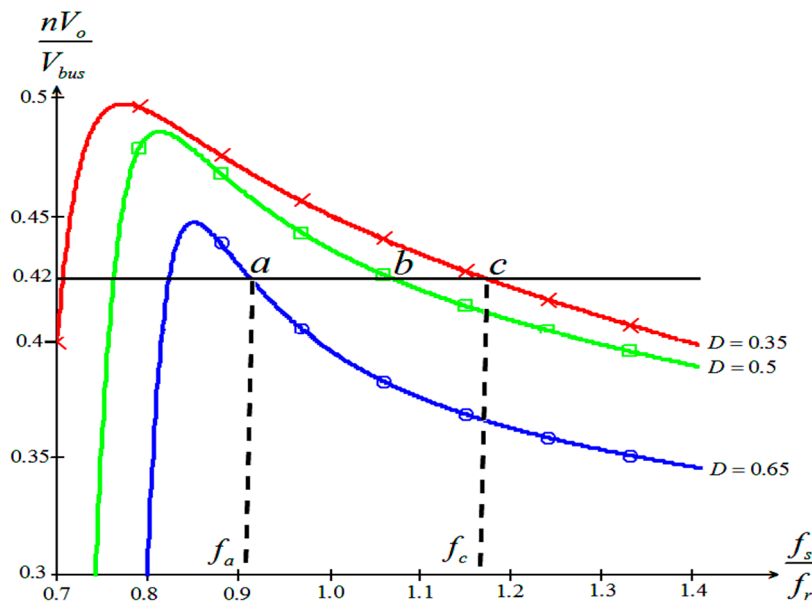
112   **Figure 2.** Voltage transfer ratio versus normalized switching frequency.

113   From Figure 1, Q_2 is the boost-cell stage main switch, therefore the intermediate bus voltage V_{bus}
114   is regulated by the D to Q_2 duty ratio. Unfortunately, changing the D to Q_2 duty ratio will affect the
115   asymmetrical half-bridge fly-back converter output voltage. For example, when the D to Q_2 duty
116   ratio is increased, the asymmetrical half-bridge fly-back converter output voltage will decrease.
117   Conversely, when the D to Q_2 duty ratio is decreased, the asymmetrical half-bridge fly-back
118   converter output voltage will increase. To overcome the change in D to Q_2 duty ratio causing
119   unstable asymmetrical half-bridge fly-back converter output voltage, a VFC has been added to the
120   feedback control loop. When the asymmetrical half-bridge fly-back converter output voltage is
121   decreased, the switching frequency f_s will decrease to provide larger voltage gain for regulated
122   output voltage. Conversely, when the output voltage is increased, the switching frequency f_s will be
123   increased to provide lower voltage gain. According to the above analysis, the intermediate bus
124   voltage V_{bus} and output voltage V_O of the proposed converter can be regulated simultaneously from
125   the PWM control and VFC.

126   Figure 3 depicts the key waveforms of the proposed single-stage asymmetrical half-bridge
127   fly-back converter with resonant mode. Six states are required to complete a switching cycle. The
128   conduction paths for each operating state are illustrated in Figure 4.

129
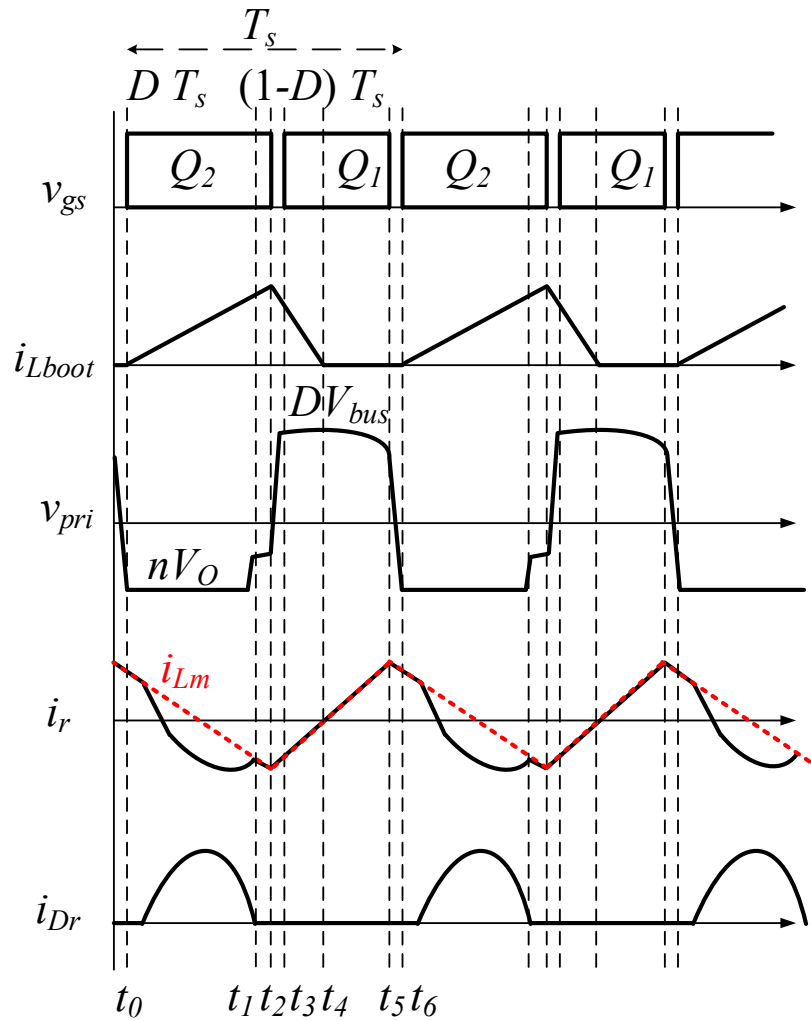
Figure 3. Key waveforms of the proposed single-stage asymmetrical half-bridge fly-back converter with resonant mode.

132   State 1: $t_0 < t < t_1$

133   As shown in Figure 4, Q_2 is turned on with the ZVS operating condition. In the meantime the
134   rectifier diode D_r is conducted and the energies stored in the transformer magnetizing inductors are
135   transferred to the output load. The output voltage is reflected to the primary side, therefore, the
136   primary transformer is clamped to $-nV_O$, and i_{Lm} decreases linearly. During this period, the resonant
137   inductor L_r and resonant capacitor C_r begin to resonate. On the other hand, the diode D_{in} is
138   conducted and the voltage across the input inductor L_{boost} is equal to the input voltage V_{IN} so the
139   input inductor current i_{Lboost} increases linearly. The input current i_{Lboost} can be expressed as

$$i_{Lboost}(t) = \frac{V_{bus}}{L_{boost}}(t - t_0) \tag{5}$$

141   The resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} are given as

$$i_{Lr}(t) = i_{Lr}(t_0) \cdot \cos\left[\omega_r(t - t_0)\right] - \frac{v_{Cr}(t_0) + nV_o}{Z_r} \cdot \sin\left[\omega_r(t - t_0)\right] \tag{6}$$

143
$$v_{Cr}(t) = nV_O + \left[v_{Cr}(t_0) + nV_O \right] \cdot \cos\left[\omega_r(t - t_0) \right] + Z_r i_{Lr}(t_0) \cdot \sin\left[\omega_r(t - t_0) \right] \tag{7}$$

144   The magnetizing current i_{Lm} of transformer can be expressed as

145
$$i_{Lm}(t) = i_{Lm}(t_0) - \frac{nV_O(t - t_0)}{L_m} \tag{8}$$

146   This interval is ended when i_{Lr} equals i_{Lm} at t_1.

147   State 2: $t_1 < t < t_2$

148   At time t_1 the input inductor current i_{Lboost} increases linearly. The resonant inductor current i_{Lr} is
149   the same as the magnetizing current i_{Lm} therefore, no current is transferred to the secondary side so
150   the rectifier diode D_r is turned off. During this mode, the resonant circuit is composed of C_r, L_r and
151   L_m. Moreover, L_m is equal to series with L_r and L_m is much larger than L_r, so that the resonant cycle is
152   much longer than the previous state. The i_{Lm}, i_{Lr} and v_{Cr} are expressed as

153
$$i_{Lr}(t) = i_{Lr}(t_1) \cdot \cos\left[\omega_{r2}(t - t_1) \right] - \omega_{r2} C_r v_{cr}(t_1) \cdot \sin\left[\omega_{r2}(t - t_1) \right] \tag{9}$$

154
$$\begin{aligned} v_{Cr}(t) &= v_{Cr}(t_1) \cdot \cos\left[\omega_{r2}(t - t_1) \right] + L_m i_{Lr}(t_1) \omega_{r2} \cdot \sin\left[\omega_{r2}(t - t_1) \right] \\ &+ L_r i_{Lr}(t_1) \omega_{r2} \cdot \sin\left[\omega_{r2}(t - t_1) \right] \end{aligned} \tag{10}$$

155
$$i_{Lm}(t) = i_{Lr}(t) \tag{11}$$

156   Where

157
$$\omega_{r2} = \frac{1}{\sqrt{C_r \cdot (L_m + L_r)}} \tag{12}$$

158   When Q_2 is turned off this interval is ended.

159   State 3: $t_2 < t < t_3$

160   The mode begins when Q_2 is turned off at $t = t_2$. The magnetizing current i_{Lm} charges the Q_2
161   junction capacitors and discharges the Q_1 junction capacitors until the Q_2 junction capacitors equal
162   V_{bus} and the Q_1 body diode conducts. Therefore, at time t_3, Q_1 can be turned on to achieve ZVS.
163   During this period, which is used to allow enough time to achieve ZVS, as well as prevent shoot
164   through in the two switches, the i_{Lr} and v_{Cr} are expressed as

165
$$i_{Lr}(t) = i_{Lr}(t_2) \cdot \cos\left[\omega_{r1}(t - t_2) \right] - \omega_{r2} C_r v_{cr}(t_1) \cdot \sin\left[\omega_{r1}(t - t_2) \right] \tag{13}$$

166
$$v_{Cr}(t) = \frac{i_{Lr}(t_2)}{\omega_{r1} C_r} \cdot \sin\left[\omega_{r1}(t - t_2) \right] + v_{cr}(t_2) \cdot \cos\left[\omega_{r1}(t - t_2) \right] \tag{14}$$

167   Where

168
$$\omega_{r1} = \frac{1}{\sqrt{(L_m + L_r) \cdot (C_{eq} \parallel C_r)}}, \quad C_{oss1} = C_{oss2}; \; C_{eq} = C_{oss1} = C_{oss2} \qquad (15)$$

169   The input current i_{Lboost} can be expressed as

170
$$i_{Lboost}(t) = -\frac{V_{IN} - V_{bus}}{L_{boost}}(t - t_2) \qquad (16)$$

171   State 4: $t_3 < t < t_4$

172   In this state, Q_1 is turned on which carries the resonant inductor current i_{Lr} and input inductor
173   current i_{Lboost}. The voltage across the input inductor L_{boost} is about $(V_{IN} - V_{bus})$ so the input inductor
174   current i_{Lboost} linearly decreasing. Referring to Figure 4(d), the rectifier diode D_r is reverse-biased and
175   in the meantime the input energy is stored in the primary magnetizing inductance L_m, while the
176   output capacitors C_O provide energy to the output load. The resonant inductor current i_{Lr},
177   magnetizing inductance current i_{Lm} and resonant capacitors voltage v_{Cr} can be expressed as

178
$$i_{Lr}(t) = i_{Lr}(t_3) \cdot \cos\big[\omega_{r2}(t - t_3)\big] + \omega_{r2} C_r v_{bus} \cdot \sin\big[\omega_{r2}(t - t_3)\big]$$
$$- \omega_{r2} C_r v_{cr}(t_3) \cdot \sin\big[\omega_{r2}(t - t_3)\big] \qquad (17)$$

179
$$v_{Cr}(t) = v_{cr}(t_3) + i_{Lr}(t_3) \cdot \cos\big[\omega_{r2}(t - t_3)\big] + \omega_{r2} C_r v_{bus} \cdot \sin\big[\omega_{r2}(t - t_3)\big]$$
$$- \omega_{r2} C_r v_{cr}(t_3) \cdot \sin\big[\omega_{r2}(t - t_3)\big] \qquad (18)$$

180
$$i_{Lm}(t) = i_{Lr}(t) \qquad (19)$$

181   The input current i_{Lboost} are given as

182
$$i_{Lboost}(t) = -\frac{V_{IN} - V_{bus}}{L_{boost}}(t - t_3) \qquad (20)$$

183   When input current i_{Lboost} reach zero level, this interval is ended.

184   State 5: $t_4 < t < t_5$

185   During this stage, Q_1 remains turned on so that the direction of i_{Lr} is reversed. As with Stage 4
186   the primary magnetizing inductance L_m stores energy and the output capacitors C_O continue to
187   provide energy through the output load. The current in L_{boost} stays at zero (DCM operation) so the
188   PFC feature can be achieved. In the meantime, diode D_{in} is in reverse bias. The resonant inductor
189   current i_{Lr}, magnetizing inductance current i_{Lm} and the resonant capacitor voltage v_{Cr} are given as

190
$$i_{Lr}(t) = i_{Lr}(t_4) \cdot \cos\big[\omega_{r2}(t - t_4)\big] + \omega_{r2} C_r v_{bus} \cdot \sin\big[\omega_{r2}(t - t_4)\big]$$
$$- \omega_{r2} C_r v_{cr}(t_4) \cdot \sin\big[\omega_{r2}(t - t_4)\big] \qquad (21)$$

191
$$v_{Cr}(t) = v_{cr}(t_4) + i_{Lr}(t_4) \cdot \cos\big[\omega_{r2}(t - t_4)\big] + \omega_{r2} C_r v_{bus} \cdot \sin\big[\omega_{r2}(t - t_4)\big]$$
$$- \omega_{r2} C_r v_{cr}(t_4) \cdot \sin\big[\omega_{r2}(t - t_4)\big] \qquad (22)$$

192
$$i_{Lm}(t) = i_{Lr}(t)$$ **(23)**

193 where

194
$$\omega_{r2} = \frac{1}{\sqrt{C_r \cdot (L_m + L_r)}}$$ **(24)**

195 When Q_1 turned off, this interval is ended.

196 State 6: $t_5 < t < t_6$

197   In this stage, Q_1 and Q_2 are turned off and the input current i_{Lboost} remains at zero, while the
198 output capacitors continue to provide energy through the output load. At this interval, the resonant
199 current i_{Lr} charges the Q_1 junction capacitors and discharges the Q_2 junction capacitors. When Q_1
200 equals V_{bus} and the body diode across Q_2 conducts, this interval is ended and the operating state
201 returns to Stage 1 to begin the next switching cycle. The resonant inductor current i_{Lr}, magnetizing
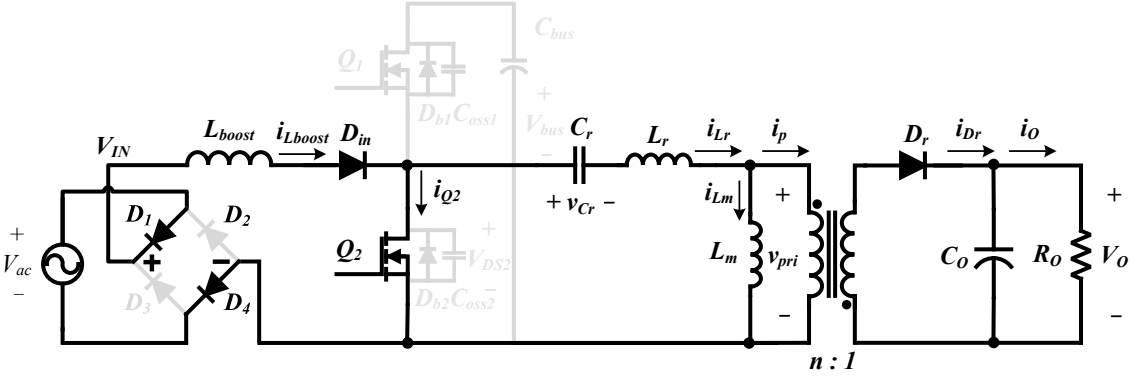202 inductance current i_{Lm} and resonant capacitor voltage v_{Cr} can be expressed as

203
$$i_{Lr}(t) = i_{Lr}(t_5) \cdot \cos\left[\omega_{r1}(t - t_5)\right] + \omega_{r1}C_r v_{Cr}(t_5) \cdot \sin\left[\omega_{r1}(t - t_5)\right]$$ (25)

204
$$v_{Cr}(t) = \frac{I_{Lr}(t_5)}{\omega_{r1}C_r} \cdot \sin\left[\omega_{r1}(t - t_5)\right] + v_{Cr}(t_5) \cdot \cos\left[\omega_{r2}(t - t_5)\right]$$ (26)
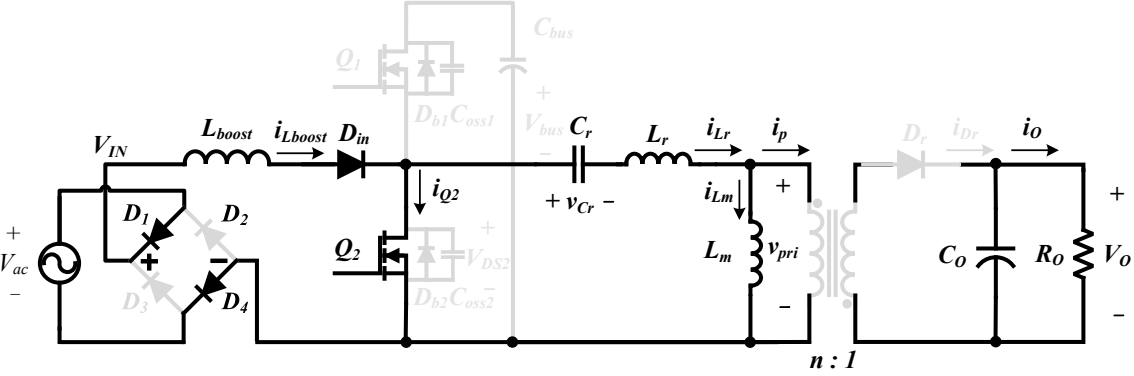
205
$$i_{Lm}(t) = i_{Lr}(t)$$ (27)

206 When Stage 6 ends the operating state returns to Stage 1 and the next switching cycle begins.

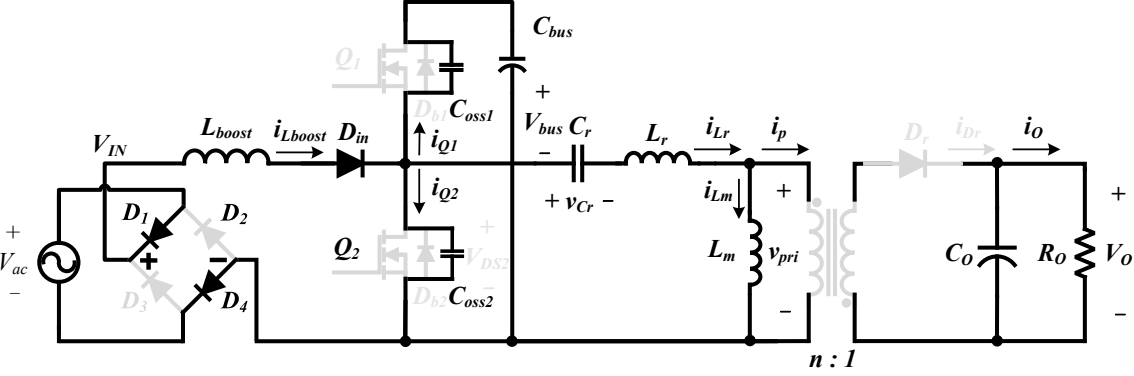207 State 6: $t_5 < t < t_6$

208   In this stage, Q_1 and Q_2 are turned off and the input current i_{Lboost} remains at zero, while the
209 output capacitors continue to provide energy through the output load. At this interval, the resonant
210 current i_{Lr} charges the Q_1 junction capacitors and discharges the Q_2 junction capacitors. When Q_1
211 equals V_{bus} and the body diode across Q_2 conducts, this interval is ended and the operating state
212 returns to Stage 1 to begin the next switching cycle. The resonant inductor current i_{Lr}, magnetizing
213 inductance current i_{Lm} and resonant capacitor voltage v_{Cr} can be expressed as

214
$$i_{Lr}(t) = i_{Lr}(t_5) \cdot \cos\left[\omega_{r1}(t - t_5)\right] + \omega_{r1}C_r v_{Cr}(t_5) \cdot \sin\left[\omega_{r1}(t - t_5)\right]$$ (28)

215
$$v_{Cr}(t) = \frac{I_{Lr}(t_5)}{\omega_{r1}C_r} \cdot \sin\left[\omega_{r1}(t - t_5)\right] + v_{Cr}(t_5) \cdot \cos\left[\omega_{r2}(t - t_5)\right]$$ (29)

216
$$i_{Lm}(t) = i_{Lr}(t)$$ (30)

217 When Stage 6 ends the operating state returns to Stage 1 and the next switching cycle begins.

218

219

(**a**)

220

221

(**b**)

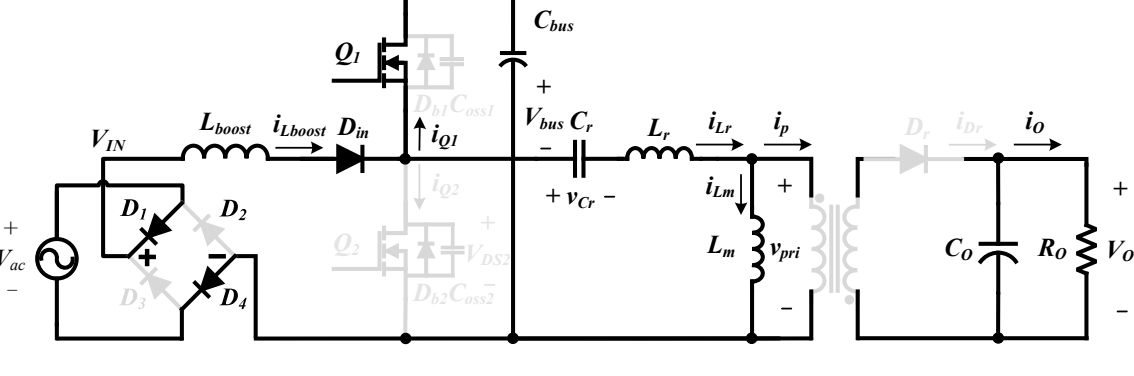222

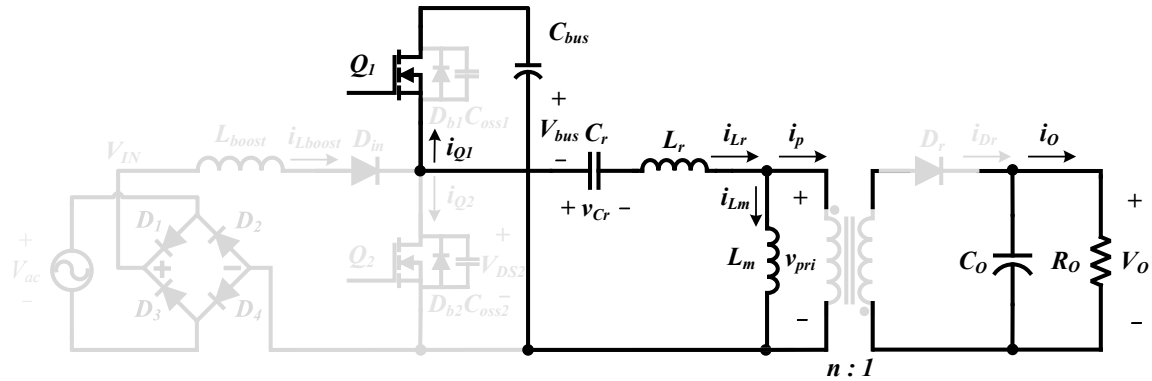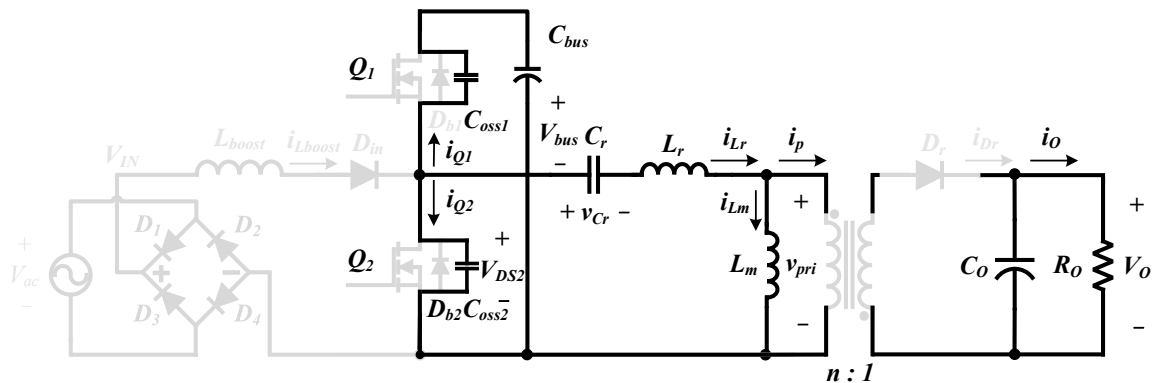223

(**c**)

224

225

(**d**)

226

227

(e)

228

229

(f)

230 **Figure 4.** Operation Modes of the proposed single-stage asymmetrical half-bridge fly-back converter during
231 one switching period: (**a**) State 1; (**b**) State 2; (**c**) State 3; (**d**) State 4; (**e**) State 5; (**f**) State 6.

232 **3. Circuit Design for the Proposed Converter**

233 D_{max} is the maximum duty cycle for the proposed converter. For to achieve high power-factor
234 the input inductor current must be operated in DCM so the input inductor L_{boost} can be expressed as

$$L_{boos} < \frac{V_{bus}T_s}{2 \cdot i_{IN\_peak}f_{s\_min}} \cdot (D_{max}) \cdot (1-D_{max})^2 \qquad (31)$$

236 Where i_{IN_peak} is the maximum peak-current of the input inductor L_{boost}, and f_{s_min} is the lowest
237 switching frequency for the proposed converter. From equation (28), when L_m is greater than the
238 resonant inductor L_r, the voltage gain can be approximated as

$$V_O = \frac{1}{n}V_{bus} \cdot (1-D) \qquad (32)$$

240 Therefore, the turn ratio of the transformer primary winding to secondary winding can be equal to

$$n = \frac{V_{bus}}{V_O} \cdot (1-D) \qquad (33)$$

242 At $t = t_3$, to ensure the ZVS operation for Q_1, the magnetizing inductance current i_{Lm} must discharge
243 the C_{oss1} until the voltage is equal to zero so the minimum i_{Lm} at t_3 can be given as

244
$$i_{Lm(t_3)\_min} = \frac{nV_O}{2L_m} \cdot D_{min} T_s \tag{34}$$

245   According to equation (31), the maximum magnetizing inductance L_m can be expressed as

246
$$L_{m(t_3)\_max} = \frac{nV_O \cdot t_{dead}}{2 \cdot V_{bus}(C_{oss1} + C_{oss2}) \cdot f_s} \cdot D_{min} \tag{35}$$

247   On the other hand, at $t = t_6$, to ensure ZVS operation for Q_2, the magnetizing inductance current
248   i_{Lm} must discharge C_{oss2} until the voltage is equal to zero so the minimum i_{Lm} at t_6 can be given as

249
$$i_{Lm(t_6)\_min} = \frac{nV_O}{2 \cdot L_m \cdot f_s} \cdot (1 - D_{max}) \tag{36}$$

250   According to equation (33), the maximum magnetizing inductance L_m can be expressed as

251
$$L_{m(t_6)\_max} = \frac{nV_O \cdot t_{dead}}{2 \cdot V_{bus}(C_{oss1} + C_{oss2}) \cdot f_s} \cdot (1 - D_{max}) \tag{37}$$

252   Form Figure 3a, the resonant capacitor C_r and the resonant inductor L_r are resonating from t_0 to
253   t_1, this time interval is during the Q_2 turn-on time, which is about half the resonant period and can be
254   approximately expressed as

255
$$C_r \leq \frac{\left(\dfrac{2 \cdot D_{max}}{\omega_r}\right)^2}{L_r} \tag{38}$$

256   The output filter capacitance C_O can be calculated as

257
$$C_O \geq \frac{\dfrac{P_O}{V_O} \cdot (1 - D_{max})}{\Delta V_O \cdot f_s} \tag{39}$$

258   Where f_s is the switching frequency and ΔV_O is the output voltage ripple. The voltage stresses of Q_1
259   and Q_2 are equal to V_{bus}. The voltage stresses of the secondary diode D_r is

260
$$D_r = \frac{D_{max} \cdot V_{bus}}{n} + V_O \tag{40}$$

261   The peak secondary diode current is expressed as

262
$$I_{Dr,max} = \frac{\pi}{2 \cdot (1 - D_{max})} \cdot I_O \tag{41}$$

263

264

265   **4. Experimental Results**

266   In order to verify the feasibility of the proposed converter, a 120 W prototype converter is built
267   in the laboratory. Figure 5. shows the proposed converter and the experimental parameters are
268   designed in Table 1.

269
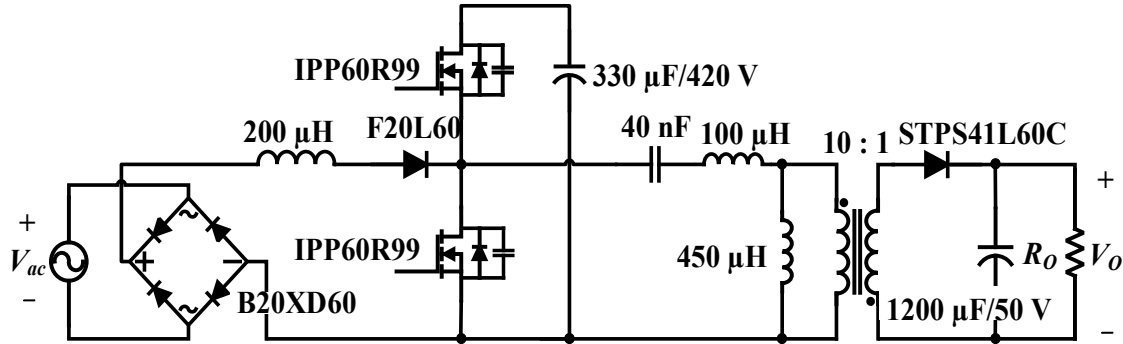
270   **Figure 5.** Implementation of the proposed single-stage asymmetrical half-bridge fly-back converter with
271   resonant mode.

272   **Table 1**. Experimental parameters of the proposed converter.

| Parameters	Value
Input ac voltage range:	85~264 V_{rms}
Output voltage:	V_O = 19 V
Output voltage ripple:	$\triangle V_O$ = 0.95 V
Intermediate bus voltage:	V_{bus}=420 V
Maximum output current:	I_O = 6.32 A
Input inductor:	L_{boost} = 200 μH
Magnetizing inductance:	L_m = 450 μH
Turns ratio:	$n = N_p/N_s$ = 3T
Resonant inductor:	L_r = 100 μH
Maximum duty cycle:	D_{max} = 0.75
Resonant capacitors:	C_r = 40 nF
Switching frequency:	f_s = 60~150 kHz
Output capacitor:	C_O = 1200 μF

273   A PQ26/20 TDK core is used for the input inductor. The PQ32/30 core is used for the isolation
274   transformer and the transformer turn ratio is calculated from (29). The magnetizing inductance L_m is
275   designed from (32) at approximately 450 μH. The IPP60R99 MOSFET is used producing output
276   capacitance C_{OSS} of about 130 pF at a 430 V drain-to-source voltage, including the output
277   capacitances of Q_1 and Q_2 it is about 260 pF. Therefore, to ensure ZVS operations, 330 ns dead time
278   was inserted between the Q_1 and Q_2 gate signals. The resonant frequency f_r is placed at about 80 kHz
279   so the resonant capacitor C_r and resonant inductor L_r can be calculated from (35). The output voltage

280   ripple ΔV_O is required to be smaller than 0.95 V. The output capacitor C_O is calculated to be greater
281   than 474 μF from equation (36). Therefore, a 1200 μF output capacitor is used.

282   Figure 6 shows the experimental results for v_{GS1}, v_{GS2}, i_{Lboost} and i_{Lr} at different output currents
283   and at $V_{In,main}$. Referring to Figure 3, six operation states can be observed in Figure 6. When Q_1 is
284   turned on and Q_2 is turned off, the i_{Lboost} linearly decreases and i_{Lr} linearly increases. When Q_1 and Q_2
285   are turned off, ZVS operation can be achieved. During the Q_1 turned off and Q_2 turned on period, the
286   i_{Lboost} increases linearly and the resonant inductor L_r and resonant capacitor begin to resonate. On the
287   other hand, Figure 6 also shows that when the output load increases from light load to full load, the
288   duty ratio of Q_2 increases from 0.5 to 0.75 for regulated bus voltage V_{bus}, and the switching frequency
289   decreases from about 125 kHz to 62 kHz for regulated output voltage V_O. Figure 7 shows the
290   measured input voltage v_{ac}, input current i_{ac} and input inductor current i_{Lboost} under full load
291   conditions. The input current near sinusoidal waveform and input inductor current are shown
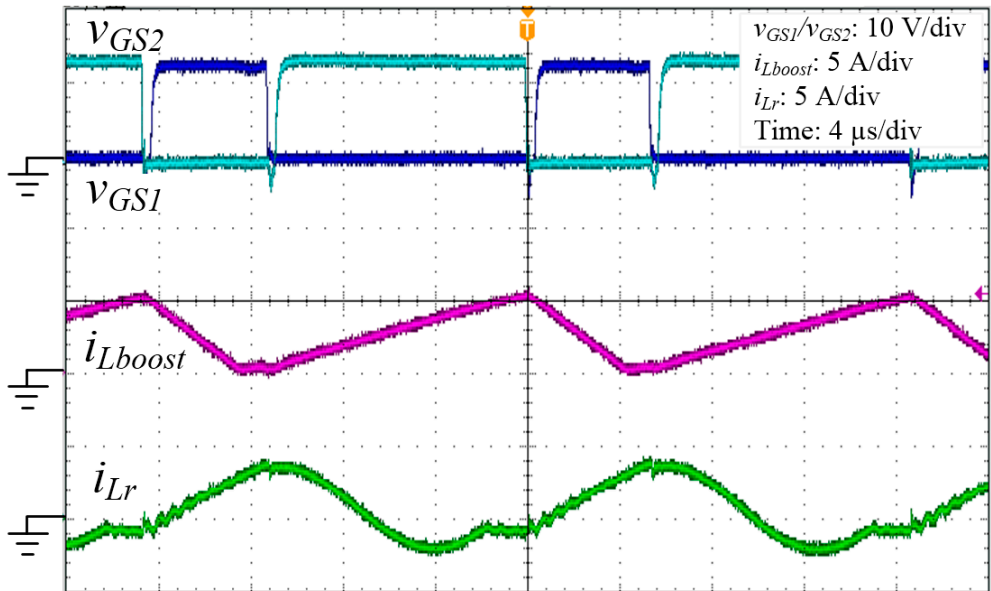292   operated in DCM so that high power factor can be achieved.

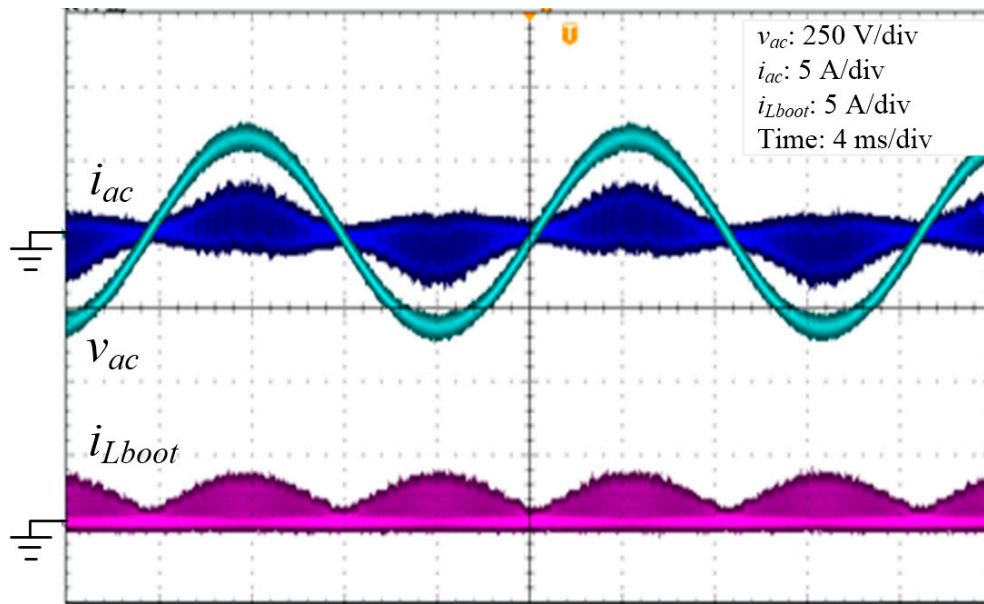

293

294   (**a**)

295

296   (**b**)

297

298
<center>(c)</center>

299

300
<center>(d)</center>
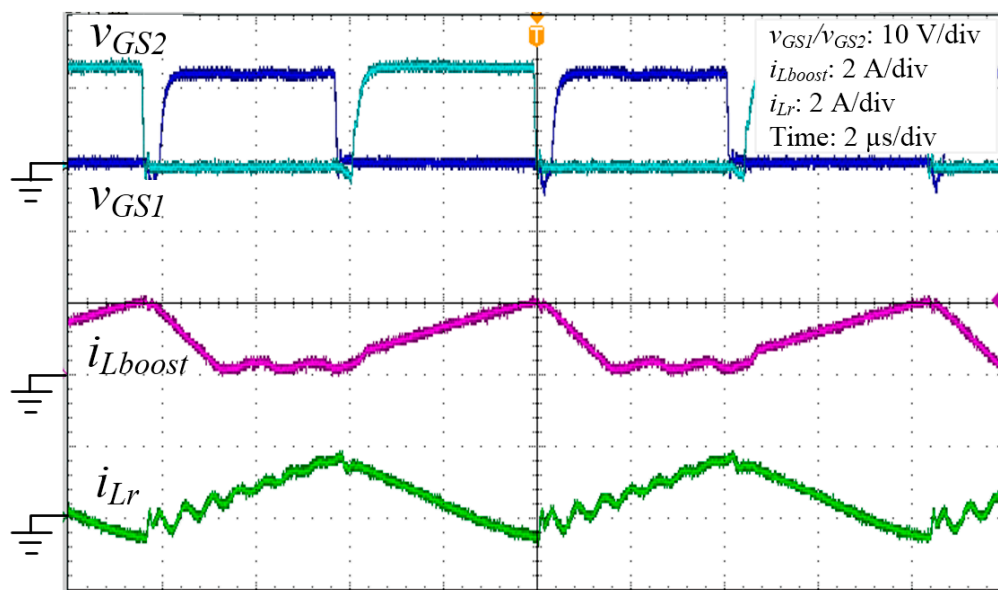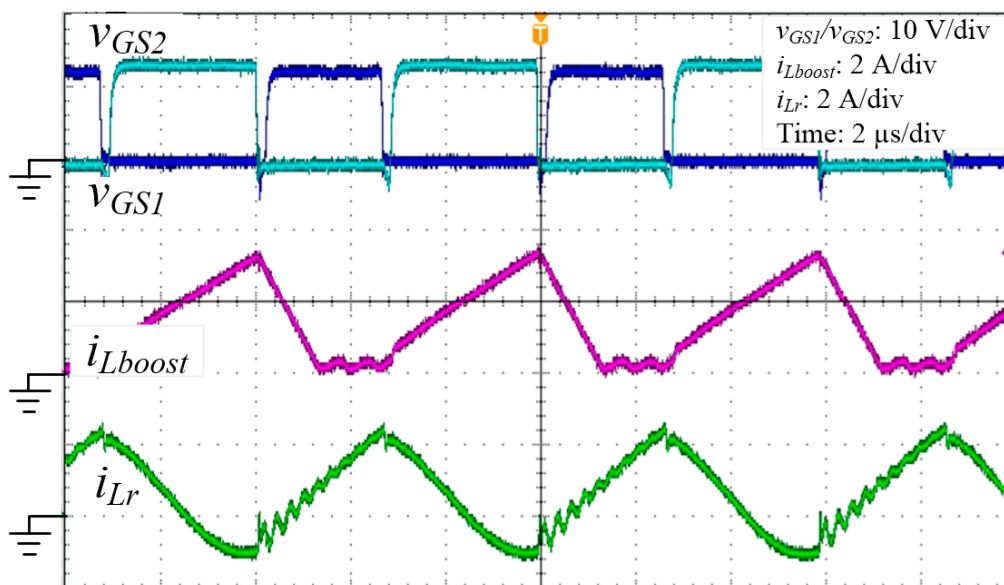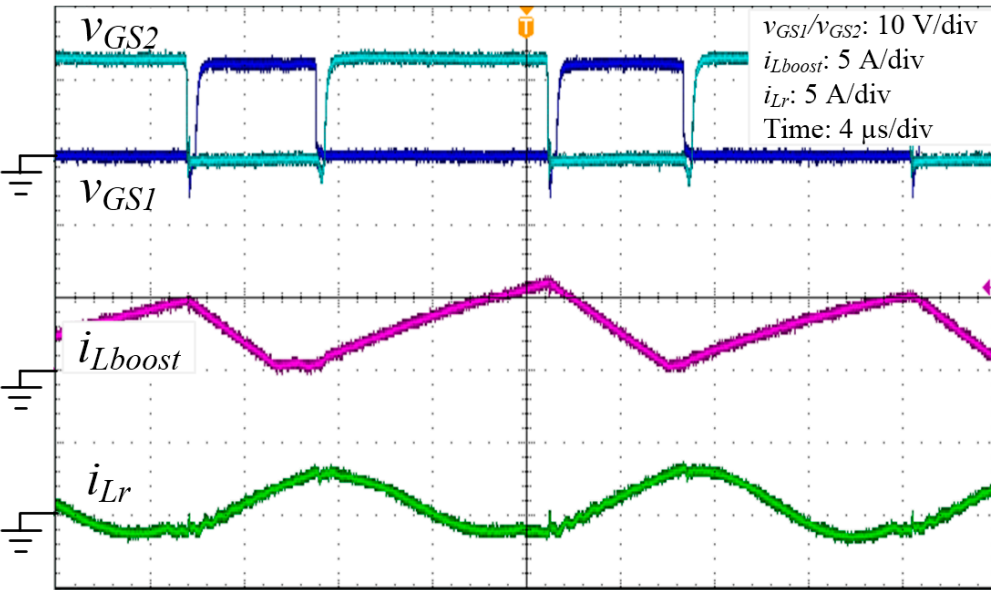
301   **Figure 6.** Waveforms for v_{GS1}, v_{GS2}, i_{Lboost} and i_{Lr} at different load current: (**a**) 1.6 A; (**b**) 3.2 A; (**c**) 4.7 A; (**d**) 6.3 A.

302

303

Figure 7. Waveforms for v_{ac}, i_{ac} and i_{Lboost} at $v_{ac} = 230\ V_{rms}$.

304   Figure 8 shows the gate-to-source waveforms and drain-to-source voltages for primary
305   switches Q_1 and Q_2 at the full-load. The waveform shows that V_{DS1} and V_{DS2} reach zero levels after Q_1
306   and Q_2 are turned on. Therefore, ZVS conduction is achieved so that overall conversion efficiency is
307   increased. The transient output voltage V_O during a step load current from 1.6 to 6.3 A and 6.3 to 1.6
308   A are shown in Figure 8 when input voltage of 230 V_{rms}, which shows that V_O can still be regulated.
309   Figure 10 depicts the bus voltage variation under 25%, 50%, 75% and 100% load condition and the
310   bus voltage is regulated around 430 V. Figure 11 also depicts the input current power factor. It
311   indicates that the power factor is greater than 0.9 at different load conditions. Figure 12 shows the
312   measured efficiencies of the proposed single stage asymmetrical half-bridge fly-back converter
313   through different outputs. The average efficiency is around 86% above which the rated full load
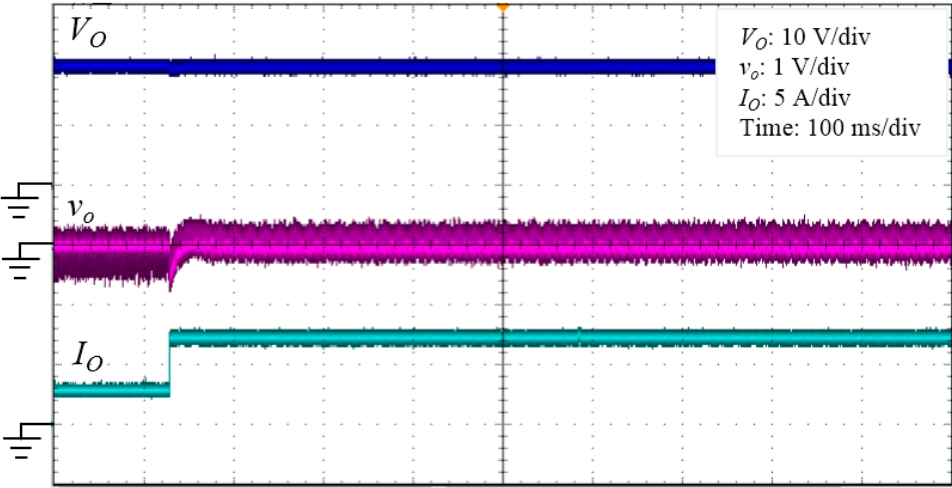314   efficiency is about 90%.

315

316
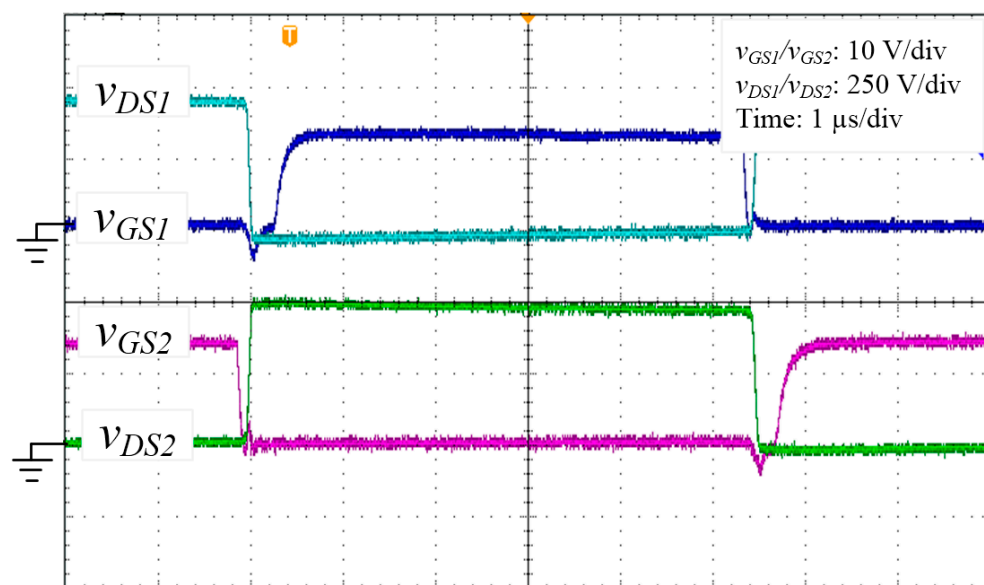
317   **Figure 8.** Zero-voltage turn-on switching for Q_1 and Q_2.

318

319

(a)

320
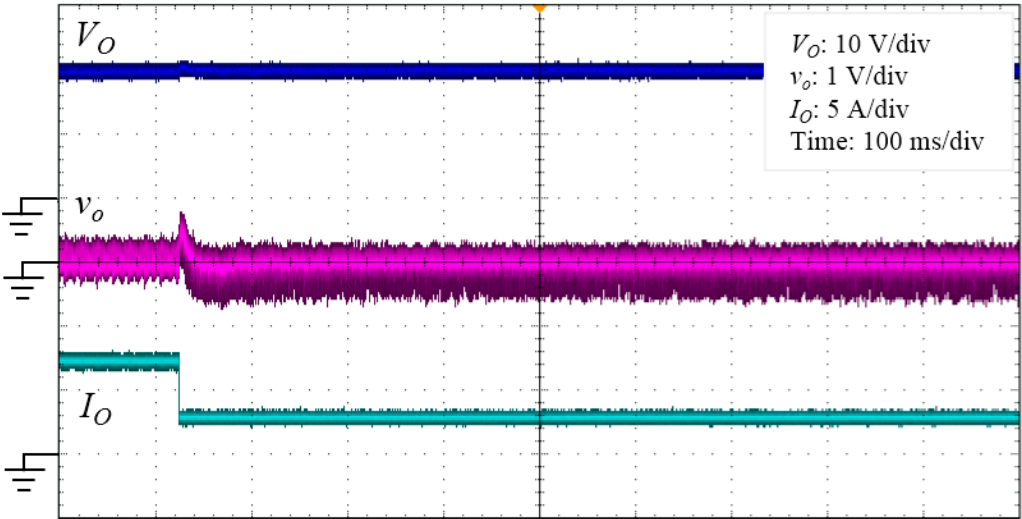
321

(b)

322   **Figure 9.** Load transient response under different loads: (**a**) 20% to 100%; (**b**) 100% to 20%.
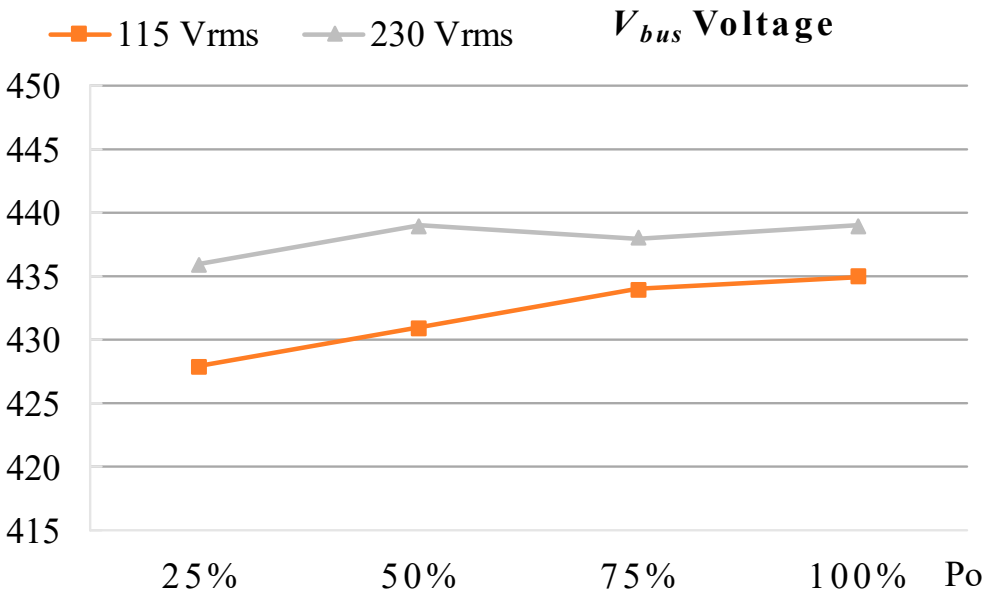
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324　　　　**Figure 10.** V_{bus} voltage variation curve for 115 V_{rms} and 230 V_{rms}.
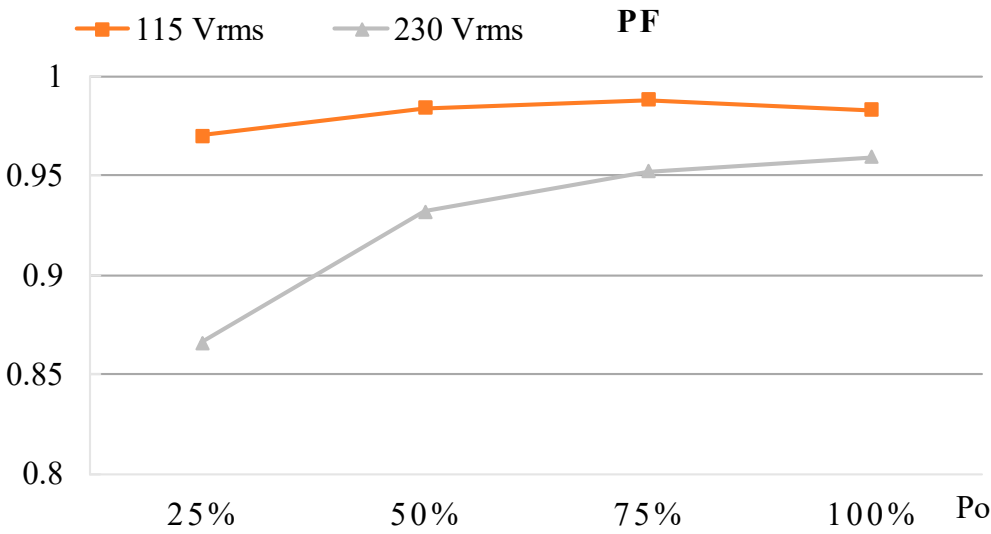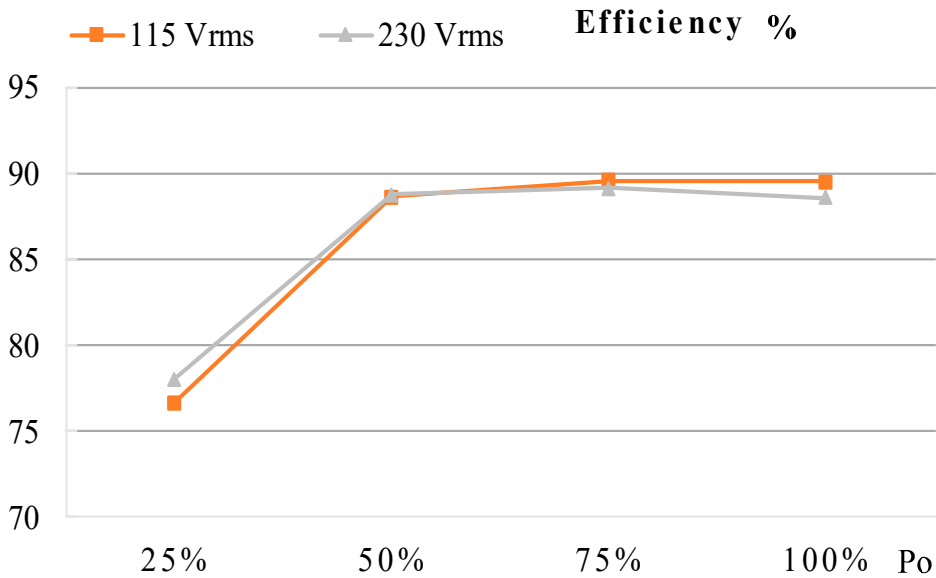

325

326　　　　**Figure 11.** PF curve for 115 V_{rms} and 230 V_{rms}.

327

Figure 12. Efficiency curve for 115 V_{rms} and 230 V_{rms}

5. Conclusions

This paper presented a single stage asymmetrical half-bridge fly-back converter with resonant mode. The switches operate simultaneously in the variable-frequency-controller (VFC) and pulse-width-modulation (PWM) control to regulate the bus voltage and output voltage. The operating modes in a complete switching cycle were analyzed and discussed in detail. The key equations were derived and the design procedures formulated. The experimental results on an AC input voltage 90 to 264 V_{rms} with output 120 W prototype were recorded to verify the theoretical scheme. The measured results show that the power factor is above 0.9, the average efficiency is around 86% and the highest conversion efficiency is about 90%. The proposed single stage asymmetrical half-bridge fly-back converter is especially suitable for low-to-medium power level applications.

Author Contributions: Chung-Yi Ting designed, simulated the work, and wrote the paper; Yi-Chieh Hsu implemented the work and performed the experiment; Jing-Yuan Lin and Chung-ping Chen provided all material for implementing the work, supervised the design, circuit simulation, analysis, experiment, and correct the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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