Article

High Step-up Modular Switched-Capacitor DC-DC Converter with Fault Tolerance Capability

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Abstract: A modular switched-capacitor (SC) DC-DC converter (MSCC) is introduced in this paper. It is designed to boost a low input voltage to a high voltage level and can be applied for photovoltaics and electric vehicles. This topology has high extensibility for high voltage gain output. The merits of the converters also lie in the fault tolerance operation and the voltage regulation with a minimum change in the duty ratio. Those features are built in when designing the modules and then integrating these into the DC-DC converter. Converter performance including voltage gain, voltage and current stress are focused and tested. The converter is modelled analytically, and its control algorithm is analyzed in detailed. Both simulation and experiment are carried out to verify the topology under normal operation and fault mode operation.

Keywords: DC-DC power converter, Fault Tolerance, Multilevel Converter, Switched-Capacitor network.

1. Introduction

With the pace of the third industrial revolution, traditional fossil fuel-based energy is meant to give away to renewable energy. To establish a low carbon economy, extensive use of power electronics is becoming a norm, for example in smart grids and electric vehicles (EVs) applications. This has led to increased controllability and energy saving as well as environmental benefits [1]. DC-DC converters are a key technology to interface two DC components so as to regulate the voltage level. They connect a low voltage input such as photovoltaic or batteries and generate a higher voltage output. Ideally, they should have high voltage step up, fault tolerance, modularization and flexible voltage output [1]–[3]. But these criteria often conflict with one another.

High step up conversion has become a topic of interest over the three decades [4]. Many methods to increase the converter output has been explored. They can be divided into following categories: switched inductor, magnetic coupling and switched capacitor.

Switched-inductor technique is typically used in providing high step up conversion. In [5], Fig. 1(a) is the overall topology of switched-inductor converter. Fig. 1(b) presents the basic switched-inductor cell, it allows the two inductors charging in parallel and discharging in series. Fig. 1(c) (d) and (e) represent the alternative structures of switched-inductor cell [6], [7]. They are the combination of switched-inductor and switched-capacitor techniques. They are simple structure and have low current ripple. However, they need to use more inductors than other structure which increase the volume of the converters.

The second technique is magnetic coupling, it utilizes high frequency transformer to generate output voltage which is proportional to the turns ratio [8], [9] (as shown in Fig. 2). By regulating the turns ratio, the output voltage can be tuned as will. However, the turns ratio is limited by leakage inductance. Very high leakage inductance can give rise to voltage drop and power losses.

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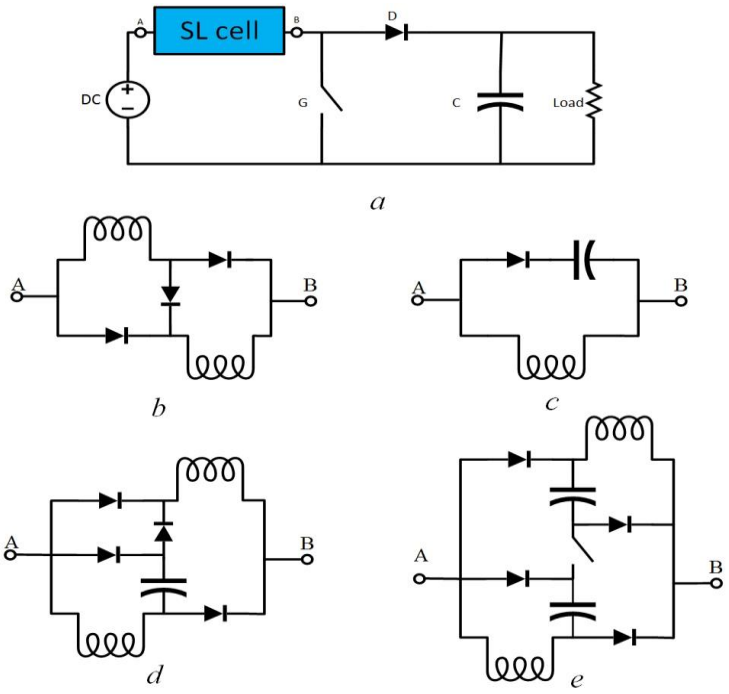

Fig. 1. *Switched-inductor topology reviewed in [5].*

(a)Switched-inductor overall topology, **(b)**Basic switched-inductor cell, **(c)**Elementary lift switched-inductor cell, **(d)**Self-lift switched-inductor cell, **(e)**Double self-lift Switched-inductor cell

Switched-capacitor technique is a common method applied for high step up conversion in recent years. In [10], a combination of coupled inductors and switched capacitor is presented, capacitors in this topology charge and discharge alone with the stages of inductors (in Fig. 3(a)). A simpler structure has been published in [11] (in Fig. 3(b)). Two capacitors charge in parallel and would discharge in series, due to the existence of the diodes. More modification shown in Fig. 3(c) and (d) are studied in [12][13]. These the converter lack fault tolerant capacity, authors focused on normal operation performance. However, in some switched-capacitor topologies, the voltage across the capacitors are different at different locations. This creates a difficulty for modularization design of the converter.

In addition to voltage regulation, the converters fault tolerance is also an important feature [14], [15]. Fault isolation operation needs to identify and isolate a happened fault. In a parallel system, controlling the corresponding switches to cut off the faulty module is sufficient, so redundant components are embedded in those fault tolerance systems. However, if the faulty components are connected in series with other components, a bypass route is needed to establish. It is understood that system performance will be reduced, while, the control strategy can compensate the effect.

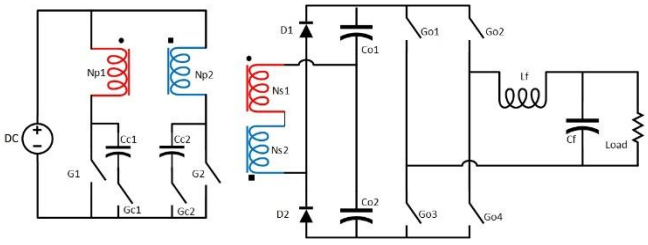

Fig. 2 *Converter in [12].*

Based on switched-capacitor topology, a new converter is proposed to combine modularization and fault tolerance feature whist maintaining high power density and low cost. This converter is designed to ride through any open circuit faults for the two kinds of the most vulnerable components: IGBTs and capacitors. Detailed explanations are divided into 4 sections: first

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the circuit architecture and operation principles are presented. Following section shows the detailed analysis including system modelling, major components stress analysis and parameter setting for passive components. Third section presents the fault tolerance methods. Last one is the demonstration of the proposed converter by means of simulation and experiment. After these explanations, a sententious conclusion is addressed at the end of the paper.

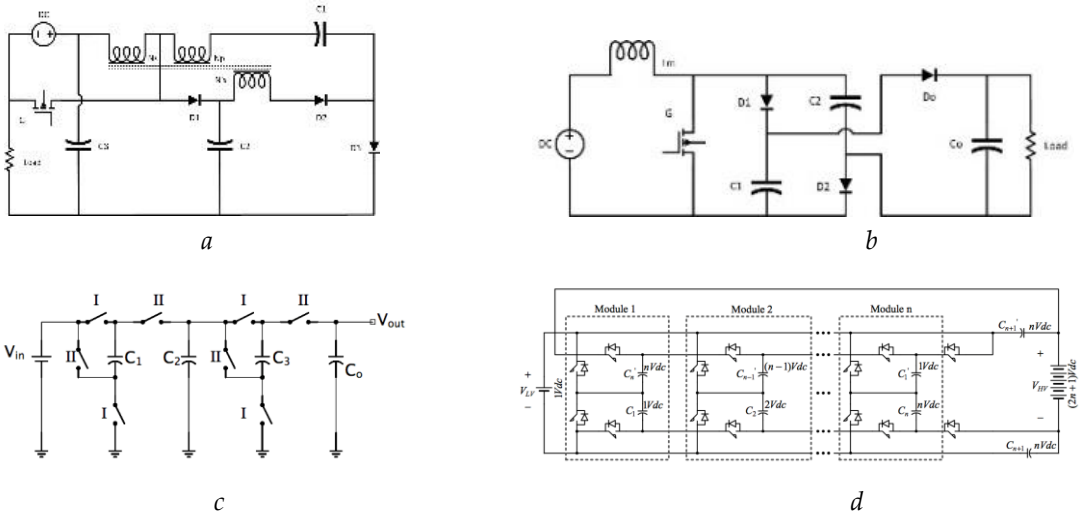


Fig. 3. *Switched-capacitor technique*

(a)Converter in [10], **(b)**Converter in [11], **(c)**Converter in [12], **(d)**Converter in [13]

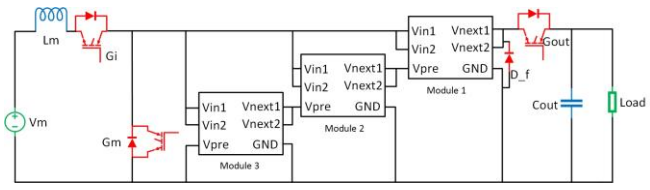
2. Circuit Description of the Proposed Converter

In this section, a detailed description of the proposed converter would be presented, along with an analysis of system performance.

2.1. Circuit Architecture

Fig. 4(a) is an illustration of the topology of the proposed MSCC. It contains 3 identical modules as shown in Fig. 4(b). Insulated Gate Bipolar Transistors (IGBTs) S1, S2 and S3, S4 control current flow from and to the capacitors; the capacitor C1 is connected between the collector end of S1 and the middle point of the half bridge formed by S3 and S4 capacitor C2 is connected to the collector end of S2, and it share the other end with C1. The collector end of S3 is solely connected to $\boldsymbol{V_{pre}}$ (representing the output end of the previous module.); the emitter of S1 and S2 are connected to the input source; the emitters of S4 is connected to the ground, the collector end of S1 and S2, as previous mentioned, are connected to $\boldsymbol{V_{next}}$ (representing the output of this module). A D_f diode is embedded in the last model for fault tolerance operation.

The module of the proposed converter is similar to traditional MSCC. Traditional MSCC would requires output capacitor with larger capacitance as the number of module increase. Meanwhile, in the proposed converter, all the component parameter is identical, it can be very easy to maintain and replace the fault module. And with voltage regulation capability, even with by faulted module remaining in the system, the entire voltage could be tuned to the rated level.



a

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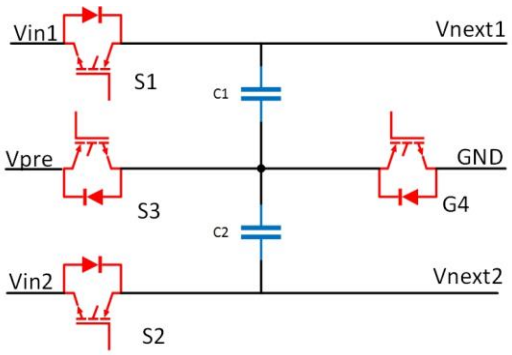


b

Fig. 4. *Proposed MSCC DC converter*

(a)Overall structure, **(b)**Module structure.

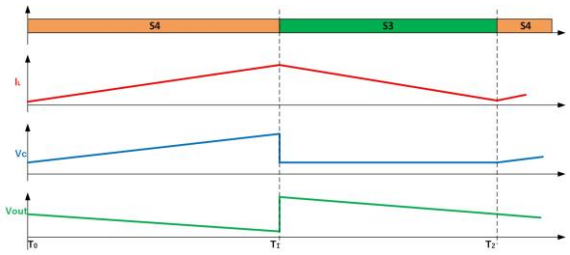
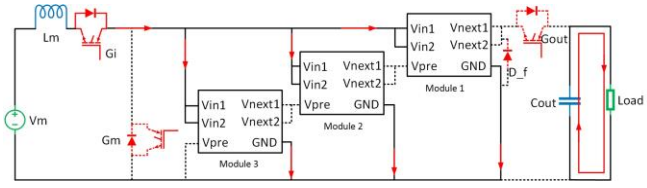


Fig. 5. *The waveform of the proposed converter*

2.2. Principles of Operation

The normal operation of this converter requires the transistor Gout turning off and Gi turning on during the entire procedure. In the reverse directional operation, Gout turning on is necessary, while when the first module needs to be bypass as fault isolation, Gi turning off is required. The normal function of the entire system is based on proper control of the transistors in all modules. The control for each module is identical. There are only two stages in the system, as presented in Fig. 5. In the first stage, S4 is switched on and S3 switched off. The input voltage is charging the module capacitors along with input inductor, the module detail is shown in Fig. 6. The second stage (shown in Fig. 7) is input voltage charging input inductor and all the output capacitor start to transfer energy to the load. In this case, the S3 is switched on and S4 is switched off. The energy would transfer from all the module capacitors to load. In normal operation mode, S1 and S2 can be turned off for the entire procedure, using freewheeling diode to charge the module capacitors. The signals for those transistors are only required when fault isolation or bidirectional operation is proceeding. In this paper, only fault isolation is discussed. The module capacitors in these two stages is charging in parallel and discharging in series, realizing the function of "switched capacitor".



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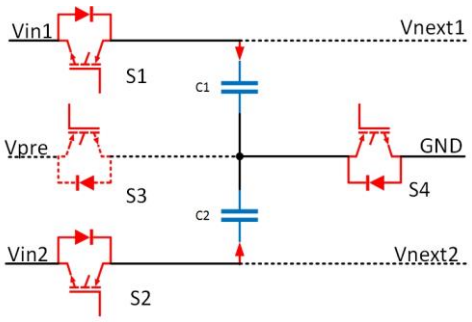
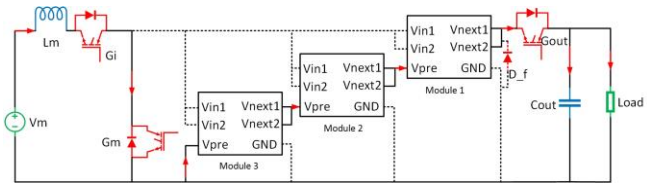


b

Fig. 6. *Charging mode of the proposed converter*

(a)Route of the overall circuit, **(b)**Route of the modules.



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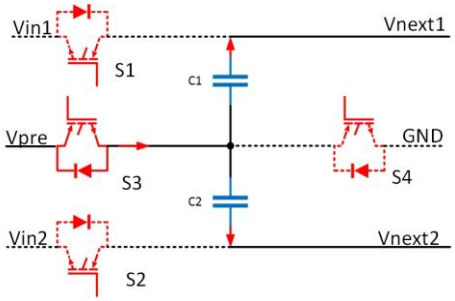

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Fig. 7. *Discharging mode of the proposed converter*

(a)Route of the overall circuit, **(b)**Route of the modules.

3. Circuit Analysis

Some assumptions are made to simplify the analysis.

- The capacitors in all modules are identical;
- All transistors are ideal;
- The dead time effect is neglected;

3.1. System modelling

In the charging stage, the system differential equations can be obtained by using the volt-time balance principle:

$$\begin{cases} (1-D)\cdot(v_{in}-v_c) = (1-D)\cdot L\cdot\frac{di_L}{dt} \\ (1-D)\cdot i_L = (1-D)\cdot C_n\cdot\frac{dv_c}{dt} \end{cases} \quad (1)$$

In the discharging stage:

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$$\begin{cases} D \cdot v_{In} = D \cdot L \cdot \frac{di_L}{dt} \\ D \cdot i_s = \frac{D \cdot N \cdot v_c}{R} = D \cdot C_n \cdot \frac{dv_c}{dt} \end{cases} \quad (2)$$

Combine the two stages:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{ND}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{IN} \quad (3)$$

$$\begin{cases} A = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{N \cdot D}{R \cdot C} \end{bmatrix} \\ B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \end{cases} \quad (4)$$

Using Laplace transform:

$$\begin{bmatrix} i_L(s) \\ v_c(s) \end{bmatrix} = (I \cdot s - A)^{-1} \cdot B = det(I \cdot s - A) \cdot \begin{bmatrix} \frac{1}{L}(s - \frac{N \cdot D}{R \cdot C}) \\ \frac{1-D}{CL} \end{bmatrix} \quad (5)$$

The output voltage small-signal transfer function of the proposed modularized switched capacitor converter can be expressed as:

$$G_{vd}(s) = \frac{b}{s^2 + a_1 s + a_2} \quad (6)$$

where:

$$\begin{cases} a_1 = -\frac{ND}{RC} \\ a_2 = \frac{(1-D)^2}{CL} \\ \mathrm{b} = \frac{1-D}{CL} \end{cases} \quad (7)$$

The bode diagrams of the proposed converter are demonstrated in Fig. 8. The system slop inclination is about -20 dB/dec. The magnitude analysis of the converter indicates an unstable state of the converter when encountering a low frequency input noise, on the other hand, the system has high stability against high frequency input noise. The phase angle is -180 degrees indicating the stability of the converter. Based on above analysis, a close loop is necessary to deal with any low frequency input disturbance. The control loop for this topology can be easily implemented as shown Fig. 9.

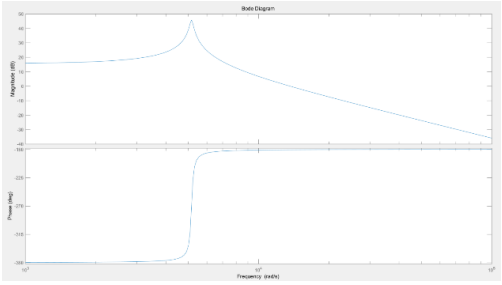

Fig. 8. *Bode analysis of the open-loop of the proposed converter*

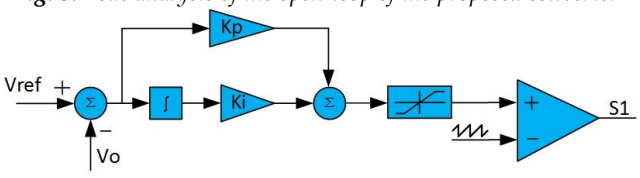

Fig. 9. *PI controller of the proposed converter*

3.2. Voltage Ratio Range.

The capacitor voltage for each module can be express as:

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$$V_c = \frac{V_{in}}{1-D} \tag{8}$$

Because at the second stage, the load is connected in series with all output capacitors in the submodule, then the entire output voltage is:

$$V_{out} = \frac{N \cdot V_{in}}{1-D} \tag{9}$$

The relationship of output voltage gains of the proposed converter and the module number is presented in Fig. 10.

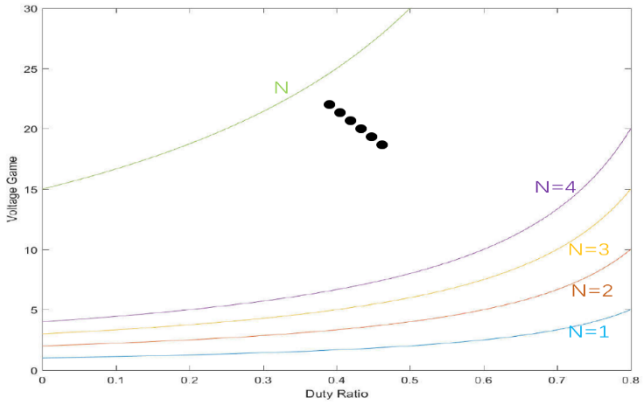

Fig. 10. *Voltage gain of the proposed converter*

3.3. Current Stress

The inductor is in series with the input voltage source, which means the inductor current stress is larger than the maximum current output of the DC voltage source. As with the switches, N modules would divide the input current into 1/N. Moreover, S2 and S3 are switched on in the same time. Thus, for L, S1, S2 and S4, the RMS current stresses are:

$$\begin{cases} I_{stress,L} = I_{in} = I_l \\ I_{stress,S1} = \frac{DI_l}{2N} \\ I_{stress,S2} = \frac{DI_l}{2N} \\ I_{stress,S4} = \frac{DI_l}{N} \end{cases} \tag{10}$$

For S3, the switch is carried the current to charge the output capacitor for the entire system. The maximum current flow through S3 is:

$$I_{stress,S3} = （1-D）I_l \tag{11}$$

3.4. Voltage stress

For each module, the voltage stress for S3 identical to the module capacitors:

$$V_{stress,S3} = V_c \tag{12}$$

The rated voltage for S1 and S2 are the same for its symmetrical connection. They are blocking the positive end of the current module capacitors, thus the voltage stress for S1 and S2 are:

$$V_{stress,S1} = V_{stress,S2} = N \cdot V_c \tag{13}$$

The voltage stress for S4 can be deduced as following analysis: due to series connection of the output module capacitors, in the Nth module, S4 needs to block the voltage from all the output former module capacitors in series connection so that, the voltage stress for S4 is:

$$V_{stress,S4} = (N-1) \cdot V_c \tag{14}$$

The common maximum stress voltages for commercial IGBT are 600 and 1200 V. In this project, 600 V stress voltage level is sufficient.

3.5. Current Ripple

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All the submodule structures are identical, and so it is with all the capacitor parameter. One module is analysis to represent the entire system. As input voltage regulator, the current ripple should be written as:

$$V_{in} = L\frac{dI_l}{dt} \tag{15}$$

where the $\boldsymbol{V_{in}}$ is the input source voltage and $\boldsymbol{I_l}$ is the input current in the above equation. In order to maintain continuous operation mode and decrease total harmonic distortion (THD), the input current ripple should be limited to certain level. To fulfil all the criteria, the inductance should obey:

$$L \geq \frac{V_{in} \cdot dt}{dI_l} \tag{16}$$

where the system switching frequency is limited to less than 20 kHz, and the output voltage is set to 20V. If the rated system power is set to 160w, the inductance for continuous operation can be calculated as:

$$L \geq 15.625\ uH \tag{17}$$

For this project, a 320 $\boldsymbol{\mu}$**H** inductor is selected to minimize the oscillation in the circuit, small inductance would cause the module capacitor voltage to oscillate for half cycle in discharging mode, when duty ration is set to 0.5, the current ripple can be derived as:

$$\Delta I_l = 1.5625\ A \tag{18}$$

3.6. Voltage Ripple

In each module, the voltage ripple is determined by the capacitance of the module capacitor, input current and switching frequency:

$$\Delta V_c = \int_0^T \frac{I_c}{C} dt \tag{19}$$

The capacitance then calculated as:

$$\mathrm{C} = \frac{k \cdot V_c \cdot f_s}{I \cdot D} \tag{20}$$

where K is the error ratio of the output voltage, $\boldsymbol{f_s}$ is the switching frequency and D is duty ratio of S1, S2 and S4.

If there are 3 modules for the system, and 5% voltage ripple is allowed, and the rest system setup is the same as mentioned before, the minimum capacitance is:

$$\mathrm{C} \geq 25\mathrm{uF} \tag{21}$$

For this project, a 47uF capacitor is selected, the current ripple can be derived as:

$$\Delta V_c = 1.064\ \mathrm{V} \tag{22}$$

3.7. Comparison of Other Switched Capacitor DC-DC converters

The output voltage gain of the proposed SC DC-DC converter is given in formula (8) and compared with traditional SC DC-DC converter in Fig. 3(c) and module SC DC-DC converter in Fig. 3 (d). The expressions of the deal voltage gains are shown in TAB. 1. For the traditional SC converter each module is capable for double the voltage and module SC DC-DC converter has an overall voltage gain of 2N+1. However, the Proposed SC DC-DC converter has an extra dimension (duty ratio) to increase the output voltage to a theoretic value of 2N when duty ratio equals to 50%. As for the voltage stress of the module capacitors, the proposed SC DC-DC converter is a fix value once the number of modules in the systems is finalized, which makes this topology easy to replace faulty module as only one module circuit is needed. For the other two topologies, the voltage stress various between different modules, which means, to replace the modules in different position, different capacitors are needed, and the circuit need to alter for different capacitors. The number of the module elements of all the compared topologies are identical, there are 2 capacitors and 4 transistors in one module. The proposed converter embeds the boost converter into the circuit to tune the output

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voltage, so there is an extra inductor is required in the topology. And another merit of the propose SC DC-DC converters is the fault tolerance capability which the other topologies lack of.

TAB. 1. Comparison of the SC converters

Topologies	SC converter in Fig. 3(c)	SC converter in Fig. 3(d)	Proposed SC converter
Voltage gain	2^N	2N+1	$\frac{N}{1-D}$
Voltage stress of module capacitors	$2M \cdot V_{in}$	$M \cdot V_{in}$	$\frac{V_{in}}{1-D}$
Number of module capacitors	2	2	2
Number of module transistors	4	4	4
Number of inductors	0	0	1
Fault tolerance capability	No	No	Yes

4. Fault Tolerance Operation

Fault tolerance operation has becoming a crucial aspect for pulse width modulation (PWM) DC-DC power converter, especially for modern industrial application such as electric vehicles, HVDC power transmission, island DC power network and even military application. Ensure normal function is important to system aforementioned regarding economic damage and safety issues. Two categories of components have higher risk of damage due to electrical and thermal stress than other component: semi-conductor and capacitors.

In this module, three fault scenarios are discussed which are open circuit faults (OCF) at IGBTs and capacitors.

4.1. Capacitor open circuit fault

The capacitor in each module is used to deliver energy from the source to the load in series connection, when one module has capacitor OCF, without fault isolation, the entire system would shut down gradually. Taking the Mth module as an example to demonstrate the fault isolation principle.

When C_{mn} is detected as a fault element (n is representing the capacitor,), the Sn switch from the current module would keep turning off for the entire fault operation stage, which means faulted capacitor is isolated from the capacitor charging stage. On the other hand, in capacitor discharging stage, the Sn switch from the next module would be switched off to eliminate any disturb from the faulted capacitor for the converter. The current path is indicated as shown in Fig. 11. However, it would increase the current stress of the other capacitor corresponding transistor.

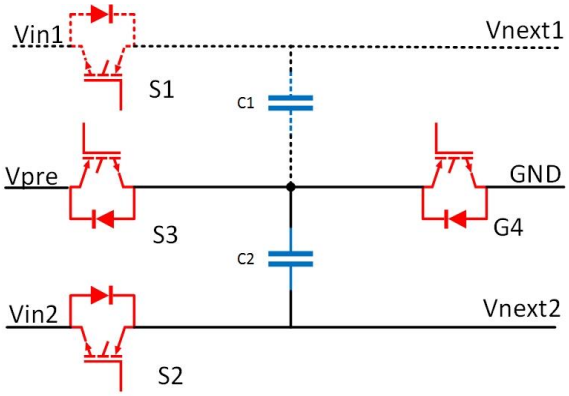

Fig. 11. *Fault isolation in the module for signal transistor or capacitor fault*

In this situation, the output voltage for the system would still be the same compared to normal operation mode.

4.2. S1, S2 open circuit fault (OCF)

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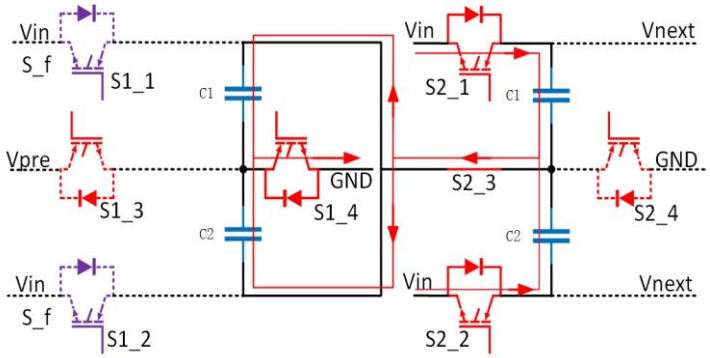
S1 and S2 OCF is the very convenient to deal with, for each individual of them has OCF, the consequence would be the same as the corresponding capacitor OCF. If S1 and S2 have OCF at the same time, the entire faulty module needs to be bypassed. The circuit would react in the following state (Fig. 12). In these two diagrams, the faulted transistor S1_1 and S1_2 is marked as S_f. To maintain the output capacitors chain, the capacitor in the next module will be charging alone with the ones in faulted module in series. To distinct the switches in different module, sub-labels are introduced in the following discretions. As presented in Fig. 12(a), the S2_1, S2_2, S2_3 and S1_4 turn on, and the rest are off. And in Fig. 12(b), S2_3, S1_3 would be turned on and the rest are off. However, the connection would result in reduction of the output voltage level, the compensation would be done by tuning the duty ratio. It would result in voltage stress raise on the capacitors in the remaining modules. In the case of this kind of fault occurs in the last module, there is no next module to help bypass the fault. As shown in Fig. 4, a bypass diode (d_f) is introduced between the ground and the output end of the last module to bypass the fault, it would not have any influence on normal operation.



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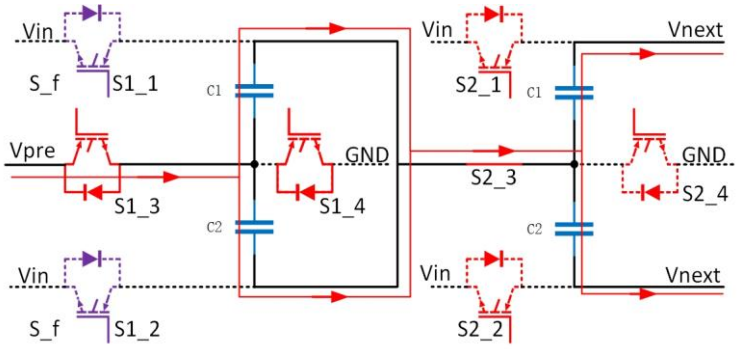

b

Fig. 12. *S1 and S2 Fault isolation mode*

(a)Charging mode, **(b)**Discharging mode

4.3. S3, S4 OCF

Dealing with S3, S4 OCF individually or together is identical, both faulty switches would be treated as open circuited in both scenarios. S1 and S2 switch from the previous module would charge the corresponding capacitors and so said switches would also be used to discharge the so said capacitors. In this way, the entire faulty module is bypassed, as shown in Fig. 13. Duty ratio will be modified to minimize the effect.

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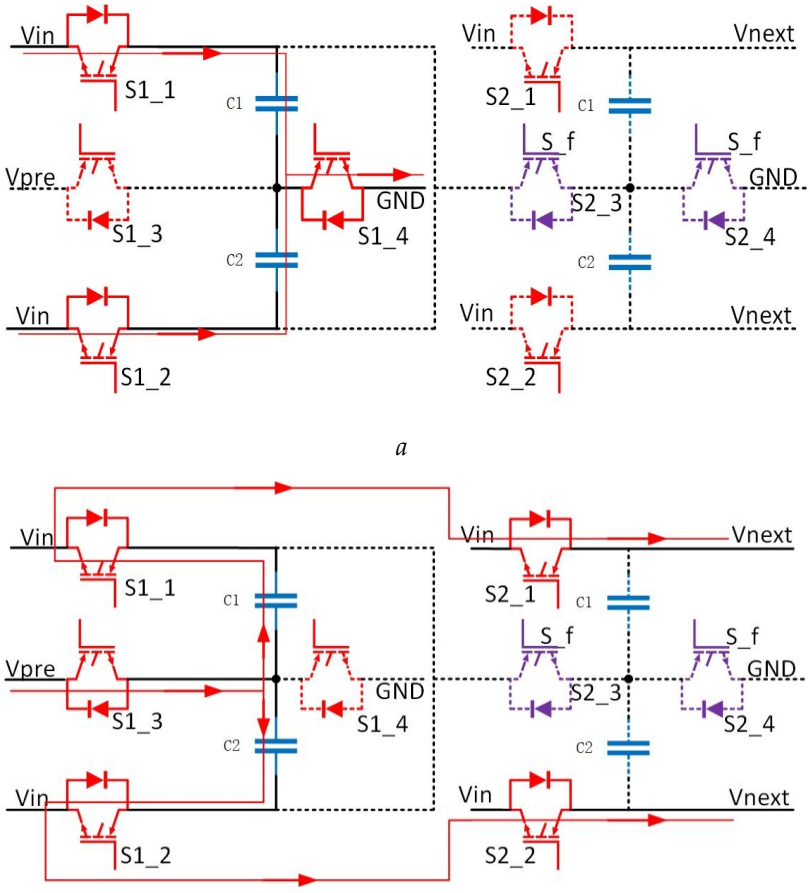

Fig. 13. *S3 and S4 Fault isolation mode*

(a)Charging mode, **(b)**Discharging mode

5. Simulation and Experimental Results

The proposed converter has been simulated in large input voltage for high power system, however, due to lab limitation, the practical experiment is carried out for lower power system. The detailed expression would be presented in the follow content.

5.1. Simulation results

A detailed inspection has been carried out for the proposed DC-DC converter. The simulation has been proceeded in PSIM software, the system parameters is presented in TAB. 2. Close loop is only carried out in simulations in this paper.

TAB. 2. Specifications of the simulated proposed converter

Module capacitor (μF)	47	Switching Frequency (kHz)	20
Input inductor (μH)	47	Input voltage (V)	200
Output capacitance(each)(μF)	470	Load resistance (Ω)	200
Number of Modules	3	Duty Ratio	35%

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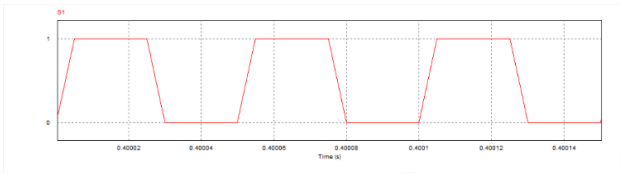

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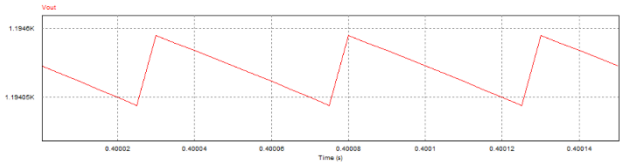

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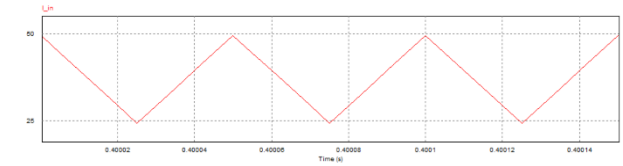

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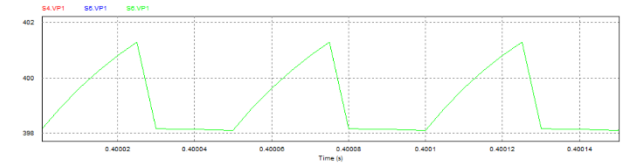


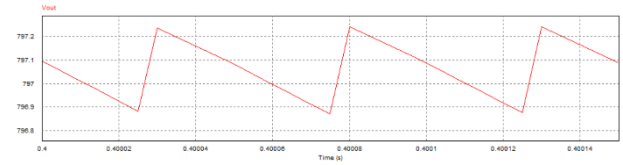
d

Fig. 14. *Simulation results of the proposed converter*

(a)S1 switching signal, **(b)**Input current waveform, **(c)**Output voltage waveform, **(d)**Capacitor voltage waveform

Fig. 14 is the simulated indication of proper function in normal operation. Fig. 14(a) presents the simulated gate signal for S1, S2 and S4. The system boosted 200V DC voltage into 1190V DC (Fig. 14(b)), the input current (Fig. 14(c)) and the module capacitor voltages (Fig. 14(d)) are similar to the analytical result in Fig. 5.

Fig. 15 and Fig. *16* are the demonstration of S1, S2 module capacitor OCF and S3, S4 OCF respectively in open circuit test. The former situations require the entire module bypassed, so that one of the module capacitor voltage drops to zero, and the others are intact. Thus, the output result is compromised into two third of the original output. In the later scenario shown in Fig. 16, the voltages of the capacitors participating in fault isolation drop to half of those in the normal function mode. It is because of the series connection in the fault isolation procedure. The close loop results are identical with the open circuit operation in the steady state.



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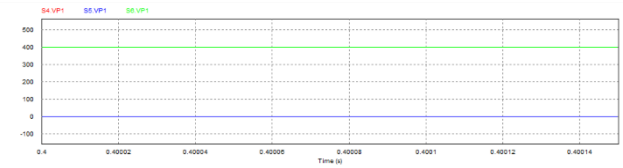

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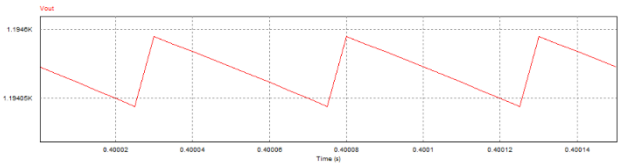
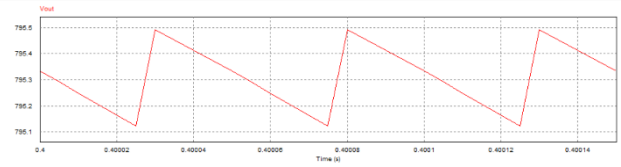


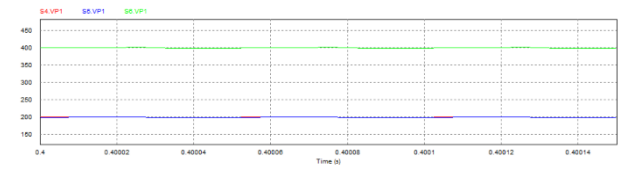
c

Fig. 15. *Simulation results of Proposed converter (S1, S2 OCF)*

(a)output voltage without voltage regulation by tuning duty ratio, **(b)**Module capacitor voltages, **(c)**output voltage with voltage regulation by tuning duty ratio



a



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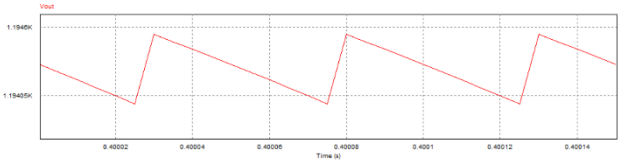

b

Fig. 16. *Simulation results of Proposed converter (S3, S4 OCF)*

(a)output voltage without voltage regulation by tuning duty ratio, **(b)**Module capacitor voltages, **(c)**output voltage with voltage regulation by tuning duty ratio

5.2. Experiment results

Experiment platform has been established to verify the simulation. Due to lab limitation, low voltage and power system was tested. TAB. 3 is the specification of the experimental parameter. The following diagrams indicate the normal and fault operation. The faulty scenarios are implement by manual toggle switches, which they simulate the open circuit fault of the transistors and capacitors. All the experiments are proceeded for open circuit tests to prove the concept.

TAB. 3. Specifications of the experiment of the proposed converter

Module capacitor (μF)	47	Switching Frequency (kHz)	20
Input inductor (μH)	47	Input voltage (V)	15
Output capacitance(each)(μF)	470	Load resistance (Ω)	100
Number of Modules	3	Duty Ratio	35%

Fig. 17 presents experimental results. Fig. 17(a) is the normal operation output voltage. According to (8), the output voltage should be 75 V, and the experiment result shows the actual output voltage is 72.12 V. The difference is caused by diode voltage drop and losses. The output voltages for fault operations are presented in Fig. 17(b) and (c). From the fault analysis and simulation, one Nth of the output voltage would be compromised due to fault bypass. Practical results show

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close output voltages: 46.46 and 47.17 V, which consists with the analytical and simulation result. Fig. 17d and e show the faulty module capacitor voltages from two faulty scenarios. They also support the analytical and simulation result. Fig. 18 shows the efficiency of the system.

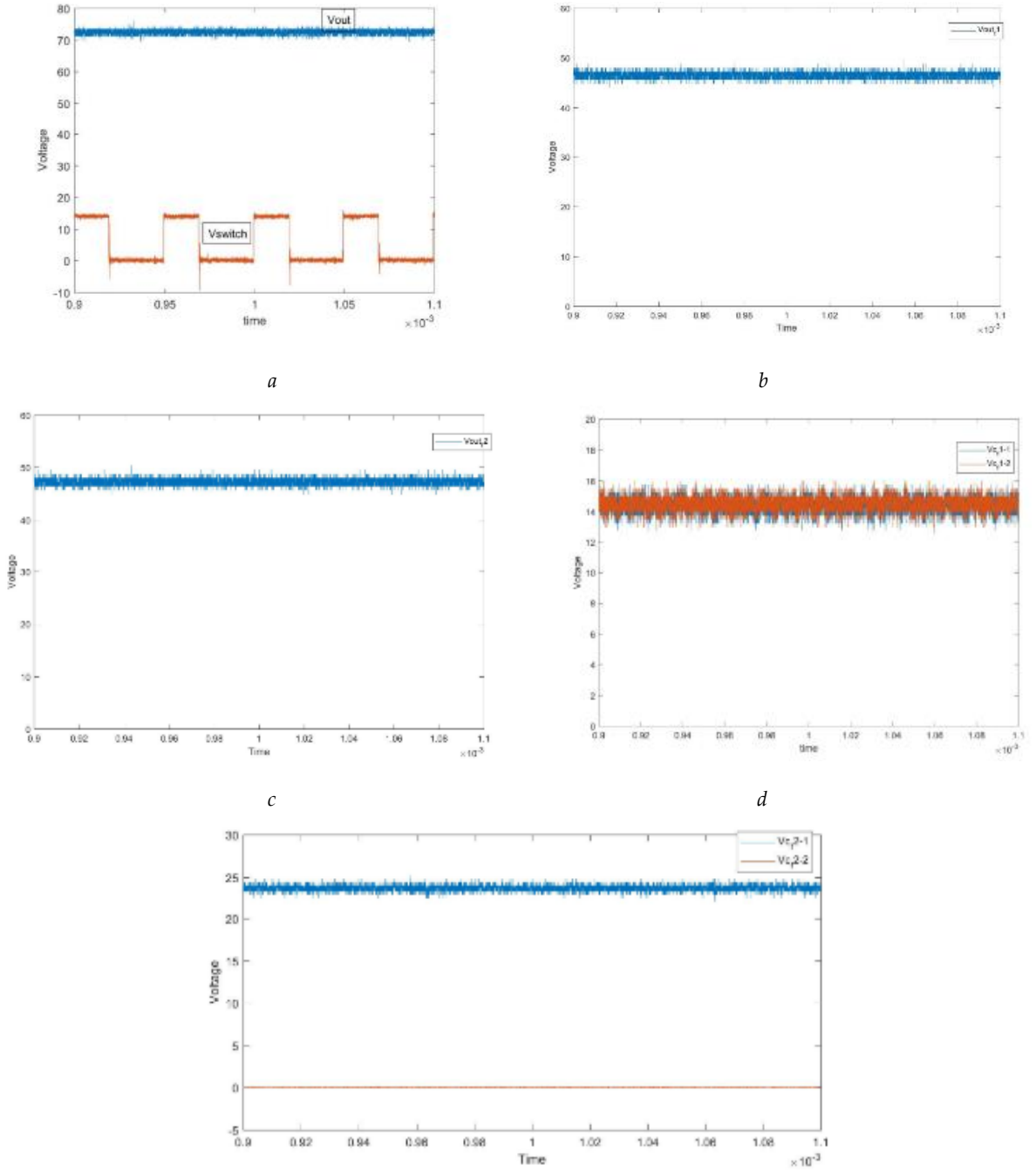

Fig. 17. *Experiment results*

(a)Normal operation output voltage, **(b)**Output voltage for S1, S2 fault operation, **(c)**Output voltage for S3, S4, capacitor fault operation, **(d)**Fault module and normal capacitor voltages for S1, S2 OCF, **(e)**Fault module capacitor voltages for S3, S4, capacitor OCF

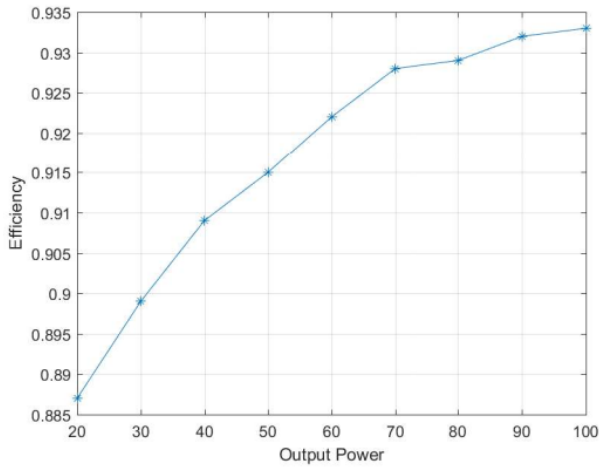

Fig. 18. *Efficiency of the proposed converter.*

6. Conclusion

This paper has presented and analyzed a modularized switch capacitor DC-DC converter. It has high extensibility for high voltage gain output and fault tolerance under open circuit faults in capacitors and transistors. Due to the ability to bypass modules, the voltage can be regulated with a minimum duty ratio change. The circuit architecture, operation principle, voltage/current stress and fault tolerance operation are explained in detailed. The voltage regulation method is also presented. In the end, simulations and experimental results have verified the effectiveness of the proposed converter and output with satisfactory fault tolerant operation and energy efficiency.

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References

1. C. C. Chan: 'The state of the art of electric, hybrid, and fuel cell vehicles', *Proc. IEEE*, 2007, **95**, (4), pp. 704–718
2. A. Khaligh and Z. Li: 'Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the Art', *IEEE Trans. Veh. Technol.*, 2010, **59**, (6), pp. 2806–2814
3. A. Emadi, Y. J. Lee, and K. Rajashekara: 'Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles', *IEEE Trans. Ind. Electron.*, 2008, **55**, (6), pp. 2237–2245
4. O.-C. Mak, Y.-C. Wong, and A. Ioinovici: 'Step-up DC power supply based on a switched-capacitor circuit', *IEEE Trans. Ind. Electron.*, 1995, **42**, (1), pp. 90–97
5. M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman: 'Step-Up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications', *IEEE Trans. Power Electron.*, 2017, **32**, (12), pp. 9143–9178
6. Y. Jiao, F. L. Luo, and M. Zhu: 'Voltage-lift-type switched-inductor cells for enhancing DC-DC boost ability: Principles and integrations in Luo converter', *IET Power Electron.*, 2011, **4**, (1), pp. 131–142
7. Y. Tang, T. Wang, and D. Fu, "Multicell Switched-Inductor/Switched-Capacitor Combined Active-Network Converters', *IEEE Trans. Power Electron.*, 2015, **30**, (4) pp. 2063–2072
8. W. Li and X. He: 'Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications', *IEEE Trans. Ind. Electron.*, 2011, **58**, (4), pp. 1239–1250
9. W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu: 'High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback-forward converter', *IEEE Trans. Ind. Electron.*, 2012, **59**, (1), pp. 599–610

10. Y. P. Siwakoti and F. Blaabjerg: 'Single switch nonisolated ultra-step-up DC-DC converter with an integrated coupled inductor for high boost applications', *IEEE Trans. Power Electron*., 2017, **32**, (11), pp. 8544–8558
11. E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun: 'A family of single-switch PWM converters with high step-up conversion ratio', *IEEE Trans. Circuits Syst. Regul. Pap*., 2008, **55**, (4), pp. 1159–1171
12. L. He and Z. Zheng: 'High step-up DC-DC converter with switched-capacitor and its zero-voltage switching realisation', *IET Power Electron*., 2017, **10**, (6), pp. 630–636
13. X. Zhu, B. Zhang, Z. Li, H. Li, and L. Ran: 'Extended switched-boost DC-DC converters adopting switched-capacitor/switched-inductor cells for high step-up conversion', *IEEE J. Emerg. Sel. Top. Power Electron*., 2017, **5**, (3), pp. 1020–1030
14. Z. Gao, C. Cecati, and S. X. Ding: 'A survey of fault diagnosis and fault-tolerant techniques part I: Fault diagnosis with model-based and signal-based approaches', *IEEE Trans. Ind. Electron*., 2015, **62**, (6), pp. 3757–3767
15. Z. Gao, C. Cecati, and S. X. Ding: 'A survey of fault diagnosis and fault-tolerant techniques part II: Fault diagnosis with knowledge-based and hybrid/active approaches', *IEEE Trans. Ind. Electron*., 2015, **62**, (6), pp. 3768–3774