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# Conducted Electro Magnetic Interference Spectral Peak Mitigation in Luo Converter Implementation Using FPGA Based Chaotic PWM Technique

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**Abstract:** Chaotic switching is a newly evolve randomization method which can suppress conducted electromagnetic interference generated within the DC-DC converter. It can suppress the spectral peaks present in the frequency band effectively by spread spectrum technique and can spread it over the wide range of frequency band implying EMI suppression. In this paper, a chaotic PWM technique based on RCFMFD scheme is generated through Field programmable gate array (FPGA) for suppressing the conducted electromagnetic interference (EMI) generated within the Luo converter. A hardware prototype of Luo converter was developed in order to analyze EMI reduction through FFT analysis by comparing both traditional periodic PWM switching and chaotic PWM switching. The results obtained from the hardware setup shows significant reduction of EMI with Chaotic switching as compared to traditional PWM switching for both boost and buck operation of Luo converter.

**Keywords:** EMI; Luo-converter; chaotic PWM technique; FPGA; RCFMFD.

## 1. Introduction

Electromagnetic interference (EMI) is one of the major issues which are faced by the industries and the users who deal with the electrical and electronic equipment on the daily basis. EMI is an undesirable noise which affects the performance of the electrical and electronics devices due to their electromagnetic radiation and conduction in the atmosphere [1]. Power conversion is one of the important fields in the industries and among various type of conversion used, DC-DC power conversion has wide employment in various applications such as regulated power supplies for computers, laptops, mobile phones, DC motor drives, electronic vehicles, telecommunications equipment and many more. EMI basically resulted from the high rate of change of voltage and current in the converters, has become a major design criterion in almost all DC–DC converters. Due to their fast switching action, DC-DC converters are main source as well as victim of EMI. So EMI is a very serious problem and has to be deal at designing level of DC-DC converter itself. Various international organizations like FCC, IEC and IEEE have made electromagnetic compatibility (EMC) standards and rules to be followed in order to reduce the effect of EMI and to keep the environment clean. Their main aim is to meet EMI regulations while not interfering with the performance of other applications nearby.

There are many methods which have been employed for suppressing EMI such as EMI filters EM shielding and soft switching technique [2]. All these conventional methods work as remedy, since they can suppress the EMI only when it is generated. Among various methods proposed in last few decades for EMI, randomization method proved to be promising method for suppressing EMI effectively at switching itself. Random PWM technique involves spread spectrum technique in which by varying any of the parameters such as pulse position or switching frequency can cause

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suppression of spectral peaks (EMI noise) that get accumulated at multiple of switching frequency and spread it over a wide range of frequency band. Chaotic PWM technique is a type of random methods which are pseudo random in nature and can suppress the EMI noise effectively at switching itself. Chaotic modulation can be implemented in either in analogue or digital way. Among all the methods, chaotic PWM generation through field programmable gate array (FPGA) [3, 4] is the simplest method for implementation. It is a simple and less expensive technique which gives more accurate results.

Luo converter is a newly developed DC to DC converter which works on the principle of voltage lift technique [5]. This converter has simple structure and produce high positive output voltage with reduced ripples. It also possesses many advantage over conventional converters including reduced effect of parasitic elements, improved power density and efficiency. In voltage lift technique, output voltage is lifted up in arithmetic progression. Output voltage is lifted higher by charging and discharging of capacitor by source voltage in the circuit, where it arranged itself to rise up to a level of output voltage and is called as self-lift [6]. Series of Luo converters [7] are there which can also perform re-lift, super-lift and multiple-lift operation for higher voltage application by repeating the operation of voltage lift technique [8,9] in the circuit.

In this paper, FPGA based chaotic PWM technique is used for suppressing the conducted EMI generated in the DC-DC Luo converter. The paper is organized in following way. In section II, topology of Luo converter and its mode of operation are discussed in detail. Section III discusses about the chaotic modulation technique and chaotic PWM generation through FPGA. Section IV discusses about the simulation results and its hardware implementation by above discussed method in Luo converter.

## 2. Luo Converter

### *A. Circuit description*

Luo converter can step up and step down the DC supply voltage depending on the duty ratio. It consists of a single switch S which can be driven by pulses having switching frequency *f*. The circuit consists of two parts- one is the pump circuit S-$L_1$-D-$C_1$ where voltage lifting action take place and other part is $L_2$-$C_2$ for filter action of output voltage. The circuit diagram of Luo converter is given below in the Figure 1.

### *B. Modes of operation*

There are two modes of operation in Luo converter. During mode I switch is in *on* condition and in mode II, switch is in *off* condition.

**Mode I:**When switch S in on, diode D will be in *off* condition. Supply voltage $V_{in}$ charges the inductor $L_1$ and inductor current $I_{L1}$ start increasing. At the same instance, inductor $L_2$ also starts absorbing energy from source voltage $V_{in}$ and capacitor $C_1$ and hence inductor current $I_{L2}$ also start increasing. Thus average input current $I_{in}$ become the sum of the two increasing inductor currents $I_{L1}$ and $I_{L2}$.

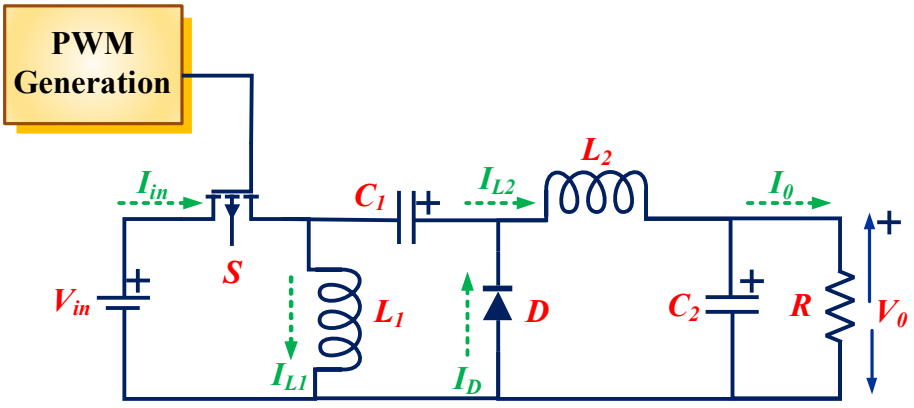


Figure 1. Luo converter circuit

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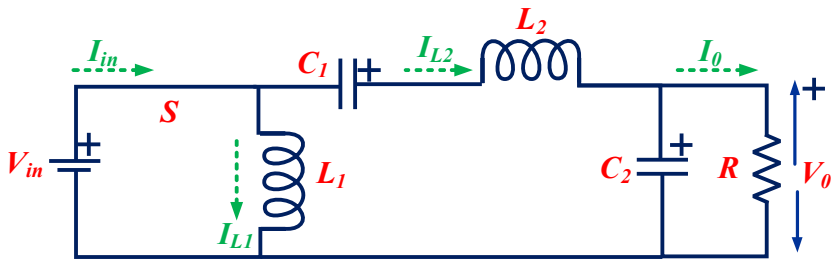


Figure 2. Mode I- switch *on* condition

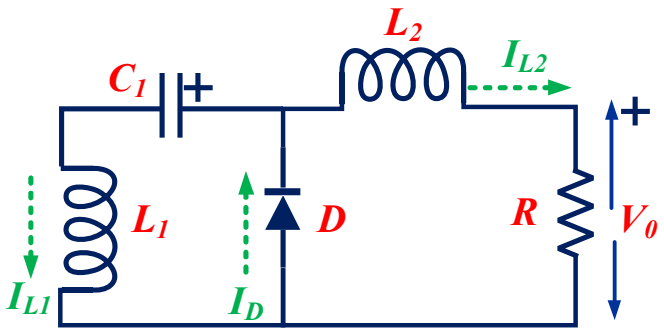


Figure 3. Mode II- switch *off* condition

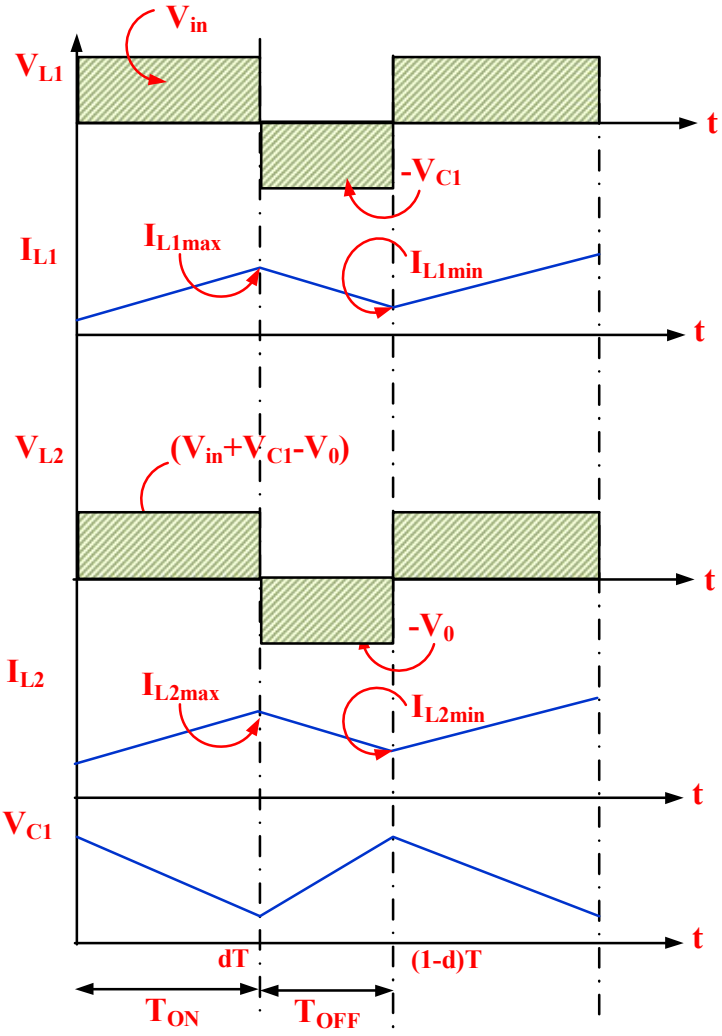


Figure 4. Switching waveforms of Luo converter

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**Mode II:** When switch S gets *off*, diode D turns *on* and performs the freewheeling action. Since circuit get disconnected from source side, source current $I_{in}$ becomes zero. Because of this, inductor current $I_{L1}$ start reducing and flow through the freewheeling diode to charge the capacitor $C_1$. At the same instance, inductor current $I_{L2}$ start reducing through the circuit $C_2$-R for making itself continuous in the circuit. The equivalent circuit diagram of Luo converter for switch *on* and switch *off* conditions [10] are shown in the Figure 2 and Figure 3 respectively.

The charge on capacitor $C_1$ decreases and the current flowing through it is $I_{L2}$ .Charge during *on* time can be equated as:

$$Q^{-} = dTI_{L2} \tag{1}$$

The charge on Capacitor $C_1$start increasing and the current flowing through it is $I_{L1}$.Charge during OFF time can be equated as:

$$Q^{+} = (1-d)TI_{L1} \tag{2}$$

Where d is the duty ratio and T $\left(T = 1/f\right)$is the total time period.

For periodic operation, $Q^{-} = Q+$

Thus, $$I_{L2} = \frac{(1-d)}{d} I_{L1} \tag{3}$$

Capacitor $C_2$act as low pass filter at load side, so the output current $I_o$ is nearly equal to Inductor current$I_{L2}$.

$$I_O = I_{L2} \tag{4}$$

Also, the value of source current is sum of two inductor currents during switch *off* time and zero during switch *off*. So the average source current can be calculated as

$$I_{in} = d(I_{L1} + I_{L2}) = d(1 + \frac{1-d}{d}) I_{L1}$$

$$I_{in} = I_{L1} \tag{5}$$

Hence, the output current obtain from (3), (4) and (5) is

$$I_O = \frac{1-d}{d} I_{in} \tag{6}$$

The average power supplied by the source side must be equal to the average power absorbed by the load:

$$P_S = P_O;\ V_{in} I_{in} = V_O I_O;\ \frac{I_{in}}{I_O} = \frac{V_O}{V_{in}}$$

Hence, the output voltage is

$$V_O = \frac{d}{1-d} V_{in} \tag{7}$$

We can see from the Figure 4, during switch *on* time, inductor $L_1$ is charged through supply voltage, $V_{L1} = V_{in}$ and during switch *off* condition, it is reversed biased by capacitor voltage,

$$V_{L1} = -V_{C1}$$

$$dTV_{in} = (1-d)TV_{C1}$$

$$V_{C1} = \frac{d}{1-d} V_{in}$$

Hence, capacitor voltage at $C_1$ is

$$V_{C1} = V_O = \frac{d}{1-d}\ V_{in} \tag{8}$$

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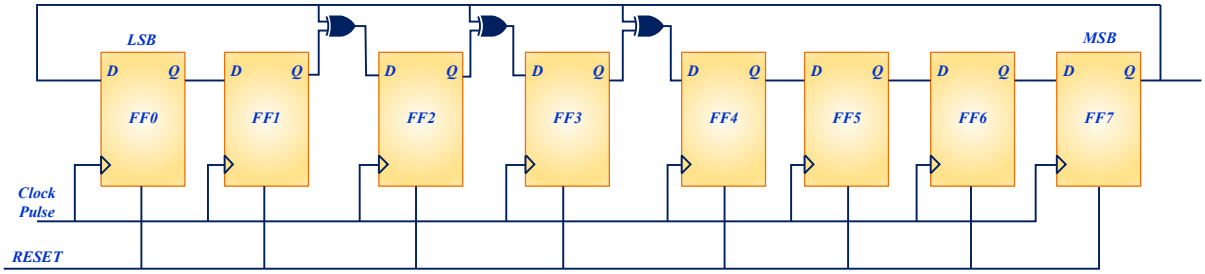


Figure 5. 8-bit linear feedback shift register

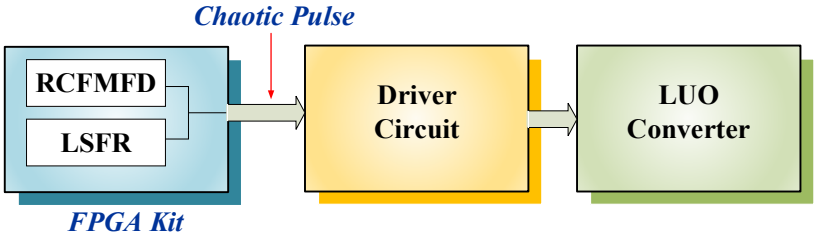


Figure 6. Block diagram of CPWM generation

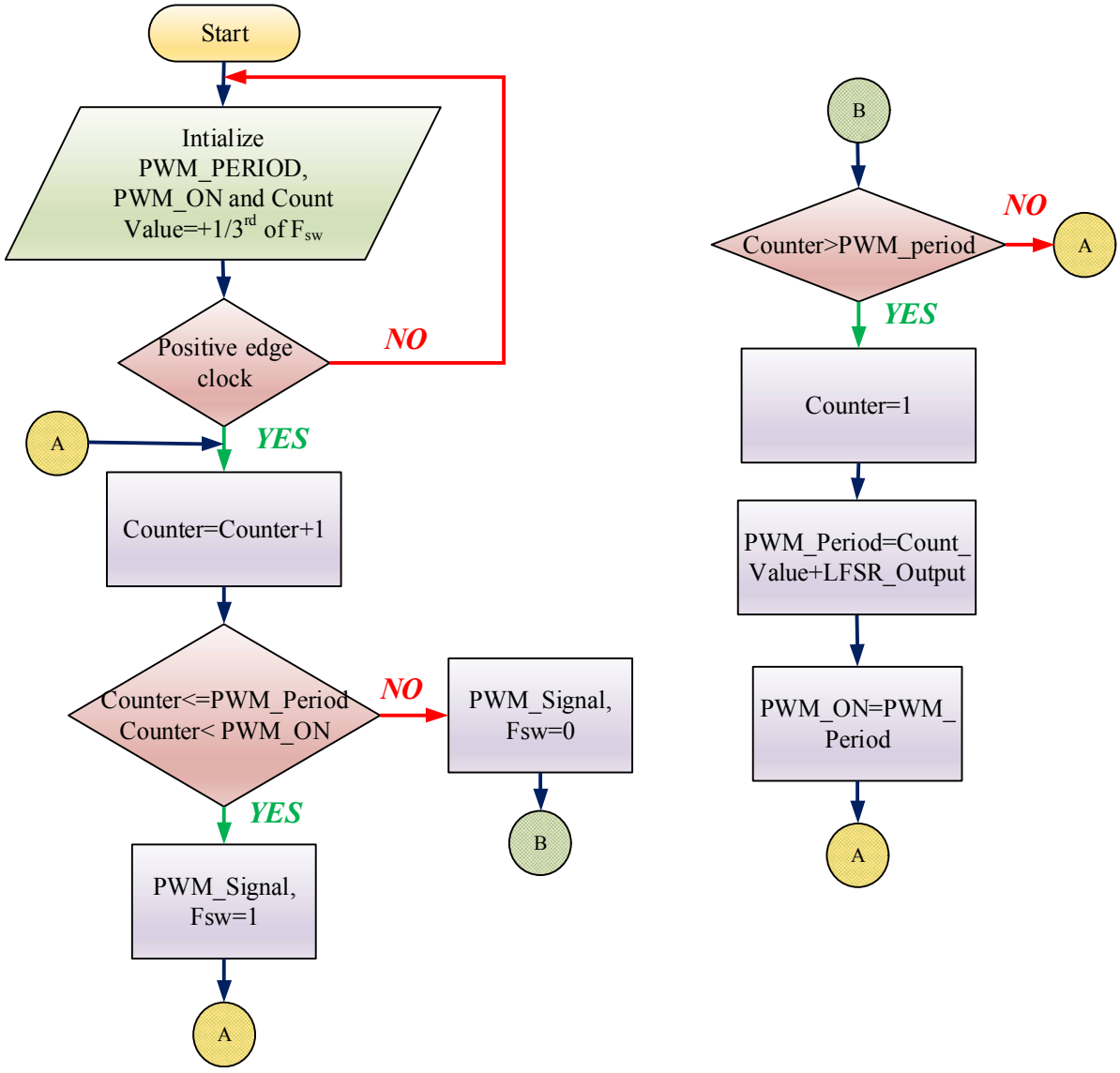


Figure 7. Flowchart depicting the generation of CPWM through RCFMFD based random technique

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## 2. Chaotic Pulse Width Modulation (CPWM)

Chaotic PWM technique is the newly proposed random method which has the feature of both spread spectrum and pseudo randomness[12]. Here PWM frequency varies chaotically and hence energy is distributed evenly to entire frequency spectrum. It involves pseudo-random modulationwhich appears to be random but is deterministic in nature. It generates random outputs which are produce ina sequence and can be repeated in a cycle.

### *A. Randomized carrier freuqency modulation with fixed duty ratio (RCFMFD)*

Chaotic PWM pulses can be generated by applying different schemes in which parameters such as position, width or carrier frequency are varied. Among different schemes, randomized carrier frequency with fixed duty cycle (RCFMFD) is most famous scheme in which carrier frequency is varied by keeping the duty cycle constant. By randomizing the carrier frequency, central switching also gets randomized and by keeping the duty cycle constant, output voltage will not vary and gives a constant DC output. This scheme proved [13] to give low frequency harmonics spectrum on PSD and therefore chosen to be best option for switching scheme in DC-DC converters. While applying RCFMFD scheme, only consideration should be taken care is on the range of randomization of switching frequency. If carrier frequency is randomized more than a certain limit, it loses its property of EMI noise reduction and start overlapping with the successive frequency in the spectrum. This can be avoided by putting randomization range of switching frequency within the limit of ± one-third of central switching frequency. Chaotic PWM pulses can be generated by applying RCFMFD random scheme [13,14,15] along with pseudo number generator. Generation of random numbers can be done with the help of linear feedback shift register. It is discussed in detail in next section.

### *B. Linear feedback shift register*

Random switching pulses can be generated with the help of linear feedback shift register (LFSR) which works on the principle of pseudo-random number generation. LFSR is a group of shift registers which use linear functions as a feedback mechanism to modify itself on each rising edge of the clock [14,15] which is shown in Figure 5. Here logic gates like XOR and XNOR gates are used as linear function to feedback the output bit to input bit. The input given at initial stage is called as 'seed'. The bit positions, where next state is affected by linear functions are called as 'taps'. The right most bit is the output bit. LFSR can produce maximum $2^n$-1 random numbers (except all 0), where n is the number of registers used. Since sequence generated is deterministic and finite, it can repeat the same stream of values from the initial stage until LFSR is clocked. It output is in the form of 1's and 0's.

### *C. Process of generating CPWM*

Chaotic PWM pulses can be generated from LFSR by applying RCFMFD scheme on it. This whole process can be incorporated with FPGA. Block diagram depicting chaotic pulse generation is given in Figure 6.

Steps followed during the RCFMFD based chaotic PWM pulses generation [15] through FPGA for triggering the switch of Luo converter are given below:

1. At every positive edge of clock pulse, seed values (except all 0) given to LFSR.
2. With the help of XOR gates at particular tap, output bit is feedback to input and at the same time generates $2^n$-1 random values.
3. Random values generated in LFSR is fed to variable frequency generator which works on the basis of RCFMFD scheme.
4. In variable frequency generator, parameters such as PWM_PERIOD and PWM_ON are initialize and count value is set to maximum limit which is equal to ±1/3$^{rd}$ of central switching frequency.
5. At every positive edge of clock pulse, calculate the PWM_ON for the PWM signal based on the required duty ratio and PWM period value.

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6. On every positive edge of clock, increment the counter with 1 till it reaches to ON time. When counter reaches to PWM_ON value, then PWM pulse i.e. logic Fsw is becomes 1.
7. When counter exceeds the PWM_ON value, the logic Fsw becomes 0 and counter again start incrementing till it reaches PWM_PERIOD.
8. If counter exceeds the PWM_PERIOD value, then count value is reinitialize to 1.
9. Next PWM_PERIOD value is obtain by adding a constant count value which corresponds to maximum switching frequency with the output of LFSR.
10. Go to step 6, repeat all the steps for next cycle.

The steps followed for RCFMFD based random pulse generation is also be explained with the help of flowchart which is mention in Figure 7.

## 3. Prototype Hardware Implementation and Results

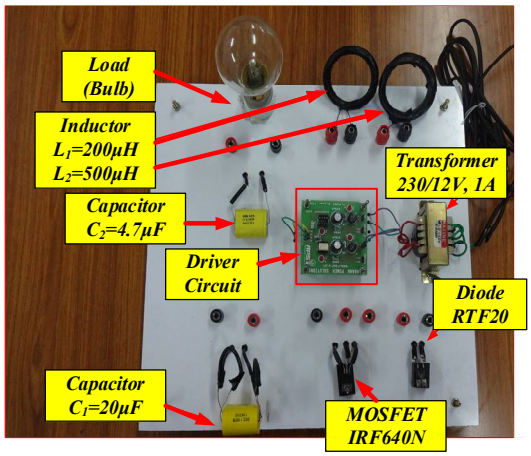


Figure 8. A hardware prototype of Luo converter

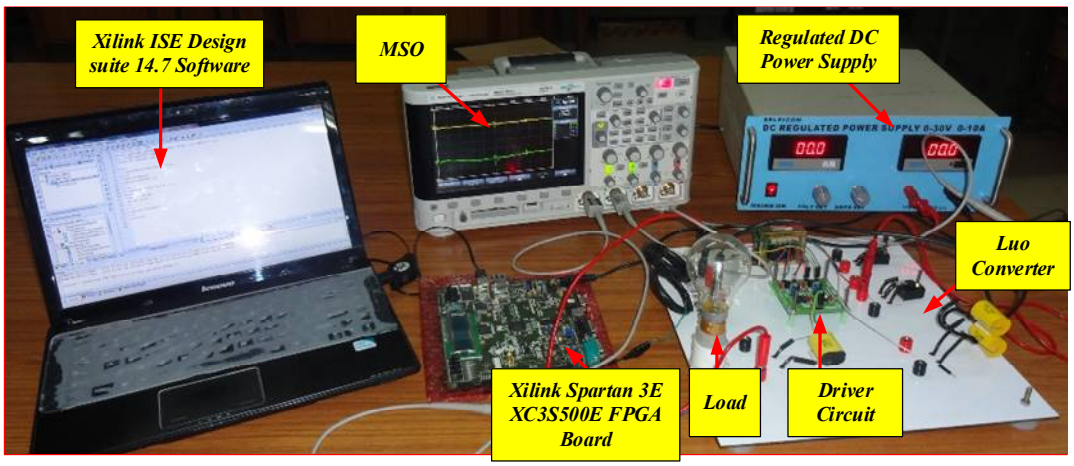


Figure 9. Complete hardware setup

Table 1. Prototype Experimental Specification

| Specifications | Values |
|---|---|
| Input voltage, $V_{in}$ | 12 V |
| Output voltage, $V_o$ | 24 V |
| Power rating, P | 40 Watts |
| Switching frequency, f | 200 KHz |
| Load (resistive) | 14.8 ohms |
| Inductor, $L_1$ | 200 µH |

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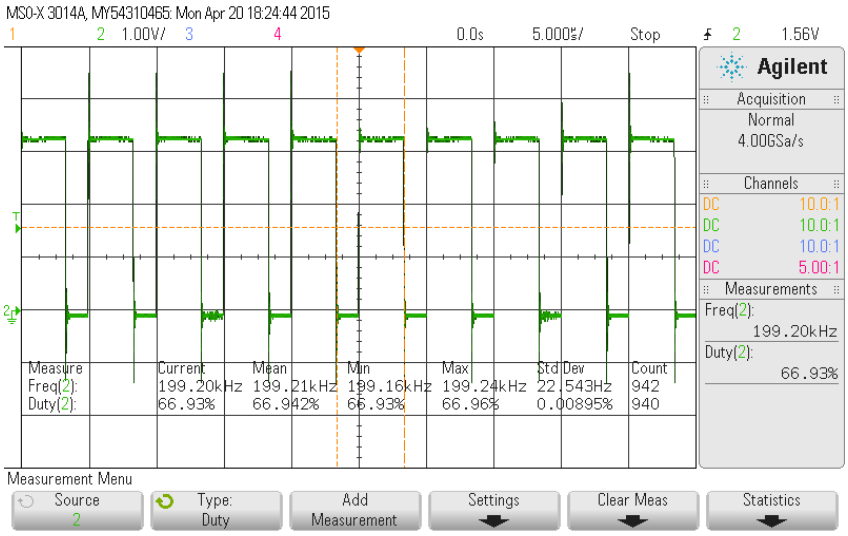
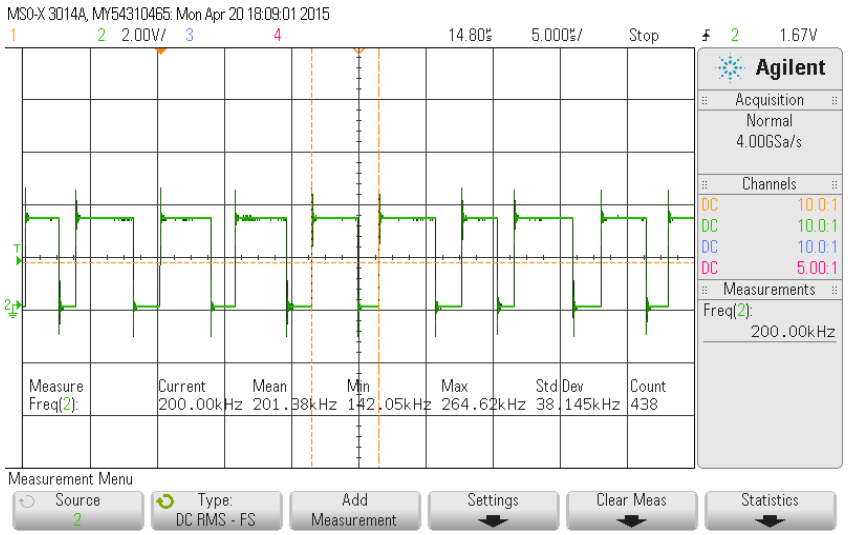
| | |
|---|---|
| Inductor, $L_2$ | 500μH |
| Capacitor, $C_1$ | 20μF |
| Capacitor, $C_2$ | 4.7μF |

In order to verify the RCFMFD scheme based chaotic PWM technique for conducted EMI suppression [16,17,18], a hardware prototype of Luo converter is designed and developed with the given specification in Table 1. Prototype of Luo converter is shown in Figure8 and complete hardware setup is shown in Figure 9.




(a)




(b)

Figure 10. Pulses for boost operation with 0.67 duty cycle and switching frequency of 200 kHz (a) Periodic PWM pulses (b) Chaotic PWM pulse in the range of ± 1/3rd of 200 KHz

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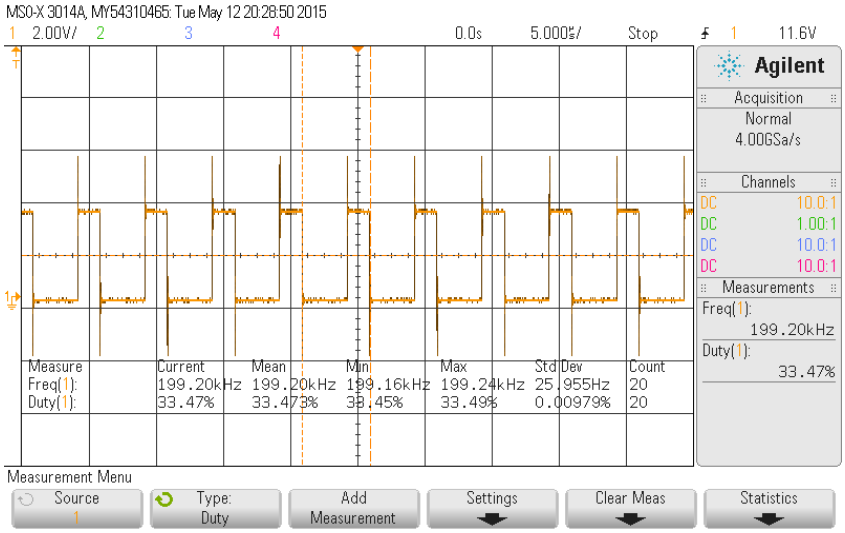
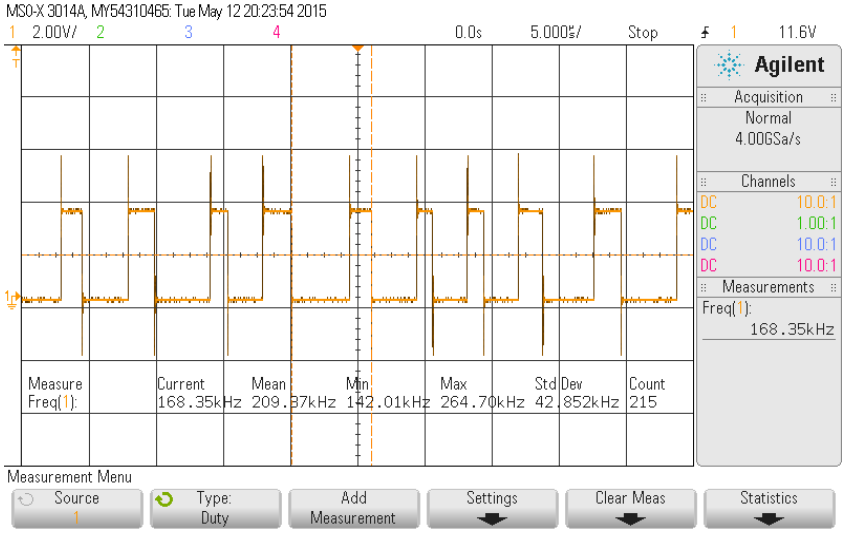
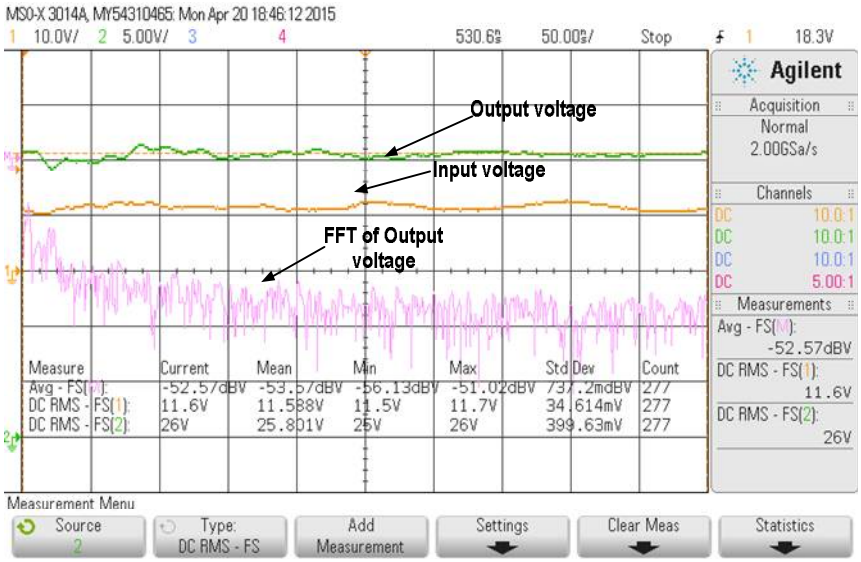



(a)




(b)

Figure 11. Pulses for buck operation with 0.33 duty cycle and switching frequency (a) Periodic pulse (b) Chaotic pulse in the range of ± 1/3rd of 200 KHz




(a)

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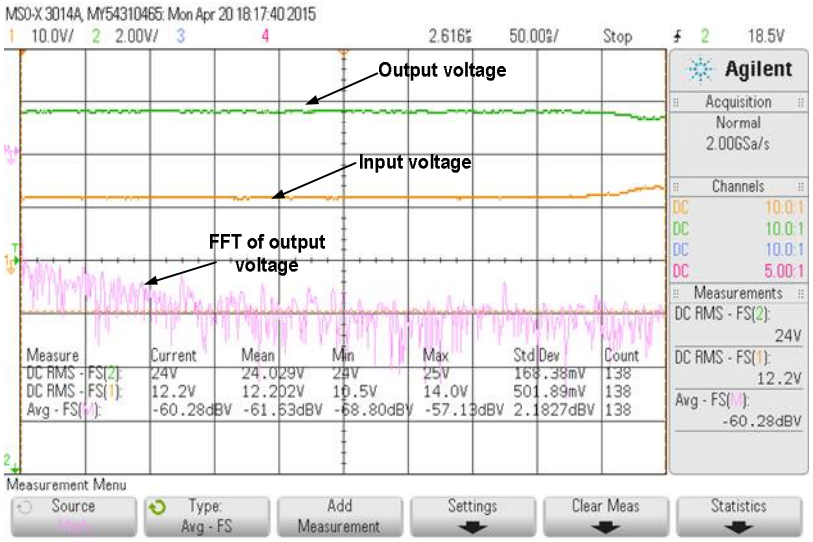
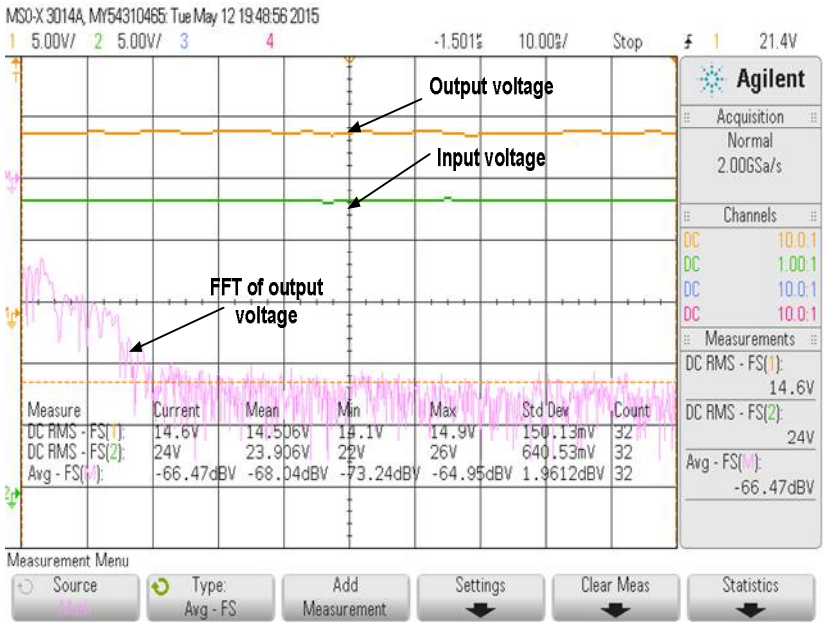



(b)

Figure 12. FFT of output voltage for duty cycle of 0.67(a) periodic pulses (b) chaotic pulses




(a)

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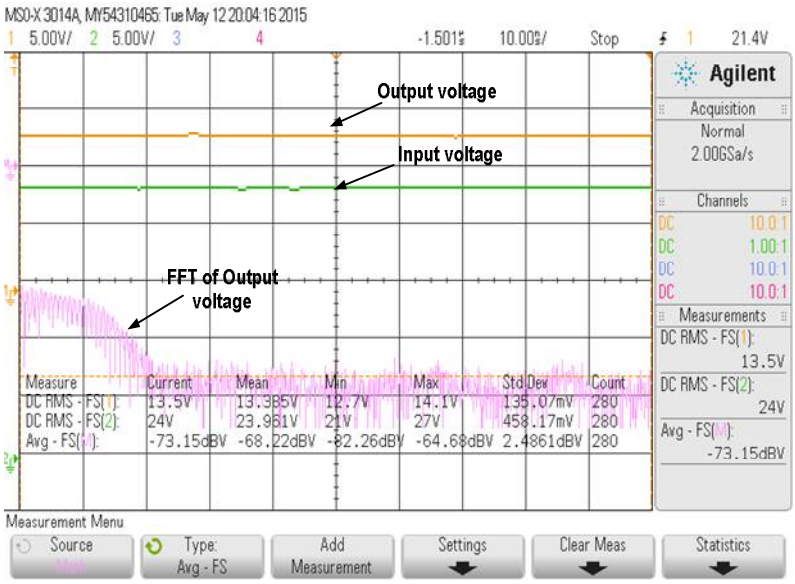


(b)

Figure 13. FFT of output voltage for duty cycle of 0.33 for (a) Periodic pulses (b) Chaotic pulses

For generation of periodic and chaotic PWM pulses [19], programming is done in Xilinx ISE design suite 14.7 software and is interfaced with Xilinx Spartan 3E XC3S500E FPGA board. The oscillator frequency of this FPGA board is 50MHz and can be down scale for desired frequency. The pulses generated from with Xilinx Spartan 3E XC3S500E FPGA [20] is fed to the driver circuit which boost up the voltage of FPGA (3.3 V) to trigger the switch of Luo converter.

Both periodic and chaotic pulses generated from FPGA board for boost and buck operating modes of Luo converter are shown in Figure 10(a), Figure 10(b), Figure 11(a) and Figure 11(b) respectively. For boost operating mode, design specification is $V_{in}$=12V, $V_o$=24V with duty cycle of 0.67 and switching frequency of 200 kHz whereas for buck operating mode $V_{in}$= 24V, $V_o$=12V with duty cycle of 0.33 and switching frequency of 200 kHz.

After getting pulses through the FPGA board, FFT analysis is done on the output voltage obtained from the Luo converter. Output voltage along with FFT obtained is shown in Figure 12 (a), 12(b), 13 (a) and 13(b) for duty cycle of 0.67 and 0.33 respectively. In Fig 12 (a) with periodic pulses, average of peak noise obtain is at – 52 dBV which is equal to 2.5mV, whereas In Fig 12 (b) with chaotic pulses, it occurs at -60 dBV which is equal to 1mV. It can be seen that there is reduction of approximately 8dBV which is equal to 1.5mV of conducted noise in chaotic mode as compared to periodic mode. In Figure13 (a) of Luo converter with periodic pulses, average peak noise obtains is at -66.47 dBV which is equal to 0.47mV whereas in Figure13 (b)with chaotic pulses, it occurs at -73.15 dBV which is equal to 0.22 mV. It can be seen that there is reduction of approximately 7dBV which is equal to 0.25mV of conducted noise in chaotic mode as compared to periodic mode.

## 4. Conclusion

A FPGA based chaotic PWM technique using RCFMFD random scheme along with conventional periodic PWM pulses were investigated on hardware prototype of DC-DC Luo converter for conducted EMI suppression. By using FFT analysis, conducted EMI noise is analyzed in buck and boost operating mode of Luo converter for both periodic and chaotic PWM modulation. Hardware implementation shows that in boost operating mode, the conducted noise reduced by 8dBV in chaotic switching as compared to periodic switching whereas in buck operating mode, reduction is 7dBV. It implies that spectral peaks present at the multiple of switching frequency get suppressed significantly in chaotic mode as compared to periodic mode. Thus, chaotic modulation technique alone is more effective as compared to periodic PWM and other conventional methods in suppressing the conducted EMI noise.

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