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Surface Modification of Electroosmotic Silicon Microchannel using Thermal Dry Oxidation

Tuan Norjihan Tuan Yaakub[1,2], Jumril Yunas[1,*], Rhonira Latif[1], Azrul Azlan Hamzah[1], Mohd Farhanulhakim Razip Wee[1] and Burhanuddin Yeop Majlis[1]

[1] Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM), 43600 UKM Bangi, Selangor, Malaysia ; jumrilyunas@ukm.edu.my; rhonira@ukm.edu.my, azlanhamzah@ukm.edu.my; m.farhanulhakim@ukm.edu.my; burhan@ukm.edu.my

[2] Dept. of Electronics Engineering, Faculty of Engineering, Universiti Teknologi MARA, Selangor, Malaysia; tuan_norjihan@siswa.ukm.edu.my

* Correspondence: jumrilyunas@ukm.edu.my; Tel.: +60-3-8911-8541

Abstract: A simple fabrication method in the surface modification of electroosmotic silicon microchannel using thermal dry oxidation is presented. The surface modification is done by coating the silicon surface with a silicon dioxide (SiO_2) layer using thermal oxidation process. The process is aimed not only to improve the surface quality of the channel to be suitable for electroosmotic fluid transport but also to reduce the channel width using a simple technique. Initially, the parallel microchannel array with dimensions of 0.5 mm length and width ranging from 1.8 μm to 2 μm are created using plasma etching on the 2x2 cm <100> silicon substrate. The oxidation of silicon channel in a thermal chamber is then conducted to create the SiO_2 layer. The layer properties and the quality of the surface are analyzed using SEM and surface profiler, respectively. The results show that the maximum oxidation growth rate occurs in the first 4 hours of oxidation time and the rate decreases by time as the oxide layer becomes thicker. It is also found that the surface roughness is reduced with the increase of process temperature and oxide thickness. The scallop effect on the vertical wall due to plasma etching process also improved with the presence of the oxide layer. After the oxidation, the channel width is reduced by ~40%. The demonstrated method is suggested for the fabrication of a uniform channel cross section with high aspect ratio in sub-micro and nanometer scale that will be useful for the electroosmotic flow (EOF) manipulation of the biomedical fluid sample.

Keywords: surface modification; electroosmotic flow; microfluidic; silicon nanochannel; thermal oxidation

1. Introduction

The past decade has seen the rapid advancement of microfluidic chip development. The main reason is because of the fluid flow characteristics in micrometer structure that allows for an extremely slow fluid movement, less sample volume consumption and precision in fluid control. In microfluidic systems, electroosmotic flow (EOF) becomes one of the most important parts in which the fluid can be manipulated by the electric potential between inlet and outlet. EOF in a microchannel has been used for numerous microfluidic applications, including for fluids transport and manipulation [1], charge separation [2] and fluids pump [3]. As an example EOF mechanism has been applied to transport fluids as in electroosmotic pump (EOP) [4]. The system was capable to generate a maximum flow rate of 15 μL/min, a significant amount of flow rate per device volume for a microfluidic system. The microchannel width in the fabricated pump is much greater than the height to ease the fabrication process. Such design suffers from clogging due to structure collapsing after bonding process for microsystem integration. Therefore, a microchannel structure for EOF requires a sufficient high

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channel aspect ratio (H/W>>1) to create a uniform electric field distribution along the channel hence induces a stable electroosmotic flow.

Microfluidic channels are typically fabricated in glass, silicon, polymeric substrate. Without doubt, the fabrication procedures of polymeric material like PDMS and PMMA offer a significant low cost and ease fabrication procedures [5,6]. In spite of that, the polymeric based materials has lower wall zeta potential and heat dissipation rate as compared to glass because glass has a superior chemical properties for surface electrostatics reaction. Glass also has an excellent dielectric property that is important for electroosmotic flow [7]. However, the glass fabricating technique is the major drawback due to its low etching rate that must be considered in designing a glass based EOF microfluidic device.

On the other hand, silicon material has been established since many years as the material to be employed for a wide range of microelectronics devices and applications. Silicon microchannel has similar electrical properties as glass substrate and it can be fabricated using the well-established integrated circuit (IC) fabrication technology [8]. A reactive ion etching using SF_6 plasma is widely used to create uniform microchannels with vertical wall for microfluidic device. But the wall quality is poor due to the scallop effect resulting from the repetitive alternating phase of the passivation gas (C_4F_8) deposition and the etching gas (SF_6) on the targeted wall. Some work has been reported in order to reduce the scallop effects by optimizing the DRIE parameter. However, this needed complicated studies, such as additional gas composition [9], an optimum etch and passivation cycle time [10] as well as the controlled flow rates of etching/passivation ratio [11]. Hence, a surface modification is preferable to improve the quality of etched surface.

Since EOF is highly driven by the surface charge properties of the microchannel wall, shrinking the channel cross-section might increase the fluids flow rate and enhance charge molecule separation in the solution [12]. For this reason, thermal oxidation of silicon surface has been used to produce a planar channel dimension down to nanoscale. In addition, the creation of SiO_2 layer enhanced the electrical property of the channel by eliminating the large leakage current encountered in bare silicon. This method is also preferable because it eliminates the complex nanolithography process.

2. Microchannel Electroosmotic System Design

The principle of electroosmotic flow (EOF) is based on the spontaneous reaction of a solid surface in contact with an ionic solution, accumulating the negative charge ions and forming an electrical double layer (EDL) on the capillary wall. EOF is induced when cations in ionic solution move due to body force effect of the EDL on the surface wall with the presence of the electric field. The cations migration will drag the bulk fluid in the capillary towards the negative potential in flat flow profile.

The microfluidic EOF system consists of several surface modified microfluidic channels in parallel array with SiO_2 coating having the length of 500 μm that is fabricated on a 390 μm thick silicon wafer <100>. The channel shape is rectangular with the width of smaller than 1 μm and depth of about 2 μm. A microchannel input (Inlet A - Outlet 1) having channel geometry of 200 μm width and 20 mm length are integrated with the SiO_2 coated silicon microchannel array. On the other end of the surface modified channel, the outlet channel (outlet 20 with similar dimension with the inlet channel is integrated. The inlet port contains buffer and ionic solution that will be transported through the microchannel array towards the outlet reservoir by electroosmotic flow. For that purpose, a voltage potential V is applied across the microchannel array to create an electric field as shown in Fig. 1.

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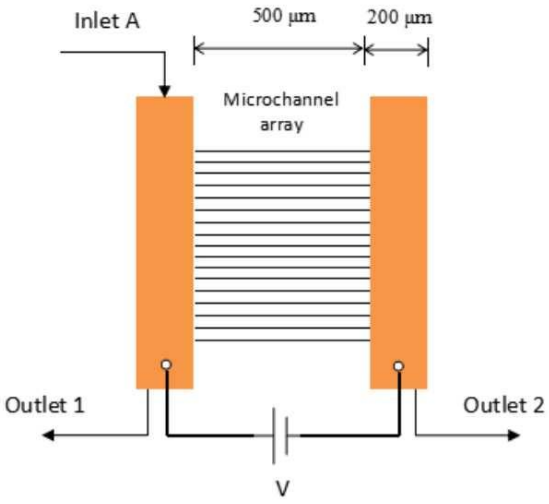

Fig. 1 The microchannel electroosmotic system

In this work, the SiO_2 coated silicon microchannel reduces not only the channel cross-section dimension but also improves the surface quality. To create micron size rectangular microchannels, we utilized standard photolithography and the reactive ion etching technique. The thermal oxidation is performed under atmospheric pressure with a constant O_2 stream flow of 2000 ml/min at various process temperature. Through the conducted procedures, a uniform oxide growth on both vertical and horizontal surface and a uniform size and shape of SiO_2 rectangular channels in parallel array are produced.

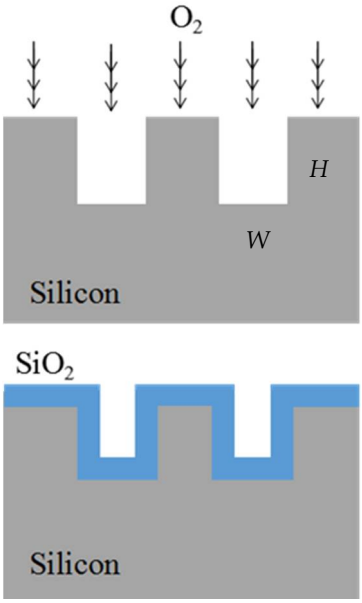

Fig. 2 Mechanism of dry oxidation on silicon microchannel

As shown in Fig. 2, the oxidation process should produce an approximately uniform oxide growth rate at both horizontal and vertical silicon walls. Hence, accurately control on depth to width ratio (H/W) of the microchannels can be achieved after the oxidation process. The final dimension width of the electroosmotic channel is in the range below 1 μm with a higher aspect ratio.

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3. Fabrication Process of EOF Channel System

3.1. Fabrication of Silicon Microchannel Using Plasma Etching Procedure

Initially, a set of electroosmotic microchannel arrays was fabricated using the standard photolithography and deep reactive ion etching (DRIE) on the silicon wafer. The parallel microchannels were designed to have a length of 0.5 mm and variation of width from 1.8 μm to 2 μm. The microchannel was in a straight line form and the distance between each channel was set to 5 μm.

The microchannel design was transferred onto a cleaned silicon surface by exposing the substrate coated with a positive photoresist under UV-light exposure. To pattern a vertical microchannel on the silicon substrate, we employed the high-density reactive ion SF_6 etching, with passivation gas C_4H_8 and O_2 at cryogenic temperature with an approximate etch rate of 1 μm per minute. After DRIE process, the mask resist was removed and the geometries of the microchannels array were observed using scanning electron microscope (SEM).

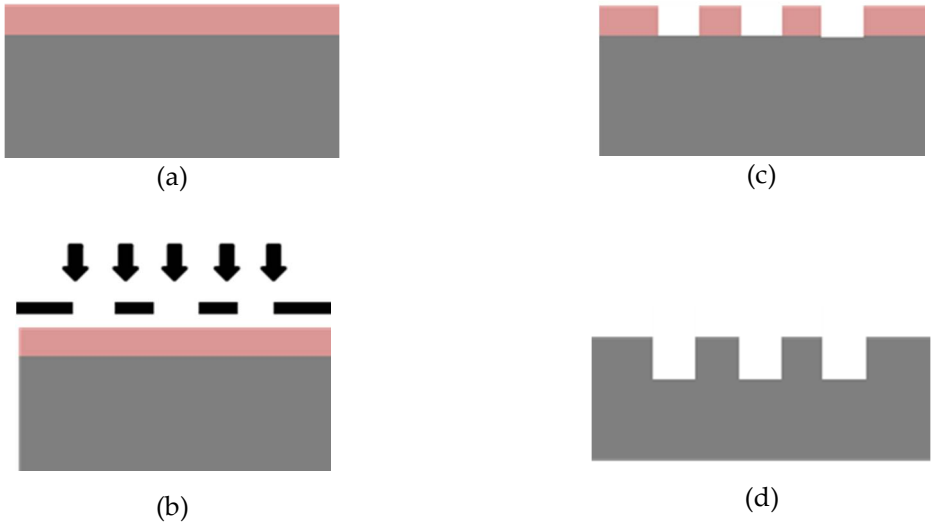

Fig. 3 The diagram of silicon microchannel fabrication process (a) Photoresist as etching mask coating, (b) Transfer pattern using photolithography, (c) Pattern development using resist developer, (d) Si DRIE along the unprotected microchannel lines & photoresist removal

3.2. Surface Modification of Fabricated Silicon Microchannel Using Thermal Oxidation

The surface modification of the prefabricated silicon microchannel was done using oxidation process in high thermal ambient. Basically, the oxide was grown on the heated silicon surface at very high temperature between 800 ~ 1200 ˚C with the presence of oxygen gas flow or water vapor, referring to dry and wet oxidation respectively. In this work, we created the SiO_2 microchannel based on oxidation of silicon in dry flowing oxygen at atmospheric pressure in three different process temperatures, 990 ˚C, 1020 ˚C and 1040 ˚C. The formation of silicon dioxide layer on silicon channels was described by the chemical reaction below,

$$Si + O_2 = SiO_2 \quad (1)$$

In dry thermal oxidation, O_2 molecules diffuse through the surface oxide layer and reacts with the silicon atom at the Si-SiO_2 interface. The resulting SiO_2 surface layer is not coplanar with the original silicon surface. Which means, a $0.44d$ of silicon is consumed for a thickness of d oxide layer growth in thermal dry oxidation process.

Before starting the oxidation procedure, the etched sample was cleaned in acetone and methanol ultrasonic bath for five minutes each followed by rinsing the substrate in DI water for 1 minute. The sample was then soaked in 10% HF solution for 60 s to eliminate undesired native oxide layer before it was rinsed again in DI water and dried with nitrogen.

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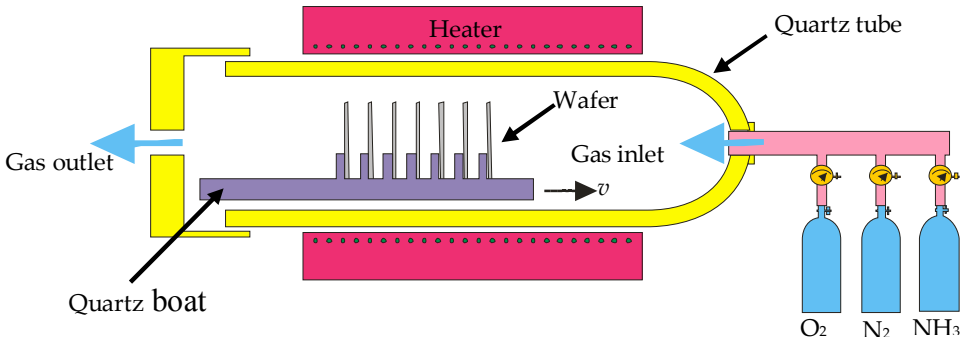

Fig. 4 Schematic diagram of oxidation furnace

Then, the samples were placed in the ceramic boat and put them at the mouth of the oxidation glass tube furnace that previously has been filled up with nitrogen (N_2) gas at 2000 ml/minute stream rate. The resistance heater on the tube furnace was then heated up according to the targeted process temperature. After the furnace temperature reached the required temperature, the sample boat was pushed to the heated zone which is at the center of the furnace tube. The oxidation process began after we stopped the supplied N_2 gas and started to flow in the dried oxygen gas into the tube furnace under a constant flow rate of 2000 ml/minute. The oxidation process was maintained under a constant oxygen flow rate at atmospheric pressure for 4 to 12 hours. Fig. 4 shows the oxidation furnace apparatus for thermal dry oxidation. A uniform color scheme with no surface abnormality appeared on the oxidized sample's surface at all experiment condition. The morphology of SiO_2 growth surface on the sample was scanned using F50 Thin Film Metrics at 20 different points while the cross-section of the SiO_2 microchannel was verified using the scanning electron microscope.

4. Results and Discussion

4.1 SiO_2 layer thickness and oxidation growth rate

The average thickness of oxide layer on the silicon microchannel was highly controlled by the process temperature and oxidation time. A plot of average oxide thickness against time at various process temperature are shown in Fig 5. In the time range of 4 to 12 hours for all oxidation temperatures, the oxidation layer thickness was found to increase linearly with the oxidation time. In addition, the higher the process temperature, the thicker the oxide layer will be grown. This relationship of temperature and time for the oxide thickness was well agreed with the finding reported in [13]. From the plot, we perceived the maximum thickness of 520 nm oxide grown at 1040 ˚C for 12 hours of oxidation time.

The oxide thickness was measured at every after 4, 6, 8, 10 and 12 hours of oxidation process. The highest growth rate was observed for the first 4 hours oxidation time for all process temperatures. The growth rate at all conducted process temperatures is presented in Fig. 6. It is shown that for the first 4 hours of oxidation, the maximum growth rate was up to 72 nm/hr at 1040 ˚C. As the oxidation time increased, we observed a consistent decrease of growth rate. The same trend was observed for other process temperature of 1020 ˚C and 990 ˚C. The decreasing growth rate by time can be explained by the slower reaction between the O_2 molecules with the Si atom on the substrate since the oxide thickness was getting thicker. We also found that the maximum oxide growth rate was 33% higher with the increasing of 50 ˚C in process temperature for 12 hours oxidation time. This finding proved the strong relation of temperature to the oxide growth rate as the oxidant diffusivity increased with the increasing temperature [14].

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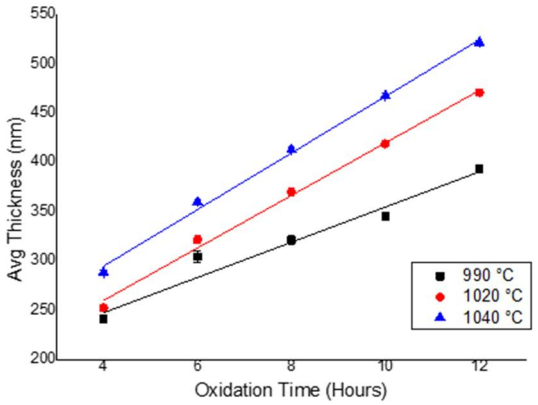

Fig. 5 Oxide thickness against oxidation time of thermal dry oxidation for silicon <100>

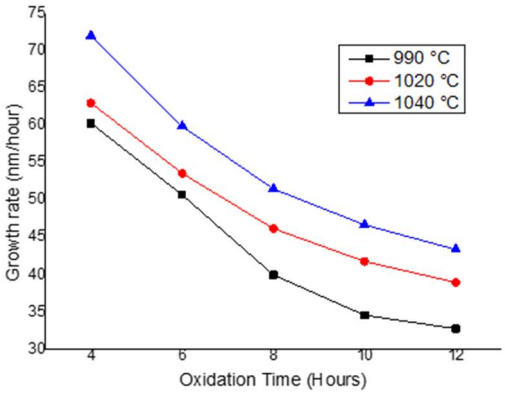

Fig. 6 Oxide growth rate of thermal dry oxidation for silicon <100>.

4.2 Surface Uniformity

The thickness of the oxide layer on the sample surface at all oxidation time was found to be uniform across 2x2 cm² samples. The thickness measurements were characterized using F50 Filmetrics at 20 random and scatter points across the samples. The measurement principle was based on the ellipsometry technique where it computes the oxide thin film thickness with Armstrong resolution.

As presented in Fig. 7, the surface roughness was evaluated based on the oxide thickness variations at every growth temperature. In general, the oxide thickness measurement showed that the oxide layer was grown with the lowest roughness as the oxidation temperature increased that is about 2.03 nm at 1040 ˚C. The oxide surface roughness also improved when we prolong the oxidation time to 12 hours. Longer oxidation time allows for a thicker oxide layer growth with better surface roughness quality of the microchannel.

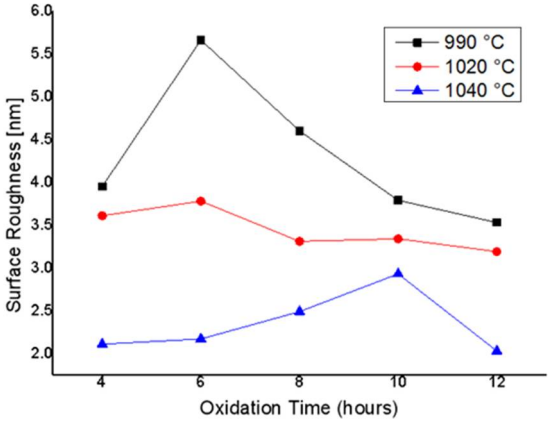

Fig. 7 Surface roughness of oxide layer for various process temperature

Figure 8 shows the SEM observations on the EOF channel before and after oxidation process. The scallop effect becomes a major challenge of high aspect ratio microchannel fabrication using DRIE [15]. The scallop roughness as shown in Fig. 8(a) was not desirable especially for an electroosmotic microfluidic system because it can create unnecessary flow characteristic and induce unwanted pressure inside the microchannel. On top of that, the surface roughness can change the EDL properties near the surface wall, hence reduce the electroosmotic flow inside the microchannel [16, 17]. Figure 8(b) shows the effect of oxidation on the side wall smoothness. . It can be seen that the scallop roughness on the vertical wall of microchannel resulted from the plasma etching process was improved by oxide layer growth on the silicon vertical wall after 12 hours oxidation.

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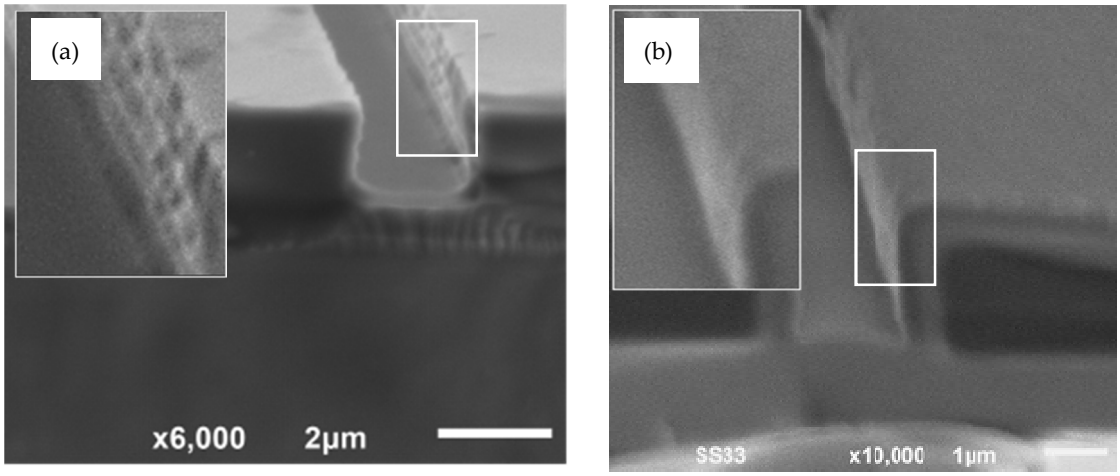

Fig. 8 Scallop effect on ther silicon vertical wall (a) before and (b) after oxidation

4.3 Microchannel Structure Improvement after Thermal Oxidation

A high aspect ratio SiO_2 microchannel was successfully created by using dry thermal oxidation that is suitable for an electroosmotic flow application. The shape and cross section of the microchannel was uniform, as demonstrated by Fig. 9(a) and (b). The width of the microchannel was reduced to 42% with the oxide layer of 520 nm on the channel wall. The color scheme on the top surface of the substrate was seen consistent without any abnormal spot.

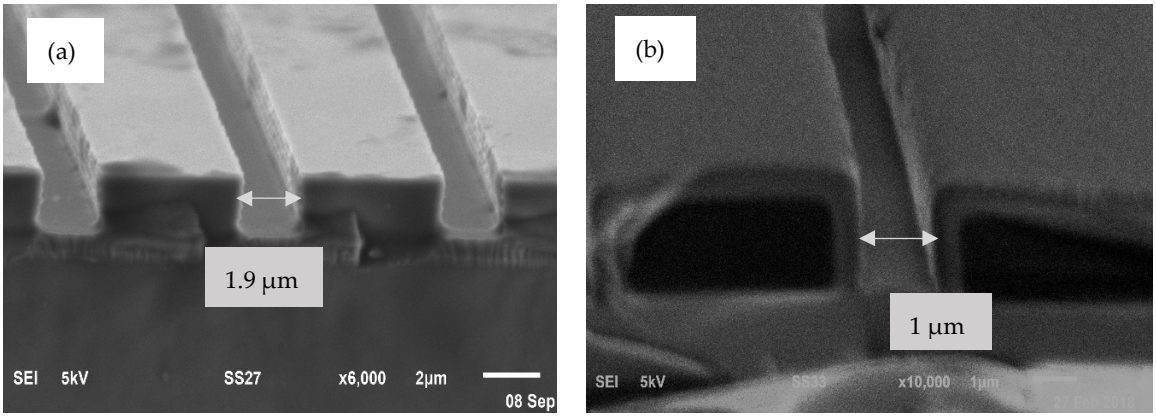

Fig. 9 (a) Silicon microchannel before oxidation process (b) SiO2 microchannel after 12 hours thermal dry oxidation at 1040 ˚C

5. Conclusions

In conclusion, we presented a simple technique to fabricate a silicon electroosmotic channel with surface modification. The microchannels array were initially realized by reactive ion etching coupled with post processed thermal dry oxidation to produce a high aspect ratio microchannels with improved cross section and surface morphology. The strong relation of oxide thickness with the temperature was presented by performing the thermal dry oxidation at 990 ˚C, 1020 ˚C and 1040 ˚C. Oxide growth rate was found to increase at higher process temperature. By using this method, the microchannel width was reduced by ~40 % with the minimum aspect ratio (H/W) of 2. The surface quality was also improved as the scallop effect from the plasma etching process was reduced by adding an adequate amount of oxide layer. A uniform cross section with a good quality of surface roughness were essential to demonstrate a steady electroosmotic flow inside the microchannel. The final structure of SiO_2 microchannels array will be integrated with PDMS structure to work as a complete electroosmotic microfluidic device. This process was foreseen to be able to produce a high aspect ratio sub-microchannel and nanochannels without implementing the nanolithography procedure.

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Author Contributions: J.Y., T.N.T.Y. and B.Y.M. conceived and designed the experiments; J.Y., and T.N.T.Y. performed the experiments and analyzed the data; A.A.H. M.F.R.W. contributed reagents/materials, T.N.T.Y., J.Y. and R.L. wrote the paper.

Conflicts of Interest: "The authors declare no conflict of interest."

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