

Article

Impact of DC Voltage Enhancement on Partial Discharges in Medium Voltage Cables - An Empirical Study with Defects at Semicon-Dielectric Interface

Aditya Shekhar^{1,2,*†}, Xianyong Feng^{1†}, Angelo Gattozzi¹, Robert Hebner¹, Douglas R. Wardell¹, Shannon Strank¹, Armando Rodrigo-Mor², Laura M. Ramirez-Elizondo² and Pavol Bauer²

¹ Center for Electromechanics, The University of Texas at Austin, 10100 Burnet Rd CEM Bldg. 133 Austin, TX 78758, USA; r.hebner@cem.utexas.edu

² Electrical Sustainable Energy, Delft University of Technology, Mekelweg 4, Delft 2628 CD, The Netherlands; p.bauer@tudelft.nl (P.B.)

* Correspondence: a.shekhar@tudelft.nl; Tel.: +31-(0)15-2785744; Fax: +31-(0)15-2781182

† These authors contributed equally to this work.

Abstract: A scientific consensus is emerging on the benefits of dc distribution in medium voltage power systems of ships and cities. At least 50 % space savings and increased power transfer capacity are estimated with enhanced voltage dc operation of electric cables. The goal of this research is to contribute to developing the empirical knowledge on the insulation performance in order to validate the feasibility of such anticipated gains of dc versus ac, and to determine the comparative impact of different operational conditions from a component engineering point of view. The partial discharge (PD) activity in cables is measured under ac and dc conditions as an indicator of insulation performance. Specifically, PDs in defects at the semicon-insulation interface are studied in terms of inception voltage, repetition rate and discharge magnitude. Empirical understanding is drawn for operating voltage and frequency dependence of the discharge behavior in such voids in the range of 10 to 20 kV and 0 to 0.1 Hz, respectively. The change in PD activity with void evolution is explored.

Keywords: ac, comparison, dc, discharges, measurements, medium voltage, pd, partial discharges.

1. Introduction

In shipboard power systems, space limitations make dc a favorable option as it can lead to reduction in cable size for the same power level [1,2]. This downsizing is envisioned not just in the cable's conductor size, but also in the insulation requirements. For land-based distribution grids, refurbished operation of underground ac cables under dc can deliver power more efficiently and at higher transfer capacity for the same thermal constraints, while avoiding extra investment in digging and infrastructure installation [3]. Further, in urban areas, need for compact power redirection with emerging energy intensive distributed resources is driving the necessity of medium voltage dc distribution.

For these applications, an underlying assumption is that as compared to ac, a higher dc voltage can be imposed on the insulation [4–6]. Applying this principle, it was shown in [7] that even with a conservative dc voltage enhancement factor of $\sqrt{2}$ times the r.m.s 50 Hz ac voltage, a capacity gain of at least 50 % could be achieved. However, a definitive proof of this assumption and its impact on cable insulation life is still missing in the literature. The goal of this research is to contribute to developing the empirical knowledge on the insulation performance in order to validate the feasibility of such anticipated gains of dc versus ac, and determining the comparative impact of different operational conditions from a component engineering point of view. The technique chosen for determining insulation performance is the measurement of partial discharge activity within the cable, with a specific focus on voids at semicon-dielectric interfaces.

1.1. Background on Partial Discharges in Insulation Systems

Solid insulation systems typically consist of dielectric materials of sufficiently high breakdown strengths bridging the gap between the high and low voltage electrodes. Their function is to provide mechanical support to the electrodes while withstanding electric and thermal stresses for long duration of time, sometimes in the order of tens of years as is the case with underground cable systems. Tiny voids present within the dielectric, as well as at electrode-insulation interface have much lower breakdown strengths, leading to partial discharges (PD) within these voids [8]. The detrimental effect of PDs resulting in material degradation due to modification in its chemical composition and its eventual complete breakdown has been discussed in [9]. In [10], it is mentioned that the rate of deterioration is expected to be greater for voids adjacent to the electrode, as compared to those completely enclosed within the dielectric. Therefore, this study concentrates on voids existing at semiconducting (semicon)-dielectric interface.

Two important parameters of PD behavior governing the lifetime performance of the insulation are the repetition rate (R_r), measured in number of discharge pulses per second, and discharge magnitude (D_m), usually measured in pico-Coulomb (pC). Deterioration depends on both R_r and D_m , but in different ways. R_r increases with applied voltage and frequency of operation [11,12]. The probable role of applied frequency, electric field and R_r in governing the deterioration limit is highlighted in [10,11]. Defining this limit as a certain discharge magnitude below which deterioration is negligible, these papers specify that it is not a sharp limit. Discussing how the void diameter has little effect on the rate of deterioration after a certain threshold, it was shown how discharges concentrate in deep un-carbonized pits of smaller diameter within the void [10]. Nevertheless, it can be inferred that the role of R_r and D_m in governing the insulation lifetime is intrinsically related.

Knowledge on the mechanism of void PD behavior and factors influencing its inception voltage, recurrence and evolution in time is necessary. A good discussion on these aspects is provided in [13–15]. Some aspects relevant in supporting our observations are discussed here.

1.1.1. PD Initiation

The two necessary conditions for a PD event are: 1) Voltage across the void is greater than its breakdown strength. 2) Availability of free electrons to initiate the discharge.

The first condition determines the inception voltage which is defined as the voltage above which discharge occurs, and depends on the kind of gas in the void, its pressure and the void dimensions. The breakdown phenomenon in an insulation void is consistent with the Paschen's curve [16]. The inception voltage is usually 10-20 % lower than the breakdown voltage obtained from the Paschen's curve [17]. It follows that under the conditions of this experiment, the inception voltage is possibly independent of frequency of applied voltage, a trend we observed under specific conditions in this work. This behavior was also reported previously in [18]. However, the presence of space charges and trapped surface charges may distort the field across the defect and may result in higher observed inception voltages, particularly under dc condition.

The second necessary condition implies that there is a finite time lag t_L after reaching inception voltage, but before a discharge is initiated. This time lag in availability of electrons to initiate a discharge is stochastic, resulting in a statistical over-voltage ΔV [19]. It was shown that the D_m is proportional to ΔV [14], which in turn affects the residual voltage across the void after the discharge has occurred.

Physical location and dimensions of the void in the insulation system are also important. For example, a flat void perpendicular to the field can have a field enhancement by the dielectric relative permittivity ϵ_r . The location may cause asymmetry in electric field, causing different discharge patterns with positive and negative polarities. But most importantly, experimental data suggests that the material acting instantaneously as the cathode influences the discharge behavior. For example, the void can be between the inner semicon layer which is in direct contact with the inner conductor and the insulation that surrounds it, or between the insulation and the outer semicon layer, which

is in direct contact with the outer shield (Figure 1). In the first instance, assuming that the central conductor is at a positive voltage and the outer shield is grounded, the insulator wall would act as the cathode, whereas in the second instance it would be the anode. This role will reverse when the central conductor is at negative polarity. Based on the availability of free electrons, it is discussed in [20] how there is a greater tendency of discharges when insulation wall acts as the cathode. On the other hand, the discharge magnitude is greater when the semicon wall in the void is negative [17]. However, unlike the observations in [17,20], the findings of [21] suggested that negative PDs have higher D_m as compared to positive PDs. The defects studied in the same reference were of different type at the termination of the medium voltage XLPE cable, but still involved the outer semicon layer and the insulation.

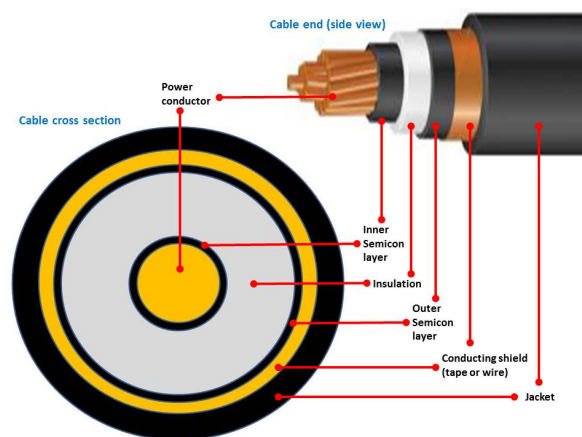


Figure 1. Cable geometry depicting different layers.

1.1.2. Recurrence

The recurrence of PD after a discharge event depends on the recovery time t_R during which the voltage across the void builds from the residual voltage to its inception and the statistical lag time. The combined effect of these two ultimately determines the PD repetition rate. It is discussed how t_L is inversely proportional to ΔV [22] but independent of the applied voltage [14,19]. On the other hand, t_R depends on the charge decay rate, which is a function of void dimensions, conductivity and the average electric field [23].

1.1.3. Void Evolution

Erosion and chemical degradation caused by the PDs leads to a gradual deterioration of the dielectric, which in turn changes the behavior of the PD [18]. This is important to take into account while empirically analyzing the data. We observed in our preliminary results that fundamental frequency ac quickly altered the test artificial void. Therefore, in order to minimize the detrimental effect of PDs while studying the trends, a frequency range of 0-0.1 Hz and an applied voltage range of 0-20 kV was used.

On the other hand, the way the void evolves as well as its subsequent effect on insulation performance is important to determine insulation life. For an ageing void at metal-insulation interface, it was observed in [24] that the PD repetition rate decreases in time, accompanied with higher D_m and increasing inception voltage. The same reference shows how trace conductor material from the copper electrode migrates towards the dielectric due to PD activity and ionized air particles. In [25], it is predicted based on the conductivity change due to the migration of metallic material towards the insulation layer that space charges may appear, thus decreasing the electric field under dc conditions. It would be interesting to explore whether the test samples used in this study exhibit

the aforementioned behavior and determine some empirical understanding about its trend with the considered operating conditions, but this information is yet unavailable as of this writing.

1.1.4. PD Behaviour with AC Versus DC Applied Voltage

It has been suggested that the PD rate in cable insulation with dc operation is lower than ac under similar conditions [15,26]. This is because the dc time constant τ determined from the cable insulation parameters governs the PD R_f . It was discussed in [15], that unlike the case of commercial 50-60 Hz ac where the $\frac{dV}{dt}$ influences the repetition rate, τ is orders of magnitude higher than the theoretical value that would give equivalent PD R_f . Our initial tests on artificially created voids embedded within insulation of Ethylene Propylene Rubber (EPR) and High-density Cross-linked Polyethylene (XLPE) medium voltage (5-30 kV) cables showed that dc voltage enhancement of at least 5 times could still give significantly lower PD R_f . The insulation performance over its lifetime also depends on the inception voltage. Further, under dc voltage, space charges are able to develop when there is conductivity gradient in the dielectric (due to thermal gradient, electrode migration or carbonization), leading to field distortion and lowering of PD activity if polarity reversal is avoided. Another reason may be that, since steady-state DC electric field is governed by the conductivity of the materials, the field strength in void is much less than that in dielectric, which may result in less PDs under dc voltage.

1.2. Research Focus

The focus of our paper is to develop empirical knowledge on PD behavior in a void at the semicon-dielectric interface of a medium voltage EPR power cable. The inferences derived from our observations will be supported by the principles discussed in Section 1.1. Measured trends at medium voltage levels (0-20 kV) and low frequency (0.01-0.1 Hz) will be analyzed as compared to dc. Change in discharge activity with void evolution will be studied in order to gather understanding on the operational practices under dc that would at least maintain the same expected insulation performance as in the case of ac.

2. Experimental Setup and Test Procedure

The schematic of the test setup is shown in Figure 2.

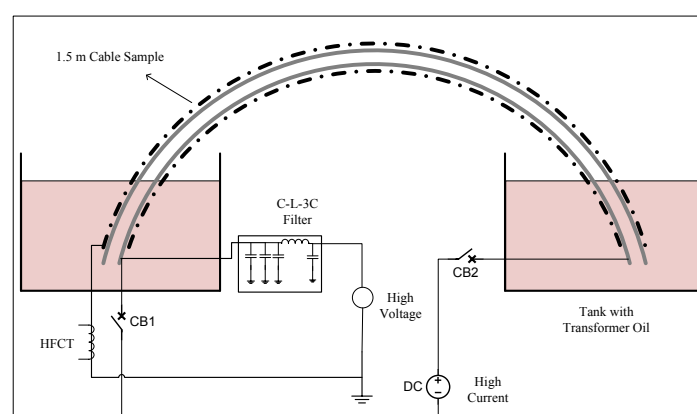


Figure 2. Schematic of the setup for PD measurements in test cable under ac and dc voltages.

Cable samples of 1.5 m were used and the layers at the termination at both ends were cut in a graded manner to ensure uniformly varying stress. These cable terminations, along with the high voltage inductor of the C-L-3C filter, were immersed in transformer oil to avoid partial discharges at these locations [27]. The C-L-3C filter, with $C=2$ nF and $L=40$ mH arranged in a configuration as

shown in Figure 2, has increasing attenuation greater than -6 dB above 10 kHz, thus filtering noise from the high voltage supply.

The high frequency current transformer (HFCT) was used to capture the small signals generated by the PD in the cable dielectric. The connection was such that a positive PD was recorded when the polarity of the inner conductor was positive. All the power equipment was reliably grounded for safe and accurate PD measurement. The data were processed in a PD Smart system manufactured by Doble with a band-pass of 100-500 kHz and transferred to a computer for visualization. Unless otherwise mentioned, the threshold for PD measurement was set at 10 pC.

A high current dc power supply capable of providing up to 600 A was used to heat the cable sample. Isolators CB1 and CB2 (shown in Figure 2) were installed to manually disconnect the high current supply during high voltage tests. Simultaneous operation of a high current and high voltage supply was avoided as this operation posed safety concerns. Furthermore, the 600 A dc source created significant radiated noise which obfuscated the measurement from the HFCT. To hold the test sample temperature at the desired value during high voltage tests, the oil in the tanks at both ends could also be heated up to 80 °C using immersion heating rods. The mathematical basis and experimental validation of this method is presented in [28]. Since the present paper only reports data at room temperature, the high current set-up was used only to thermally age the cable and the oil heating apparatus was not used.

The physical realization of the experimental setup at the test site is shown in Figure 3. The setup includes a high voltage power supply (either ac or dc), a C-L-3C filter, test cable, HFCT, and PD measurement equipment (Doble PD Smart).

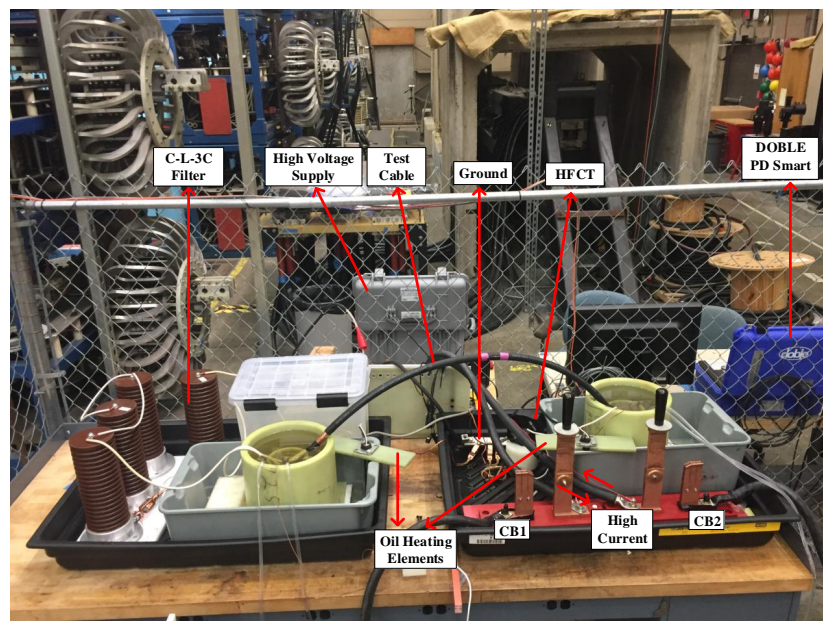


Figure 3. Experimental set-up for PD measurements in test cable under ac and dc voltages.

Figure 4 shows a snapshot of two test cables being prepared with artificial defects in the insulation at its interface with the outer semicon-layer. The location of the artificial void of 1 mm depth and 6 mm diameter in the cable at the interface of the outer semicon-layer and the insulation is also shown.

The rectangular segments of the outer layer, metallic shield and the semicon layer are carefully removed one by one without damaging the outer surface of the cable insulation. Then, an artificial defect of the desired dimensions can be drilled. The bottom surface of the defect is made to be as smooth as possible. The image shows how the Epoxy resin is applied at the surface around the

defects to firmly fix the semicon-layer. Finally, the metallic shield and the outer protective sheath are reattached to obtain the test cable samples.

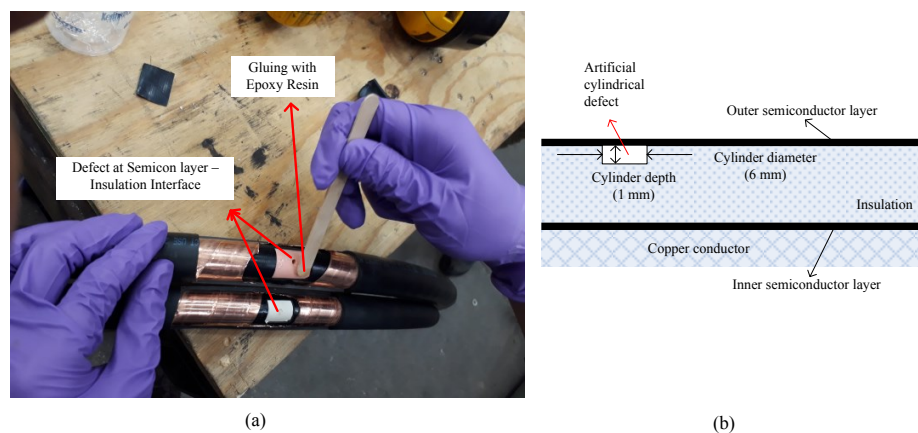


Figure 4. Preparation of test cables with artificial defects at outer semicon layer and dielectric interface (a) Snapshot of actual samples (b) Side view depicting defect location and dimensions.

The snapshots of a test cable post breakdown is shown in Figure 5.

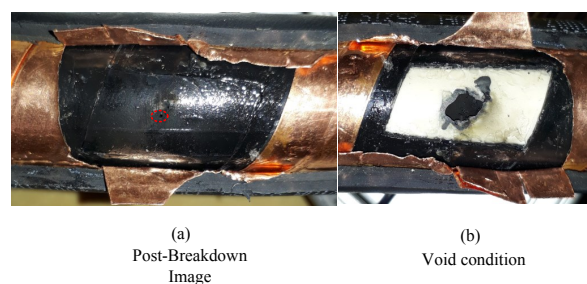


Figure 5. Snapshots of the test cable in different stages of the complete breakdown experiment.

In Figure 5. (a), the post breakdown semicon layer segment above the artificial defect is shown. A pinhole developed in this damaged layer is highlighted. After reopening the semicon layer, Figure 5. (b) shows the carbonized insulation layer. These images provide physical evidence of significant discharge activity at the defect location. The analysis results presented in this paper are from a different cable sample with identical specifications, void dimensions and preparation procedure.

A healthy undamaged cable was tested under similar conditions in the set-up and no discharge activity was measured in this configuration. This observation, together with the physical evidence of localized post-breakdown at the artificial defect increased confidence that the measurement results offered in this paper are partial discharges in the insulation layer void created at its interface with the semicon layer.

In addition, testing was performed to determine if the process of preparing the artificial void resulted in unintended excessive PD activity. For this purpose, the procedure described by Figure 4 (a) was followed without creating the artificial void in a separate cable sample of identical specifications. In other words, the semicon layer was removed and re-fixed similar to the test sample without drilling the void. The altered cable was then tested in the same ranges of frequencies and applied voltages. Measurement results for PD repetition rate of defect cable as compared to the one without defect is shown in Table 1.

Table 1. PD repetition rate for (a) cable with artificial defect (b) Cable without artificial defect under different frequencies at 20 kV applied voltage.

f_a (Hz)	$R_{\text{defect,neg}}$ (s^{-1})	$R_{\text{no_defect,neg}}$ (s^{-1})	$R_{\text{defect,pos}}$ (s^{-1})	$R_{\text{no_defect,pos}}$ (s^{-1})
0	-	-	2	<0.005
0.01	1	<0.01	1	< 0.01
0.1	11	<0.1	9	<1

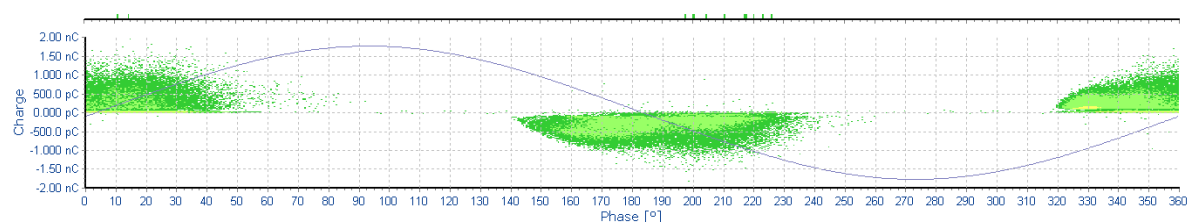
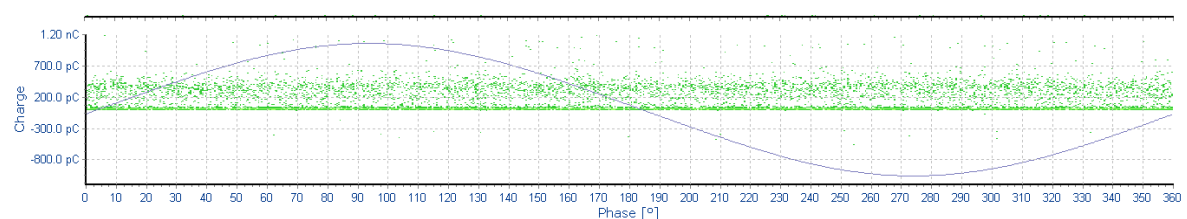
It can be observed that even at the highest test voltage level of 20 kV, the total PD activity is significantly lower in the cable in which no defect is present even though the semicon layer had been previously removed and replaced. Furthermore, the values reported in Table 1 for the altered cable were predominantly out of phase with the applied voltage, a condition which indicates that the source of the measured PD activity was located outside the cable (this point will be discussed in more detail later). In conclusion, the confidence level that the PD activity measured in the cable with a void defect does indeed result from the void itself is very high.

3. DC Voltage Enhancement Ratio with respect to the Fundamental ac

The preliminary results of this section were presented in [29]. A 5 kV EPR cable (5 kV 133% insulation Cu 2 EPR cable) with an artificial defect was used. The defect was a cylindrical void of 6 mm diameter and 1 mm depth and was created at the interface of the inner semicon layer and the insulation.

This is considered to be the worst case scenario as the void is not internal to the insulation [10]. Further, the location is such that the void experiences the maximum electric field. In the first test, the cable was tested under 60 Hz ac voltage. In the second test, the same sample was tested under dc voltage. The operating condition was at ambient room temperature and pressure. The voltage was slowly raised until the inception voltage and the PD was measured from HFCT installed around the ground return from the cable shield using a PD Smart meter. The connection was made such that a positive PD corresponded to positive cycle of the applied voltage.

The pattern diagrams for partial discharges measured at 4.5 kV rms 60 Hz ac and 6.6 kV dc are shown in Fig. 6 and Fig. 7 respectively. Note that the internal meter voltage reference shown in the figures is delayed with respect to the actual imposed ac voltage by 130 degrees: this must be considered in evaluating the expected phase angle at which the discharges are observed in Fig. 6.

**Figure 6.** Pattern diagram for partial discharges under 4.5 kV rms ac conditions.**Figure 7.** Pattern diagram for partial discharges under 6.6 kV dc conditions.

In the dc case at 6.6 kV, which was the PD inception voltage, the repetition rate was sporadic at ≈ 5 pulses per second. In the ac case, the repetition rate was much higher at 200 per second at 4.5 kV rms 60 Hz voltage (with a peak voltage of 6.4 kV). The inception voltage for 60 Hz ac was 3.5 kV rms (almost 5 kV peak) at which the repetition rate was 5-70 pulses per second with an average of pulses 20 pulses per second. The maximum discharge magnitude was the same (≈ 2 nC) for both ac and dc and the PD activity was audible.

When the cable was retested under 60 Hz ac sine wave, the inception had increased from 3.5 kV to 4 kV rms, at which the rate was 2 pulses per second. Further, at 4.5 kV rms, the rate had decreased from 200 pulses per second to 100-120 pulses per second. This behavior could possibly indicate the change in conductivity in the vicinity of the void.

Under repeated dc test, no PD activity was observed until 7.2 kV. At 7.8 kV dc, PD activity was observed, but immediately there was significant audible PD activity near the void location and shortly thereafter, the high voltage dc supply tripped, indicating complete breakdown of the cable.

4. Void Discharge Behavior with Applied Voltage and Frequency

Experience with the cable sample from Section 3 showed that the void quickly deteriorated. It was decided to perform the next experiments at a lower frequency range of 0.01-0.1 Hz, thus minimizing the deterioration while studying the trends. A second 5 kV 133% insulation Cu 2 EPR cable sample was prepared with an artificial void of 6 mm diameter and 1 mm depth. However, this time, the void was located at the interface of outer semicon layer and the insulation as highlighted in Figure 4.

Figure 8 shows the distribution of the PD R_r with respect to D_m for different voltage levels from 10 to 20 kV in steps of 2 kV. The results are shown for dc, as well as 0.01 Hz and 0.1 Hz sine wave. The voltages are stated in terms of their peak for sinusoidal voltages. The experiments are conducted at room temperature (22 °C). All measurements, done on the same day with dc tests last, are listed as 'Test Series 1' in Table 2. The duration of test and inception voltage are reported.

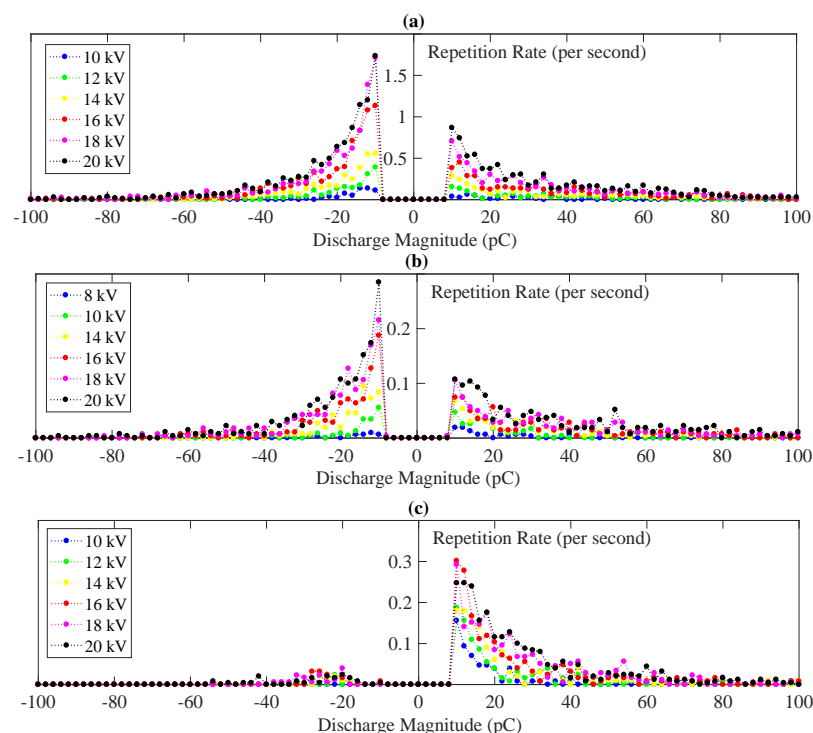


Figure 8. Voltage dependence of PD discharge magnitude versus repetition rate for (a) 0.1 Hz (b) 0.01 Hz (c) dc.

The following trends can be observed:

- Both negative and positive PD R_r have a specific distribution pattern with respect to the D_m , with a maximum (R_{max}) at 15 pC. The distribution is asymmetrical, with negative R_r having higher values for lower D_m as compared to positive R_r .

We know that the electric field across the void is asymmetrical due to the relatively large void size and the cylindrical cable geometry [23]. But a more convincing reasoning for the asymmetry in distribution comes from considering the material in the role of cathode in each case [17,20]. When the inner conductor is at negative polarity (resulting in measured negative PDs), the EPR insulation wall acts as the cathode, thus exhibiting a higher rate of discharges consistent with observations in [20]. During positive polarity however, semicon layer is the cathode, resulting in higher over-voltages and therefore, higher discharge magnitudes [17,19].

- As the applied voltage is increased, the PD R_r increases for both positive and negative sides. Its distribution pattern with respect to discharge magnitude and the position where R_{max} occurs does not vary significantly. The theory presented in [14,19] supports these observations. Further, the charge decay rate increases with average field across the void, and therefore the recovery time decreases [23].
- The value of R_{max} increases with applied voltage, but this trend is not always followed. For instance, as we go higher in voltage from 16 kV dc to 20 kV dc in Figure 8 (c), R_{max} decreases. This behaviour will be further explored in the subsequent section.
- As frequency is increased from 0.01 Hz to 0.1 Hz, the R_r significantly increases. The relationship between $\frac{dV}{dt}$ and repetition rate is explained in [15]. With higher applied frequency, the lag time t_L is expected to decrease. The position at which R_{max} occurs does not change significantly. With higher frequencies, greater levels of over-voltages (on which the D_m depends) above the inception voltage are achievable more quickly. However, with higher over-voltages, the statistical time lag decreases [22].
- There are only positive PDs under dc conditions, which is expected as there is no polarity reversal. While negligible PDs can be observed in the negative side, for dc these signals are considered to be caused by processes outside the cable under test, thus essentially extraneous to our experiment and equivalent to noise. The positive R_r under dc voltages is higher than the positive R_r under 0.1 Hz. However, the sum of positive and negative R_r for 0.01 Hz is greater, indicating that the total PD activity in time is slightly greater than dc.

4.1. Voltage Dependence

Figure 9 (a) & (b) describe the trend of negative and positive R_{max} with respect to applied voltage.

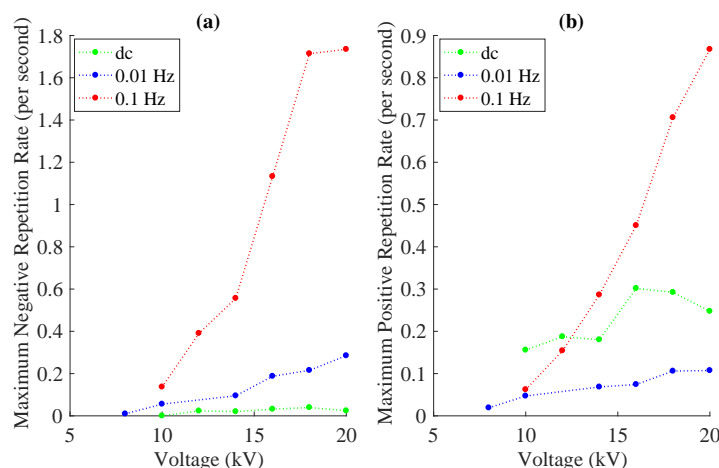


Figure 9. Voltage dependence of maximum PD repetition rate for (a) Negative Rate (b) Positive Rate.

Results are shown for dc, 0.01 Hz and 0.1 Hz. The sinusoidal voltages are represented by their peak magnitudes. The positive R_{\max} for dc is higher than that for 0.01 Hz and also for that of 0.1 Hz in the lower voltage range. The negative R_{\max} is nearly double of the positive for both 0.01 Hz and 0.1 Hz. A direct dependence with increasing sinusoidal voltages was observed, but this is not the case with dc, where the trend is less predictable. To derive a deeper understanding, R_{tot} , the total repetition rate cumulative over all discharge magnitudes, is shown in Figure 10 with respect to applied voltage.

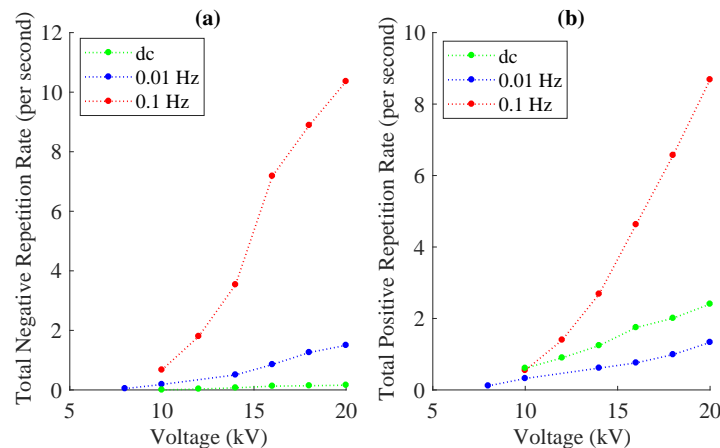


Figure 10. Voltage dependence of total PD repetition rate for (a) Negative Rate (b) Positive Rate.

The following inferences can be drawn:

- Under similar applied voltage and frequency conditions, the positive and negative R_{tot} have comparable values. This observation from Figure 10, in combination with Figure 8, possibly implies that the discharges are occurring in the same void with a specific R_r distribution in D_m .
- The difference in positive and negative R_{\max} in Figure 9, in combination with the above inference, indicates that more number of higher D_m positive PDs are present as compared to negative PDs. For negative PDs, a higher number of lower D_m are observed. This behavior is in agreement with the observations of the role of cathode material described in [17,20], leading to asymmetry in the PD activity during positive and negative voltage cycles.
- The total PD activity with 0.01 Hz (sum of positive and negative R_{tot}) is slightly higher than the PD activity under dc conditions.
- While the observed trend in R_{\max} under dc conditions was less predictable, R_{tot} consistently increases with voltage.
- The frequency dependent increase in R_{tot} is more significant for voltages higher than the inception. While PD repetition rate is an important factor governing the insulation life [11], inception voltage is also relevant. The inception voltage showed weak dependence on applied frequency in the conditions tested in this study, in agreement with similar observations made in [18]. It is important to know whether inception voltage of PD activity is above the nominal operating value if the dc voltage enhancement factor as compared to ac is to be determined based on the insulation performance over its lifetime.

After the series of tests discussed above (Series 1), two more series of tests were conducted. These test series comprised of experiments conducted on the cable sample to investigate the gradual deterioration due to PD activity. Each series was conducted in one day. The discussion up to this point was based on 'Test Series 1'. 'Test Series 2' was conducted as a verification of the first series and to understand the frequency trend in more detail. Finally, 'Test Series 3' was conducted after thermal exposure of the sample to understand the PD behavior after void evolution. Applied voltage was varied from 0–20 kV in steps of 2 kV for each test and the rate distribution over discharge magnitudes was measured for 5 minutes.

In order to quantify the observed empirical trends numerically, the linear regression tool was used. It should be noted that the parameters presented herein are used solely to study the comparative trends with applied voltages and frequency specific to this study and may change with different operating conditions and void evolution. The theoretical model attempting to derive the underlying physics is discussed in [30]. To correlate the parameters of the trend-line equation with physical quantities, equation (1) was used.

$$R_{\text{tot}}(V_{a,\text{peak}}, f_a) = \underbrace{\frac{dR_{\text{tot}}(V_{a,\text{peak}}, f_a)}{dV_{a,\text{peak}}}}_m (V_{a,\text{peak}} - V_{\text{inc}}(f_a)) \quad (1)$$

Where, $R_{\text{tot}}(V_{a,\text{peak}}, f_a)$ is the total PD repetition rate (either positive or negative) in s^{-1} dependent on the applied voltage and frequency and $V_{a,\text{peak}}$ is the peak of the applied voltage in kV. The slope m is the variation of $R_{\text{tot}}(V_{a,\text{peak}}, f_a)$ with respect to the applied voltage with units $\text{kV}^{-1}\text{s}^{-1}$. The constant term $V_{\text{inc}}(f_a)$ is the estimated inception voltage in kV. The slope m and constant term $V_{\text{inc}}(f_a)$ are the parameters estimated using regression analysis to fit the linear equation defined in (1) onto the measured variation in total PD repetition rate with peak applied voltage at different frequencies. The results of the regression analysis are presented in Table 2. The parameters were obtained from the curve fitting tool of MATLAB, including the coefficient of determination (R^2) indicating the goodness of fit. Time for which the experiment was conducted and the observed inception voltage $V_{i,\text{obs}}$ are also tabulated.

Table 2. Linear regression results for empirically measured variation in total repetition rate with applied voltage for different frequencies at room temperature.

f _a (Hz)	Time (min)	V _{i,obs} (kV)	Positive R _{tot}			Negative R _{tot}		
			m (kV ⁻¹ s ⁻¹)	V _{inc} (kV)	R ²	m (kV ⁻¹ s ⁻¹)	V _{inc} (kV)	R ²
Test Series 1 (Threshold: 10 pC)								
0	25	7	0.18	7	0.99	-	-	-
0.01	45	8	0.09	7	0.97	0.12	8	0.96
0.1	20	9	0.83	10	0.98	1.05	10	0.98
Test Series 2 (Threshold: 10 pC)								
0.01	25	10	0.06	10	0.96	0.06	10	0.95
0.03	30	12	0.19	12	0.99	0.18	12	0.98
0.05	30	12	0.33	11	0.99	0.34	12	0.996
0.07	30	12	0.44	12	0.98	0.41	11	0.98
Test Series 3 (Post-Thermal Room Temperature, Threshold: 10 pC)								
0	7	-	-	-	-	-	-	-
0.01	30	18	-	-	-	-	-	-
0.05	30	12	0.32	12	0.99	0.3	12	0.99
0.1	30	12	0.48	10	0.99	0.6	11	0.99

The high R^2 value, greater than 0.95 and sometimes as high as 0.99, indicates acceptable confidence on the goodness of fit of the proposed linear relationship between total PD repetition rate with applied peak voltage. The slope m for dc is double that for positive R_{tot} in case of 0.01 Hz, mathematically supporting the empirical inference that the time for which high voltage is imposed governs the PD behavior. At this extremely low frequency, the influence of $\frac{dV}{dt}$ on PDs is not observable. Further, sinusoidal polarity reversal every 50 s does not significantly effect the discharge

behavior in terms of R_{tot} and its variation with peak applied voltage as compared to dc. The inception voltage is also similar.

In order to gain statistical significance of the linearity of R_{tot} with applied voltages that curve fitting indicates, further experiments were conducted for PD activity at 0.03 Hz, 0.05 Hz and 0.07 Hz and different voltage levels. These are listed under 'Test series 2' in Table 2. The experiments suggest a strong linear relationship between R_{tot} - $V_{a,peak}$ at all measured frequencies, within the voltage range studied. These results also offered insight on the frequency dependence of PD activity, which is discussed in the subsequent section.

4.2. Frequency Dependence

Figure 11 shows that the slope of the voltage variation in both positive and negative R_{tot} non-linearly increases as the applied frequency is increased.

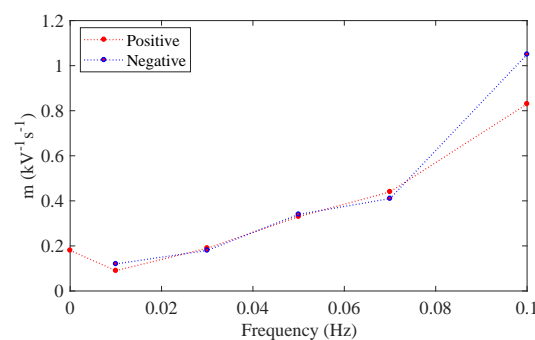


Figure 11. Frequency dependence of the voltage variation in R_{tot} .

This increase showcases the greater influence of $\frac{dV}{dt}$ than the inception voltage on the PD activity. The non-linearity is understandable, considering that the time for which the voltage higher than inception, as well as the $\frac{dV}{dt}$ imposed during such voltages are non-linear functions of frequency. It cannot be inferred from these results, however, whether the effect of $\frac{dV}{dt}$ itself on the PD activity is non-linear. Addressing this question is relevant from a transient behavior standpoint, but is beyond the scope of this research.

Further, evidence suggests that the void gradually evolves, leading to higher inception voltages and lower PD repetition rates with higher discharge magnitudes. Such observations and their possible reasons were also reported in [24]. Since tests for 0.03 Hz, 0.05 Hz and 0.07 Hz were conducted later, the artificial void had already been subjected to considerable aging under high voltage. The evidence of void evolution is revisited in subsequent section. In Figure 12, the results for frequency variation in R_{tot} for select applied voltages are shown.

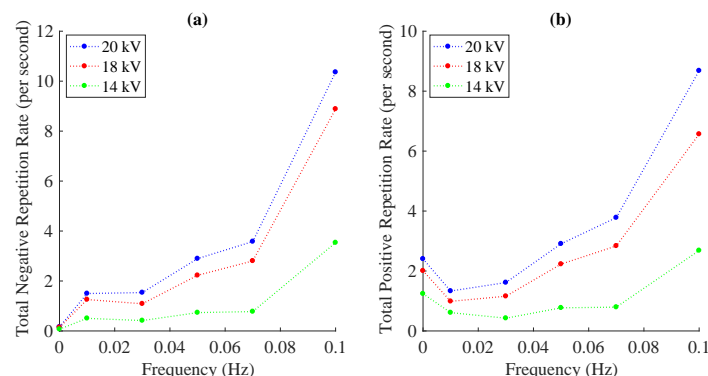


Figure 12. Frequency dependence of total PD repetition rate for (a) Negative Rate (b) Positive Rate.

The non-linear dependency of PD activity on frequency, is visible in this figure. The slope is similar for positive and negative PD activity. From the results, there is no clear trend indicating that one is discernibly higher than other at this voltage and frequency range.

4.3. Void Evolution

Low frequency was used to study the trends in PD activity while minimizing their deleterious effect of ac voltages. It is however, also interesting to see how the void evolves in time. After imposing high temperature (measured 60 °C at the sheath), post-thermal, room temperature tests were conducted. These are presented as 'Test Series 3' in Table 2. The repetition rate distribution with discharge magnitude for different voltages in 'Test Series 3' is shown for 0.1 Hz, 0.01 Hz and dc in Figure 13.

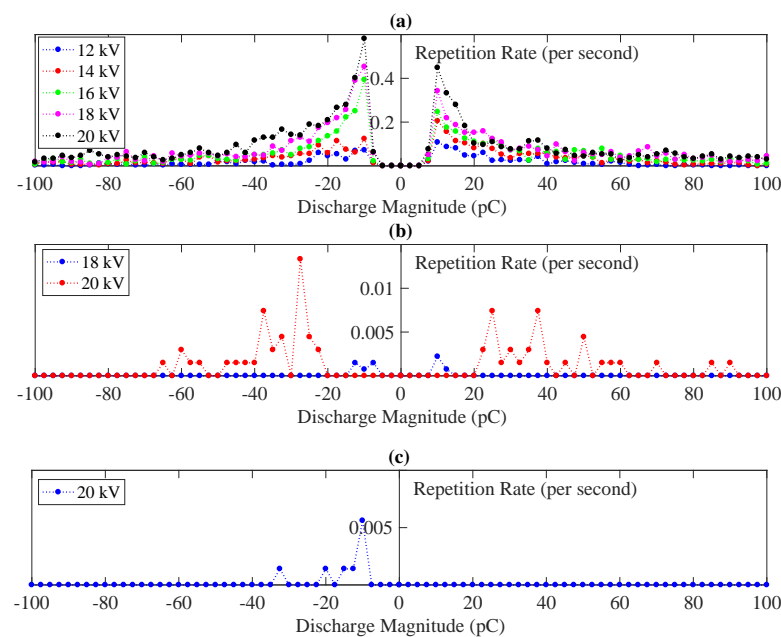


Figure 13. PD discharge magnitude versus repetition rate for different voltages in 'Test Series 3' (a) 0.1 Hz (b) 0.01 Hz (c) dc.

It can be observed that the repetition rate is significantly lower as compared to those presented in Figure 8. It was observed that the inception voltage had significantly increased as compared to 'Test series 1'. For 0.1 Hz and 0.05, the inception was observed at 12 kV, while for 0.01 Hz it was at 18 kV. For dc, no positive PD was observed even at the maximum imposed voltage of 20 kV. It is possible that the space charges and conductivity change are playing a role as predicted in [24,25]. Observations suggest that ageing resulted in EPR conductivity larger than the unaged case in the vicinity of the void since it is much easier to induce space charge at the same voltage level. Since 20 kV is applied on a 5 kV cable (2.9 mm insulation thickness), considerable space charges can develop [31].

Specific to the voids at the semicon-dielectric interface of the cable, evolution of voids are accompanied by metal migration towards the dielectric material. This erosion changes the conductivity of the void walls, leading to change in PD behavior. For example, the copper content at the EPR surface was 0.2 % [24]. The similar phenomenon could be expected with the semicon-interface.

Figure 14 shows the distribution of PD R_r with respect to D_m for 0.1 Hz sinusoidal ac from test series 1 and 3 measurements.

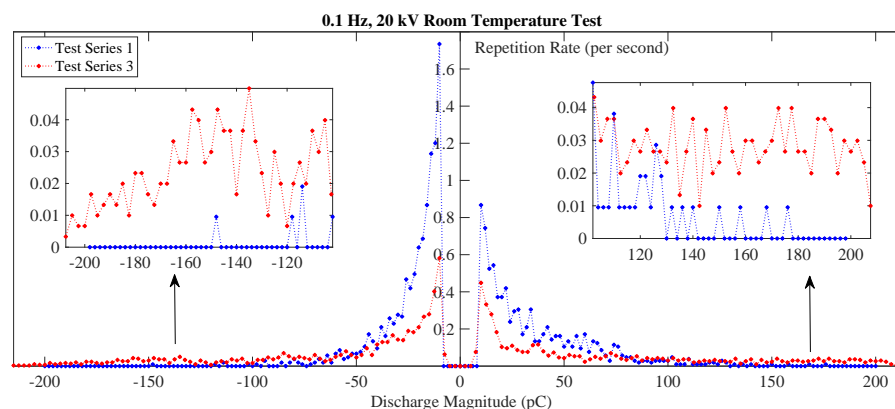


Figure 14. Evidence of void evolution for 0.1 Hz ac sinusoidal wave at 20 kV.

It can be observed that the total PD rate is significantly lower with ageing. There is, however, an increase in the PDs at higher discharge magnitudes. This is consistent with the observations in [24].

5. Conclusion

The PD activity in the artificial void at the semicon-dielectric interface has been observed to linearly increase with applied voltage in the range 10-20 kV for 0.01-0.1 Hz frequencies as well as dc. The maximum of repetition rate distribution over the discharge magnitude occurred at about 15 pC and did not shift position with varying applied voltage and frequency. The increase in repetition rate with frequency appeared non-linear, but this could be due to the void evolution.

The density distribution of PD repetition rate was asymmetrical, with negative PDs having a higher maximum of repetition rate distribution over the discharge magnitude, but positive PDs having higher repetition rate at higher discharge magnitudes. Similar evidence was reported in [17,20]. The total repetition rates, however, were found to be comparable.

In the initial tests, the total PD repetition rate at dc voltage was lower as compared to ac sinusoidal voltage. However, it was observed to be comparable to 0.01 Hz ac voltage results. The inception voltage did not exhibit observable frequency dependence. Therefore, it is important to know whether the inception voltage of PD activity is above the nominal operating value if the dc voltage enhancement factor as compared to ac is to be determined based on the insulation performance over its lifetime.

In agreement with the preliminary tests using 60 Hz ac sinusoidal wave on the 5 kV Cu 2/0 EPR cable, the second sample (5 kV Cu 2/0 EPR cable) showed signs of gradual deterioration over time even when subject to low frequencies. The PD activity had lower repetition rate and higher inception voltages after a high temperature exposure at 60 °C, while at the same time higher discharge magnitudes were observed. No PD activity was seen till 20 kV with dc voltage at room temperature after the void had evolved. This could possibly indicate the change in void surface conductivity and effect of space charges predicted in [25] due to the phenomenon of semiconductor layer material migration consistent with the observations of [24].

The main observation is that the PD rate under dc voltage is significantly lower than that under 0.1 Hz and 60 Hz ac sinusoidal voltages with the same peak value. The intentional void did evolve over time, especially under the thermal exposure. The preliminary observation and test experience on medium voltage cables with intentional defects made us gain more confidence on our hypothesis that dc voltage helps to reduce cable weight/volume as compared with 50/60 Hz ac voltages. Obviously, more extensive experimental tests and theoretical investigations are still required to support this hypothesis.

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