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Ultra Low Power Process Tolerant 10T (PT10T) SRAM with Improved Read/Write Ability for Internet of Things (IoT) Applications

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Abstract: An ultra-low power (ULP), power gated static random access memory (SRAM) is presented for Internet of Things (IoT) applications, which operates in sub-threshold voltage ranges from 300mV to 500mV. The proposed SRAM has tendency to operate in low supply voltages with high static and dynamic noise margins. The IoT application involves battery enabled low leakage memory architecture in subthreshold regime which has low power consumption. Therefore, to improve power consumption along with better cell stability, a power gated 10T SRAM is presented. The proposed cell uses a power gated p-MOS transistor to reduce the leakage power or static power in standby mode. Moreover, due to the schmitt triggering and read decoupling of 10T SRAM the static and dynamic behavior in read, write and standby mode has shown enhanced tolerance at different process, voltage and temperature (PVT) conditions. The proposed SRAM shows better results in terms of leakage power, read static noise margin (RSNM), write static noise margin (WSNM), write-ability or write trip point (WTP), read-write energy and dynamic read margin (DRM). Further, these parameters are observed at 8-Kilo bit (Kb) and compared with already existing SRAM architectures. It is observed that the leakage power is reduced by 1/81×, 1/75× of the conventional 6T (C6T) SRAM and read decoupled 8T (RD8T) SRAM, respectively at 300mV VDD. On the contrary, RSNM, WSNM, WTP and DRM values are improved by 3×, 2×, 11.11% and 31.8% as compared to C6T SRAM, respectively. Similarly, proposed 10T has 1.48×, 25% and 9.75% better RSNM, WSNM and WTP values as compared to RD8T SRAM, respectively at 300mV VDD.

Keywords: power gating; read decoupling; read-write static noise margin; dynamic noise margin; read-write energy; schmitt trigger; leakage power.

1. Introduction

The massive constrain headed for internet of things (IoT) devices has led to developments of ultra-low power (ULP) systems-on-chip (SoCs) that are capable of operating in sub-threshold voltages [1, 2]. One way to guarantee low power and energy consumption is to scale down the supply voltage to the sub-threshold region [3]. However, the reduced on-to-off current ratio (I_{ON}/I_{OFF}) and the exponential dependence of the current on the threshold voltage (V_{th}) in the sub-threshold region introduces many challenges especially in rationed circuits such as the traditional 6T static random access memory (SRAM) bit-cell. Since, conventional non-volatile memories consume higher read and write power, the scaling of supply voltages and the techniques to reduce leakage at sub-threshold voltages needed. However, the low cell stability is also one of the factor which defy conventional SRAM architecture to not to work at sub-threshold region [4].

However, due to rapid growth of internet market through all over the world, Internet of Things (IoT) brings connectivity, communication, and data gathering to existing devices. IoT includes countless devices connected and communicated with each other to enrich the present lifestyle, and its applicability ranges widely from traditional internet to industrial internet and also to consumer internet [5]. Independent of its application, there is always one common trait: the need of on chip memory that drives the connected world by enabling the capture, transmission, analysis and storage of the data up and down to power the IoT. In addition, IoT applications in which portable devices communicate with each other and thus require an enormous amount of memory to store and process data. The memory used in IoT can differ with the need of applications related to market. For instance, in case of huge amount of data storage and handling information for a long period of time and where the data usage is not much frequent, a high density memory like DRAM and Flash are used. In case of high data transfer rate systems, a fast SRAM memory is required, where a high clock frequency is required to communicate between IoT devices. Therefore, SRAM is always preferred to be used as cache memory due to its faster response. Moreover, the robustness of such memory systems, for the variations in environmental conditions and power efficiency are two of the most important design constraints [4]. As per the literature, more than 40% of the active energy is consumed due to the leakage currents in modern high performance processors [6, 7]. Also, most of the time a large number of SRAM cells used in today's on-chip cache memory stay in the standby mode where leakage power dominants over the dynamic power. Thus, leakage reduction has become the imperative concern in the SRAM memory design.

Implementation of ULP SRAM is also has a significant purpose in embedded systems such as biomedical implants, self-powered wireless sensors, and battery enabled portable electronic devices in which battery life or input power is a main concern [8]-[11]. Simultaneously, cell stability is also considered as one of the major concerns in SRAM architectures. It is observed that for standard 6T SRAM cell, read static noise margin (RSNM) is vulnerable at subthreshold regions, while reading through full swing sense amplifier (SA) [12]-[15]. It is well known that the best way to reduce the power in a digital circuit is to lower the supply voltage as it has a direct impact on the power consumption [16]-[20]. SRAM design remains challenging and becomes more interesting due to the rapid advancement of CMOS technologies and with increased demand of on-chip memory in the wireless implantable and wearable biomedical sensors. Subsequently, the SRAM memory contributes as the major source of power consumption in an electronic device due to introduction of leakage in subthreshold region. Emerging memory technologies are continuing to make steady progress towards product intercepts, including phase change random access memory (PCRAM) and

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resistive RAM (ReRAM). However, embedded SRAM continues to be a critical technology enabler for a wide range of applications from high-performance computing, graphics for mobile applications, wearable electronics and internet of things (IoT) applications [21]. Nevertheless, the vigorous scaling of process technologies driven by Moore's law resulted in statistical process variations in the transistor parameters such as threshold voltage (V_{th}), channel length (L), and mobility [22]. Therefore, device variability in modern processes has become a major concern in SRAM design, degrading performance, bit density, power, yield, and reliability. Other challenges for SRAM include VDD_{min}, leakage and dynamic power reduction. However, stability has long been a major concern for SRAM architectures. Low voltage operation and increased process variation caused by random dopant fluctuation (RDF) & line edge roughness (LER) have been shown to degrade the stability and performance of SRAM, and may lead to functional failure [23]. Aggressive power reduction can be achieved by subthreshold operation. However, operation at these reduced voltages degrades robustness, due to depleted noise margins and higher susceptibility to process variations and device mismatch. However, substantial amount of research has so far been reported regarding noise margin improvement, including RSNM, WSNM, HSNM, data retention and yield improvement of SRAM [24-26], like P-P-N based 10T SRAM [27], decoupled latch [28], [29] and 5T SRAM cell [30]. Some popular methods include voltage scaling, switching activity reduction, architectural techniques, and device sizing and new device structures [31-33]. All these works analyze and quantify the impact on cell stability degradation in lifetime circuit performance.

In order to achieve high RSNM, a basic and effective way is the decoupling of a storage node from the bit-lines during read operation [28]. Kim. *et al*. [34] introduced a new 8T SRAM cell that can operate up to 200mV by utilizing the reverse short channel effect (RSCE). The operation of standard 6T and standard 8T SRAM at subthreshold voltage is unachievable, primarily due to the degraded static noise margins (SNMs) and extreme fluctuations in the device currents under process variations. Therefore, the work in [30] presents a robust, low-voltage SRAM bit cell with a reduced transistor count, as compared to the standard 6T. Multi-threshold devices are also used to achieve better noise margins. To further improve cell functionality, the pull-up PMOS devices are implemented with high voltage threshold (HVT) devices. In [35], cell breaks the feedback loop of the cell during the read operation to guarantee the stability of stored data. In [36], a suitable read operation is provided by suppressing the drain-induced barrier lowering (DIBL) effect and controlling the body-source voltage dynamically. Proper usage of low-threshold voltage transistors in the SRAM design helps to reduce the read access time and enhance the reliability in the subthreshold region. Due to superior gate control, improved electrostatic integrity and variability, FinFET have demonstrated satisfactory scalability and feasibility for mass production of post 22nm node. Thus, FinFET is an ideal alternative to planar CMOS in SRAM designs [37], [38]. However, while considering bulk-CMOS SRAM, the need of diminution in leakage power at subthreshold region has still a primary challenge. Due to continuous device scaling and reduction in supply voltage the leakage power value has come out as equal as dynamic power. Though, some of the above mentioned works on bulk-CMOS SRAMs has considered vital for power reduction, but it degrades noise margins and read-write speed. The same has appeared with some existing works, which has significant improvement in the noise margin and read-write speed but at the same time the overall power has increased. To overcome the tradeoff between power, delay and noise margin we have proposed a feedback controlled 10T SRAM which improves the SNM, speed as well as total power consumption at the same time.

To overcome the process intolerance occurred due variations in various process parameters like channel length, gate-oxide, DIBL etc. and the variability in device due to noise occurred from temperature variations for IoT applications a differential process tolerant 10T SRAM cell is proposed in this paper. The rest of the paper is organized as follows: Related work and motivation are detailed in section II. Proposed 10T SRAM architecture with 64×128 array (8-Kb) is presented in section III. Operations and working of 8KB SRAM is explained in section IV. The simulation results and discussion of proposed 10T SRAM is mentioned in section V. Lastly, section VIII concludes our work.

2. Related Work and Motivation

From the literature, it is observed that the leakage power and cell stability are the key concern in subthreshold SRAM architectures to improve reliability, yield and susceptibility of portable electronic devices for IoT applications. Moreover, SRAM cells are in static or hold state for most of the time, which contributes to more and more leakage power. Furthermore, the cell stability is also a foremost concern in subthreshold region. The noise generated from threshold variation, process variation, half select issue and multiple bit errors, reduces the stability of SRAM cell. Consequently, various techniques have been employed to overcome those limitations, such as scaling the supply voltage using process variation tolerant Schmitt trigger based ST10T SRAM [39], a read static noise margin free 7T SRAM [40], differential data aware power supplied D2AP8T SRAM [41], low leakage variation tolerant LP8T [42], LP9T [43] and LP10T SRAM [44] for ULP applications. Besides the advantages provided by these cells, there are some limitations like read stability, consequences of temperature variations in leakage power, low WTP and higher power delay product (PDP) in subthreshold regime. To compensate, all these factors along with low leakage power and better cell stability, a differential ultra low power process tolerant 10T SRAM is proposed in this paper. Fig. 1(a) to Fig. 1(d) shows various acrichteure of SRAM cells proposed earlier. The conventional 6T SRAM shown in Fig. 1(a) has a tendency to fail at subthreshold voltages due to the read path sharing of the M5 and M1. Though, to improve read noise margin an 8T SRAM is proposed as shown in Fig. 1(b), which reads information through a decoupled read path. But, in case of decoupled read the read access time increases. To overcome that a Schmitt triggered 10T (ST10T) is offered [39] as shown in Fig. 1(c), however, the charge sharing is still exists at read and write, which eventually degrades the read/write noise margin. To overcome the problem related to read delay and static noise margin a low leakage 10T SRAM is presented in [44] as shown in Fig. 1(d), which improves the leakage power by the virtual ground path and noise margins by differential decoupled read. However, the stack transistor MN8 used in [44] at ground pushes storage node to meta-stability. The meta-stability is not considered as a good choice to exist in subthreshold supply voltages, where a small gain in storage node voltage flips the state of the cell. To overcome the issue of meta-stability instead of virtual ground a power gating at VDD is considered as better option and to improve read noise margin schmitt triggered logic is used in proposed 10T SRAM as shown in Fig. 1(e).

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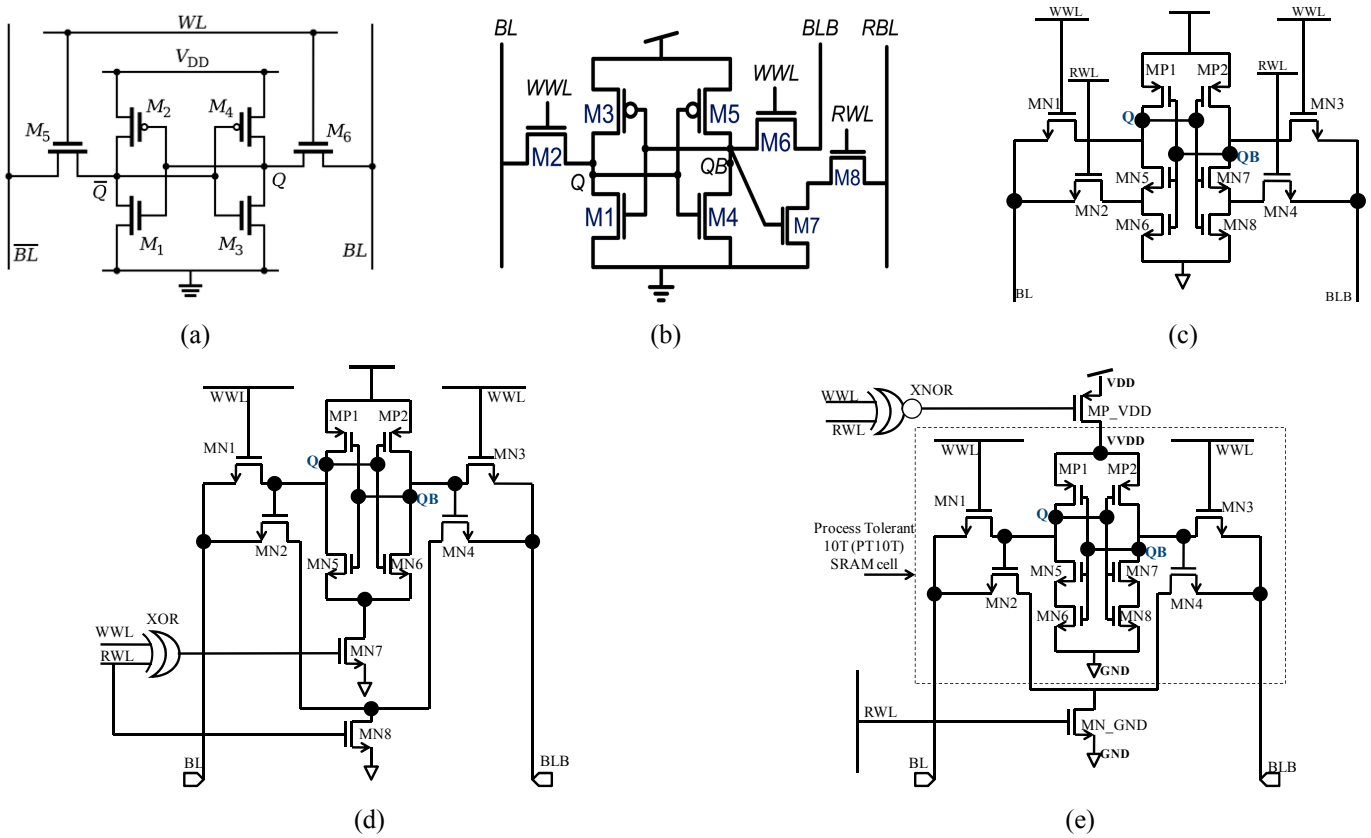

Figure 1. (a) Architecture of convetional (C)-6T SRAM cell. (b) Architecture of read decoupled (RD)-8T SRAM cell. (c) Structural design of schmitt trigger (ST)10T SRAM cell [39]. (d) Schematic of low power (LP10T) SRAM cell [44]. (e) Schematic of proposed process tolerent 10T (PT10T) SRAM cell.

3. Architecture of 10T SRAM Cell

Technological advances and cost reduction have resulted in remarkable development of computing devices. If continued, this trend might result in tens of billions of computing systems consisting of personal computers, desktop machines, smartphones, wearables and many units connected to the internet; collectively known as the Internet of Things (IoT). This dramatic growth in compute devices results in a data explosion and would require millions of Zettabytes of memory in order to perform this large scale of computing. Thus, memories play a critical role in future energy efficient computing systems and considering the points, a subthreshold, low leakage power with high stability SRAM is presented in this section.

The proposed cell has two write access n-MOS transistors, MN1 and MN3 and two read access transistor MN2 and MN4. The *BL* contains single bit information to write and at the same time *BLB* contains the complementary of that. In addition, n-MOS transistors MN2 and MN4 which are connected with virtual ground n-MOS transistor MN_GND are used as a read path. The *BL* and *BLB* are precharged to VDD before the read operation is performed. The MP1-MP2-MN5-MN6-MN7-MN8 transistors form a latch, where, MP1 and MP2 are the pull-up transistors linked to virtual VDD (VVDD). In addition, MN5 to MN8 forms Schmitt triggered logic, which eventually enhances the read noise margin [39]. Furthermore, two transistors MP_VDD and MN_GND are shared with each row of 8-Kb SRAM as shown in Fig. 3, where, MP_VDD is used as a power gating p-MOS transistor, which disconnects the path between VDD and GND at hold state to improve the leakage power. On the other hand, the MN_GND is used as a virtual ground path to read information from the cell.

Table I Comparison of cell layout area at 65nm standard CMOS technology

SRAM cell	Numbers of low voltage threshold (LVT) transistors used	Layout Area [Width (W) × Height (H)]
C6T	6 (2 LVT p-MOS, 4 LVT n-MOS)	**1×** (2.33µm×1µm=**2.33µm²**)
RD8T	8 (2 LVT p-MOS, 6 LVT n-MOS)	**1.2×** (2.33µm ×1.2µm=**2.8µm²**)
ST10T [39]	10 (2 LVT p-MOS, 8 LVT n-MOS)	**1.58×** (2.52µm ×1.46µm=**3.68µm²**)
LP10T [44]	10 (2 LVT p-MOS, 8 LVT n-MOS)	**1.71×** (2.8µm ×1.46µm=**4µm²**)
PT10T	10 (2 LVT p-MOS, 8 LVT n-MOS)	**1.35×** (2.16µm ×1.46µm=**3.15 µm²**)

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Table II Logic Truth table for various operations in proposed PT10T SRAM

Operation	WWL	RWL	BL	BLB
Write 1	1	0	1	0
Write 0	1	0	0	1
Read 1	0	1	Discharging	1
Read 0	0	1	1	Discharging
Hold	0	0	1	1

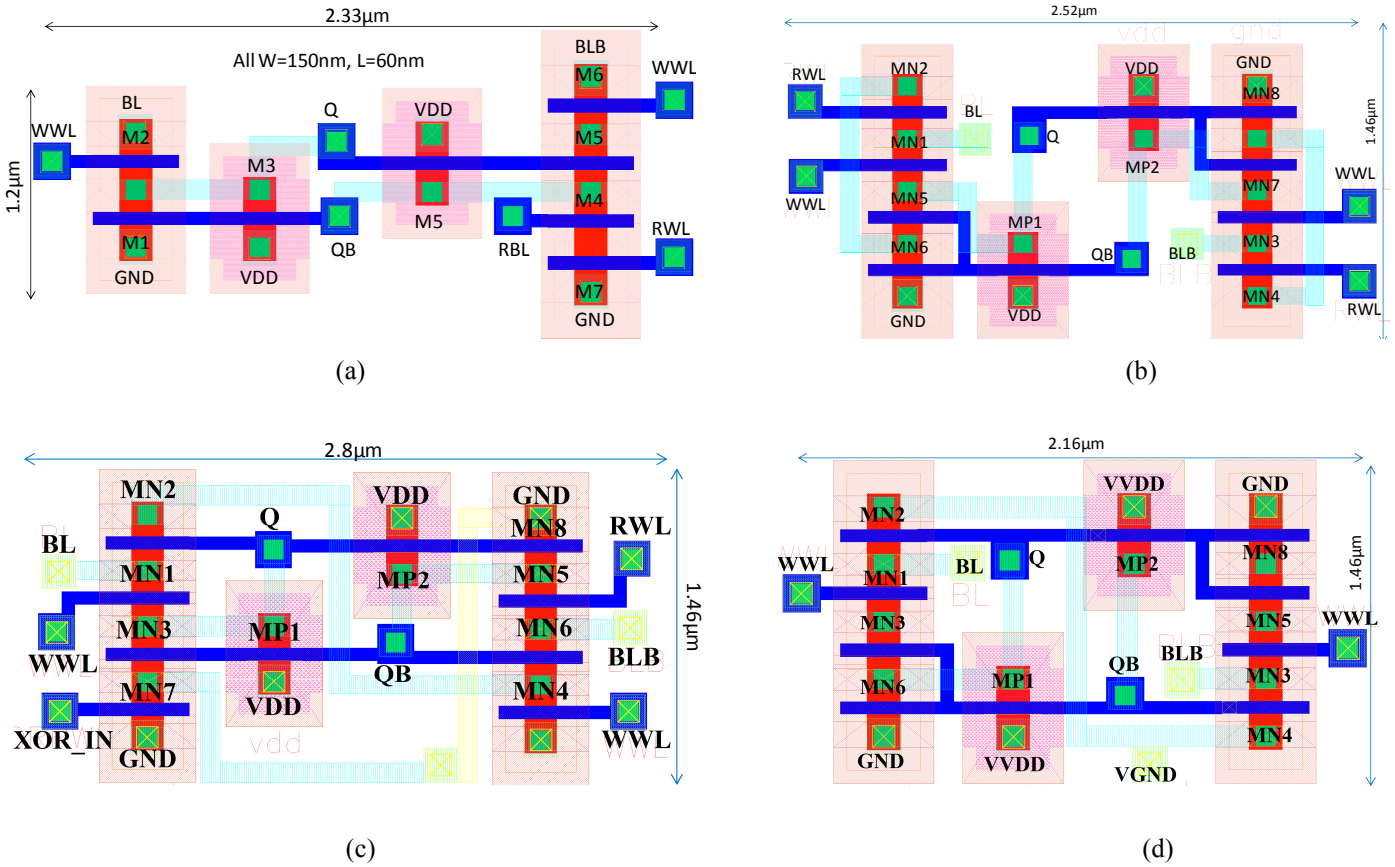

Figure 2. The layout of various SRAM architecture at W=150nm and L=60nm at 65nm Standard CMOS Technology. (a) Layout of convetional RD-8T SRAM cell. (b) Layout of schimtt trigger 10T SRAM cell [39]. (c) Layout of low power 10T (LP10T) SRAM cell [44]. (d) Layout of proposed process tolerent 10T (PT10T) SRAM cell.

4. 10T SRAM Cell Based 8kb Marcoblock and Area Overhead

To observe the area overhead and to have a better view towards the functionality and placing of SRAM cell and various controlling blocks at array level a simplified architecture of 10T SRAM array is portrayed in Fig. 3. In addition, the functioning of 10T SRAM is explained in Table II. The table shows the truth table of various operations takes place in the proposed SRAM architecture. The SRAM array uses internal inputs derived from *RWL* and *WWL* signal to control the power gated p-MOS transistor. However, the proposed SRAM array in Fig. 3 shows the complete correlation of various controlling signals and demonstrates how single bit information is written and read using a high speed differential current compensation sense amplifier (DCC-SA) [45-47]. The layout area of different SRAM architectures is shown in Fig. 2 and the comparison between cell areas is mentioned in Table I. It shows that the proposed SRAM has 17% and 27% reduction in footprint area as compared to ST10T [39] and LP10T [44] SRAM, respectively.

In addition, leakage power is also improved due to power gating of supply voltage VDD using MP_VDD transistor. By means of combining the advantages of both ST10T and LP10T, we addressed a significant improvement in static noise margin and leakage power at different process, voltage and temperature (PVT) conditions in sub-threshold supply voltages. However, to improve leakage power and noise margins at different PVT condition an extra amount of overhead is needed at array level. Fig. 3 shows the overhead area over the SRAM array by introducing two extra transistors at each row of the Marco. MP_VDD (p-MOS) and MN_GND (n-MOS) are the two overhead transistors included at each row to improve leakage power (through power gating

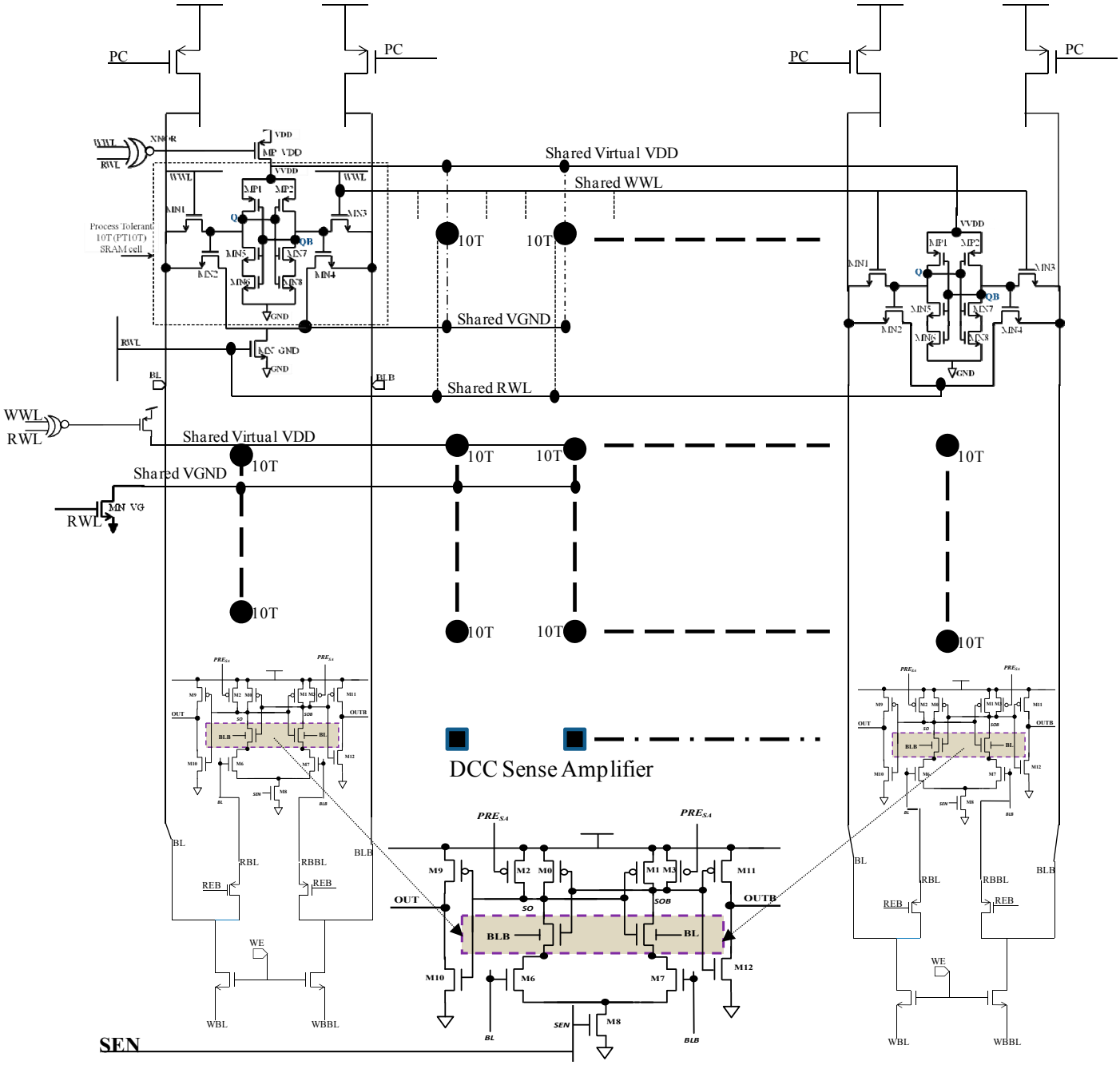

Figure 3. Simplified array acrchitecure of 10T SRAM, where read is perforemed using high speed differentail current compensation sense amplifier (DCC-SA) [45].

using MP_VDD) and read static noise margin (RSNM), dynamic read margin (DRM) using MN_GND. A XNOR gate is also introduced at each row of the SRAM Macro to provide a sleep input to the power gated p-MOS transistor MP_VDD. The XNOR gate has 4 MOS transistor (2 n-MOS and 2 p-MOS) integrated at each row of the array. These extra transistors bear a channel width of 2µm which is 13.33× more than that of the SRAM MOS transistors width (150nm). Consequently, including all overhead and SRAM cell layout area, we observed a total footprint area of 8-Kb SRAM array of C6T, RD8T LP10T, ST10T and proposed SRAM cell as shown in Table III. From the table it observed that the proposed cell has 35% and 12.5% higher Macro area as compared to C6T and RD8T, respectively. On the other hand, the proposed 10T SRAM has 17% and 27% lesser Macro area as compared to ST10T and LP10T, respectively.

Table III Comparison of 8-Kb layout area at 65nm standard CMOS technology

SRAM	Cell Layout Area [Width (W) × Height (H)]	8-Kb (Kilo-bit) Layout Area using 2 Metal-1 Poly Layer Architecture
C6T	2.33 µm^2	18.75 mm^2 (1×)
RD8T	2.8 µm^2	22.63 mm^2 (1.2×)
ST10T [39]	3.68 µm^2	29.60 mm^2 (1.58×)
LP10T [44]	4.0 µm^2	32.17 mm^2(1.71×)
PT10T	**3.15 µm^2**	**25.34 mm^2 (1.35×)**

5. Operations and Working of 10T SRAM Using Differntial Current Compentation - Sense Amplifier (DCC-SA)

A. Read operation

Before reading the information, *BL* and *BLB* are precharged to VDD using the precharge logic input *PC* as shown in Fig. 3. The read operation is obtained through ultra fast differential current compensation sense amplifier (DCC-SA) [38-40]. The read operation is performed by keeping read word line (*RWL)* to HIGH and write word line (*WWL)* to LOW and *XNOR_I/P* kept at LOW value. Since, for read '1' (Q=1), logic 1 is stored at the storage node Q and *RWL* is kept HIGH, which eventually turns ON MN_GND and MN2. This forms a discharging path across *BL-MN2-MN_GND* and a voltage difference, ΔV_{BL}= *{(VDD* (V_{BLB})*-(VDD-*$I_{read,\ BL}$×$R_{MN2\text{-}GND}$*)}* appears between *BL* and *BLB* line which is sensed by the full swing inverter sense amplifier [45-47]. Where, I_{read} is the cell current and $R_{MN2\text{-}GND}$ is the resistance through MN2 and MN_GND. The read access time is measured as the time the *RWL* signal is activated until the *BLB* is discharged to minimum required potential needed by SA to read. The sensing voltage ΔV_{BL} required for DCC-SA [45-47] here is ranges between 50mV-80mV. The read access time and power is measured across a 64-bit column of the SRAM cell. The parasitic capacitance of SRAM column is measured after RC-extraction in Cadence layout design at 65nm UMC Technology. The read operation of proposed cell is shown in Fig. 4(a). The sense amplifier works well in subthreshold or near threshold voltages ranging from 0.3V to 0.7V. The circuit topology of DCC-SA is shown in Fig. 5(a) and the simulated transient voltage at 0.7V VDD is shown in Fig. 5(b). Fig. 5(b) shows the working of SA, as the *SEN* and *RWL* is activated and chip select (CS) is HIGH, the SA detects the voltage difference (sensing voltage) between *BL* and *BLB*. As soon as, the voltage difference reaches to range of sensing voltage, the output node *SOB* gets logic HIGH, which redirects that logic '1' stored at storage node Q of the SRAM.

B. DCC-SA architecture and operation

Fig. 5(a) illustrates the detailed schematic of differential-current-compensation based SA (DCC-SA) [45-47], which is capable of overcoming sensing device V_{th} mismatch effect on SA differential current. Differential current is defined as $|I_L\text{-}I_R|$. Here I_L and I_R are current in the left and right branch of SA. The SA approach differs significantly from other approaches, which use different MOS devices for compensation/calibration of offset, resulting in increased vulnerability to mismatch between devices. In Fig. 5(a) transistors M0-M8 configured the DCC-SA. The body terminals of NMOS M4 and M5 in latch are connected to decoupled bitline (*DL*) and decoupled bitline bar (*DLB*), respectively. Before sensing, SA pre-charge signal (*PRESA*) will be at logic LOW to ensure that the nodes *SO* and *SOB* are pre-charged at VDD. Since DLs are also pre-charged, it results in equal body bias of transistors M4 and M5. A read access starts by the activation of word line (*RWL* in our case) signal. This generates the differential voltage at *BLs* which results in different body bias voltage for M4 and M5 devices. Thus for read '1' case before the activation of *SEN* signal the body of the left NMOS M4 will be at higher potential than the body of NMOS M5, this resulted in $I_{DS}(M4) > I_{DS}(M5)$. In case of no offset in sensing devices, this will results in correct sensing. However in case of offset $(V_{th}\ (M4) > V_{th}\ (M5))$ this compensates the current in the corresponding branch. Thus, at the beginning, the transistor with a lower V_{th} sources a larger current, which eventually creates a high current in corresponding branch is compensated because of the higher body voltage for a smaller threshold voltage. In other words, before *SEN* activation, a differential voltage is developed between the bit-lines which compensates the threshold voltage difference of M4 and M5 to achieve higher effective current in corresponding branch. Thus the device with higher body bias has lower V_{th}. This helps in dynamically adjusting the overdrive potential of this device and compensates for the branch current reduction due to offset in sensing devices. Fig. 5(b) shows the transient voltage at various nodes of the design for read '1' [45].

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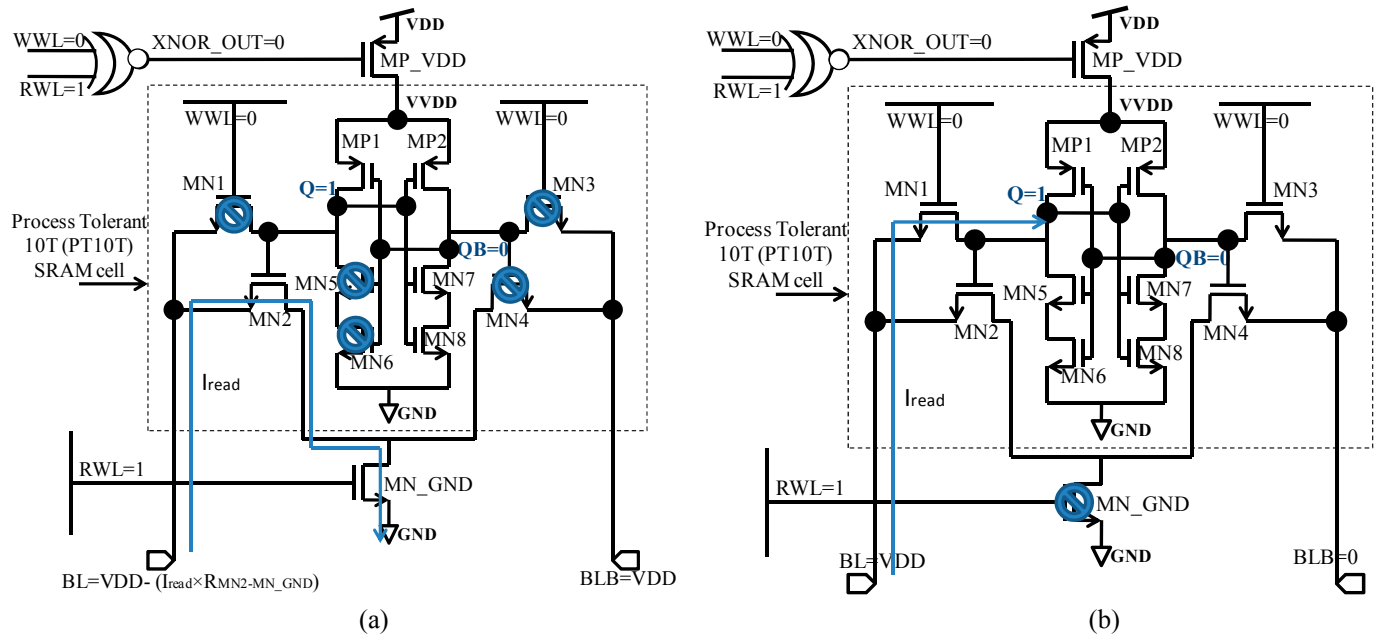

Figure 4 (a) State of read '1' operation in proposed 10T SRAM. (b) State of write '1' operation in proposed 10T SRAM. The power gated PMOS is turned ON for read-write operation.

C. Write operation

For write operation, *WWL* must be kept HIGH and *RWL* is at LOW. However, by making *WWL* (HIGH) and *RWL* (LOW); *XNOR_OUT* is switched to LOW value. The logic 1 is written to storage node *Q* through *BL-MN1-Q* as shown in Fig. 4(b*)*. However, the write '1' access time is measured as the time when *WWL* signal is activated and reaches to its VDD/2 value and storage node *Q* reaches to 90% of VDD value. Similarly, write '0' time is measured as the time when *WWL* signal is activated and reaches to its VDD/2 and storage node *Q* reaches to 10% of VDD. The half select issue in write operation is also taken care of by putting a *WE* signal at each column of SRAM array as shown in Fig. 3. By making read and write path separate using *WE* and *REB* the sensing and writing operations are separated which eventually helps to negate the half select read and write issue.

D. Data Retention

Generally, the memory cell remains in static or hold state at most of time. Therefore, there would be very high possibility of increase in leakage power in SRAM cell in different PVT conditions. In proposed PT10T SRAM, the control signal *XNOR_OUT*

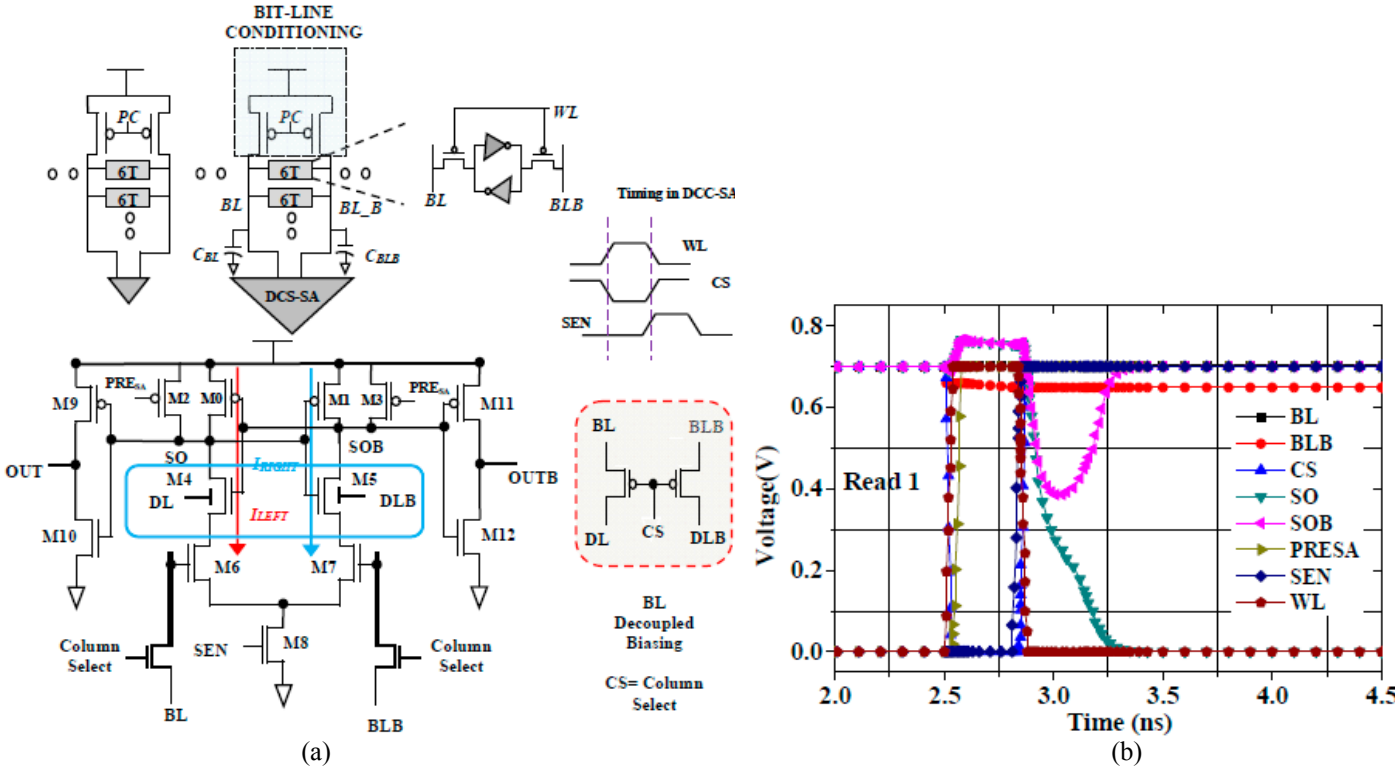

Figure 5 (a) Schematic of proposed DCC-SA with memory column [45]. (b) Simulated transient voltage at various nodes [45].

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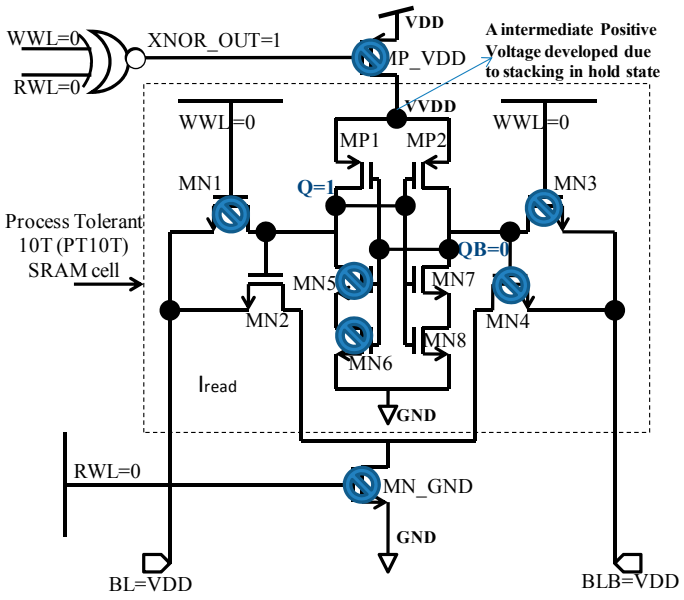

Figure 6. Architecture/Schematic of proposed 10T SRAM cell at hold mode.

turns OFF MP_VDD which helps to reduce the leakage current by disconnecting the path of the latch from VDD to GND. The leakage power in C6T SRAM cell introduces due to non-availability of virtual VDD transistor such as MP_VDD.The standby or leakage power dissipation is one of the major problems with embedded cache in sub-nanometer technology nodes. Leakage power is the major contributor to the total power consumption of SRAM, as most of the cells remain in the idle state. The leakage current has mainly three components, i.e. Gate leakage, Junction leakage and subthreshold leakage through different transistors [48]. If two devices are connected in series, then they form a stack and if one terminal of a stack is connected to VDD and the other end is connected to ground, and then the intermediate node rises to certain value, which is higher than the ground potential. In proposed SRAM at hold mode, the master transistor (MP_VDD) is turned OFF as output of the XNOR-gate is HIGH (due to both *WWL* and *RWL* are LOW). Therefore, the cross-coupled inverters are decoupled from the VDD and a stack is formed between MP1, MP2 and MP_VDD. Because of this effect, the intermediate node VVDD rises to some positive voltage [49]. This positive voltage reduces leakage and hold power during standby mode. However, in C6T and RD8T SRAM cells, there is a potential difference of VDD in-between VVDD and GND terminal. But due to the power gating of VDD the virtual node VVDD now set at a positive voltage VVDD lower than VDD, which eventually reduces the hold static noise margin (HSNM) but improves the leakage power at ultra-low power applications.

6. Simulation Results of PT10T SRAM

The proposed 10T SRAM is simulated in 65nm standard CMOS technology. Post layout simulation at 6-sigma (σ) process variations are observed and compared with C6T, RD8T, ST10T [39] and LP10T [44] SRAMs to determine various constraints like leakage power, read-write delay and power, power delay product (PDP), read static noise margin (RSNM), dynamic read margin (DRM), write static noise margin (WSNM) and write trip point (WTP). Further, all the listed constraints are observed at different temperature values ranging from 0˚C to 100˚C and at different process corners namely fast-fast (FF), slow-slow (SS), typical-typical (TT), slow-fast (SF) and fast-slow (FS) using 1000 Monte Carlo (MC) simulations

A. Simulation Setup

The simulation setup is observed through Monte Carlo post layout simulations on an 8Kb SRAM array. The read-write access time and power is measured by applying a write and read operation at single column of the array. The proposed SRAM macro has 64-bit column coupled with a DCC-SA. The DCC-SA is used as a sense amplifier which takes a small differential positive sensing voltage as an input and attains an output which is equivalent to the stored information in the SRAM cell. To read and write a read and write access transistor used to separate the read and write path. The row and column decoder are used to activate the *WWL* and *RWL* of the Marco. The setup for all operations is observed at the worst case process corner. The write and read operation are taken from *BL* and *BLB* of the SRAM. While reading the information from the SRAM the bit-lines are pre-charged to VDD using pre-charge (*PC)* signal. Further, all the observations are taken using 1000 Monte Carlo simulations.

B. Write and Read Analysis

The write ‘1’ access time is measured as the time when *WWL* signal is triggered and storage node *Q* reaches to 90% of VDD value. Similarly, write ‘0’ access time is defined as the time when WWL signal is activated and storage node *Q* reaches to 10% of VDD value. The write dynamic power is measured as the product of average current dissipation and the source voltage at the write access time. Additionally, Fig. 7(a) and 7(b) show the write ‘1’ and write ‘0’ delay observed at various supply voltages in the SS process corner, respectively. The delay is compared with existing cells like C6T, RD8T, LP10T [44] and LP9T [43], which shows that the proposed PT10T SRAM has similar write access time considering an overhead of a stacked p-MOS transistor. Similarly, Figure 8(a) and 8(b) show write ‘0’ and write ‘1’ dynamic power at various supply voltages, voltages in the FF process corner, respectively. The results obtained show an improvement in dynamic write ‘1’ power by 8.5%, 12.6%, 19.35% and 19.3%

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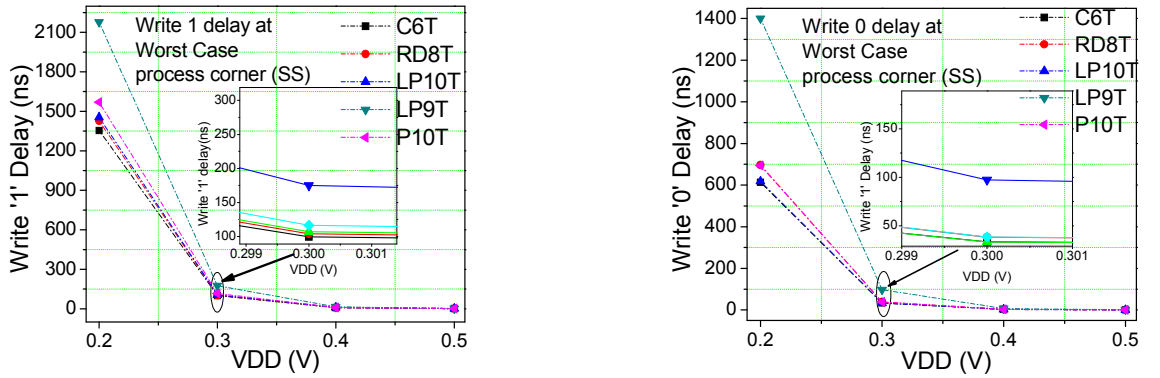
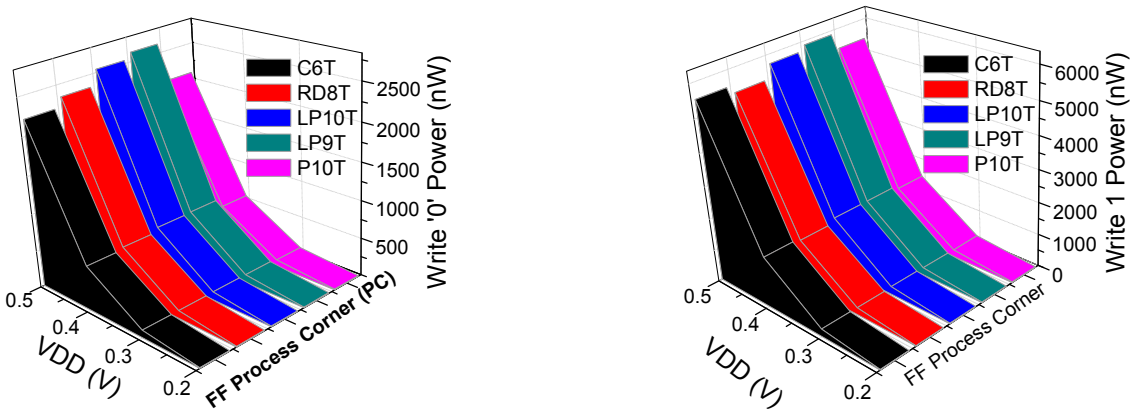
as compared to C6T, RD8T, LP10T [44] and LP9T [43] SRAM, respectively at 300mV supply voltage. The outcome achieved illustrates an enhancement in dynamic write '0' power by 5.2%, 1%, 10% and 6.6% as compared to C6T, RD8T, LP10T [44] and LP9T [43] SRAM, respectively at 300mV supply voltage.



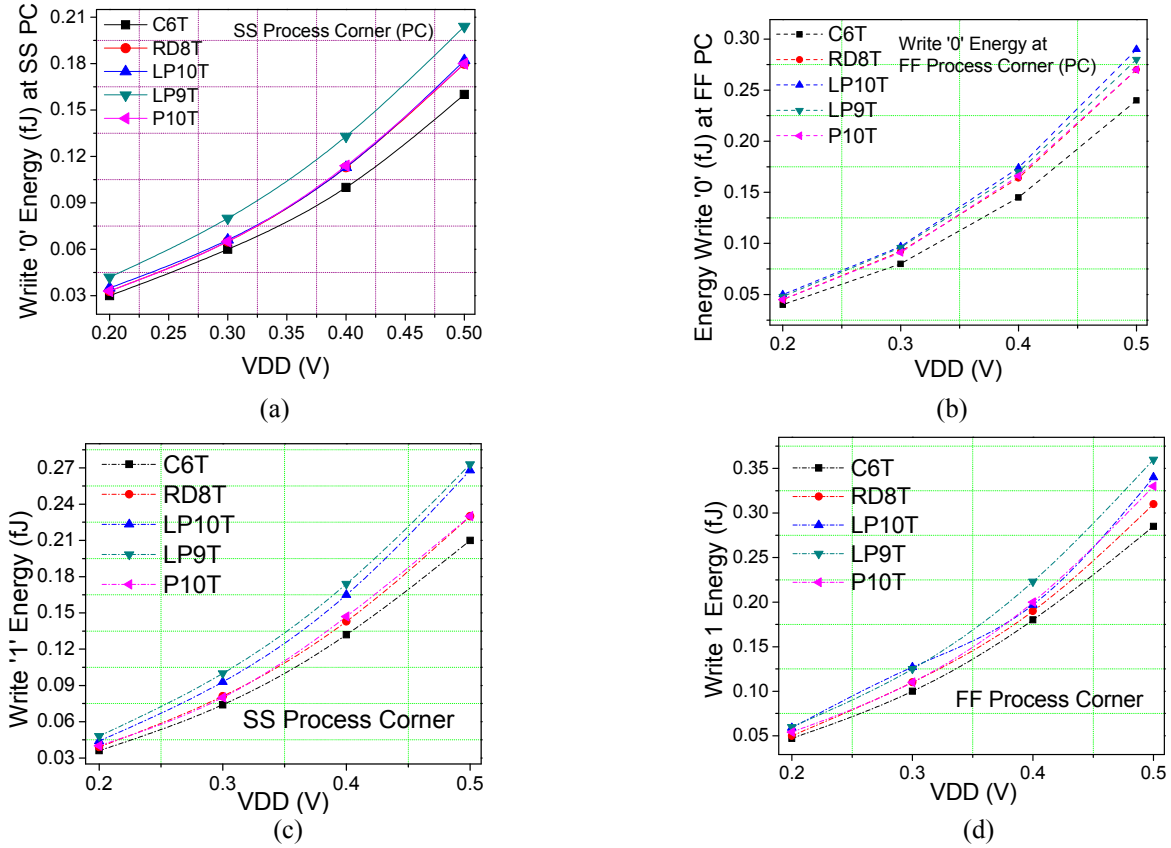
(a) (b)

Figure 7. (a) Write '1' delay, (b) Write '0' delay at slow-slow (SS) Process corner.



(a) (b)

Figure 8. (a) Write '0' power, (b) Write '1' power at fast-fast (FF) Process corner.



(a) (b) (c) (d)

Figure 9. (a) Write '0' energy at SS Process corner (b) Write '0' energy at FF Process corner (c) Write '1' energy at SS Process corner and (d) Write '1' energy at FF Process corner.

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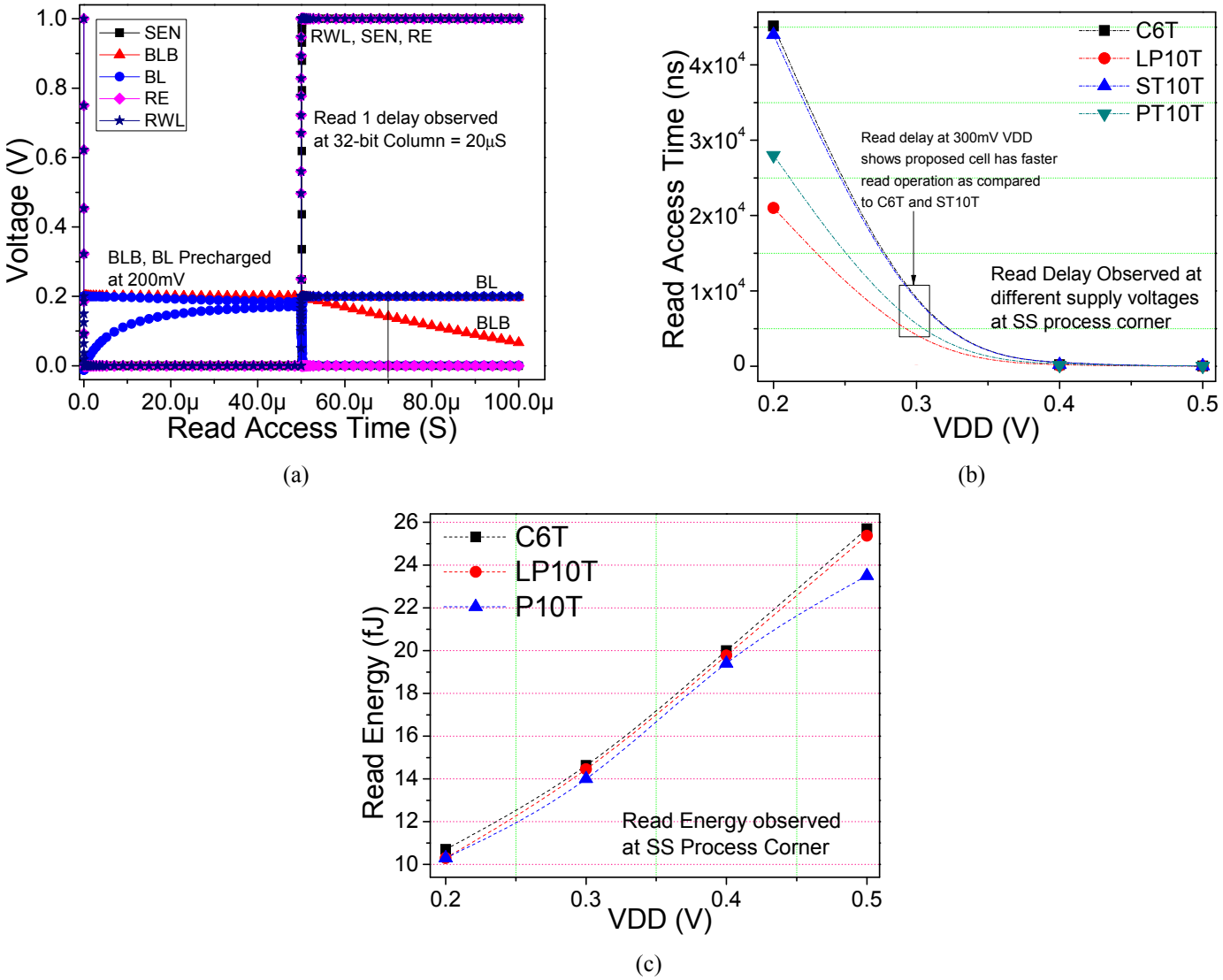

Figure 10. (a) State of input variables in read operation where micron (µ) is 10^{-6}, (b) Read access time at SS process corner at different supply voltages and (c) Read energy premeditated at different supply voltages.

Further, Fig. 9 shows the energy consumption of various SRAM cells at different supply voltages at SS and FF process corner in write '0' and write '1' operation. The results obtained show an improvement in write '1' energy by 1.23%, 14% and 20% as compared to RD8T, LP10T and LP9T SRAM, respectively at 300mV supply voltage. However, write'0' energy is improved by 1%, 6.2% and 5.2% as compared to RD8T, LP10T and LP9T SRAM, respectively at 300mV supply voltage. Furthermore, the read delay is measured when *RWL* is activated and precharged bit-lines discharges and reaches to the minimum sensing voltage required by SA [38-40]. In our proposed DCC-SA architecture [45-47], by estimating the read sensing voltage at worst case process corner, we examined a differential voltage of range 50mV-80mV required for generating an output signal to read data from SRAM. Fig 10(a) shows the simulation states of SRAM at read time. The proposed SRAM fast read access as compared to the existing SRAM cells as stated in Fig 10(b). However, the power measured until the time, where the difference of bitline voltage reaches to the sensing voltage is defined as a read power. Fig. 10(c) illustrates the plot of read energy and it can be observed that proposed SRAM have less energy consumption as compared to C6T and LP10T SRAM cells. The read access time of proposed SRAM is 1.6×, 1.57× better than that of C6T and ST10T [39] SRAM in SS process corner at 300mV VDD. In addition, the read energy of proposed cell is 4% and 3% better than C6T and LP10T SRAM in SS process corner at 300mV VDD.

C. Standby or Leakage power

Leakage current is measured as the current drawn from VDD to GND while the SRAM cell is in static or hold condition. The static power or leakage power is the amount of power dissipated at hold operation. Fig. 11(a) shows the leakage power variations w.r.t. the supply voltages for already existing and proposed SRAM. However, after determining the leakage power of proposed 10T SRAM comes out to be 10.5pW which is 0.012×, 0.013×, 0.93× of the C6T, RD8T and LP9T SRAM, respectively at 300mV VDD. In addition, Fig 11(b) shows the occurrences of leakage power variations of proposed cell at different supply voltages, which rationalize the peak value of leakage power at sub-100pW at different supply voltages. The spread of distribution curves of leakage power for C6T, RD8T and proposed 10T SRAM at various temperature values is shown in Fig. 12 (a), (b) and (c), respectively. It is observed that the spread of leakage power of C6T and RD8T SRAM has a wider range as compared to PT10T. The distribution curve articulates that in extreme PVT conditions the proposed SRAM has a tendency to overcome the leakage values and dissipate very low leakage power.

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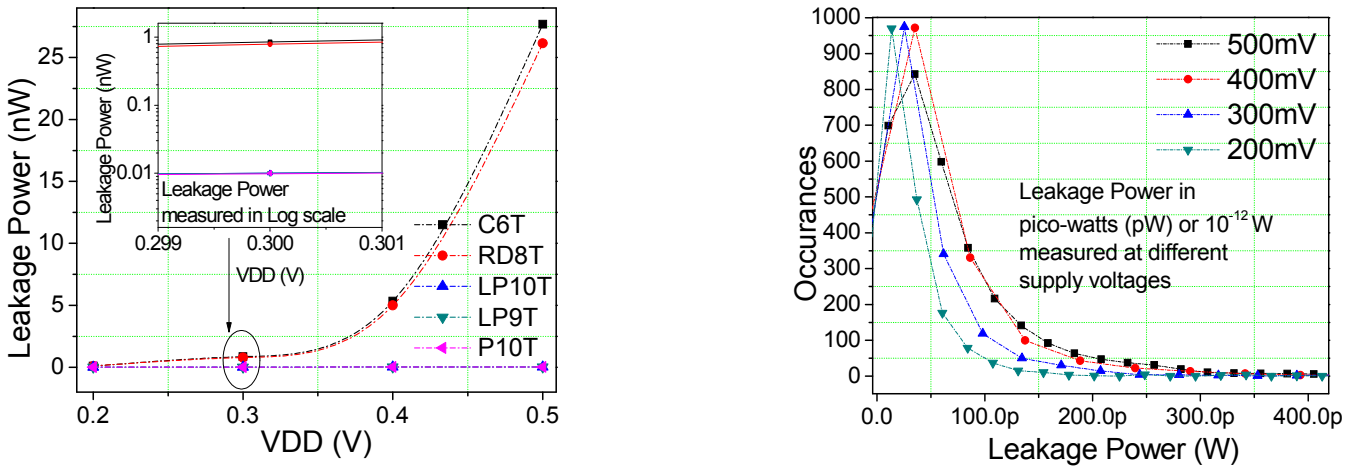
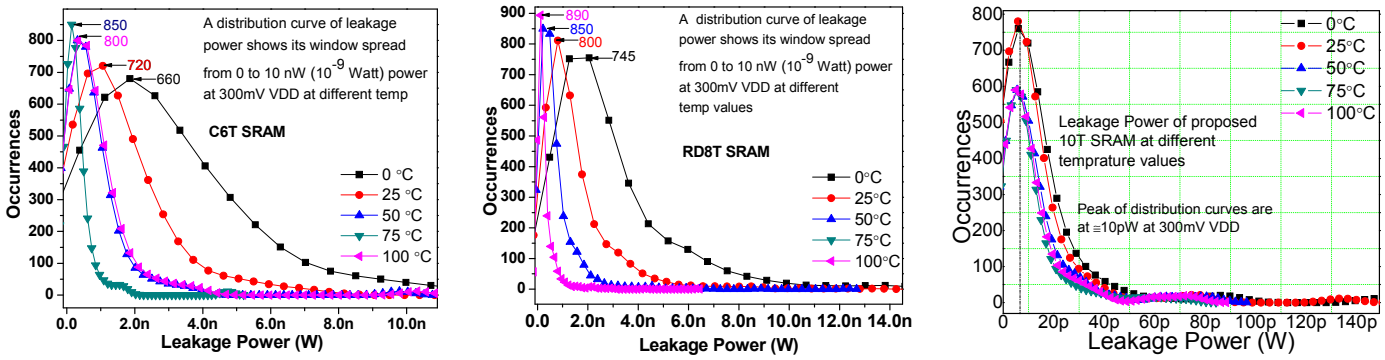


(a) (b)

Figure 11. (a) Leakage power at different supply voltages. (b) Distribution of leakage power of proposed SRAM at various supply voltages, where Pico (p) is 10^{-12} of unit.



(a) (b) (c)

Figure 12. (a) Distribution curves of leakage power of 6T SRAM. (b) Distribution curves of leakage power of RD8T SRAM at various temperature values at 300mV VDD. (c) Distribution curves of leakage power of proposed 10T SRAM at various temperature values at 300mV VDD. Where, Nano (n) is defined as 10^{-9} of unit and Pico (p) is 10^{-12} of unit.

D. RSNM and read margin

Read static noise margin (RSNM) is measured by applying a DC noise voltage source at one of the storage node *Q* or *QB* and investigating the effect on other storage node. The RSNM is examined in the read operation when *RWL* is HIGH and *WWL* is LOW. The decoupled read path through *BL-MN2-MN_GND* doesn't affects the storage nodes of the SRAM cell, which would further help to neglect the consequences of static noise and as a result, improves the RSNM. The RSNM of the proposed PT10T SRAM cell comes out to be 107mV, which has 3×, 1.48× and 1.48× improved values as compared to than C6T, RD8T and LP10T SRAM, respectively at 300mV VDD as shown in Fig. 13. Consequently, read margin is measured in a situation where there is no static DC noise hampered the storage nodes. While measuring read margin, the *RWL* is activated HIGH and *WWL* is kept at LOW. The read dynamic noise margin (RDNM) is observed when the *bitline* reaches to the sensing voltage. Simultaneously, the voltage difference between storage node *Q* and *QB* is defined as RDNM. In our case the RDNM value comes out to be equivalent to 290mV which is 7.5% better than C6T SRAM as shown in Fig. 14(a) and Fig. 14(b) at 300mV VDD.

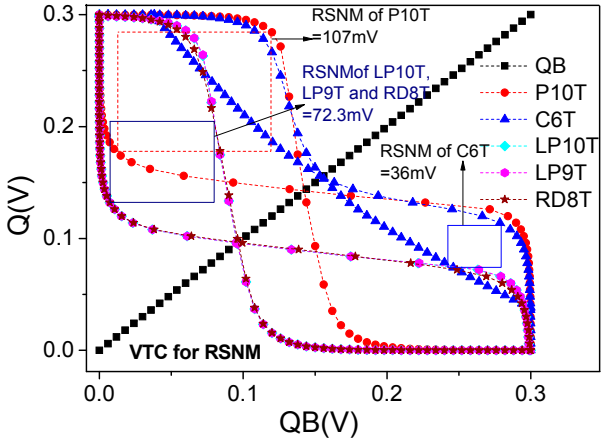


Figure 13. Read static noise margin (RSNM) of C6T, RD8T, LP10T and PT10T SRAM observed at 300mV VDD.

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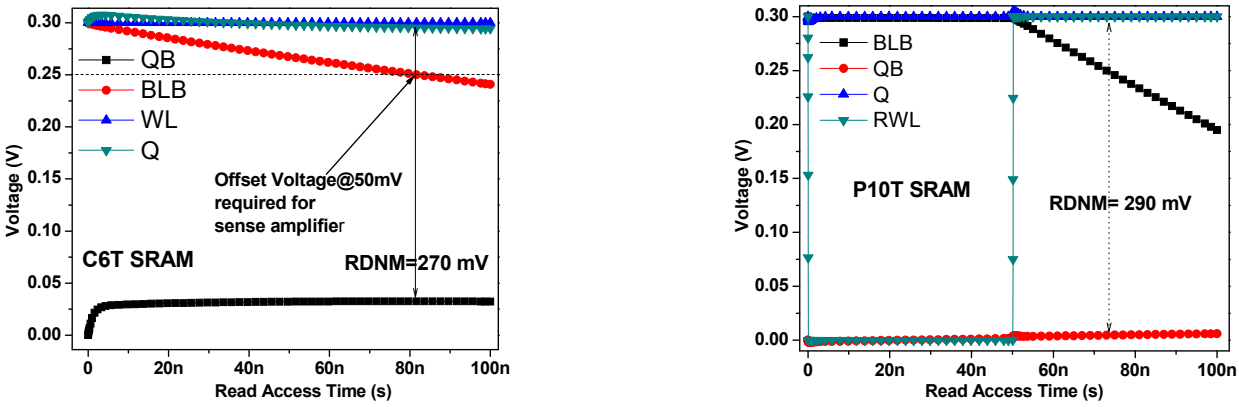
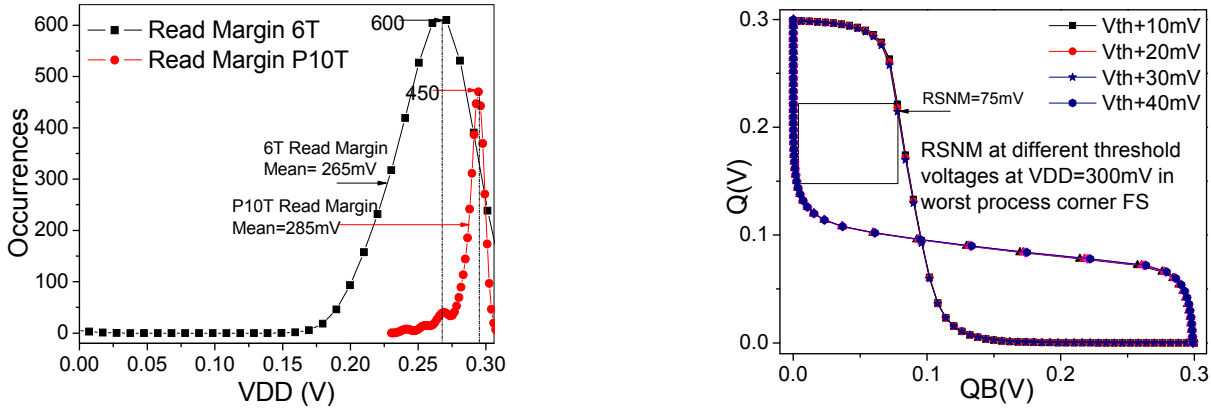


(a) (b)

Figure 14. (a) RDNM of C6T SRAM and (b) RDNM of proposed PT10T SRAM at 300mV VDD.



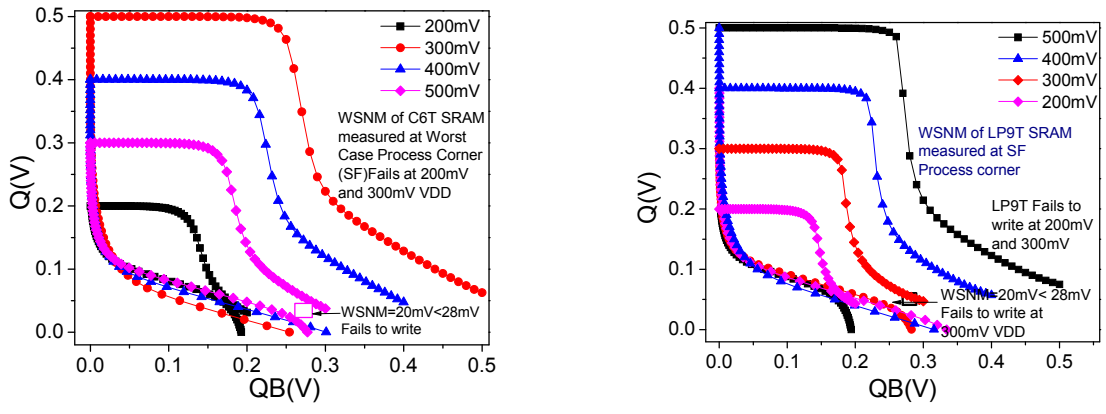
(a) (b)

Figure 15. (a) Distribution curves of RDNM of C6T and PT10T SRAM. (b) RSNM of proposed 10T SRAM at different threshold value of MN5 and MN6 at 300mV VDD.

In addition, In Fig. 15(a), the RDNM distribution curve is plotted using 1,000 Monte Carlo simulations which show that the proposed cell has an average dynamic read margin of 285mV which is 7.5% better than C6T (265mV) at 300mV. Further, in Fig. 15(b), the RSNM value is also observed at different threshold values. The threshold values of the pull down NMOS transistors MN5 and MN6 are varied and the value of RSNM experiential as 75mV at worst case process corner i.e., slow-fast (SF).

E. WSNM and Write Trip Point (WTP)

The write static noise margin (WSNM) is measured at the time of write operation by initiating a linear DC noise at one of the storage nodes and observing the effect of the noise at the other end. The *WWL* is kept HIGH, the *RWL* is LOW. The plots in Fig. 16(a), Fig. 16(b), Fig. 17(a) and Fig. 17(b) determines the WSNM of C6T, LP9T, LP10T and PT10T SRAMs at worst case (SF) process corner. Besides, from Fig. 16(a) and 16(b), it is observed that the WSNM of C6T and LP9T SRAM has fail to write at 200mV and the WSNM is 20mV at 300mV VDD which is less than the thermal voltage (~28mV), and therefore it not good practice to operate at 300 mV VDD. However, the LP10T has a WSNM value of 10mV at 200mV VDD and 30mV at 300mV VDD, consequently it fails to work at 200mV and has near threshold value at 300mV (WSNM=30mV). Therefore, it is suggested to operate LP10T SRAM above 300mV supply voltage. Furthermore, the proposed 10T SRAM has a WSNM value of 21mV at 200mV VDD and 40mV at 300mV VDD, which shows that PT10T can't able to operate at 200mV VDD, but can work at 300mV VDD. It also shows 2×, 2× and 1.5× better WSNM values as compared to C6T, LP9T and LP10T SRAM at 300mV VDD, respectively.



(a) (b)

Figure 16. WSNM (a) C6T SRAM and (b) LP9T SRAM at different supply voltages in worst case slow-fast (SF) process corner.

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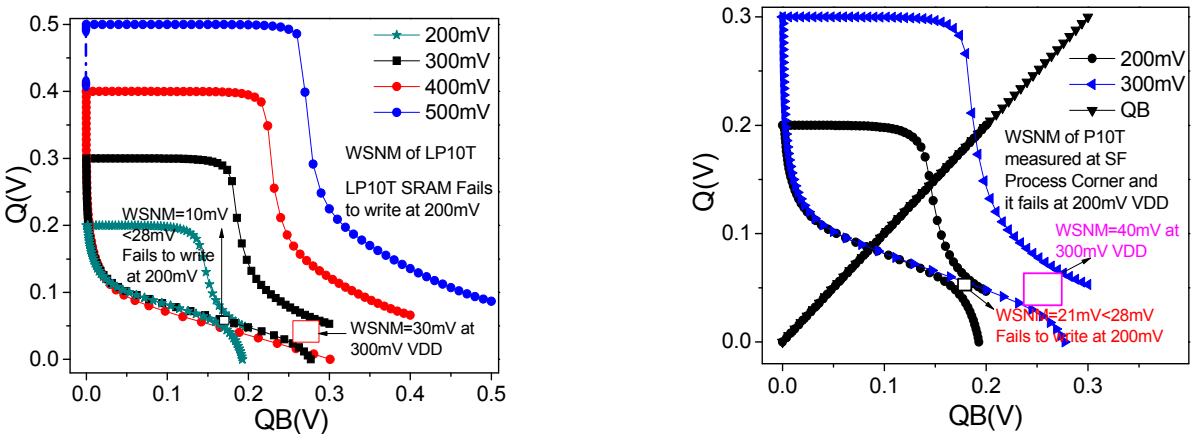

Figure 17. WSNM (a) LP10T SRAM and (b) Proposed PT10T SRAM at different supply voltages in worst case slow-fast (SF) process corner.

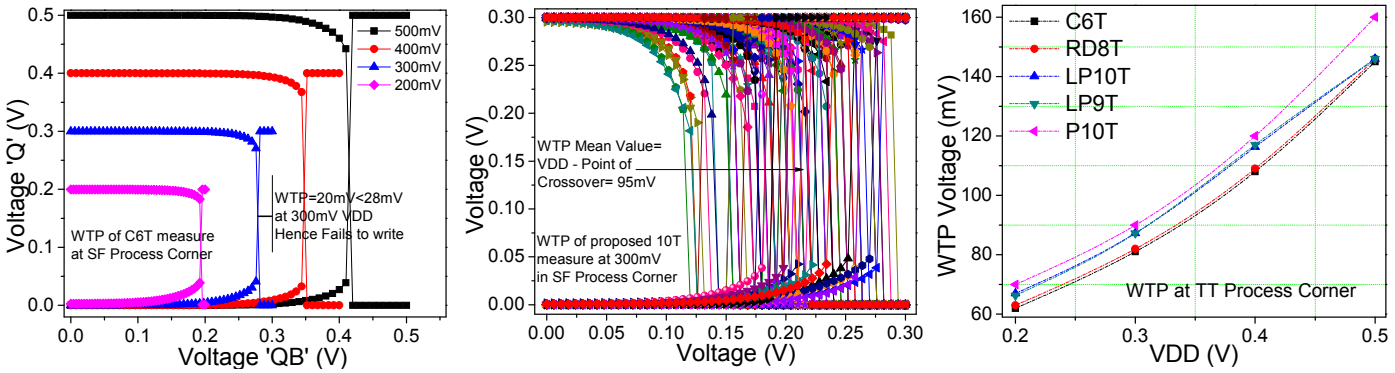

Figure 18. (a) WTP measurement of C6T SRAM at 300mV in SF process corner, (b) WTP measurement of proposed 10T SRAM at 300mV in SF process corner and (c) Comparison of various WTP values at different VDD in TT process corner.

Further, the write trip point (WTP) is measured at the time of write operation while *WWL* asserted HIGH and *RWL* is LOW. It is observed by two methods one by adding a linear variable DC voltage source at *BL* and observing its effect on the *BLB* and other by varying *WWL* and writing through the *BL* and *BLB* [50]. The WTP, when *WWL* is varied is observed at the crossover point of *Q* and *QB* as shown in Fig. 18(a) and comes out to be 20mV for C6T SRAM and 95mV for proposed 10T SRAM as shown in Fig. 18(b) which is 4.75× better than C6T SRAM at 300mV VDD in the worst case (SF) process corner. However, the WTP is compared at different supply voltages in the TT process corner as shown in Fig. 18(c). It shows that the proposed SRAM has 11%, 9.75%, 3.3% and 3.4% better WSNM as compared to C6T, RD8T, LP10T and LP9T SRAM, respectively at 300mV VDD.

F. Half selected issue

Half-selected column and row cells require a careful investigation under write and read operation [51]. As in proposed cell read operation is done by decoupling logic, therefore there would be no effect of row half select read issue on storage nodes as shown in Fig. 19(a). Fig. 19(b) shows the column half select read under read operation when the bitlines are selected for read and *RWL* is activated HIGH. As we know that the only single cell is selected for read operation among 64 SRAM cells in a column, which introduces a noise in either storage node for C6T SRAM.

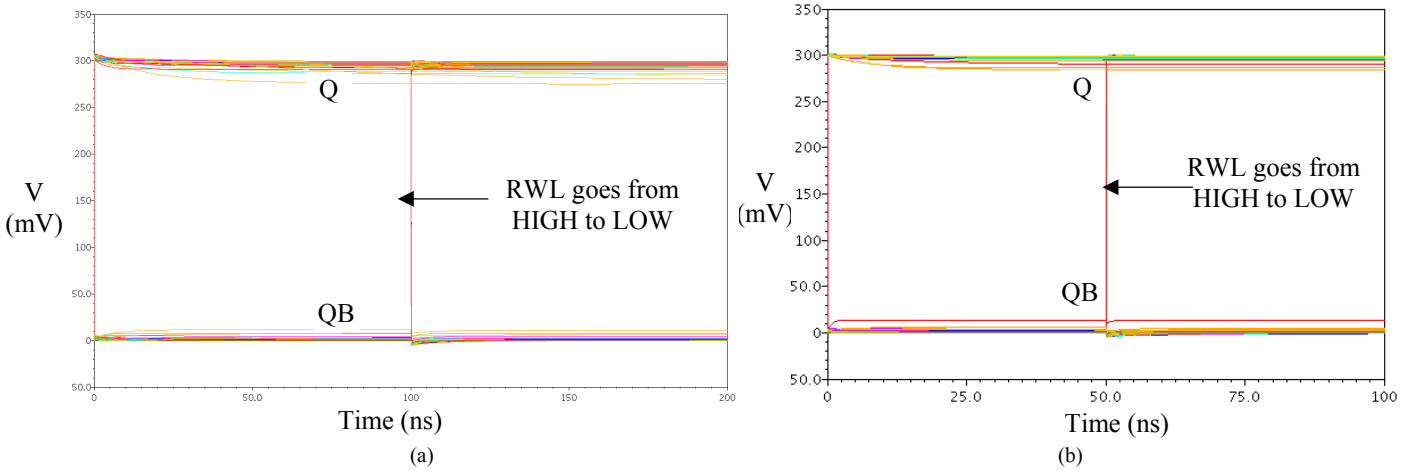

Figure 19. P10T SRAM (a) Row half select read and (b) Column half select read at 300mV VDD.

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The column half select write and row half select write operation processed at 1,000 MC simulations are shown in Fig. 20(a) and 20(b), respectively. The proposed cell shows that due to half select issue in write operation there is a slight bump of noise formed at the storage node as shown in Fig. 20(a) and 20(b). The noise is generated due to differential write operation through *BL* and *BLB* when *WWL* is activated to HIGH and *RWL* is deactivated. However, it shows that the storage node attains its original value when *WWL* is deactivated.

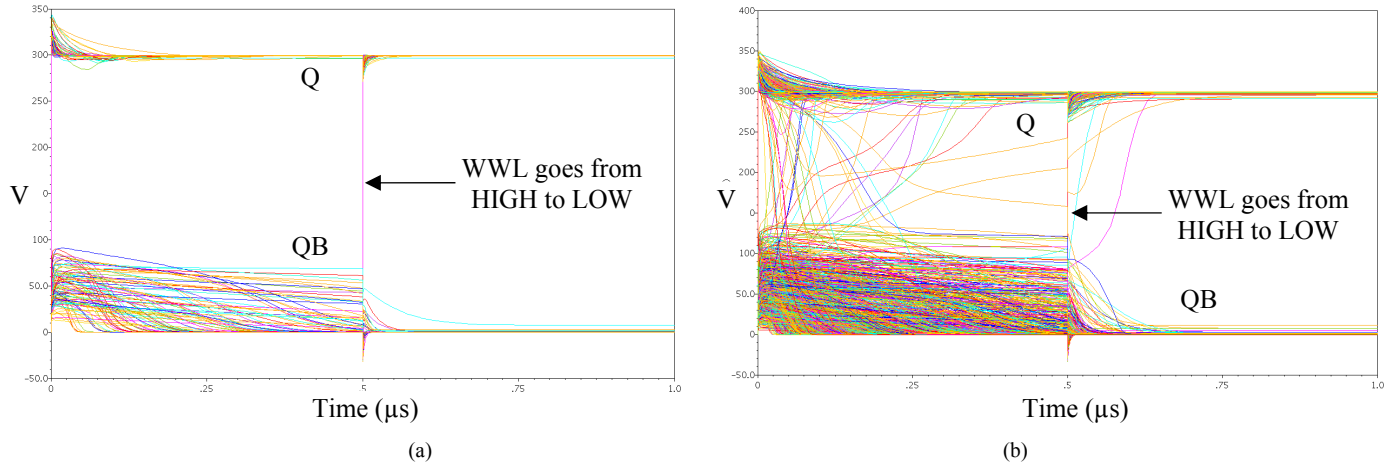

Figure 20. P10T SRAM (a) Row half select write and (b) Leakage power of C6T SRAM at 300mV VDD.

Table IV
Summary of mean (µ) value of simulation results of proposed PT10T SRAM in Standard 65-nm CMOS Technology in 6σ process variance at 300mV VDD in room temperature 27°C conditions

SRAM	WSNM at SF Process Corner (mV)	RSNM at TT Process Corner (mV)	RDNM at TT Process Corner (mV)	WTP at TT Process Corner (mV)	Leakage Power at TT (pW)	Write '1' Energy at FF (pJ)	Read '1' Energy at SS (fJ)
C6T	20	36	220	81	850	**100**	14.63
RD8T	32	72.3	**299.5**	82	786	110	19.5
LP9T	20	72.3	295	87.3	**11.3**	125	15.5
LP10T	30	72.3	**299**	87.25	**10.1**	127	14.45
ST10T	35	103	268	82	583	133	14.5
PT10T	**40**	**107**	290	**90**	**10.5**	110	**14**

7. Result Summary and Conclusion

This paper proposes a robust ULP process tolerant 10T SRAM cell for low power Internet of Things (IoT) applications. The low voltage operations put a stringent concern towards variation tolerant ultra-low power memory design. However, the low leakage and high read/write stability of proposed cell at different process variations makes proposed cell as leading alternative over the conventional memory cells for IoT applications. In proposed process tolerant 10T (PT10T) SRAM, various parameters are observed under different process voltage and temperature (PVT) values. The proposed SRAM uses power gating technique to reduce the standby power at the cost of low hold static noise margin (HSNM). The proposed cell also has a tremendous improvement in RSNM, WSNM and WTP values as compared to the existing SRAMs .i.e., C6T, RD8T, LP9T, LP10T and ST10T SRAM. The proposed cell has shown significant improvement in total static and dynamic power, the read-write energy values shows the slight development as compared to existing SRAMs. The proposed cell used differential current controlled-sense amplifier (DCC-SA) to sense the required minimum sensing voltage across the bitlines. The DCC-SA has shown remarkable performance in terms of sensing speed and read access time with better robustness. The DCC-SA also has a better yield as compared to conventional current mode SA. This property of DCC-SA helps us to generate a required output with better read access time, which eventually improves the processor frequency. The summary of our proposed 10T SRAM is shown in Table IV.

Table IV shows the summary of post-layout simulation results of proposed PT10T SRAM cell based 8-Kb SRAM array at 300mV power supply. The parameters are observed at 27˚C room temperature in the worst case process corner, where all transistors are taken as low-V_{th} transistors. Table IV shows that the proposed 10T SRAM has 1/81×, 1/75×, 1/1.07× and 1/55× lower leakage power as compared to C6T, RD8T, LP9T and ST10T SRAM, respectively. The WSNM value is improved by 200%, 25%, 200%, 33.33% and 14.3% as compared to C6T, RD8T, LP9T and ST10T SRAM at worst case (SF) process corner, respectively. The RSNM value is enhanced by a factor of 3×, 1.48×, 1.48×, 1.48× and 3.88% as compared to C6T, RD8T, LP9T and ST10T SRAM at TT process corner, respectively. The dynamic read margin determined at the time of read operation and the dynamic read margin values showed 31.8% and 8.2% improved values as compared to C6T and ST10T SRAM, respectively. Moreover, the WTP is also improved by 11.11%, 9.75%, 3%, 3%, and 9.75% as compared C6T, RD8T, LP9T and ST10T SRAM at TT process corner, respectively. The write '1' energy is reduced by 12%, 13.38% and 17.3% as compared to LP9T, LP10T and ST10T SRAM at worst case (SS) process corner, respectively. However, the read '1' energy is reduced to 4.3%, 28.2%, 9.67% and 9.63% as compared to C6T, RD8T, LP9T and ST10T SRAM at worst case (SS) process corner, respectively.

On the other hand, if we consider the cell layout area the proposed cell has 35% and 12.5% more area overhead as compared to C6T and RD8T SRAM cell. Moreover, from the comparison between the layout area of proposed cell and other 10T SRAM cell, namely LP10T and ST10T SRAM, it is observed that our proposed cell shows better performance in terms of leakage power and at the lower cost of fabrication and has a higher density as compared to ST10T and LP10T SRAM. Therefore, the proposed 10T SRAM has emerges as an attractive choice for today's battery operated IoT enabled system on chip (SoC) applications, where the leakage power consumption and the cell stability are of primary concerns.

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