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Review

High Speed All-Optical Logic Gate Using QD-SOA and its Application

Hongyu Hu[1*], Xiang Zhang[1], and Shuai Zhao[2]

[1] Department of Physics, University of Connecticut, 2152 Hillside Road, U-3046, Storrs, CT 06269, USA

[2] Giner Inc, 89 Rumford Avenue, Newton, MA 02466, USA

*Corresponding author: hongyu.hu@uconn.edu

Abstract: The scheme to realize high speed (~250Gb/s) all-optical Boolean logic gates using semiconductor optica amplifiers with quantum-dot (QD-SOA) is introduced and analyzed in this review. Numerical simulation method was presented by solving the rate equation and taking into account nonlinear dynamics including carrier heating and spectral hole-burning. Binary phase shift keyed (BPSK) signal and on-off keyed signal are used to generate high speed all-optical logic gates. The applications based on all-optical logic gates such as, all-optical latches, pseudo random bit sequence (PRBS) generation and all-optical encryption, are also discussed in this review. Results show that the scheme based on QD-SOA is a promising method for the realization of high speed all-optical communication system in the future.

Key Words: QD-SOA; All-optical logic gates; PRBS; All-optical latches; All-optical encryption

1. Introduction

In future high-speed optical communication systems, logic gates will play important roles, such as signal regeneration, addressing, header recognition, data encoding and encryption [1]. In recent years, people have demonstrated optical logic using different schemes, including using dual semiconductor optical amplifier (SOA) Mach-Zehnder interferometer(MZI) [2, 3], semiconductor laser amplifier (SLA) loop mirror [4], ultrafast nonlinear interferometer (UNI)[5], four-wave mixing (FWM) in SOA [6] and cross gain (XPM)/cross phase (XPM) modulation in nonlinear devices [7]. Among above schemes, the SOA based MZI has the advantage of being relatively stable, simple and compact. However, optical logic gates have been demonstrated at 40 Gb/s [8] and demultiplexing at 160 Gb/s [9] using regular SOA based Mach-Zhender interferometer. In order to realize higher speed data processing, faster device and schemes are needed. The emergence of semiconductor optical amplifiers with quantum dot active region, i.e. QD-SOA, in recent years, provides a faster device for signal processing. QD-SOAs have high saturated output power, low noise figure [10], fast carrier relaxation rate between QD energy states [11, 12] and a much smaller carrier heating impact on gain and phase recovery times [13] which makes them suitable for high speed Boolean logic operations.

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The current optical communication system does not work entirely in optical domain. A larger amount of the switches and data processors are made of electrical circuits which limits the ultimate speed of the existing lightwave transmission system. One promising solution is all-optical packet switching networks in which the header recognizing, payload processing, buffering, and forwarding of optical packets are all carried out in the optical domain, bringing together the wide fiber bandwidth and high routers forwarding capacity [14]. In addition, the security of information is very important and all-optical encryption and decryption can be used to protect the information for future all-optical communication system. The key building blocks of optical switching and encryption are the all-optical Boolean logic gates, include XOR, AND, OR, NAND, NOT and functional circuits built using these gates such as optical latches. Thus, it is very important to build all-optical logic gates capable for high speed and high output quality.

In order to further enhance operation speed of all-optical logic gates, besides using QD-SOA, the other method involves in the use of two-photon absorption (TPA) effect which is an ultrafast nonlinear process of SOA. With a high intensity pump light injected into SOA, a fast changing TPA induced phase shift becomes dominant in the total phase change experienced by a weak probe signal. As a result, the SOA will quickly respond to the injected short pulse in the active region which makes it suitable for high speed operation. Several researches have demonstrated that all-optical logic gates based on TPA effect in common bulk SOA are capable of handling data at speed up to 250Gb/s [15-17]. However, the method using TPA effect needs a very high intensity pump light usually with ultrashort pulse width [18-20] which increases the expense and complexity of practical all-optical system. In order to obtain better output quality of all-optical logic gates, binary phase shift keyed (BPSK) signal instead of on-off keyed (OOK) signal can be used to realize all-optical logic gates. Because binary phase shift keyed (BPSK) signals carry information on the phase part while keeping the amplitude as a constant, the impairments from optical nonlinear effects and amplified spontaneous emission are greatly reduced.

2. All-optical logic gates based on QD-SOA

In this part, a model which simulates two QD energy level carrier dynamics and nonlinear effects affecting the gain spectrum of the device is presented. Using this model, a more accurate simulation of fast all-optical logic gates including AND, XOR and NOT is provided. The effect of device induced ASE noise is also discussed.

2.1. QD-SOA structure and rate equations

The commonly used QD-SOA is InAs/GaAs QD-SOA, with InAs Stranski-Krastanov (SK) quantum dots embedded in GaAs layer [21, 22]. This

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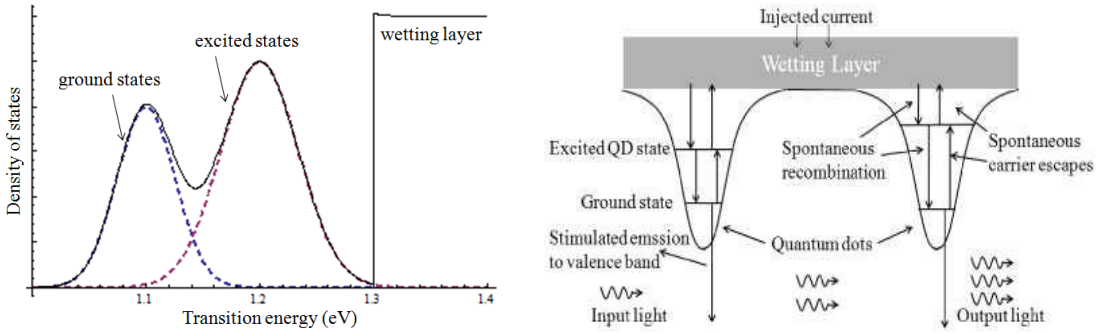
type of device can provide ~15dB gain at wavelength 1550nm with noise figure as low as 7 dB [12]. The active layer of the device consists of alternately stacked InAs island layers and GaAs intermediate layers. This configuration can significantly increase areal dot density and the modal gain of the SOA [18] and the gain is nearly polarization independent [23]. The density of state of the InAs/InGaAsP/InP QD-SOA [24] is shown in Figure 1 (a). From the graph, we see the carriers in the QD's are mostly populated on two groups of almost discrete energy levels (simplified here as two discrete states: QD ground state and QD excited state). The wetting layer has a continuous set of energies, supplying the two levels with carriers through interstate transitions and is able to refill itself using external electric current injection. The transition among the wetting layer, the QD excited state (ES) and the QD ground state (GS) is schematically illustrated in Figure 1 (b). The GaAs layer is the "wetting layer" in Figure 1 which used to feed the ground state and excited state with carriers through interstate recombination. External current is applied to the device and mostly accumulated in the wetting layer.



(a) (b)

Figure 1 (a): The QD-SOA density of states as a function of transition energy. (b): The transition diagram of InAs/InGaAsP/InP QD-SOA.

Rate equations are used to describe gain and phase dynamics in QD device [25]. The carrier density dynamics can be described as:

$$\frac{dw}{dt} = \frac{I}{eVN_{wm}} - \frac{w}{\tau_{wr}} - \frac{w}{\tau_{w-e}}(1-h) + \frac{N_{esm}}{N_{wm}}\frac{h}{\tau_{e-w}}(1-w) \quad (1)$$

$$\frac{dh}{dt} = -\frac{h}{\tau_{esr}} + \frac{N_{wm}}{N_{esm}}\frac{w}{\tau_{w-e}}(1-h) - \frac{h}{\tau_{e-w}}(1-w) + \frac{N_{gsm}}{N_{esm}}\frac{f}{\tau_{g-e}}(1-h) - \frac{h}{\tau_{e-g}}(1-f) \quad (2)$$

$$\frac{df}{dt} = -\frac{f}{\tau_{gsr}} - \frac{f}{\tau_{g-e}}(1-h) + \frac{N_{esm}}{N_{gsm}}\frac{h}{\tau_{e-g}}(1-f) - \frac{\Gamma_d}{A_d}a(2f-1)\frac{1}{N_{gsm}}\frac{S(t)}{\hbar\omega} \quad (3)$$

Where w, h and f are the occupation probabilities of the wetting layer, the QD excited state and ground state, respectively; Nwm, Nesm and Ngsm are the maximum possible carrier densities of each state; Γ_d is the active layer confinement factor, I is the injected current, V is the effective volume of the active layer, a is differential gain, S(t) is photon density in the active region.

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The gain dynamics in the QD-SOA include the contribution from the carrier density pulsation dynamics and nonlinear processes including carrier heating (CH) and spectral hole-burning (SHB) effect. Generally, the linear part of gain coefficient is based on the stimulated emission from the QD ground state to the valence band,

$$g_l = \Gamma_d a(N_g - N_t) \tag{4}$$

Where N_t is the transparent carrier density of the QD ground state. The suppression of the gain coefficient brought by nonlinear CH and SHB effects can be expressed as:

$$g(t) = g_l + \Delta g_{CH} + \Delta g_{SHB} \tag{5}$$

To a first approximation, Δg_{CH} and Δg_{SHB} are proportional to instantaneous light intensity $S(t)$.

$$\Delta g_{CH} = -\varepsilon_{CH} g S(t) \tag{6}$$

$$\Delta g_{SHB} = -\varepsilon_{SHB} g S(t) \tag{7}$$

Where ε_{CH} and ε_{SHB} are the gain suppression factors of carrier heating and spectral hole burning effect, respectively. From equations (5) to (7), we can get [26]:

$$g(t) = \frac{a(N - N_t)}{1 + (\varepsilon_{CH} + \varepsilon_{SHB}) S(t)} \tag{8}$$

The injected light and changed temperature result from carrier heating also changes the refractive index of the active region, and thus a phase change to any probe wave injected.

$$\phi(t) = \frac{1}{2} (\alpha G_l(t) + \alpha_{CH} \Delta G_{CH}(\tag{9}$$

Where $G_{l(t)} = e^{g(t)l}$ is the gain factor of the device with l being the effective length of the active layer, α and α_{CH} are the linewidth enhancement factor of the device.

2.2. Principles of QD-SOA-MZI based all optical logic gates

A QD-SOA based Mach-Zehnder Interferometer can be used to realize all-optical XOR, AND, NOT operations. As is shown in Figure 2, two identical QD-SOAs are in the two arms of the interferometer, three optical data streams carried by different wavelengths are injected into the two arms, where the control beam at λ_2 is symmetrically split into two branches at port C and guided into the two arms separately. The two beams then interact with data stream A, B and will experience a modulated gain and phase via XGM and XPM processes.

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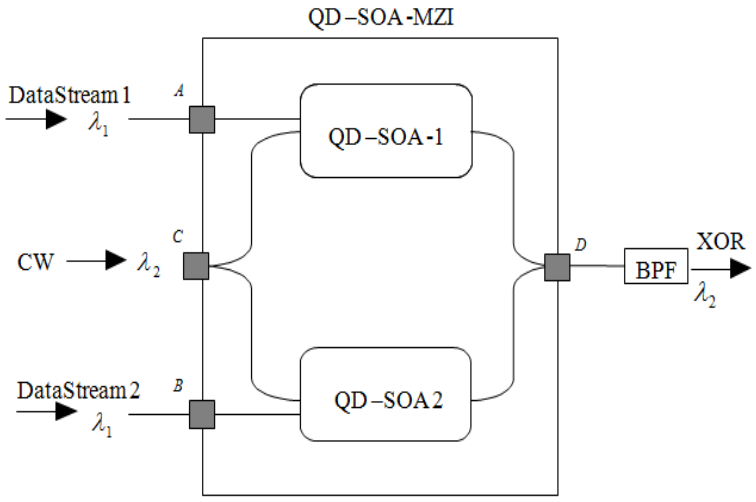

Figure 2 Schematic of a QD-SOA based Mach-Zehnder Interferometer. BPF: bandpass filter (central wavelength λ_3)

The light in two beams will combine and interfere at port D, after screening the other wavelengths using a band-pass filter (BPF), the output power at wavelength λ_2 can be expressed as:

$$P_{out} = \frac{P_{cb}}{4}[G_1(t) + G_2(t) + 2\sqrt{G_1(t)G_2(t)}\cos(\phi_1(t) - \phi_2(t) + \phi_0)] \quad (10)$$

Where P_{cb} is the control beam power at port C, we can tune the initial phase difference between the two arms φ_0 by (for example,) adding a tunable phase shifter in one of the arms. For our logic gates used here, we typically tune $\varphi_0 = \pi$ so that equation (10) becomes:

$$P_{out} = \frac{P_{cb}}{4}[G_1(t) + G_2(t) - 2\sqrt{G_1(t)G_2(t)}\cos(\phi_1(t) - \phi_2(t))] \quad (11)$$

XOR logic gate: Set control beam as clock wave at the same repetition rate as data A and B, the QD-SOA MZI will function as a XOR logic gate. When A = B = 0 or A = B = 1, the control beams in each arm will see the same cross gain or phase modulation as they go through the QD-SOA. And the output branches of the control beam will have a destructive interference pattern at output because of the initial π phase difference, and the output will be 0 at wavelength λ_2. When A and B are not the same, the branches of control beam will undergo different gain, we can have a constructive interference at output port if we can change the power of modulating data streams A and B to make $\varphi_1(t) - \varphi_2(t) = \pi$, in this case the output will be 1 for wavelength λ_2.

AND logic gate: In order to realize AND operation, a scheme similar to Dong's [27] can be used: data A and a continuous wave (CW), both at wavelength λ_1, are injected into each of the two QD-SOAs. Set the power of the CW so that it is the same as the average background optical power to balance the gain and phase impact from the "0" data components, data stream C at wavelength λ_2 is injected to both arms as control beam, this configuration will provide a process which gives "1" at output at λ_2 only when both data A and C is "1", functionally the same as all optical AND gate.

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NOT logic gate: Similar to XOR gate, if we change data stream B into a clock wave at wavelength λ_1, we will have the setup of an all-optical NOT logic gate, which gives inversed value of data stream A at wavelengthλ_2 at the output.

2.3. The role of amplified spontaneous emission (ASE) noise

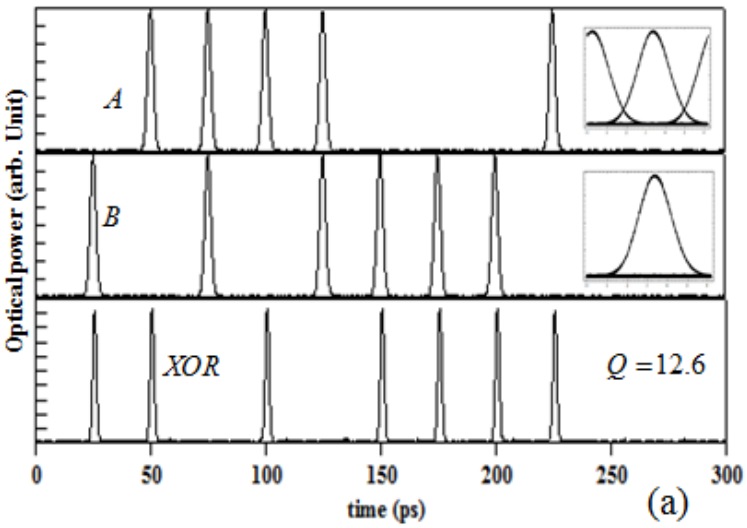
As the pulse trains go through the amplifier, spontaneous emission will be added to the initial wave pattern in the form of white noise. This noise will reduce the signal to noise ratio, the effect is quantitatively described by the noise figure of the amplifier:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{12}$$

With SNR_{in} *and* SNR_{out} are corresponding to the signal to noise ratio at the input and output, respectively.

2.4. Simulation results and output quality study

The simulated result can be obtained by solving rate equations (1-3) and setting input light beam power within non-saturated regime. Results of XOR, AND, OR logic operations are shown in Figures 3, 4 and 5, respectively [28], 2^7-1 PRBS data signals are used as input. The output eye-diagram is also plotted as inset in each figure to show qualitatively the output quality. Quantitative quality evaluation can be done using quality factor method, as described below.



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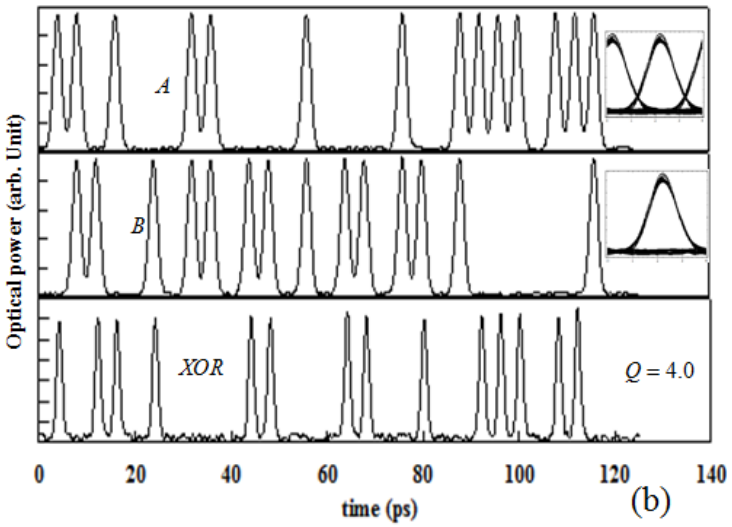

Figure 3 A side-by-side comparison of XOR result for (a) 40 Gb/s and (b) 250 Gb/s XOR operation, insets are the simulated eye-diagram of the output wave.

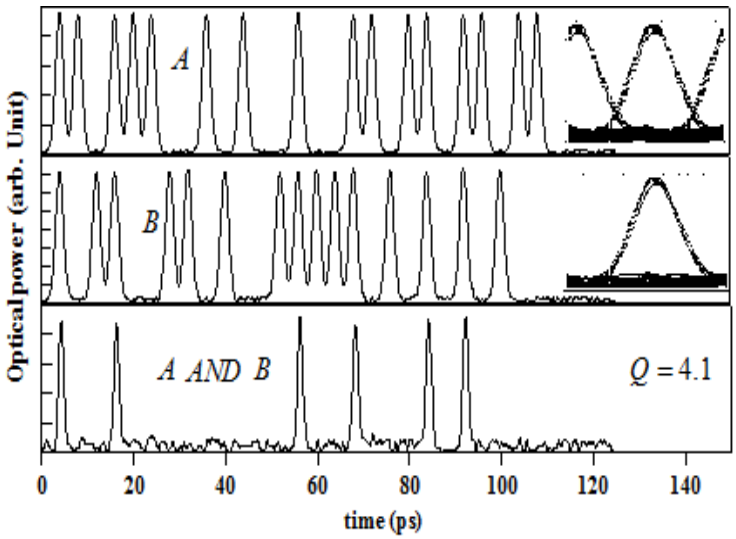

Figure 4 Simulated result for all-optical AND gate operating at 250 Gb/s. Insets are eye diagrams and corresponding quality factor Q for output wave.

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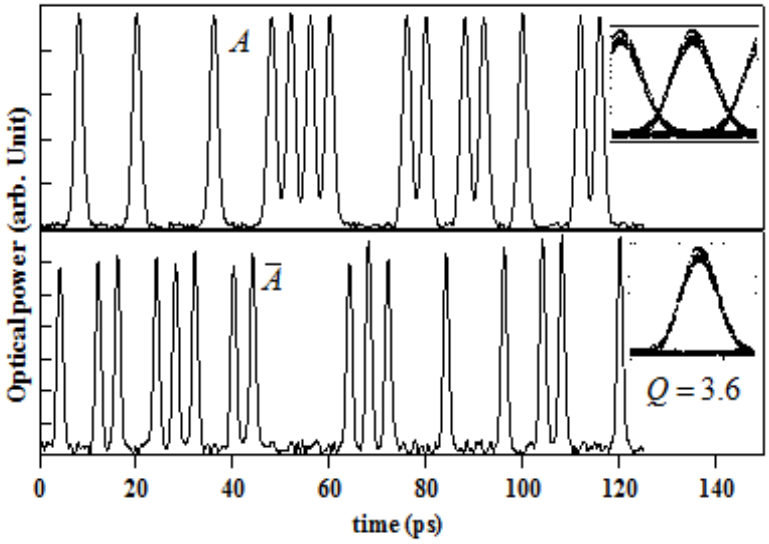
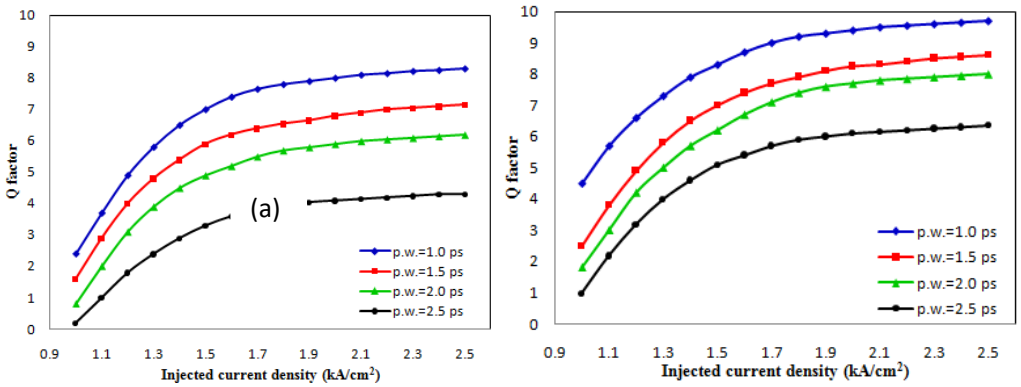


Figure 5 Simulated results for all-optical NOT gate operating at 250 Gb/s. Up: data stream A, down: inverted A, insets are eye diagrams and corresponding quality factor Q for output wave.

The quality factor for the output data waveform can be expressed as, $Q=(S_1-S_0)/(\sigma_1+\sigma_0)$where $S_1$and $S_0$are the average value for all the out coming "1" and "0" data's peak power, respectively; σ_1 and $\sigma_0$are their standard deviations. The quality factor is related to the gate's bit-error rate (BER) in terms of $\text{BER} \approx \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}}$.

Since the mechanism for the three different types of logic gates are basically the same, similar output quality for different gates can be obtained at a certain repetition rate. And the quality of this scheme is evaluated without relating to any specific logic operation.



(a) (b)

Figure 6 Calculated operation quality factor Q at different pulse width and injected current density, single pulse energy is set to 0.5 pJ. (a): 250 Gb/s XOR operation (b): 160 Gb/s operation.

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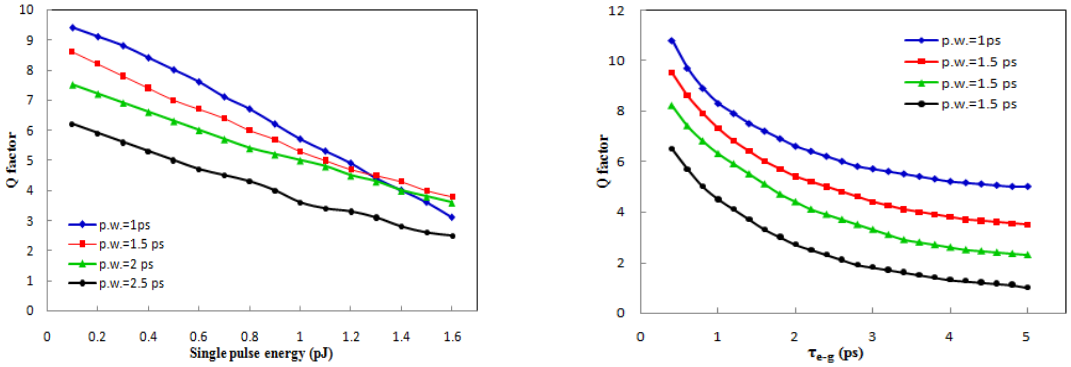
The calculated quality factor shows significant dependence on injected current density, pulse width, transition lifetime from QD excited state to ground state $\tau_{e\text{-}g}$ and single pulse energy. Figure 6 shows the contribution to output quality from injected current and pulse width, at high logic operation bit rate, input single pulse energy is set to 0.5 pJ to make sure the operation takes place in the non-saturated regime of the QD-SOA. From the results we find that at low injected current density level ($J < 1.8$ kA/cm^2), the Q factor is lower and will increase rapidly with increased current density. This can be explained as follows: with increased current density, more carriers are injected to the wetting layer, thus each energy level in the quantum dot can recover faster to initial carrier density level after carrier depletion following optical pulse injection and amplification. This reduces the pattern effect considerably. For very high current density Q values saturate. The smaller pulse width (less energy and hence less carrier depletion) also results in better performance (higher Q value)



(a) (b)

Figure 7: Calculated 250 Gb/s operation quality factor Q at different single pulse energy and transition lifetime from QD excited state to ground state. Injected current density is set to 1.8 kA/cm^2. (a): Q factor dependence on single pulse energy (b): Q factor dependence on ES to GS transition lifetime.

Figure 7 shows the calculated Q factor as a function of single pulse energy and carrier transition lifetime between QD excited state and ground state. The calculation is done with an injected current density of 1.8 kA/cm^2. From the results we see a decrease in output quality (Q factor) with the increase in single pulse energy of the input data and $\tau_{e\text{-}g}$. As single pulse energy increases, the carrier density of the active region of the device is depleted more, thus it takes longer to recover to initial level. The transition lifetime determines the speed of gain and phase recovery speed in the active region, thus Q-factor is higher for shorter transition times for high speed operation.

3. All-optical logic gates using BPSK Signal based on QD-SOA

Although all-optical logic gates using OOK signals based on

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QD-SOA-MZI have been proved at data rates of ~ 250Gb/s the patterning effects and amplified spontaneous emission are very strong for the schemes using OOK signal which will degrade the output quality. Thus, an alternative method of improving the output quality and achieving high-speed all-optical logic operations has been proposed [29, 30]. This method utilizes a QD-SOA-MZI pair each differentially driven by a data input and its complement.

3.1. Operation Principles of all-optical logic gates using BPSK signal

The proposed scheme accomplishing all-optical XOR operations is shown in Figure 8. It consists of a pair of QD-SOA-MZIs. Each QD-SOA-MZI is differentially driven by data and complement. The arrangement in Figure 8, in contrast to the conventional single SOA-MZI XOR set up, ensures that each QD-SOA receives a nearly constant-power stream of input pulse train. This is also illustrated in Figure 8 using an example of an on-off-keyed (OOK) signal A=[101]. Hence the patterning effects can be mitigated that arise from the fluctuation in the signal optical powers when QD-SOAs are directly modulated by OOK signals without a differential set up. For instance, the most deleterious situation is avoided, where the QD-SOAs receive a long sequence of 1's followed by a long sequence of 0's, or vice versa. Furthermore, because binary phase shift keyed (BPSK) signals carry information on the phase part while keeping the amplitude as a constant, the impairments from optical nonlinear effects and amplified spontaneous emission are greatly reduced. The working principle as follows: the top QD-SOA-MZI converts the input OOK data streams A and its complement into BPSK signal, $\exp(j\pi A)$.The bottom QD-SOA-MZI similarly outputs a BPSK signal $\exp(j\pi B)$. The conversion of OOK into BPSK was first used for all-optical wavelength conversion of DPSK signals and its process is detailed in [31, 32]. The next step in XOR operation is the linear optical interference between these two BPSK signals. The interference yields two OOK signals, one is XOR logic and the other is NXOR logic. The intensity envelops of the output signals emerging from the constructive and destructive ports of the 2x2 coupler are calculated using:

$$\left|\exp(j\pi A)+\exp(j\pi B)\right|^2 \square \overline{A\oplus B} \tag{13}$$

$$\left|\exp(j\pi A)-\exp(j\pi B)\right|^2 \square A\oplus B \tag{14}$$

We can use a similar scheme to realize logic AND and NAND operations as shown in Figure 9. From Boolean algebra, we know $\overline{\mathrm{A}}$ XOR $(\overline{\mathrm{A}}+\mathrm{B})$=A AND B . In this scheme, the top QD-SOA-MZI converts the input OOK data $\overline{\mathrm{A}}$ and its complement A into BPSK signal $\exp(j\pi\overline{\mathrm{A}})$.The bottom QD-SOA-MZI similarly outputs a BPSK signal $\exp(j\pi(\overline{\mathrm{A}}+\mathrm{B}))$. Thus, one output after interference is

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$\bar{A}$ XOR$(\bar{A}+B)$ which is the same as A AND B and the other output after interference is A NAND B. $\bar{A}+B$ is simply realized by an optical coupler.

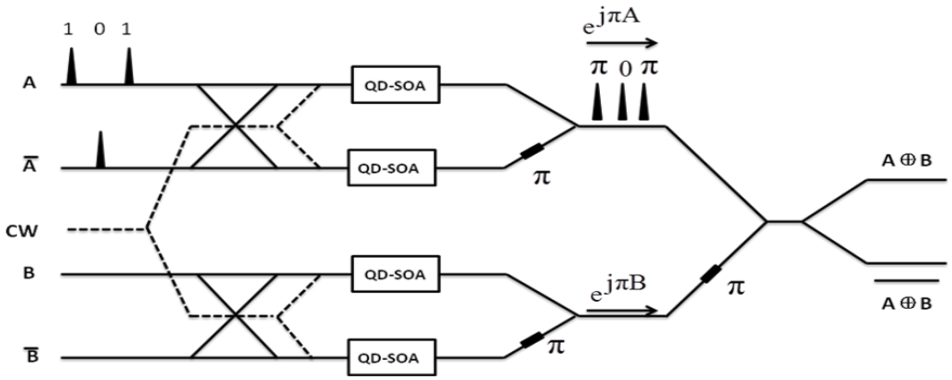

Figure 8 Schematic of the all-optical XOR logic gate, CW: continuous wave

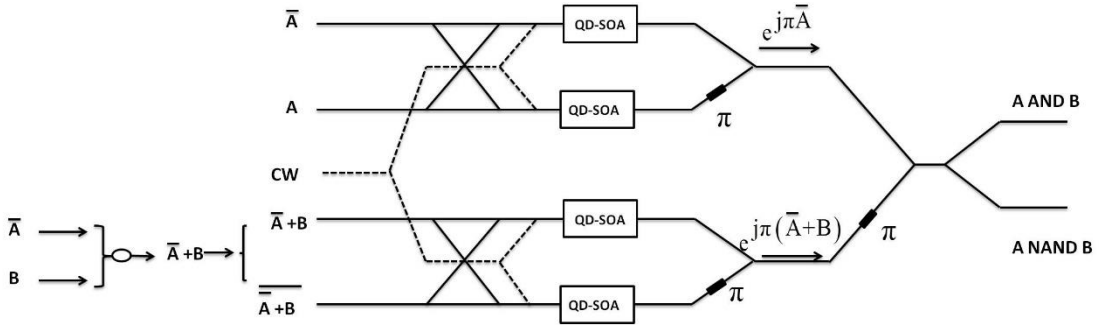

Figure 9 Schematic of the all-optical AND and NAND logic gates, CW: continuous wave

3.2. Numerical Simulation results

Simulated results of all-optical XOR, AND and NAND logic gates using the schemes in Figure 8 and Figure 9 are shown in Figure 10, Figure 11 and Figure 12 [29,30]. The output eye-diagrams are also plotted to show the output quality. From the simulated results, it is shown that all-optical XOR, AND and NAND logic gates using BPSK signal, scheme of a pair of QD-SOA-MZIs, @ ~ 250 Gb/s are feasible and have improved output quality.

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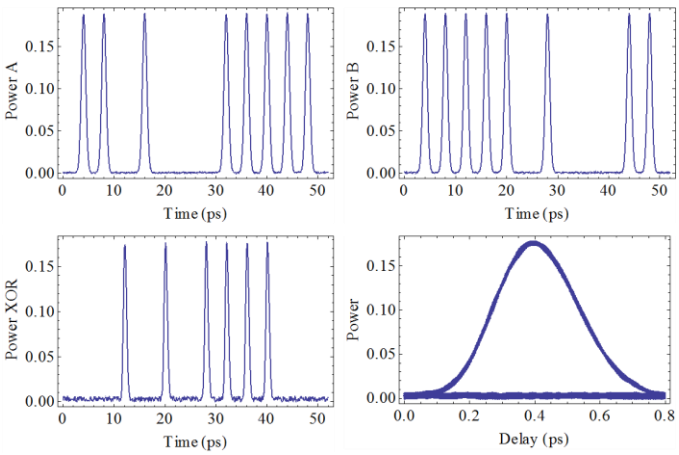

Figure 10: Date A and Date B are shown on the top. Simulated results of output (XOR) and eye diagram of the output are shown below. The above set of figures is for 250Gb/s data rate.

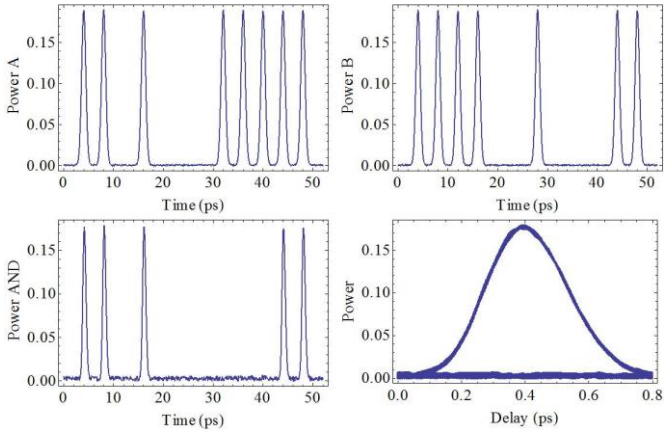

Figure 11 Date A and Date B are shown on the top. Simulated results of output (AND) and eye diagram of the output are shown below. The above set of figures is for 250Gb/s data rate.

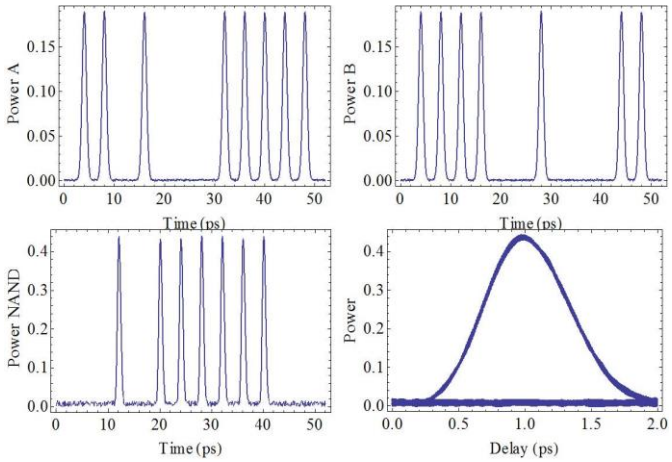

Figure 12 Date A and Date B are shown on the top. Simulated results of output (NAND) and eye diagram of the output are shown below. The above set of figures is for 250Gb/s data rate.

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4. All-optical latches Using QD-SOA

All-optical latches are important for a wide range of applications including communication systems, optical random access memory (RAM) and encryption. For communication system, it can be used for SONET scrambling and descrambling. The basic optical latches are the Set-Reset latch and the D-Flip-Flop. Both of these types of devices can be built using all-optical Boolean logic operations such as NAND and NOT. These operations are also important for all-optical signal processing such as bit pattern matching, pseudo random bit sequence (PRBS) generation and label swapping.

4.1. Schematic of All Optical Latches and QD-SOA Structure

The Set-Reset Latch is considered as one of the most basic logic circuit possible. This simple latch is basically a one-bit memory bistable device that has two inputs, one of which will "SET" the device (meaning the output = "1"), and another which will "RESET" the device (meaning the output = "0"). Then the SR description stands for "Set-Reset". The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level "1" or logic "0" depending upon this set/reset condition. The simplest way to make Set-Reset Latch is to connect together a pair of cross-coupled 2-input NAND gates. The schematic of Set-Reset Latch and the truth table for the Set-Reset function are showed in Figure 13.

The D-Flip-Flop is also widely used as the building block of a logic circuit. It is also known as a data or delay flip-flop. The D-Flip-Flop captures the value of the D-input at a definite portion of the gate cycle (such as the rising edge of the gate pulse). That captured value becomes the Q output. At other times, the output Q does not change. The D- Flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. We can use the NAND and NOT gates to make a D-Flip-Flop. The schematic of D-Flip-Flop and the truth table for D-Flip-Flop function are showed in Figure 14.

Because the NAND operation is just a series combination of AND and NOT operations, then we can realize the all-optical logic NAND operation by using this QD-SOA-MZI scheme as shown in Figure 15. The first QD-SOA-MZI serves in the system as an optical logic AND gate. After screening out all other wavelength components using a band-pass filter (BPF), the A AND B output data stream (λ_2) is amplified to desired power by an amplifier and guided into port 5 as data to one arm of the second MZI for INVERT operation. In this way, the result centered at λ_1 coming out of port 8 will be the INVERT of signal injected into port 5, which is the same as logic A NAND B. Based on Figure 13 and 14, NAND logic gate is the building block of all-optical latches such as Set-Reset and D-Flip-flop. Thus, we can use the QD-SOA-MZI system in Figure 15 to realize all-optical latches.

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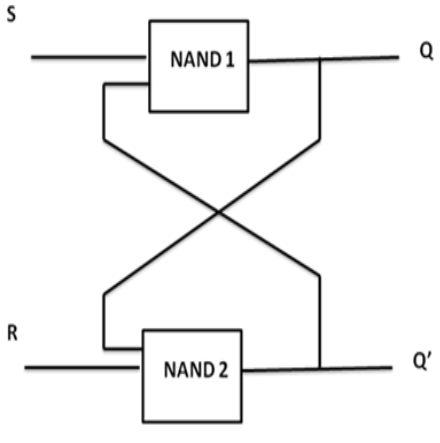
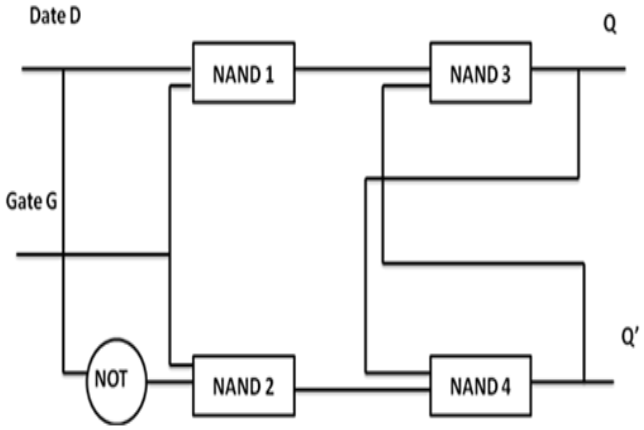


S	R	Action
0	0	Restricted Combination
0	1	Q=1, Q'=0
1	0	Q=0, Q'=1
1	1	No Change

Figure 13 The left figure is the schematic of the Set-Reset Latch. The right figure is the truth table for the Set-Reset function.



Gate	D	Q next
Rising edge (1)	0	0
Rising edge (1)	1	1
Non-Rising (0)	*	Q

Figure 14 The left figure is the schematic of the D-Flip-Flop. The right figure is the truth table for D-Flip-Flop function.

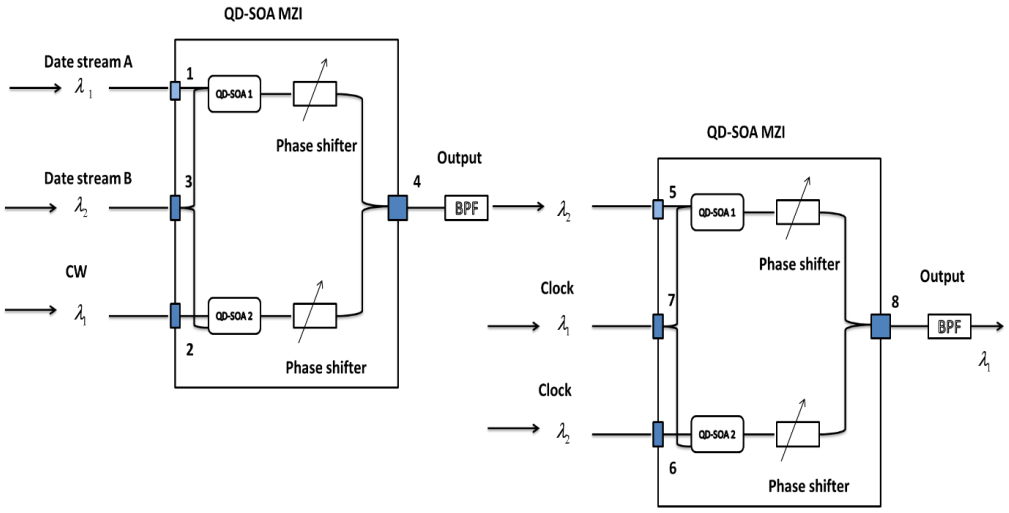


Figure 15 Schematic of all-optical NAND logic gate based on QD-SOA-MZI.

4.2. Simulation result

Simulated results of logic gate NAND, Set-Reset latch and D-Flip-Flop are

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shown in Figure 16, 17 and 18, respectively [10.11]. The output eye-diagram is also plotted to show the output quality. Based on the simulated results in Figure 16, 17 and 18, it is proved that all-optical Set-Reset latch and D-Flip-Flop operation @ ~ 250 Gb/s is feasible.

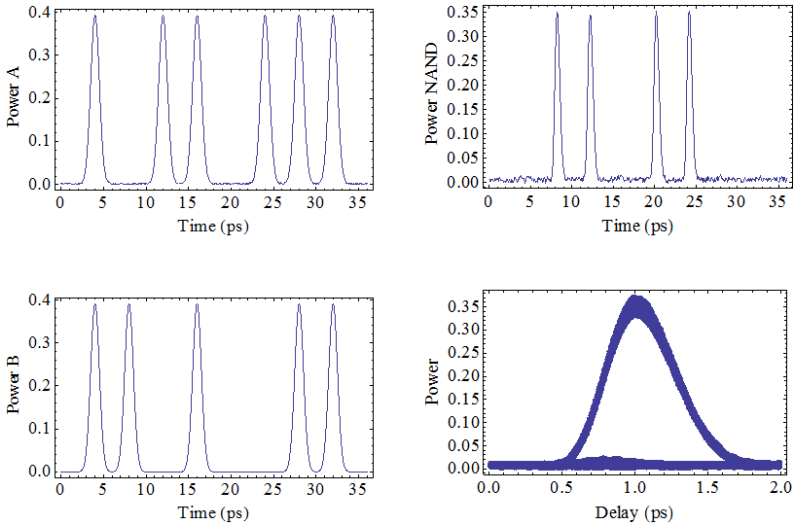

Figure 16 Date A and Date B are shown in the left. Simulated results of output (NAND) and eye pattern of the output are shown in the right. The above set of figures is for 250Gb/s data rate.

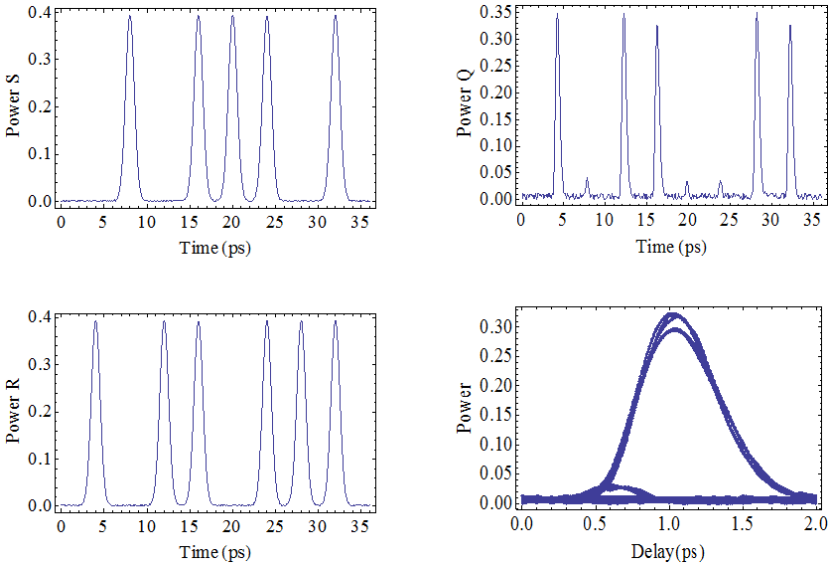

Figure 17 Set and Reset are shown in the left. Simulated results of output (Q) and eye pattern of the output are shown in the right. The above set of figures is for 250Gb/s data rate.

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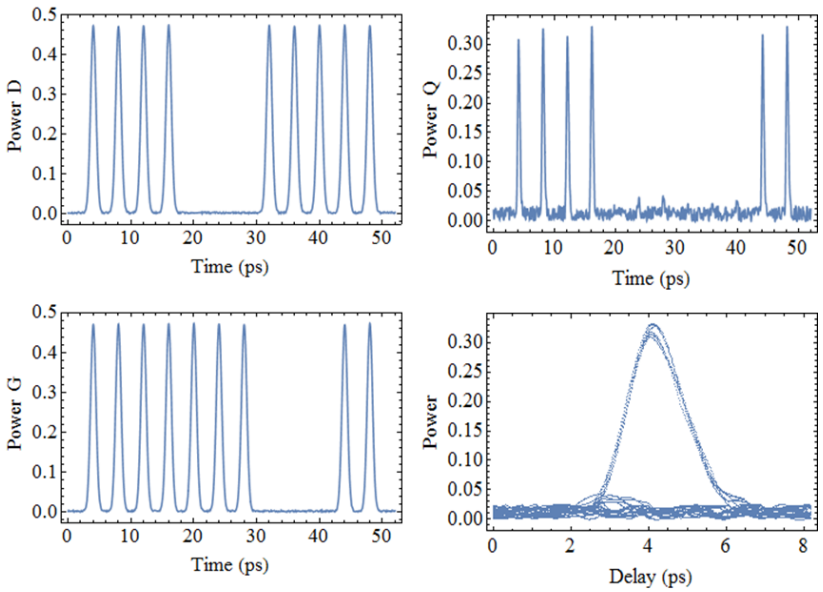

Figure 18 Date and Gate are shown in the left. Simulated results of output (Q) and eye pattern of the output are shown in the right. The above set of figures is for 250Gb/s data rate.

5. All-Optical Encryption and Decryption using QD-SOA

Encryption and decryption has long been used by governments to facilitate secret communication. It is now commonly used in protecting information within many kinds of civilian systems. For example, encryption can be used to protect data being transferred via internet, mobile telephones, wireless intercom systems and prevent unauthorized use or reproduction of copyrighted material. In an encryption scheme, the message is encrypted using an encryption algorithm. This is usually done with the use of an encryption key, which specifies how the information is to be encoded. An encryption scheme usually needs a key-stream generator to randomly produce keys. The pseudorandom bit sequence (PRBS) can be used as the key for encryption and decryption.

The pseudorandom bit sequence (PRBS) using linear feedback shift registers (LFSR), which were first introduced in electronics, are characterized by its simplicity of generation, good repeatability and statistical properties [33]. It thus received wide application, including in simulation of noise in signal transmission, data encryption/decryption, and in bit error rate testers (BERT) [34]. The recent achievements in photonics signal processing spurred more interest towards realizing high speed all-optical PRBS generation. A pseudorandom bit sequence (PRBS) can be generated using a linear feedback shift register (LFSR) [35]. The PRBS sequence generated with a shift register of length m has a period of 2^m-1. To generate a stable all-optical PRBS sequence using LFSR, an optical XOR logic gate is needed. A model to simulate the process of high speed all-optical encryption and decryption is presented in

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[25]. The encryption algorithm and the key we used in this model are XOR operation and pseudorandom bit sequence (PRBS). Both of the high speed all-optical XOR operation and PRBS are realized by using the QD-SOA Mach-Zehnder interferometer. Two other kinds of more secure key-stream generators: cascaded design and parallel design were also designed and investigated.

5.1. Schematic of all-optical Encryption and Decryption

The logic XOR operation can be used to realize the encryption and decryption of the message. The message can be encrypted by applying the bitwise XOR operation to every character using a given key. To decrypt the coded message, we merely reapply the XOR operation with the same key which is used for encryption. The schematic of encryption and decryption using the same key are shown in Figure 19. The high speed all-optical logic operations which are used for all-optical encryption and decryption are realized using QD-SOA-MZI as shown in Figure 2.

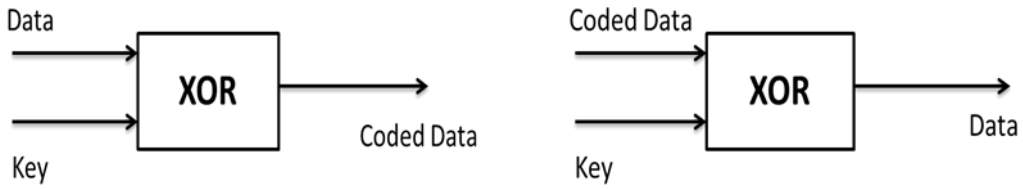

Figure 19 The left figure is the schematic of encryption. The right figure is the schematic of decryption. The same key stream is used for both encryption and decryption.

5.2. Generation of the key

The key used for encryption and decryption is high speed all-optical pseudo random bit sequence (PRBS) which is generated by a linear feedback shift register (LFSR) composed of QD-SOA-based logic XOR and AND gates, shown in Figure 20(a). An LFSR has m data storing units (optical delay line in all-optical system), each unit is capable of storing one binary data bit for one clock period [36]. The whole system is synchronized with a clock. At each period, the n_{th} and m_{th} bit go through an XOR process [37]. Their XOR result gets reshaped and its wavelength is converted back to system's operation wavelength through an AND gate, and then goes back to the front of LFSR. The output PRBS signals can be tapped from the end of the LFSR. Figure 20(b) shows the design of the logic functional unit. The main parts of this unit are two Mach-Zehnder interferometers (MZI) each arm of which has a semiconductor optical amplifier (SOA) with a quantum dot (QD) active region. The first MZI serves as an all-optical logic XOR gate for the two bits (m, n), while the other MZI serves as logic AND gate.

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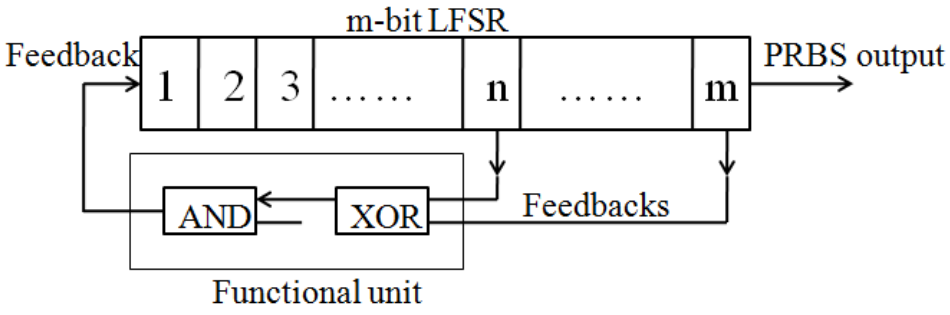
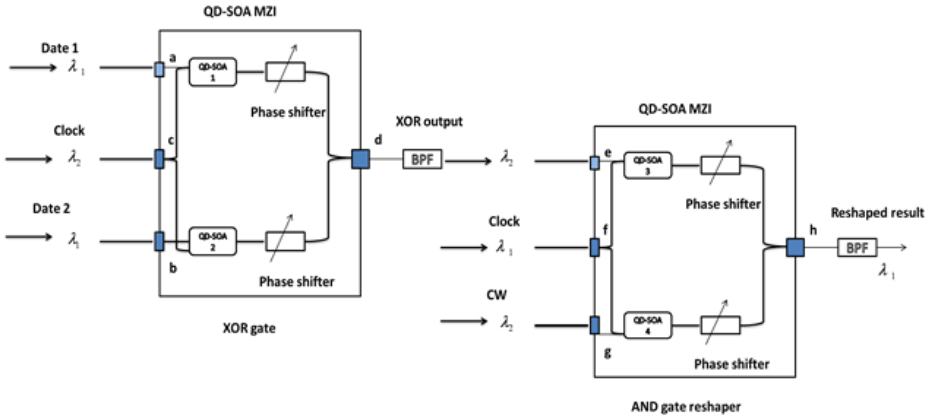


(a)



(b)

Figure 20 Design of PRBS generator. (a): Block diagram of a LFSR (b): functional unit, including two QD-SOA MZIs operating as XOR and AND gates.

The PRBS sequence generated using this scheme has a repetition bit period of $T=2^m-1$. Basically, the PRBS sequences are different from truly random bit sequences in that the latter has a continuous spectrum while the former has a discrete spectrum with harmonics [38]. As m increases the generated PRBS spectrum becomes more and more continuous and the output can better represent a truly random signal. The frequency space between two neighboring lines in the frequency spectrum of PRBS sequences is given by [38]

$$\Delta f = \frac{f_b}{2^m - 1} \tag{15}$$

where f_b is the bit rate. From the above equation, we can see as m increases the frequency space becomes smaller which means the PRBS frequency spectrum becomes more and more continuous. Thus, as m increases the randomness of PRBS sequence becomes better.

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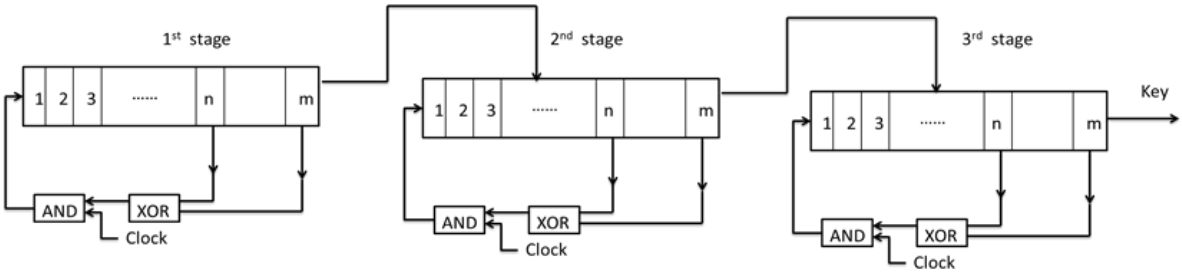

Figure 21 Block diagram of cascaded designed key-stream generator

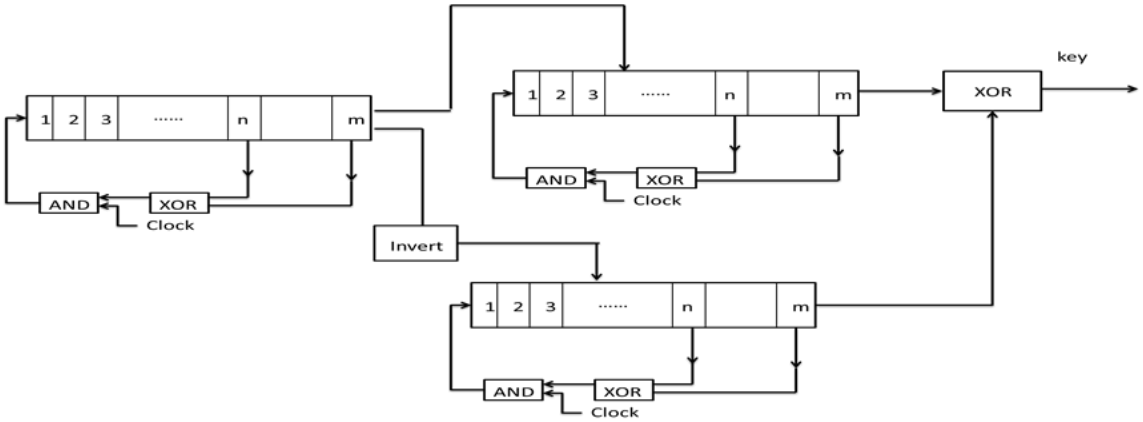

Figure 22 Block diagram of parallel designed key-stream generator

Two other kinds of more secure key-stream generators, cascaded design and parallel design were also presented, shown in Figure 21 and Figure 22 [22]. The cascaded design consists of three cascaded linear feedback shift registers (LFSR) which can generate all-optical PRBS. The output of the first LFSR can be used as the input of the second LFSR and the output of the second LFSR can be used as the input of the third LFSR. All these three LFSR are realized using the QD-SOA MZIs. The parallel design is composed of three linear feedback shift registers (LFSR), an INVERT gate and a XOR gate. The output of the first LFSR and its invert are used as the input of the second LFSR and the third LFSR respectively. The final output is the XOR of the output of second LFSR and third LFSR. The three LFSR and all the logic gates are realized by using QD-SOA MZIs too.

5.3. **Simulation Results**

The simulated results of encryption and decryption for the QD-SOA based XOR operation are shown in Figure 23 [25]. Input data is on the top right and a key (chosen any of bots in this case) is shown on top left. The encrypted in XOR of the input data and key is shown on bottom left. The decrypted data which should be the original data is shown on bottom right. Note that top right and bottom right traces are identical as it should be. Thus, it is proved that all-optical encryption and decryption operation at ~250Gb/s is feasible. The Q factor was also calculated for the decrypted data in Figure 23. The Q factor is 8.7, which means a good quality of the decrypted data.

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The key used for encryption and decryption is high speed all-optical pseudo random bit sequence (PRBS). The all-optical PRBS generated by a 7-bit optical LFSR is simulated by modeling the logic XOR and AND operations based on QD-SOAs as shown in Figure 24.

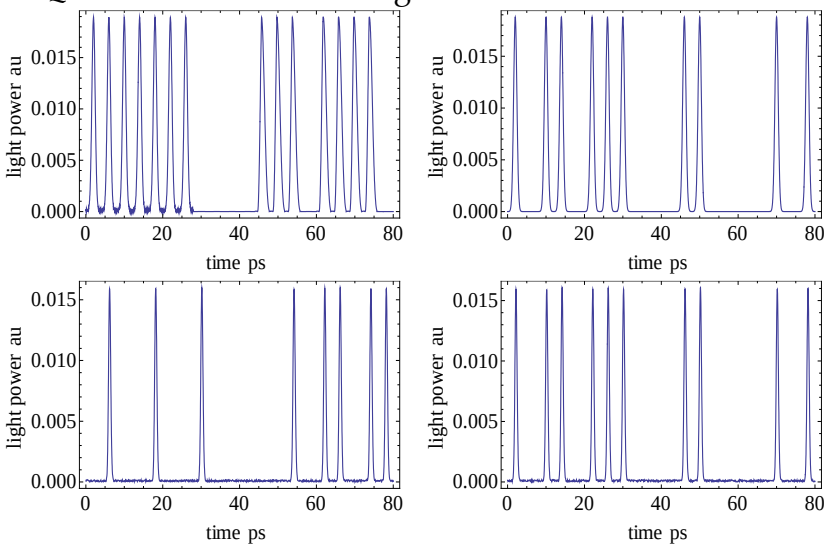

Figure 23 Input date is shown at the top-right corner and key is shown at the top-left corner. Simulated results of encrypted data and decrypted data are shown at the bottom-left corner and bottom-right corner respectively. The above set of figures is for 250Gb/s data rate.

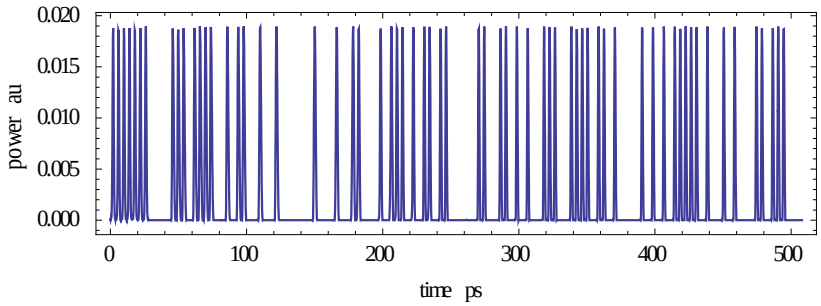

Figure 24 Simulation result of PRBS sequences generated by 7-bit LFSR, operating at 250Gb/s. The input of all-optical LFSR is seven "1"s.

The numerical simulation results of cascaded design and parallel design key stream generators are shown in Figures 25 and Figure 26 respectively. As shown in figure 25 and 26, the cascaded design and parallel design key-stream generators operating at ~250Gb/s is feasible. Thus, we can use these two kinds of key-stream generators to produce various more secure keys.

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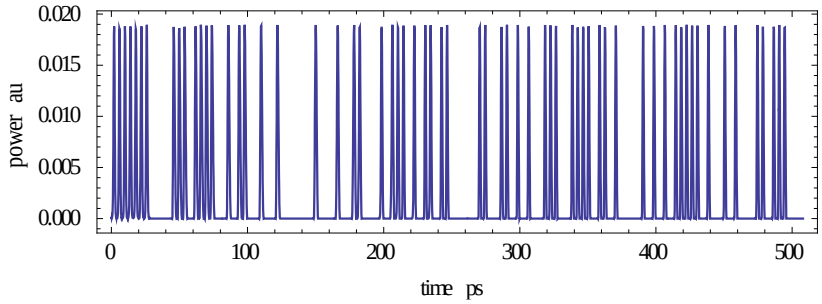
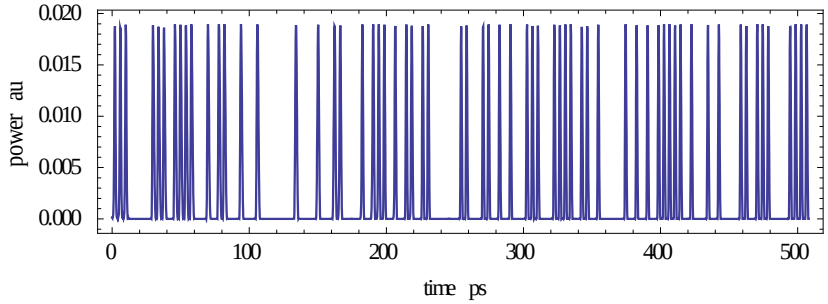
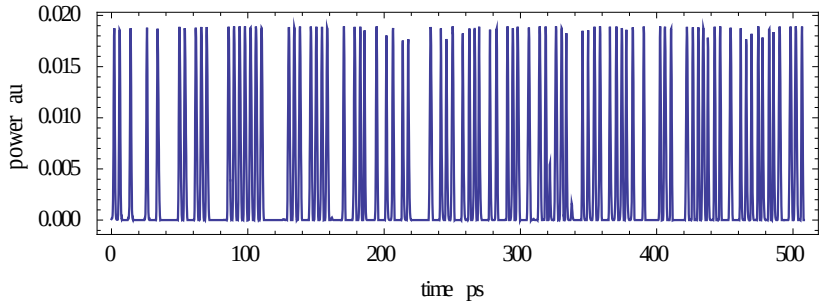


(a)

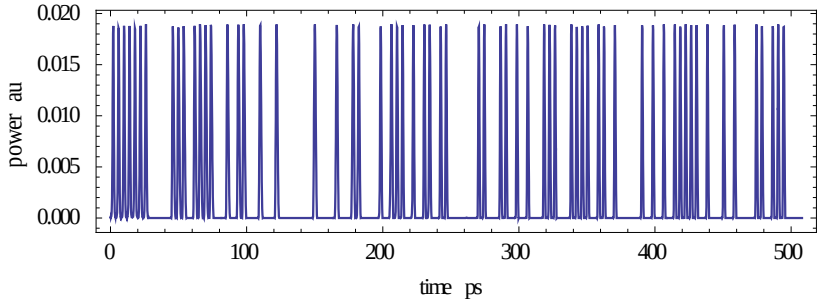


(b)



(c)

Figure 25 (a) Simulation result of the first stage in cascaded design, input is seven "1"; (b) Simulation result of the second stage in cascaded design, input is "8th-14th" of the output of the first stage; (c) Simulation result of the third stage in cascaded design, input is "15th-21st" of the output of the second stage.



(a)

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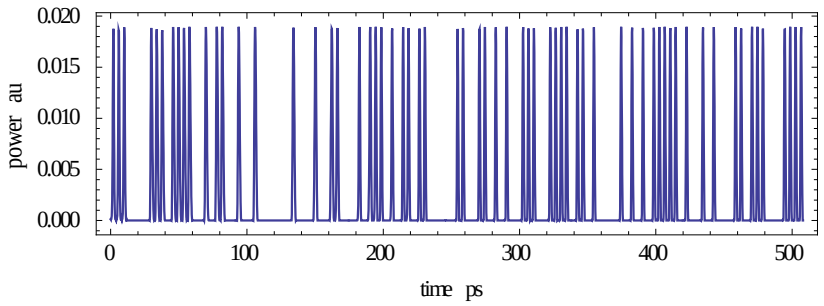
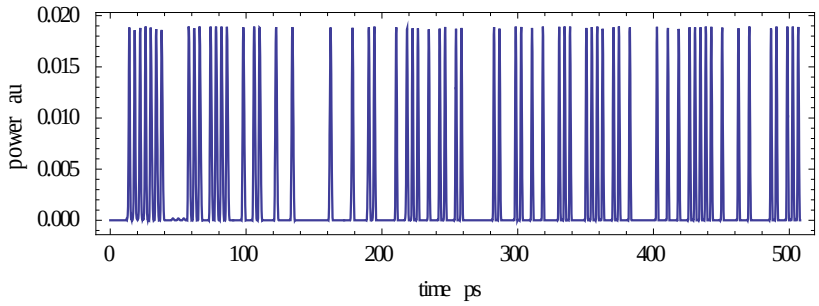
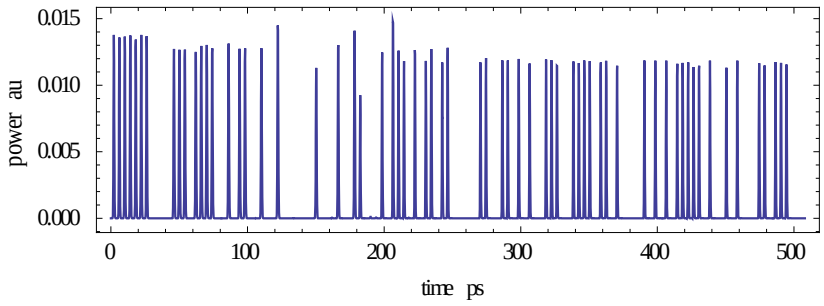


(b)



(c)



(d)

Figure 26 (a) Simulation result of the first LFSR in parallel design, input is seven "1"; (b) Simulation result of the second LFSR in parallel design, input is "8th-14th" of the output of the first LFSR; (c) Simulation result of the third LFSR in parallel design, input is the invert of "8th-14th" of the output of the first LFSR; (d) the final output of parallel design: XOR of the output of second and third LFSR.

6. Summary and Perspective

The model to simulate high speed all-optical logic gates using QD-SOA based Mach-Zehnder Interferometer was presented. Results show that QD-SOA based MZI can perform logic operations such as AND, XOR, NOT and NAND at high speed up to 250 Gb/s. The impact on the high speed output quality (Q-factor), from injected current density, transition lifetime between QD excited state and ground state, pulse width and single pulse energy, are also studied and discussed. The design and simulation of all-optical latches and all-optical encryption using QD-SOA were also presented and investigated. These research results proved that high speed

all-optical logic generation based on QD-SOA-MZI is a feasible and promising method to realize all-optical network in the future. Further investigation on more complex all-optical circuit based on all-optical logic gates is required.

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