Transistor Clamped H-Bridge Five-Level Multilevel Inverter for Photovoltaic Application – A Hardware Prototype Implementation Using Inverted Double Reference Single Carrier PWM Technique

Mahajan Sagar Bhaskar 1, Sanjeevikumar Padmanaban 1,*, Frede Blaabjerg 2, Anzari Mohammed 3

1 Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, South Africa; sagar25.mahajan@gmail.com; sanjeevi_12@yahoo.co.in
2 Centre for Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Denmark; fbl@et.aau.dk
3 Power Electronics Design, Research and Development, Opzet Solutions Pvt. Ltd, Ernakulam (Kerala), India; anzarim@gmail.com

* Correspondence: sanjeevi_12@yahoo.co.in; Tel.: +27-79-219-9845

Abstract: Inverters are Power Electronic System (PES) and proficient to converting Direct Currents (DC) into Alternating Currents (AC). Conventional two-level inverter has drawbacks like high Total Harmonic Distortions (THD), high voltage across power switch, high \( \frac{dv}{dt} \) of output voltage and electromagnetic interferences. Multilevel Inverters (MLIs) are employed to overcome the drawbacks of conventional two-level inverter. Multilevel Inverters generate an AC voltage using small voltage steps obtained with the help of DC supplies or capacitor banks. This paper deals with the implementation of a Transistor Clamped H-Bridge Multilevel Inverter (TCHB-MLI) using Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) technique for photovoltaic application. The proposed TCHB-MLI requires less number of power switches and drivers to achieve maximum number of output level. The analysis of the multilevel inverter output is done in terms of its harmonic spectrum, output voltage and output current for modulation indices 0.85, 1 and 1.25. The control signals for the power switches of the proposed TCHB-MLI are developed by using SPARTAN 3E-XCS250E trainer kit. Experimental results will verify the functionality, design of the proposed TCHB-MLI and IDRSCPWM Technique.

Keywords: Multilevel Inverter; Cascaded H-Bridge; Inverted Double Reference Single Carrier PWM; Transistor Clamped H-Bridge (TCHB), Total Harmonic Distortions (THD); FPGA

1. Introduction

The ultimatum for energy is getting incremented day by day which is also increasing the requirement of energy generation. The main source of energy available now is from non-renewable sources based on fossil fuels. The over exploitation of these sources to meet our daily requirements have put it in a degraded state. Hence there is a rapid development in the research of harnessing energy from alternate sources such as wind, solar, tidal, etc. Among them, the energy extracted from photovoltaic systems plays a vital role. The energy extracted from a photovoltaic system (PV system) is DC in nature. Since most of the equipments used for domestic and industrial purposes are working on an AC source, the DC output from a PV system needs to be converted into AC. For this, power inverters play a major role [1-10]. Two level inverters need high frequency carrier pulses in order to get better output performance. They have drawbacks like fast switching devices are require, very high \( \frac{dv}{dt} \) of output voltages, high electromagnetic interferences (EMI), bulky filters and faster heating of switches [11-12]. The multilevel inverter concept came as a solution for the difficulties mentioned above. Inverters with output voltage level more than two comes under the multilevel configuration. As the number of output voltage level increases the harmonic contents in
the output decreases. By giving proper pulses to the power switches multilevel inverter can synthesize the input DC into small voltage steps approximating them with a sinusoidal wave. The multilevel inverters can maximize the power and minimize the harmonic contents in the output AC voltage side [13-14]. Diode Clamped MLI, Flying capacitor MLI and Cascaded H-Bridge MLI are three conventional multilevel inverter topologies [15-33].

![Image](image_url)

**Figure 1.** (a) Power circuit of five-level TCHB-MLI (b) Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) Technique.

Diode clamped MLI and flying capacitor MLI have problems like voltage balancing and dynamic voltage sharing at higher output levels. Thus, among the conventional MLI topologies cascaded H-Bridge configuration is widely accepted due to their modular structure and fault tolerant capability [34]. Multilevel inverters are widely used in renewable energy applications, static reactive power compensators and adjustable speed drives [35-39]. The switching pulses for multilevel inverters can be generated by using various modulation techniques. Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), and Selective Harmonic Elimination (SHE-PWM) are the most used modulation techniques [37-43]. Further SPWM technique is classified as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) and Phase Shifted techniques (PS).

This paper deals with the hardware implementation of a five-level Transistor Clamped H-Bridge Multilevel Inverter (TCHB-MLI) using Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) technique for photovoltaic applications. The proposed TCHB-MLI requires less number of power switches and drivers to achieve maximum number of output level. The obtained result is compared with the performance of a conventional five level cascaded H-Bridge inverter. This paper is organized in such a manner that section-2 covers the details of proposed five-level transistor clamped H-Bridge Multilevel Inverter (TCHB-MLI). In Section-3 experimental results and observations are discussed in detail and finally a conclusion is provided in section-4.

2. Five Level Transistor Clamped H-Bridge MLI (TCHB-MLI)

The power circuit of TCHB-MLI is shown in Figure 1(a). The power circuit of a five level Transistor Clamped H-Bridge Multilevel Inverter (TCHB-MLI) consists of H-Bridge inverter and an auxiliary circuit. The auxiliary circuit comprised of a power MOSFET switch. The capacitors used ‘C1’ and ‘C2’ act as two voltage sources. They split the input voltage given into two equal voltages. The TCHB-MLI can generates output levels $V_{in}$, $V_{in}/2$, 0, $-V_{in}/2$, and $-V_{in}$ by giving proper switching pulses to power switches. Proposed MLI needs only five power switches to generate five levels in
output voltage. The auxiliary circuit is responsible for generating the output voltage levels $V_{in}/2$ and $-V_{in}/2$.

### Table 1. Switching sequence of the TCHB-MLI

<table>
<thead>
<tr>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>$V_o$</th>
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<tbody>
<tr>
<td>OFF</td>
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<td>OFF</td>
<td>OFF</td>
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<td>ON</td>
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<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>$V_{in}/2$</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>0</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>0</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>$-V_{in}/2$</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>$-V_{in}$</td>
</tr>
</tbody>
</table>

### 2.1. Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) Technique

Figure 1(b) shows the Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) technique. In this modulation technique two inverted references one with an offset value added equal to the amplitude of the carrier is compared with the single triangular carrier to obtain the pulses for the power switches $S_1$-$S_3$. Compliment pulses of 50Hz frequency are used for power switches $S_4$ and $S_5$. The modulation index is given by the equation (1). Where ‘$A_m$’ is the amplitude of the reference wave and ‘$A_c$’ is the amplitude of the triangular carrier wave. Table 1 shows the switching sequence of Transistor Clamped H-Bridge Multilevel Inverter (TCHB-MLI).

$$m = \frac{A_m}{2A_c}$$ (1)

### 2.2. Working mode of TCHB-MLI

The operating modes of five-level TCHB-MLI topology are explained in this section. Figure 2(a) shows the equivalent power circuit of proposed inverter to generate the output voltage level $V_{in}$. Power switches $S_2$ and $S_5$ are in ON state to achieve $V_{in}$ voltage level. Figure 2(b) shows the equivalent power circuit of proposed inverter to generate output voltage level $V_{in}/2$. Power switches $S_1$ and $S_5$ are in ON state to achieve $V_{in}/2$ voltage level. Figure 2(c) shows the equivalent power circuit of proposed inverter to generate the output voltage level zero. To achieve zero level power switches $S_1$ and $S_5$ are in ON state. Figure 2(d) shows another possibility to obtain the zero voltage level. Power switches $S_1$ and $S_5$ are in ON state to generate the zero level. Figure 2(e) shows the equivalent circuit of proposed inverter to generate output voltage level $-V_{in}/2$. To generate $-V_{in}/2$ voltage level power switches $S_1$ and $S_4$ are in ON state. Figure 2(f) shows the equivalent circuit of proposed inverter to generate output voltage level $-V_{in}$. To generate $-V_{in}$ voltage level power switches $S_3$ and $S_4$ are in ON state.
3. Experimental Result and Discussion

The switching logic for the power switches of proposed inverter are implemented with the help of SPARTAN-3E XCS250E FPGA trainer kit. The clock frequency of the processor is 20MHz. The Spartan-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The Spartan-3E family architecture consists of five fundamental programmable functional elements:

1. Configurable Logic Blocks (CLBs): These Blocks contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
2. Input/output Blocks (IOBs): These Blocks controls the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow, plus 3-state operation.
3. Block RAM: These Blocks provides data storage in the form of 18-kbit dual-port blocks.
4. Multiplier Blocks: These Blocks accept two 18-bit binary numbers as inputs and calculate the product.
5. Digital Clock Manager (DCM) Blocks: These Blocks provides self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

Figure 3 shows the SPARTAN-3E FPGA trainer kit. The input for the experiment is taken from PV panels. In peak time each panel can provide a maximum voltage ranging from 32V-33V. For the implementation of a transistor clamped H-Bridge MLI four PV panels are connected in series. The experiment is conducted for modulation indices 0.85, 1 and 1.25 with R and RL-Load. The output results in each case are obtained and investigated with the help of Fluke-43B power quality analyzer. The experimental setup for the TCHB-MLI is shown in Figure 4. Table-2 specifies the hardware specification details of proposed inverter.
Figure 3. SPARTAN-3E FPGA Kit

Figure 4. Experimental set up of CHB-MLI

Table 2. Hardware specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (Vin)</td>
<td>4 PV Panels (each of 32V)</td>
</tr>
<tr>
<td>Capacitors(C1-C2)</td>
<td>2200uF</td>
</tr>
<tr>
<td>Switching frequency(fs)</td>
<td>1kHz</td>
</tr>
<tr>
<td>Power resistor</td>
<td>100Ω, 5A (Maximum rating)</td>
</tr>
<tr>
<td>Inductor</td>
<td>12mH</td>
</tr>
<tr>
<td>MOSFET</td>
<td>IRFP460</td>
</tr>
<tr>
<td>Fast Diode</td>
<td>DPG10I400PA</td>
</tr>
<tr>
<td>MOSFET Driver IC</td>
<td>TLP250</td>
</tr>
</tbody>
</table>

Figure 5 (a) and (b) shows the output power, output voltage and output current for a modulation index of m=0.85 (Under Modulation) with R-load respectively. It is observed that for R-load obtained power is 114W, 114VA, 8VAR with the 79.7V and 1.442A. Figure 5 (c) and (d) shows the output power, output voltage and output current for a modulation index of m=0.85 with RL-load respectively. It is observed that for RL-load obtained power is 104W, 108VA, 31VAR with the 80.1V and 1.343A. Separately fundamental component of voltage and current is obtained for a modulation index m=0.85 with R-load is shown in Figure 5(e) and (f). It is observed that the fundamental voltage is 78.9 V, 49.98 Hz with 32.4% THD. It is also observed that the fundamental current is 1.426 V, 49.98 Hz with 32.0% THD. Separately fundamental component of voltage and current is obtained for a modulation index m=0.85 with RL-load is shown in Figure 5(g)-(h). It is observed that the fundamental voltage is 79.3V, 49.98 Hz with 32.9% THD. It is also observed that the fundamental current is 1.337 V, 49.98 Hz with 19.4% THD.
Figure 5. (a) Output power of TCHB for m=0.85 with R-load. (b) Output voltage and current of TCHB for m=0.85 with R-load. (c) Output power of TCHB for m=0.85 with RL-load. (d) Output voltage and current of TCHB for m=0.85 with RL-load. (e) 1st Harmonics (Voltage) or Fundamental for m=0.85 with R-Load. (f) 1st Harmonics (Current) or fundamental for m=0.85 with R-Load. (g) 1st Harmonics (Voltage) or Fundamental for m=0.85 with RL-Load. (h) 1st Harmonics (Current) or fundamental for m=0.85 with RL-Load.

Figure 6 (a) and (b) shows the output power, output voltage and output current for a modulation index of m=1 (Unity Modulation) with R-load respectively. It is observed that for R-load obtained power is 152W, 152VA, 10VAR with the 91.6V and 1.654A. Figure 6 (c) and (d) shows the output power, output voltage and output current for a modulation index of m=1 (Unity Modulation) with RL-load respectively. It is observed that for RL-load obtained power is 142W, 146VA, 33VAR with the 92.0V and 1.577A. Separately fundamental component of voltage and current is obtained for a modulation index m=1 with R-load is shown in Figure 6(e)-(f). It is observed that the fundamental voltage is 91.0 V, 49.98 Hz with 22.6% THD. It is also observed that the fundamental current is 1.638 V, 49.98 Hz with 22.5% THD. Separately fundamental component of voltage and current is obtained for a modulation index m=0.85 with RL-load is shown in Figure 6(g)-(h). It is observed that the fundamental voltage is 91.2V, 49.98 Hz with 23.6% THD. It is also observed that the fundamental current is 1.574 V, 49.98 Hz with 13.7% THD.
Figure 6. (a) Output power of TCHB for m=1 with R-load. (b) Output voltage and current of TCHB for m=1 with R-load. (c) Output power of TCHB for m=1 with RL-load. (d) Output voltage and current of TCHB for m=1 with RL-load. (e) 1st Harmonics (Voltage) or Fundamental for m=1 with R-Load. (f) 1st Harmonics (Current) or fundamental for m=1 with R-Load. (g) 1st Harmonics (Voltage) or Fundamental for m=1 with RL-Load. (h) 1st Harmonics (Current) or fundamental for m=1 with RL-Load.

Figure 7 (a) and (b) shows the output power, output voltage and output current for a modulation index of m=1.25 (Over Modulation) with R-load respectively. It is observed that for R-load obtained power is 183W, 183VA, 9VAR with the 100.8V and 1.821A. Figure 7 (c) and (d) shows the output power, output voltage and output current for a modulation index of m=1.25 (Over Modulation) with RL-load respectively. It is observed that for RL-load obtained power is 177W, 180VA, 33VAR with the 101.7V and 1.769A. Separately fundamental component of voltage and current is obtained for a modulation index m=1.25 with R-load is shown in Figure 7(e) and (f). It is observed that the fundamental voltage is 100.1V, 49.98 Hz with 18.2% THD. It is also observed that the fundamental current is 1.805V, 49.98 Hz with 18.0% THD. Separately fundamental component of voltage and current is obtained for a modulation index m=1.25 with RL-load is shown in Figure 7(g)-(h). It is observed that the fundamental voltage is 101.1V, 49.98 Hz with 18.5% THD. It is also observed that the fundamental current is 1.760V, 49.98 Hz with 12.5% THD.
Figure 7. (a) Output power of TCHB for m=1.25 with R-load. (b) Output voltage and current of TCHB for m=1.25 with R-load. (c) Output power of TCHB for m=1.25 with RL-load (d) Output voltage and current of TCHB for m=1.25 with RL-load (e) 1st Harmonics (Voltage) or Fundamental for m=1.25 with R-Load. (f) 1st Harmonics (Current) or fundamental for m=1.25 with R-Load. (g) 1st Harmonics (Voltage) or Fundamental for m=1.25 with R-Load. (h) 1st Harmonics (Current) or fundamental for m=1.25 with R-Load.

The graphical analysis is done based on the results obtained from the power quality analyzer (Fluke 43B). A study on THD and odd harmonics of both the current and voltage of TCHB-MLI is performed for modulation indices in 0.85, 1 and 1.25 with R and RL-load. Figure 8 (a) and Figure 8(b) show the voltage and current harmonic spectrum analysis with R-load is graphically. Figure 8(c) and Figure 8(d) show the graph study of voltage and current harmonic spectrum of TCHB-MLI with RL-load respectively. Figure 8(e) and Figure 8(f) show the Total Harmonic Distortions of both voltage and current of TCHB-MLI for modulation indices of 0.85, 1 and 1.25 with R and RL load respectively. From the observations, it is found that: The THD content of over modulated (m=1.25) condition is low for TCHB-MLI but their odd harmonic (3rd, 5th, 7th, 9th) contents are higher compared to m=0.85 and m=1. Using the same input DC supply the over modulated condition can produce more output voltage compared to unity modulated and under modulated condition. TCHB-MLI is able to produce a five-level output with five power switches whereas CHB-MLI requires eight power switches thereby reducing the power circuit complexity.
4. Conclusions

A five-level Transistor Clamped H-Bridge MLI (TCHB-MLI) is implemented with the help of a SPARTAN3E XC3S250E FPGA kit. Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) technique is used to generate five levels at the output side. A detailed study of the harmonic spectrum of the TCHB-MLI is done for modulation indices 0.85, 1 and 1.25 with R and RL load using Fluke-43B power quality analyzer. The TCHB-MLI is able to generate a five level output voltage with reduced number of power switches thereby reducing the circuit complexity. Experimental results are provided and which verifies the functionality, design of the proposed inverter and PWM Technique.

Acknowledgments: No funding source.

Author Contributions: “S. B. Mahajan, P. Sanjeevikumar and Anzari M. had developed the proposed research concept with the complete theoretical background study. Further hardware prototype implementation tasks are carried out the same authors. F.Blaabjerg has contributed his expertise to validate the proposal both theoretical background and hardware results obtained as co-author in technical aspect of the proposal. All authors involved in framing its current format of the full research paper work”.

Conflicts of Interest: Declare conflicts of interest or state “The authors declare no conflict of interest.

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