Multistage DC-DC Step-Up Self Balanced and Magnetic Component Free Converter for Photovoltaic Applications—Hardware Implementation

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Abstract: This article presents a self balanced multistage DC-DC step-up converter for photovoltaic applications. Proposed converter topology is designed for unidirectional power transfer and provides a doable solution for photovoltaic applications where voltage is required to be stepped up without magnetic components (Transformer-less and Inductor-less). The output voltage obtained from renewable sources will be low and must be stepped up by using a DC-DC converter for photovoltaic applications. K diodes and K capacitors along with two semiconductor control switch are used in the K-stage proposed converter to obtain an output voltage which is (K+1) times the input voltage. The conspicuous features of proposed topology are i) Magnetic components free (Transformer-less and Inductor-less). ii) Continuous input current iii) Low voltage rating semiconductor devices and capacitors iv) Modularity v) Easy to add a higher number of levels to increase voltage gain vi) Only two control switches with alternating operation and simple control. The proposed converter is compared with recent existing transformer-less and Inductor-less power converter in term of voltage gain, number of devices and cost. The application of proposed circuit is discussed in detail. The proposed converter has been designed with rated power of 60W, input voltage is 24V, output voltage is 100V and switching frequency is 100 kHz. The performance of the converter is verified through experimental and simulation results.

Keywords: DC-DC; self biased; magnetic component free; multistage; step-up; photovoltaic application

1. Introduction

The renewable energy resources are getting popular and trendy with the increase in demand and cost of energy. The proper utilization of energy resources is one of the most important issues of the present century. There are various renewable energy resources with zero pollution emission consisting of solar, tidal, wind, bio, nuclear and geothermal. Solar energy is free, inexhaustible source of energy and is increasingly competitive with other energy sources. This energy is utilized with the help of arrays, consisting of a number of solar panels, connected in series [1-3]. In past, various method or structure of PV system is adopted to minimize the cost to efficiency ratio. In [4-8], Photovoltaic Central Inverter Structure (PV-CIS) is employed to feed photovoltaic energy to the electric grid. In PV-CIS PV strings are arranged in parallel and connected to one central inverter as shown in Figure 1. The drawback of CIS are i) Large number of panels are required which increases the cost of system ii) Need more number of DC cables with high-voltage rating iii) Losses in String iv) Loss of Power due to module mismatch v) Common MPPT (Maximum Power Point Tracking) is used vi) system reliability is depends on the single inverter.

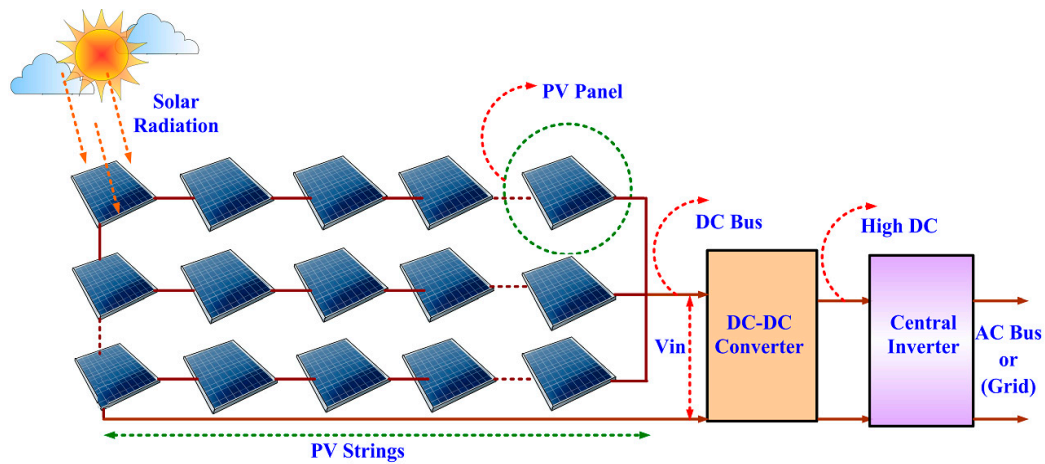



Figure 1. Photovoltaic Central Inverter Structure (PV-CIS) for transfer PV Energy to electric grid.

In [4-8], Photovoltaic String Inverter structure (PV-SIS) is employed to feed photovoltaic energy to electric Grid. In PV-SIS, several PV string are used which is made from several series connected PV Panel as shown in Figure 2. All the PV strings are connected to separate inverter via DC-DC Converter and outputs of inverter are connected in parallel and feed to the electric grid. The drawbacks of the PV-SIS system are i) Require large number of panel to design a several PV string ii) Large number of converters are required to feed grid iii) Cost is high due to separate MPPT and complex control circuitry is required to synchronous all Inverters.

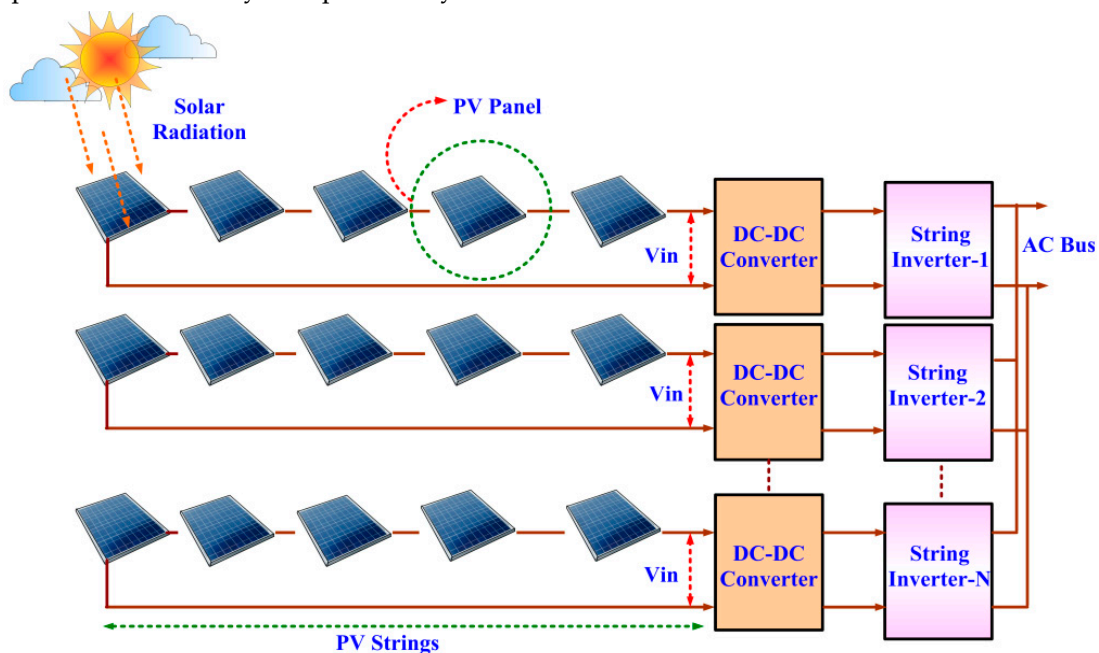



Figure 2. Photovoltaic String Inverter Structure (PV-SIS) for transfer PV Energy to electric grid.

In [4-8], Photovoltaic AC Module Structure (PV-ACMS) is discussed to fed photovoltaic energy to electric grid and it provide a viable solution to overcome the drawback of PV-CIS and PV-SIS. In PV-ACMS single photovoltaic panel is connected to electric grid via inverter as shown in figure 3(a). The drawbacks of PV-ACMS are i) Required several module inverter which increases the cost of the system ii) separate MPPT is needed for each panel iii) overall efficiency is low. In [4-8], Photovoltaic Multi-String Inverter Structure (PV-MSIS) is discussed to overcome the drawback of PV-CIS, PV-SIS and PV-SIS structure. In PV-MSIS several PV panels are connected to single inverter is connected via several DC-DC Converters as shown in Figure 3(b). This structure combines the features of PV-SIS and PV-ACMS. The drawback of the PV-MSIS are i) required several DC-DC converter before transfer energy to inverter ii) high cost due to more number of converters and separate MPPT.

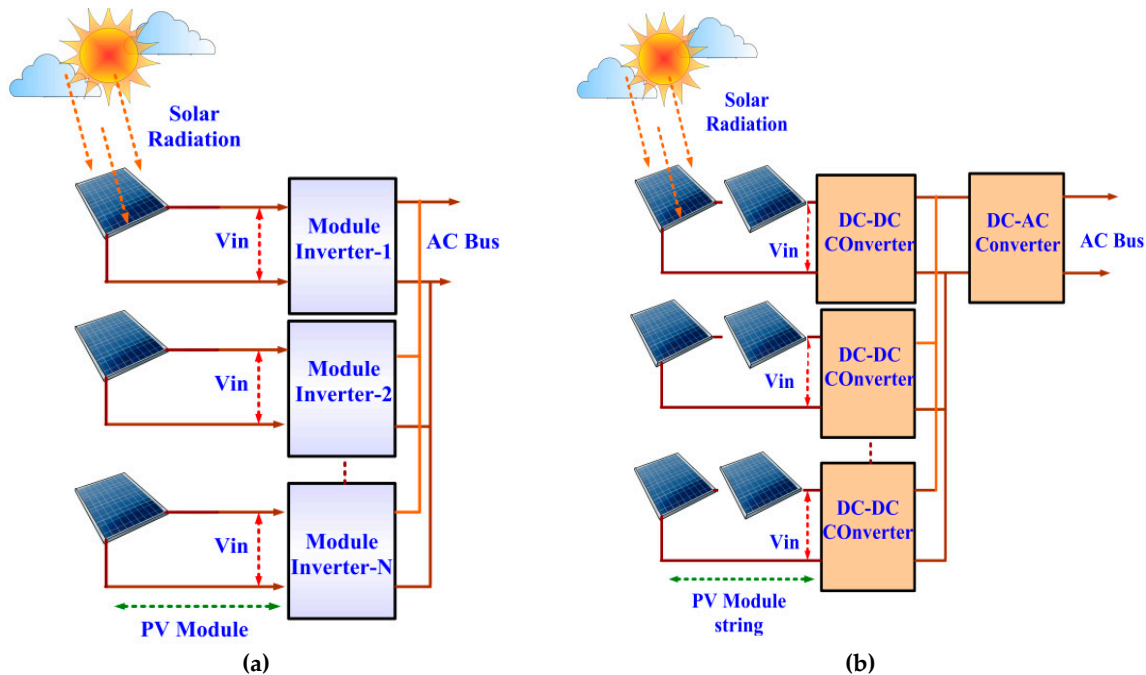



Figure 3 (a). Photovoltaic AC Module Structure (PV-ACMS) (b) Photovoltaic Multi-String Inverter Structure (PV-MSIS) for transfer of PV energy to electric grid.

The output obtained from the photo voltaic cell/array is usually low, so before feeding this voltage to the inverter for practical application purpose, it is needed to be stepped up using conventional DC-DC boost converter [1-15]. With the increase in the duty-cycle of switch and leakage resistance of inductor, the performance of the converter degrades. Due to these practical problems, the conventional DC-DC converters are unable to provide doable solution for step up voltage applications [15]. In theory, when a duty cycle approaches 100%, infinite voltage conversion ratio is achieved from the conventional boost converter. But in practice, inductor leakage resistance of inductor limits the voltage conversion of the converter [16]. So the traditional converters cannot be used where the required conversion ratio is four or more [16]. Furthermore, to achieve a high conversion ratio by using large duty cycle compromise the utilization of high frequency for Pulse Width Modulation (PWM) because of semiconductor control devices inherent switching delay. Unluckily, large reactive network follows the limited switching frequency which is employed to protect the ripple condition of voltage and current [17]. Traditional Buck-Boost converter is not reliable due to discontinuous input current, which results in low utilization of input source [13], [15]. By increasing the switching frequency of the converter, the problem of leakage resistance for certain values of ripple can be overcome. The finite switching time in a normal power device limits the switching frequency if the duty ratio is either too high or too small. So, in order to abolish above crisis and simultaneously acquire essential high voltage, isolated converters can be engaged. Many isolated and non isolated converter topologies are proposed over the period of time, which makes the use of inductor, coupled inductors and transformers [16-27]. The high voltage stress occurring due to the transformer leakage inductance leads to the switching losses and electromagnetic interference (EMI) problem, resulting in the reduced efficiency of conventional converters. The hard switching converters are inconvenient to use for high voltage applications due to circuit complexity, higher voltage stress across the switch and the increased cost of the converter. Hence, for isolated topologies size, weight and losses of power transformer are limiting factors. In recent, various combinations of coupled inductors, voltage multipliers or switched capacitor multipliers [23-30] along with a Switched inductor (SI), Switched capacitor (SC), voltage lift switched inductor (VLSI) and modified VLSI principles are used to accomplish the necessity [15], [26]. Figure 4(a)-(c) shows the recent inductive network of SI, VLSI and modified VLSI. For acquiring the high boost ratio, cascaded approach is introduced. To design a Cascaded Boost Converter (CBC), a number of

inductors are essential, which is the most complex part. In addition, losses and increased current ripple prove out as a barrier to achieve a high conversion ratio and better efficiency [36]-[38]. With an objective to acquire high voltage gain just by using a single switch, the Quadratic Boost converter (QBC) is proposed. Though, in Quadratic Boost converter, the higher voltage rating switches are required with higher RDS-ON, as voltage stress raised across the switch is equal to the output voltage [39-41]. Multilevel converter provides a suitable solution for power conversion because of low voltage stress across each device [42]. High voltage is achieved by multilevel DC-DC converter using the capacitors and diode circuitry at output end and the output voltage level can be increased without actually disturbing the actual circuit. By varying the number of output levels and duty cycle, the voltage gain of multilevel converter can be varied [43-44]. For conventional multilevel converters, designing magnetic components like inductor is a complex task, which also induces electromagnetic emission noise. Other than these issues the inductor and transformer in the power circuit degrades the integrating capability and increases the cost, weight and size of the converter. Switched Capacitors (SC) power circuit provides a good integrating ability due to small volume and weight, since the magnetic components like transformers and inductors is not needed to design Switched Capacitors (SC) converter [33].

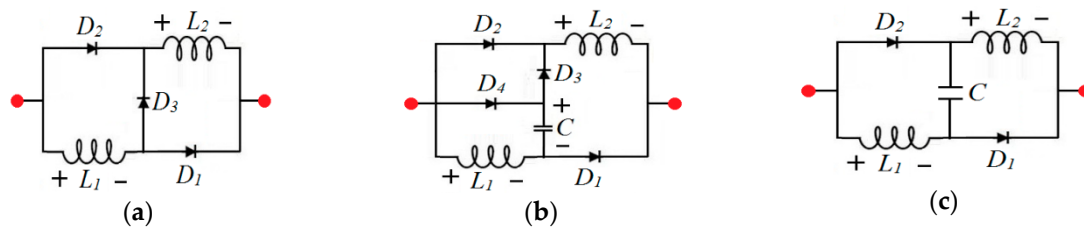



Figure 4. Inductive networks (a) Switched Inductor (b) Voltage Lift switched Inductor cell (c) modified voltage lift switched inductive cell

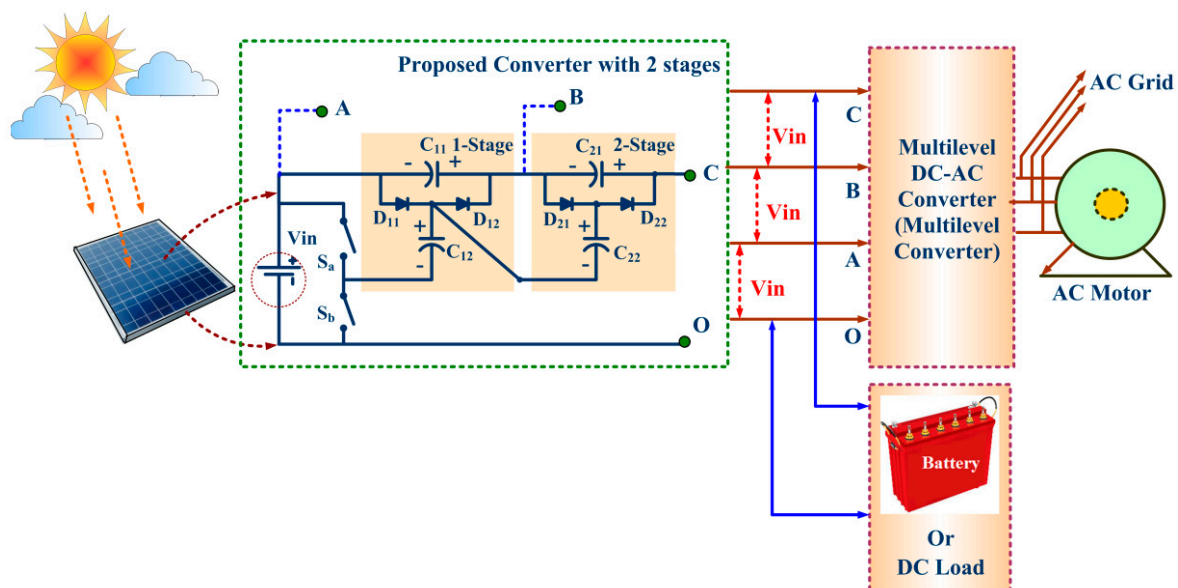



Figure 5. Proposed Multistage self balanced and magnetic component free DC-DC Converter in Photovoltaic System for transfer photovoltaic energy to DC load, grid or motor.

In this article, a new magnetic components free (Transformer-less and Inductor-less) DC-DC converter is proposed to overcome the drawback of PV-CIS, PV-SIS, PV-ACMS, PV-MSIS and above discussed converter topology. Proposed converter provides a viable solution for existing photovoltaic applications system where voltage is needed to be stepped up without magnetic component before transferring energy to Multilevel-Inverter. The single proposed converter is sufficient to transfer energy to Multilevel Inverter as shown in Figure 5. The proposed converter is also suitable for the DC link application in DC-AC system where capacitor voltage balancing is the

main challenge. The proposed converter also provides a viable solution for low power application, since the inductor and transformer are not required to design proposed converter.

2. Recent Transformer-less and Inductor-less DC-DC Converters

In this section recent transformer-less and Inductor-less DC-DC Converter power circuit topology and its drawbacks are discussed in detail. Recently various multilevel DC-DC Converter and switched Capacitor topologies without inductor are addressed in the literature.

2.1. Series-Parallel Switched Capacitor (SC) Converter

In [45-47], Series-Parallel Switched Capacitor (SPSC or Series-Parallel SC) converter is proposed using only control switching element and capacitors. In Figure 6(a) three-level Series-Parallel SC converter is depicted. The operation of this topology is simple and divided into only two modes (two switching state only). All the switches are controlled in such a ways that all the capacitors are charges in series and discharges in parallel. The conversion ratio of N-Level Series-Parallel SC Converter is 1/N (in Step-Down Mode) and N times (in Step-Up Mode). More than 90% efficiency is reported in the literature.

(a)   **(b)**

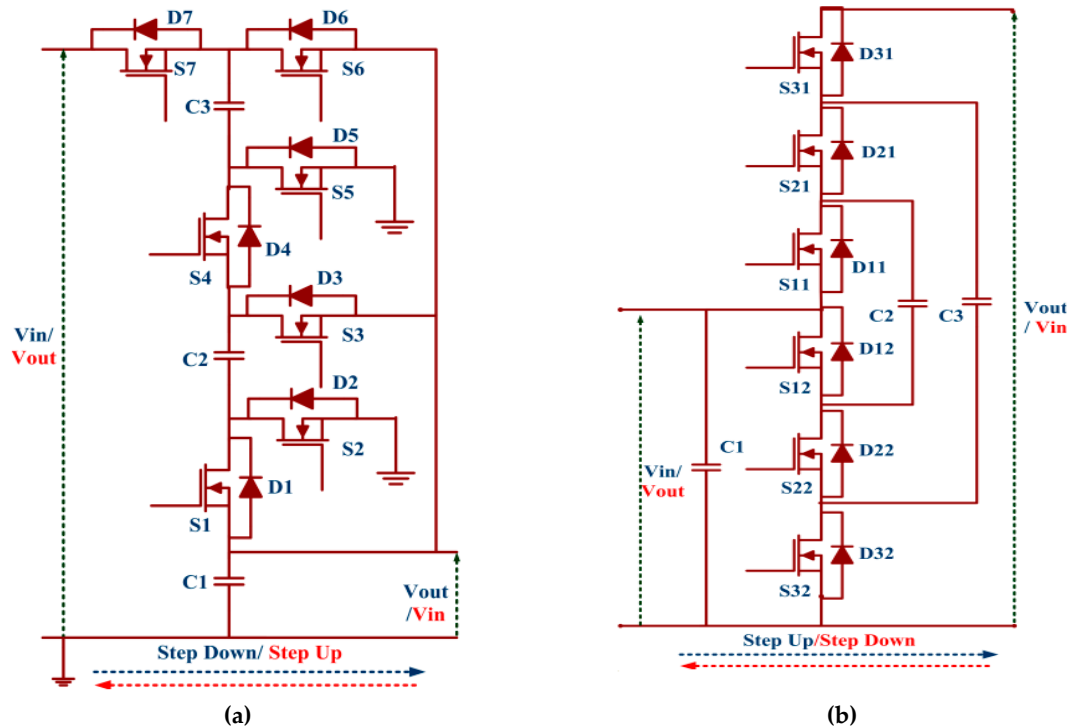



Figure 6. (a) Three–Level Series-Parallel Switched Capacitor (Series-Parallel SC) Converter **(b)** Flying Capacitor Multilevel DC-DC Converter (FCMDC)

However the Series-Parallel SC Converter has following drawbacks:
1. Difficult to change the switching state of converter due to several number of switching elements.
2. Unequal Voltage across switches. Thus, required various rating of power switches.
3. Series-parallel SC is bidirectional, but it is not possible to control the power flow. It depends on the voltages at the input and output DC Buses.
4. If switching is not properly control. It may instigate the charge unbalance situation among the capacitors of converter.
5. Non Modularity, since required large number of switches, gate drivers and diodes. And number of devices is increases with number of levels. Due to this series parallel converter is large in size and has high cost.

2.2. Flying Capacitor Multilevel DC-DC Converter (FCMDC)

In [48-49], Flying Capacitor Multilevel DC-DC Converter (FCMDC) is proposed. Figure 6(b) depicts the power circuit of three–level FCMDC. The conversion ratio) of N-Level FCNDC is 1/N (in Step-Down Mode) and N times (in Step-Up Mode). FCMDC is Bidirectional Converter with efficiency is higher than 95%. Also Voltage stress of switches is equal and thus requires same rating of switching devices. However FCMDC have following drawback:

1. Required large number of transistors and capacitors (2N number of switches and N number of capacitors are required to design N-Level FCMDC). Hence this converter is large in size and also has high cost.

2. Difficult to extend power circuit to increase the number of stages to change the output conversion ratio. Since converter does not have modular structure.

3. Complicated Switching Scheme is required to operate the converter.

4. FCMDC is inefficient at high switching frequency when ON time is comparable with rise and fall time of the switches. Since, to transfer energy from input source to the capacitors very small time frame is allowed.

5. Utilization of component is less. It is not possible to control the power circuit if anyone of the switch is fails.

2.3. Magnetic-Less Multilevel DC-DC Converter (MMDC)

In [50-51], Magnetic-Less Multilevel DC-DC Converter (MMDC) is proposed by connecting two transistor and one capacitor switching cells (Modular Block) in mesh pattern. Figure 7 depicts the power circuitry of the three-level MMDC. The conversion ratio of N-Level MMDCC is 1/N (in Step-Down Mode) and N times (in Step-Up Mode). The voltage stress of each transistor of switching cell is same and equal to V_{in} and also it is independent on the duty cycle and conversion ratio of the converter. However, Following are the drawback of the MMDC:

1. Very large number of switching devices and capacitors are required to design MMDC N(N+1) switches, N(N+1) diodes and 0.5N(N+1) capacitors are required to design the N-Level MMDCC.

2. Difficult to manage direction of power flow of converter due to more number of transistors are presents in conducting path.

3. The power flow of the converter is also depends on the voltages at the input and output DC Buses. Thus not a good option for the application where source voltage is may vary.

2.4. Fibonacci DC-DC Converter

In [52], fibonacci DC-DC converter is proposed using capacitors and switching devices circuitry. The voltage conversion ratio of the converter is follows the well-known Fibonacci series. Figure 8 depicts the power circuitry of the three stage-fibonacci Converter. High voltage is achieved but still required large number of switching devices and capacitors. Following are the drawbacks of the fibonacci DC-DC Converter:

1. Large number of control switches are required to design converter (3N+1 number of control switches are required to design N-stage Converter)

2. Fibonacci DC-DC converter follows the fibonacci series and thus it is not possible to achieve voltage conversion ratio like 2, 4….(which is not present in Fibonacci Converter)

3. Not capable to transfer power in both direction.

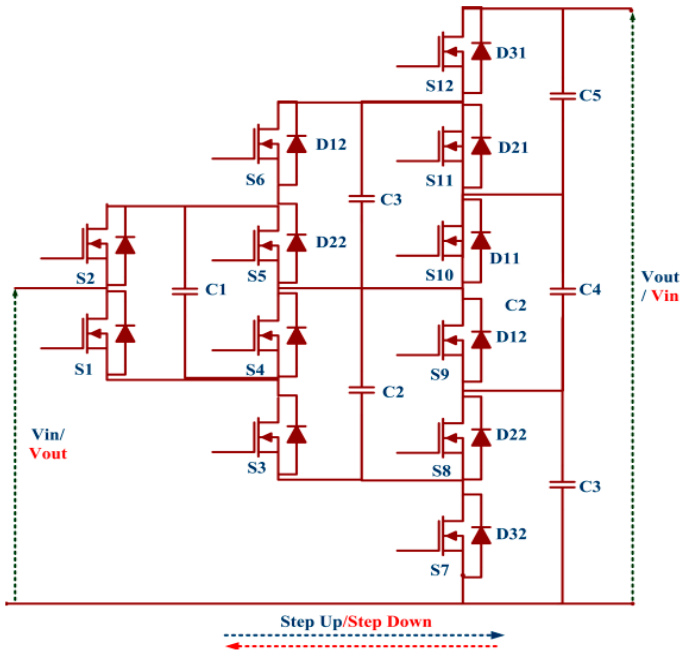



Figure 7. Three-Level Magnetic-Less Multilevel DC-DC Converter (MMDC)

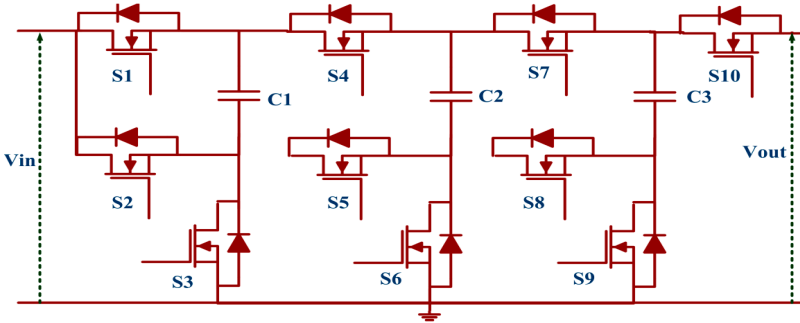



Figure 8. Three-Level fibonacci DC-DC converter

2.5. Modified Step-up DC-DC Converter (Switch Mode DC-DC Converter)

In [53], Modified Step-up DC-DC Converter (Switch Mode DC-DC Converter) is proposed which have continuous input current capability. Figure 9 depicts the Switch Mode DC-DC Converter and its power circuitry is divided into two parallel parts. The detail study about mode of operation and capacitors state is given in Table-1.

Table 1. Mode of operation and state of capacitors of Modified Step-up DC-DC Converter

Operation Mode	Switches State								Capacitors of Left Part (Section-I)	Capacitors of Right Part (Section-II)
	S1	S2	S3	S4	S5	S6	S7	S8		
Mode-I	OFF	ON	OFF	ON	ON	OFF	ON	OFF	Charging	Discharging
Mode-II	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	No action	Discharging
Mode-III	ON	OFF	ON	OFF	OFF	ON	OFF	ON	Discharging	Charging
Mode-III	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	Discharging	No Action

The operation of proposed converter is simple and conversion ratio of the converter is adjusted by varying the duty cycle. In addition, the continuous input current from low voltage input sources reduces the EMI Problem. However this converter has following drawbacks:
1. Large number of switching devices is required.
2. Introduce high switching losses and thus efficiency of the converter is less.
3. Moreover, there is not extension of the circuit to increase the voltage conversion ratio.

4. This converter is not suitable for high power high voltage application due to lower voltage conversion ratio.

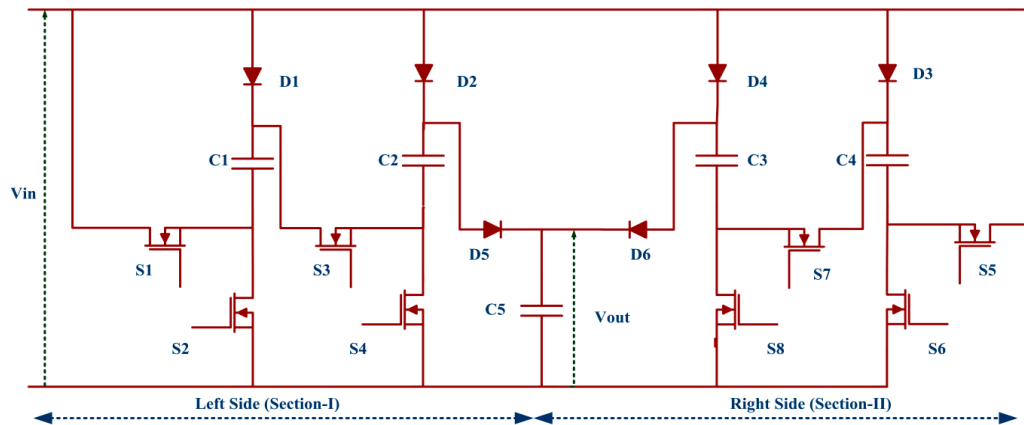



Figure 9. Modified Step-up DC-DC Converter (Switch Mode DC-DC Converter)

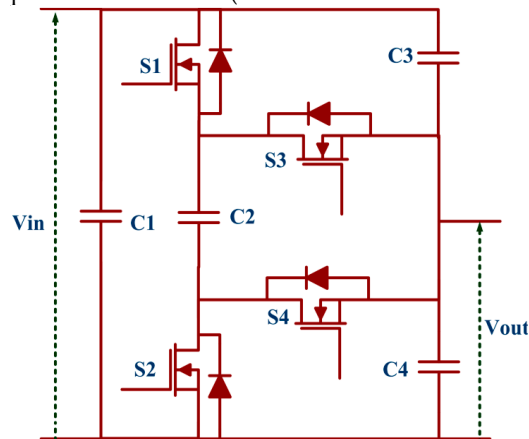



Figure 10. Switched Capacitor DC-DC Converter)

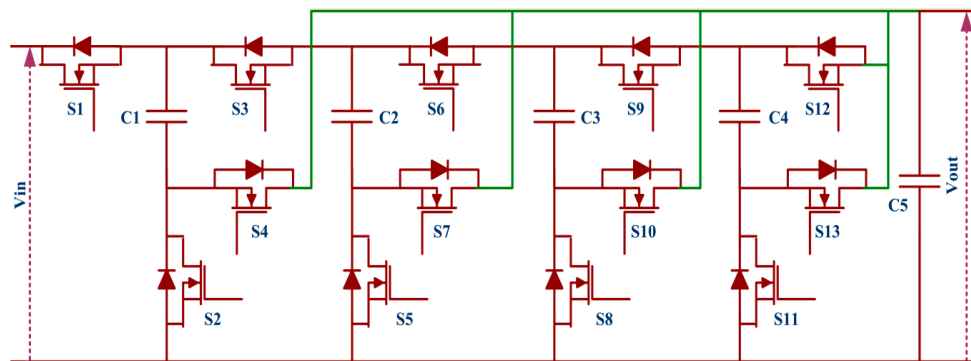



Figure 11. Multilevel Modular Capacitor Clamped DC-DC Converter (MMCCC)

2.6. Switched Capacitor DC-DC Converter

In {54], a new Switched Capacitor DC-DC Converter is proposed with low ripple input current. Figure 10 depicts the power circuit of converter. The low ripple and continuous input current helps to reduce EMI of the circuit. However circuit has no provision to increase the voltage conversion ratio.

2.7. Multilevel Modular Capacitor Clamped DC-DC Converter (MMCCC)

In [55], Multilevel Modular Capacitor Clamped DC-DC Converter (MMCCC) is proposed. Figure 11 depicts the power circuit of the MMCCC for five level. Following are the drawbacks of the MMCCC:

1. Using this topology high voltage conversion ratio is achieved but required large number of switching devices and capacitor.
2. Voltage stress across switch of the converter is high. Voltage stress of N-2 switching devices is equal to 2Vin and remaining switches have V_{in} voltage stress.

3. Self Balanced and Magnetic Component Free Multistage DC-DC Proposed Converter

The power circuit of a proposed self balanced and magnetic component free (Transformer-less and Inductor-less) multistage DC-DC converter for K stages is depicted in Figure 12. The conspicuous features of proposed topology are i) Magnetic components free ii) Continuous input current iii) Low voltage rating semiconductor devices and capacitors iv) Modularity v) Easy to add a higher number of levels to increase voltage vi) Only two control switches are used with alternating operation and vii) simple control. The proposed DC-DC converter topology is free from a magnetic component like inductors and is designed for unidirectional power transfer application. The proposed topology provides an output voltage higher than the input voltage without any magnetic component. The operation at high frequency permits a reduction in size of capacitor thus enabling the reduced size of the circuit without external components. In this topology the number of control switches does not depend on the number of levels. The required number of diodes and capacitors depend on the number of output levels. Two diodes and two capacitors are required to increase the level of the proposed converter by one. Thus, to design 4-stage proposed step-up DC-DC converter topology, two control switches, 8 uncontrolled (power diodes) and 8-capacitors are required.

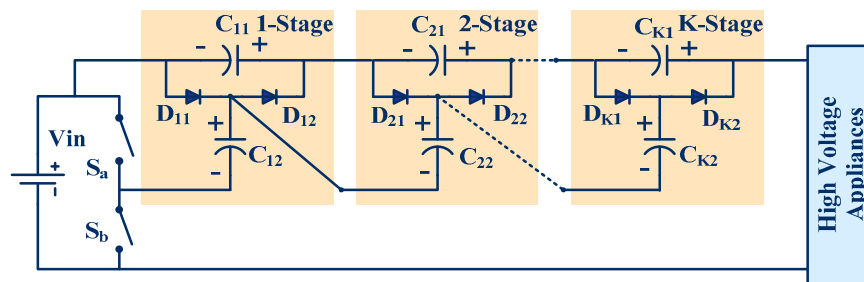



Figure 12. Self balanced and magnetic component free multistage converter for K stages

3.1. Mode of Operation

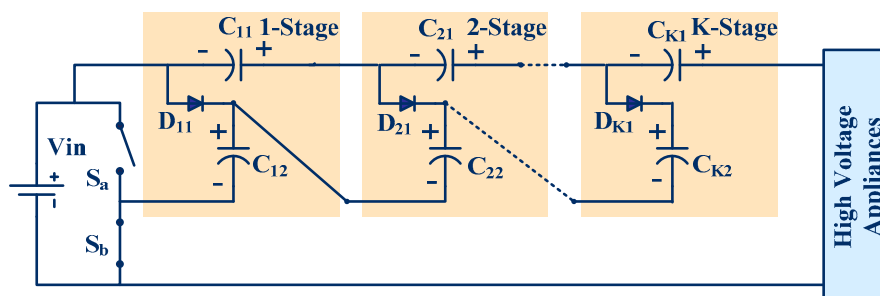



Figure 13. ON state of proposed magnetic component free multistage DC-DC converter

To explain the operation modes of proposed magnetic component free K-stages converter circuit is considered. The mode of operation of the converter is divided in two modes-mode one when switch S_b and S_a is act as short circuit (turned ON) and open circuit (turned OFF) respectively, and mode two when switch S_a and S_b is act as short circuit (turned ON) and open circuit (turned OFF) respectively. Hence, switch S_a and switch S_b are complementary in operation. The proposed topology has simple control and is operated at fixed duty cycle 0.5 to provide voltage to photovoltaic devices. The complex gate driver is also not required to drive the switch, instead an oscillator is also sufficient to provide gate signal.

In Mode1 (Figure 13), switch S_b is turned ON and switch S_a is turned OFF, capacitor C_{12} is charged by input voltage through diode D_{11} and switch S_b when the voltage across capacitor C_{12} smaller than the input voltage. When voltage across capacitors $C_{12}+C_{22}$ smaller than the voltage $V_{C11}+V_{in}$, then the energy stored in the capacitor C_{11} is transferred to capacitor C_{22} through D_{21} and switch S_b. Similarly capacitor $C_{(k-1)1}$ transfer its energy to C_{K2} when the voltage across capacitors $C_{12}+C_{22}+….+C_{K2}$ is smaller than voltage $V_{in}+V_{C11}+C_{C21}+…..+V_{C(K-1)1}$ through diode D_{K1}. And in this mode output voltage is equal to the input voltage (V_{in}) $+V_{C11}+V_{C21}+…+V_{CK1}$.

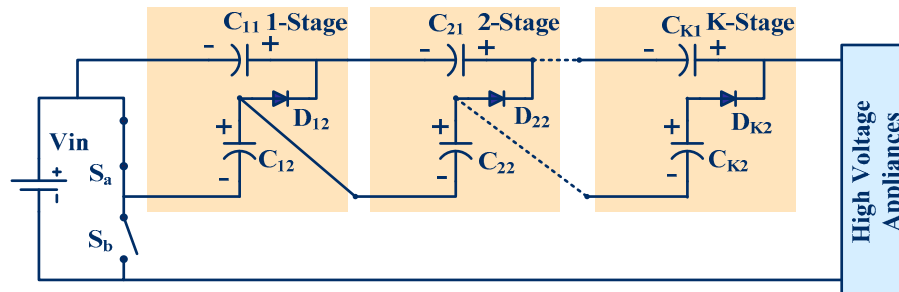



Figure 14. OFF state of proposed magnetic component free multistage DC-DC converter

In Mode2 (Figure 14), control switch S_a is turned ON and switch S_b is turned OFF, when the voltage across capacitor C_{11} is smaller than capacitor C_{12}, then capacitor C_{11} is charged by capacitor C_{12} through diode D_{12} and switch S_a. When voltage across capacitor $C_{11}+C_{21}$ smaller the voltage across capacitor $C_{12}+C_{22}$, then capacitor C_{22} transfers its energy to capacitor C_{21} through diode D_{22} and switch S_a. Similarly capacitor C_{K2} transfers its energy to capacitor C_{K1} through D_{K2} when the voltage across capacitor $C_{11}+C_{21}+…+C_{k1}$ is smaller than the voltage $C_{12}+C_{22}+C_{K2}$. And in this mode output voltage is equal to the input voltage$(V_{in})+V_{C12}+V_{C22}+…+V_{CK2}$.

3.2. Voltage Gain Analysis of Multistage Converter without Diode and Switches Loss

(**a**)   (**b**)

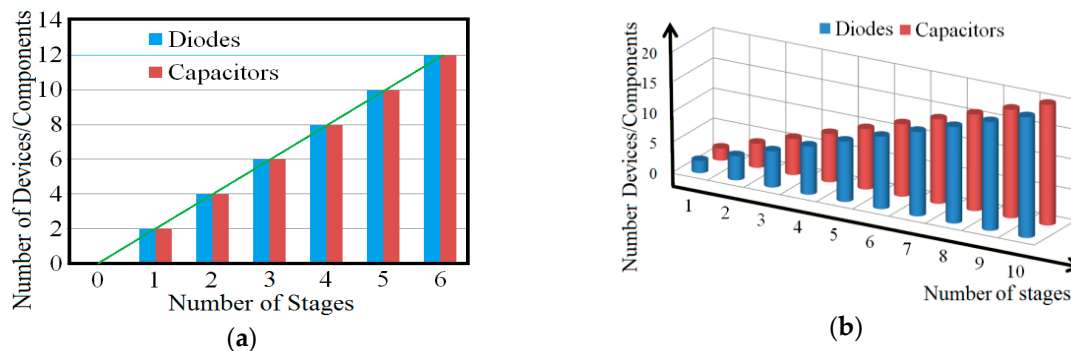



Figure 15. Number of devices/component versus number of stages (**a**) 2-dimensional view (**b**) 3-Dimensional view

When the voltage drop across diodes and switches are not considered, all capacitors are subjected to the same voltage V_{in}. The voltage conversion ratio or voltage gain is equal to the $(K+1)$ i.e. number of stages+1 and also depends on number of capacitors. Figure 15 (a)-(b) depicts the graph of required number of devices/components versus the number of stages in 2-dimensional and in 3-dimensional view respectively. From figure 15(a)-(b) it is observed that the number of devices/components are linearly increases as the number of stages are increased. Thus, with increase of each stage 2 more diodes and capacitors are needed. It is also observed that the number of diodes is equal to number of capacitors.

$$V_{C11} = V_{C12} = V_{C21} = V_{C22} = V_{CK2} = V_{in} \tag{1}$$

$$V_o = (K+1) \times V_{in} \tag{2}$$

$$V_o = \frac{K_C + 2}{2} \times V_{in} \tag{3}$$

$$V_o = \frac{K_D + 2}{2} \times V_{in} \tag{4}$$

$$K_C = K_D = 0.5\,K \tag{5}$$

Where, K_C and K_D number of capacitor and diode used to design the proposed circuit. The graph of voltage gain versus number of stages is shown in Figure 16(a). It is observed that the proposed converter with K stages provides a K+1 voltage conversion ratio. The graph of number of stage devices/Components versus voltage gain is shown in Figure 16(b). It is observed that the number of devices/components are linearly increases as the requirement of voltage gain is increased. Thus, 2 diodes and 2 capacitors are needed to be connected to increase voltage gain by factor 1. It is also observed that the 2K diodes and 2K capacitors are required to attain voltage gain K+1.

The graph of voltage gain (Vo/Vin), number of stages (K) and duty cycle (D) is shown in Figure 16(c). It is observed that 2 capacitors and 2 diodes are required to design one stage of proposed converter. The graph of output voltage for stages 1 to 9 by considering input voltage 25V is shown in Figure 16(d). It is observed that the output voltage is increased as the number of stages is increasing. And each stage contributes the voltage equal to the input voltage (25V) to an output voltage of proposed converter.

3.3. Voltage Gain Analysis of Multistage Converter with Diode and Switches Loss

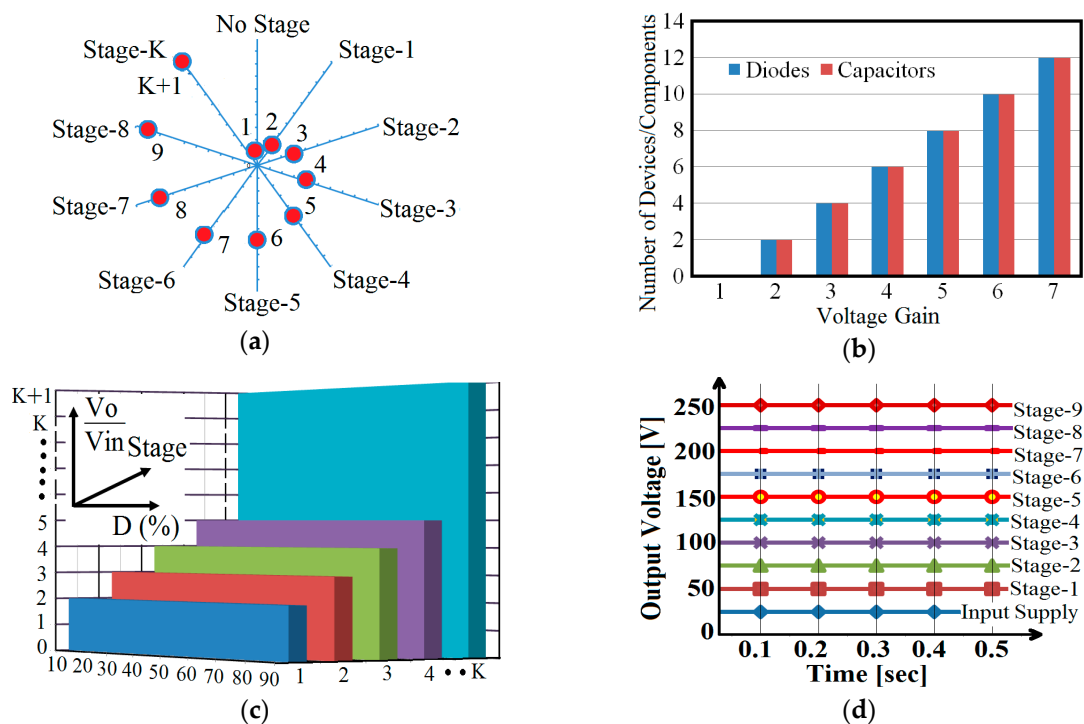



Figure 16. Relations of Converter Parameters **(a)** Graph of voltage gain versus number of stages **(b)** Graph of number of devices/component versus voltage gain **(c)** Graph of voltage gain (Vo/Vin), number of stages (K) and duty cycle (D) **(d)** Output voltage for stage 1 to 9 for 25V input voltage.

The voltage drop across power diodes and switches is ignored in medium and high power application, but in low power application it is considered. The analysis of the circuit is done with consideration of voltage drop across diodes and switches. For simplicity, the voltage drop across diodes and switches is assumed to be equal to V_d.

$$V_{C11} = V_{C12} - V_{D12} - V_{Sa} \tag{6}$$

$$V_{C11} = V_{in} - 4V_d \tag{7}$$

$$V_{C12} = V_{in} - 2V_d \tag{8}$$

$$V_{C21} = V_{C12} + V_{C22} - V_{C11} - V_{D22} - V_{Sa} = V_{in} - 4V_d \tag{9}$$

$$V_{C22} = V_{in} + V_{C11} - V_{C12} - V_{D21} - V_{Sb} = V_{in} - 4V_d \tag{10}$$

$$V_{CK1} = V_{in} - 4V_d \tag{11}$$

$$V_{CK2} = V_{in} - 4V_d \tag{12}$$

It is investigated that the voltage across each capacitor is equal to $V_{in}-4V_d$ except voltage across capacitor C_{12}. The voltage across capacitor C_{12} is equal to $V_{in}-2V_d$. Thus, proposed topology is self balanced and magnetic component free. Thus the output voltage of the converter is limited by the devices forward voltage and number of devices. The graph of proposed converter output voltage versus number of stages with practical diode (V_d=1) and ideal diode is shown in Figure 17 (a). The graph of proposed converter output voltage versus number of diodes or capacitors with practical diode (V_d=1) and ideal diode is shown in Figure 17 (b). From Figure 17(a) and 17(b) it is observed that the difference between ideal and practical output voltage increases as the requirement of number of stages, diodes and capacitor is increased. The difference in ideal and practical output voltage is depending on the number of stages of proposed converter and it is equal to $4KV_d$ as given in equation (15).

(a)   (b)

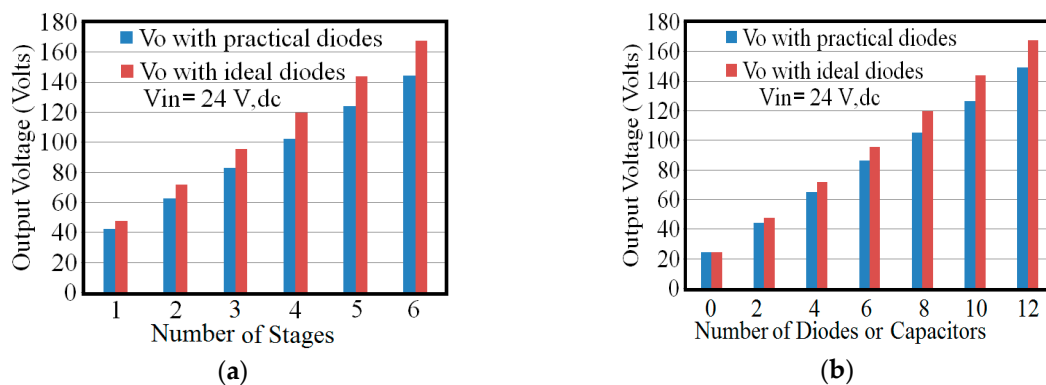



Figure 17. Comparison graph with considering Vin =24V **(a)** Graph of converter output voltage versus number of stages (practical and ideal diode) **(b)** Graph of converter output voltage versus number of diodes or capacitors (practical and ideal diode).

$$V_{C11} = V_{C21} = V_{C22} = V_{CK1} = V_{CK1} = V_{in} - 4V_d \tag{13}$$

$$V_{C12} = V_{in} - 2V_d \tag{14}$$

$$V_0 = (K+1)V_{in} - 4KV_d \tag{15}$$

4. Design Calculation of Capacitors of Proposed Converter

To explain the designed calculation of proposed converter 1-stage proposed converter is considered. Power circuit of 1-stage proposed converter is shown in figure 18(a). ON state and OFF state equivalent circuit of 1-stage proposed converter is depicted in figure 18(b) and figure 18(c) respectively, where R_D is the forward resistance of the diode, R_S is the forward resistance of the switch, I_{Sb} is current through the switch S_b and I_{Sa} is current through switch S_a.

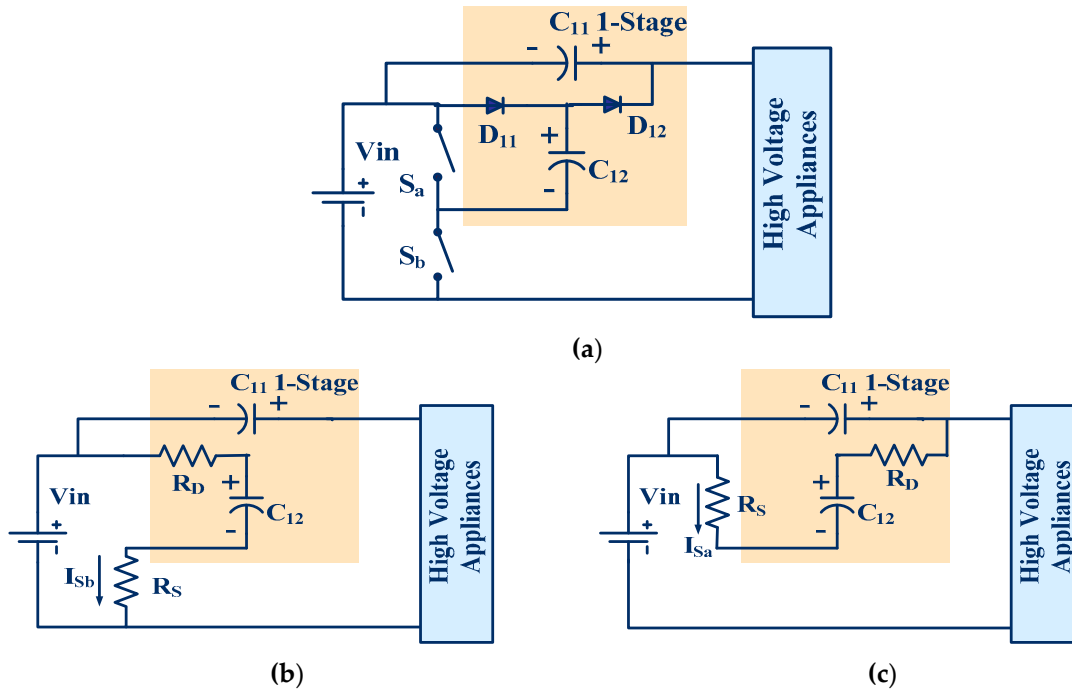



Figure 18. (a) Power circuit 1-stage of proposed converter **(b)** Equivalent circuit of ON state of 1-stage proposed converter (c) Equivalent circuit of OFF state of 1-stage proposed converter.

Initially voltage across capacitor C_{12} and C_{11} is zero. Capacitor C_{12} is charged through a resistance R_D and R_S from a supply voltage V_{in} when switch S_b is closed. Voltage across C_{12} does not increases to V_{in} instantaneously, but build up exponentially not a linearly.

$$\left.\begin{aligned}
V_{in} &= \frac{C_{12} d(v_{C12})}{dt}\left(R_D + R_S\right) + v_{C_{12}} \\
\frac{d(v_{C12})}{V_{in} - v_{C_{12}}} &= \frac{dt}{\left(R_D + R_S\right)C_{12}}
\end{aligned}\right\} \tag{16}$$

$$\left.\begin{aligned}
\int \frac{d(v_{C12})}{V_{in} - v_{C_{12}}} &= \int \frac{dt}{\left(R_D + R_S\right)C_{12}} \\
\log(V_{in} - V_{C_{12}}) &= -\frac{t}{\left(R_D + R_S\right)C_{12}} + K, \quad K = \log V_{in} \\
V_{C_{12}} &= V_{in}(1 - e^{\frac{-t}{T}}), \quad T = \left(R_D + R_S\right)C_{12}
\end{aligned}\right\} \tag{17}$$

$$V_{in} = i_{C_{12}}\left(R_D + R_S\right) + v_{C_{12}} \tag{18}$$

$$i_{C_{12}} = \frac{d(C_{12}v_{C12})}{dt} = \frac{C_{12}d(v_{C12})}{dt} \tag{19}$$

Similarly

$$i_{Sb} = \frac{V_{in}}{(R_D + R_S)}e^{\frac{-t}{T}} \tag{20}$$

Capacitor C_{11} is charged through a resistance R_D and R_S from a capacitor C_{12} voltage when switch S_a is closed. Thus, when switch S_a is closed capacitors C_{11} and C_{12} is charging and discharging respectively.

$$\left. \begin{array}{l} V_{C_{12}} = i_{C_{11}}(R_D + R_S) + v_{C1} \\ V_{C_{12}} = i_{C_{12}}(R_D + R_S) + v_{C_{11}} \end{array} \right\} \tag{21}$$

$$\left. \begin{array}{l} V_{C_{12}} = \frac{C_{11}d(v_{C11})}{dt}(R_D + R_S) + v_{C_{11}} \\ \frac{d(v_{C11})}{V_{C_{12}} - v_{C_{11}}} = \frac{dt}{(R_D + R_S)C_{11}} \end{array} \right\} \tag{22}$$

$$\left. \begin{array}{l} \int \frac{d(v_{C11})}{V_{C_{12}} - v_{C_{11}}} = \int \frac{dt}{(R_D + R_S)C_{11}} \\ \log(V_{C_{12}} - V_{C_{11}}) = -\frac{t}{(R_D + R_S)C_{11}} + K, K = \log V_{C_{12}} \\ V_{C_{11}} = V_{C_{12}}(1 - e^{\frac{-t}{T}}), T = (R_D + R_S)C_{11} \end{array} \right\} \tag{23}$$

Similarly

$$i_{Sa} = \frac{V_{C_{12}}}{(R_D + R_S)}e^{\frac{-t}{T}} \tag{24}$$

In steady state and at high switching frequency, the voltage across capacitor C_{11} and C_{12} at any instant during charging is cycle is given in equation (25) and equation (26) where, $V_{C'11}$ and $V_{C'12}$ is the initial voltage of capacitor C_{11} and C_{12}.

If initial storage voltage of C_{11} and C_{12} is positive
$$\left. \begin{array}{l} V_{C_{12}} = (V_{in} - V_{C'12})(1 - e^{\frac{-t}{T}}) + V_{C'12} \\ V_{C_{11}} = (V_{C_{12}} - V_{C'11})(1 - e^{\frac{-t}{T}}) + V_{C'11} \end{array} \right\} \tag{25}$$

If initial storage voltage of C_{11} and C_{12} is negative
$$\left. \begin{array}{l} V_{C_{12}} = (V_{in} + V_{C'12})(1 - e^{\frac{-t}{T}}) - V_{C'12} \\ V_{C_{11}} = (V_{C_{12}} + V_{C'11})(1 - e^{\frac{-t}{T}}) - V_{C'11} \end{array} \right\} \tag{26}$$

The time required for the capacitor C_{12} to attain any value of V_{C12} during the charging cycle is given in equation (27) and equation (28).

When initial voltage across capacitor is positive

$$t = T\log(\frac{V_{in} - V_{C'12}}{V_{in} - V_{C_{12}}}) = (R_D + R_S)C_{12}\log(\frac{V_{in} - V_{C'12}}{V_{in} - V_{C_{12}}}) \tag{27}$$

When initial voltage across capacitor is negative

$$t = T \log(\frac{V_{in} + V_{C'_{12}}}{V_{in} - V_{C_{12}}}) = (R_D + R_S)C_{12} \log(\frac{V_{in} + V_{C'_{12}}}{V_{in} - V_{C_{12}}}) \tag{28}$$

The time required for the capacitor C_{11} to attain any value of VC_{11} during the charging cycle is given in equation (29) and equation (30).

When initial voltage across capacitor is positive

$$t = T \log(\frac{V_{C_{12}} - V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) = (R_D + R_S)C_{11} \log(\frac{V_{C_{12}} - V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) \tag{29}$$

When initial voltage across capacitor is negative

$$t = T \log(\frac{V_{C_{12}} + V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) = (R_D + R_S)C_{11} \log(\frac{V_{C_{12}} + V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) \tag{30}$$

$$\left. \begin{array}{l} C_{12} = \dfrac{1}{2\pi fs X_{C12}} = \dfrac{1}{2\pi fs \dfrac{V_{C12}}{I_{C12}}} = \dfrac{I_{C12}}{2\pi fs V_{C12}} \\[3em] C_{11} == \dfrac{1}{2\pi fs X_{C11}} = \dfrac{1}{2\pi fs \dfrac{V_{C11}}{I_{C11}}} = \dfrac{I_{C11}}{2\pi fs V_{C11}} \end{array} \right\} \tag{31}$$

Voltage and current of all the capacitors are same during the complete switching cycle. Thus the equal rating of all capacitors is suitable to design proposed converter whose voltage rating is greater than the input voltage.

5. Comparison of Proposed Converter With Recent DC-DC Inductorless Converters

In this section proposed circuit is compared with recent transformer-less and Inductor-less DC-DC Converter (Discussed in Section 2 of this article) in terms of number of controlled switches, diodes, capacitors, voltage gain. The requirement of number of switches to design DC-DC converters is tabulated in table 2.

Table 2. Number of switches required to design DC-DC Converter

Converter Type	Number of Levels/Stages								
	1	2	3	4	5	6	7	8	N
SPSC	1	4	7	10	13	16	19	22	3N-2
FCMDC	2	4	6	8	10	12	14	16	2N
MMDC	2	6	12	20	30	42	56	72	N(N+1)
Fibonacci	4	7	10	13	16	19	22	25	3N+1
Switch Mode	4	8	12	16	20	24	28	32	4N
MMCCC	1	4	7	10	13	16	19	22	3N-2
Proposed	2	2	2	2	2	2	2	2	2

It is observed that proposed converter required less number of switches compared to recent transformer-less and Inductor-less converters. It is also observed that the requirement of switches is independent of levels of converter (only two switches are required to design proposed converter). It is also observed that the requirement of number of switches to design SPSC and MMCCC is same. The requirement of number of diodes and number of capacitors to design DC-DC converters is tabulated in table 3 and table 4 respectively. It is observed that proposed converter required less number of diodes compared to recent proposed transformer-less and inductor-less DC-DC

converter. Maximum number of diodes is required to design fibonacci converter. To design SPSC and MMCCC requirement of number of diodes is same. It is observed that proposed converter required less number of capacitors compared to MMDCC and switch mode converter. Also, proposed converter required less number of components in total compared to other converter.

Table 3.   Number of diodes required to design DC-DC Converter

Converter Type	Number of Levels								
	1	2	3	4	5	6	7	8	N
SPSC	1	4	7	10	13	16	19	22	3N-2
FCMDC	2	4	6	8	10	12	14	16	2N
MMDC	2	6	12	20	30	42	56	72	N(N+1)
Fibonacci	4	7	10	13	16	19	22	25	3N+1
Switch Mode	4	6	8	10	12	14	16	18	2N+2
MMCCC	1	4	7	10	13	16	19	22	3N-2
Proposed	2	4	6	8	10	12	14	16	2N

Table 4.   Number of capacitors required to design DC-DC Converter

Converter Type	Number of Levels								
	1	2	3	4	5	6	7	8	N
SPSC	1	2	3	4	5	6	7	8	N
FCMDC	1	2	3	4	5	6	7	8	N
MMDCC	1	3	6	10	15	21	28	36	N(N+1)/2
Fibonacci	1	2	3	4	5	6	7	8	N
Switch Mode	3	5	7	9	11	13	15	17	2N+1
MMCCC	1	2	3	4	5	6	7	8	N
Proposed	2	4	6	8	10	12	14	16	2N

Table 5.   Voltage Conversion ratio of the DC-DC Converter

Converter Type	Number of Levels								
	1	2	3	4	5	6	7	8	N
SPSC	1	2	3	4	5	6	7	8	N
FCMDC	1	2	3	4	5	6	7	8	N
MMDCC	1	2	3	4	5	6	7	8	N
Fibonacci	1	3	5	8	Not feasible to design for higher levels				
Switch Mode	2	3	4	5	6	7	8	9	N+1
MMCCC	1	2	3	4	5	6	7	8	N
Proposed	2	3	4	5	6	7	8	9	N+1

In Figure 19(a)-(d) proposed converter is compared with DC-DC converters (discussed in section 2) in terms of number of switches, diodes, capacitors and voltage gain.   Graphically it is also observed that proposed converter provides a viable solution in term of number of components. In Table 6 proposed converter is compared in terms of cost. And it is calculated that proposed converter required less cost compared to other DC-DC converters. Only two switches are required to design N-stage proposed converter hence required simple control circuit.

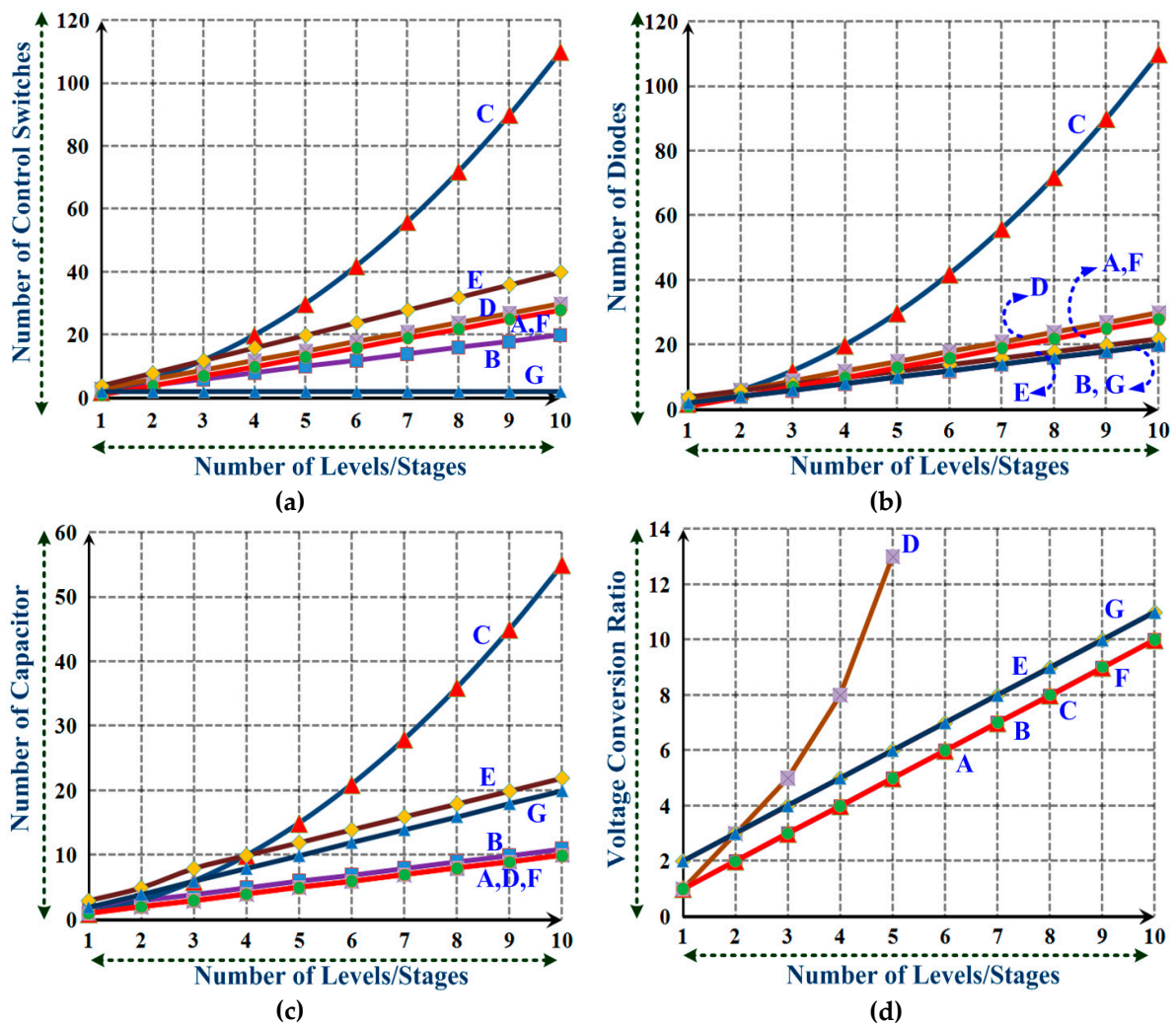



Figure 19. Comparison of proposed converter with recent transformer-less and inductor-less Converters (Discussed in section 2) **(a)** Graph of number of switches versus number of levels/stages **(b)** Graph of number of diodes versus number of levels/stages **(c)** Graph of number of capacitors versus number of levels/stages **(d)** Graph of voltage Conversion ratio versus number of levels/stages. (A: SPSC, B: FCMDC, C: MMDCC, D: Fibonacci, E: Switch Mode, F: MMCCC, G: Proposed Converter)

Table 6. Cost of the proposed and recent DC-DC Converter (Discussed in section 2)

Converter	Costing of converter
SPSC	3N-2 (Cost of each switch + cost of each diode) +N (cost of each capacitor)
FCMDC	2N (Cost of each switch + cost of each diode) + N(cost of each capacitor)
MMDCC	N(N+1){ (Cost of each switch + cost of each diode) + 0.5 (cost of each capacitor)}
Fibonacci	3N+1 (Cost of each switch + cost of each diode) +N (cost of each capacitor)
Switch Mode	4N (Cost of each switch) +2(N+1)(cost of each diode) + (2N+1)cost of each capacitor)
MMCCC	3N-2 (Cost of each switch + cost of each diode) + N (cost of each capacitor)
Proposed	2 (Cost of each switch) +2N (cost of each diode + cost of each capacitor)

6. Experimental and Simulation Result of Self Balanced and Magnetic Component Free Multistage DC-DC Proposed Converter

The proposed self balanced and magnetic component free multistage DC-DC converter simulation and experimental result are discussed in this section. The proposed multistage converter has been designed for four stages with rated power 60W, switching frequency 100 kHz, output voltage is 100V and the supply voltage is 24V. Switches S_a (here S_1) and S_b (here S_2) are operated complementary with duty cycle 50%. High switching frequency is used to reduce the rate of the capacitor.

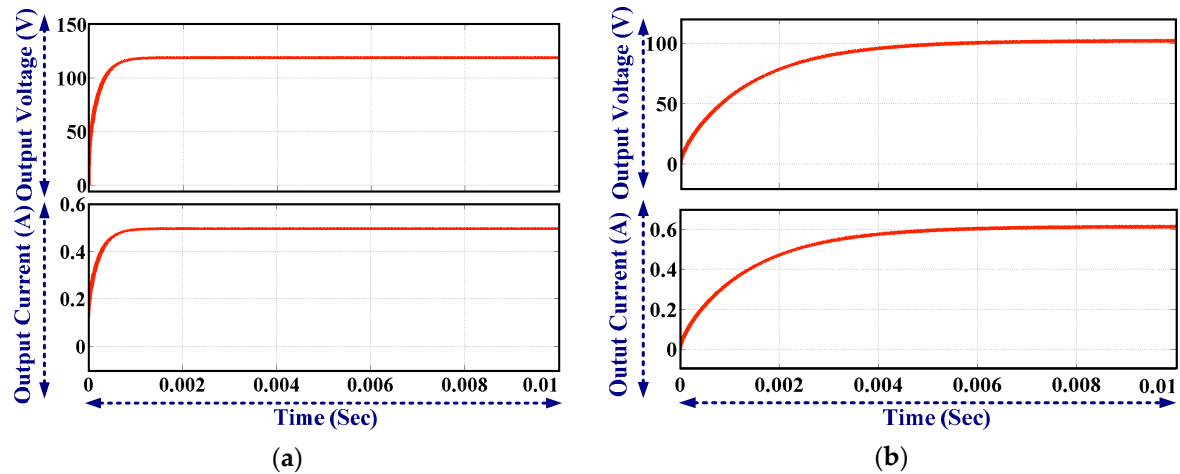



Figure 20. Simulation results **(a)** Output voltage and current waveform with ideal components and Vin =24V **(b)** Output voltage and current waveform with practical component and Vin =24V

(e)

(f)

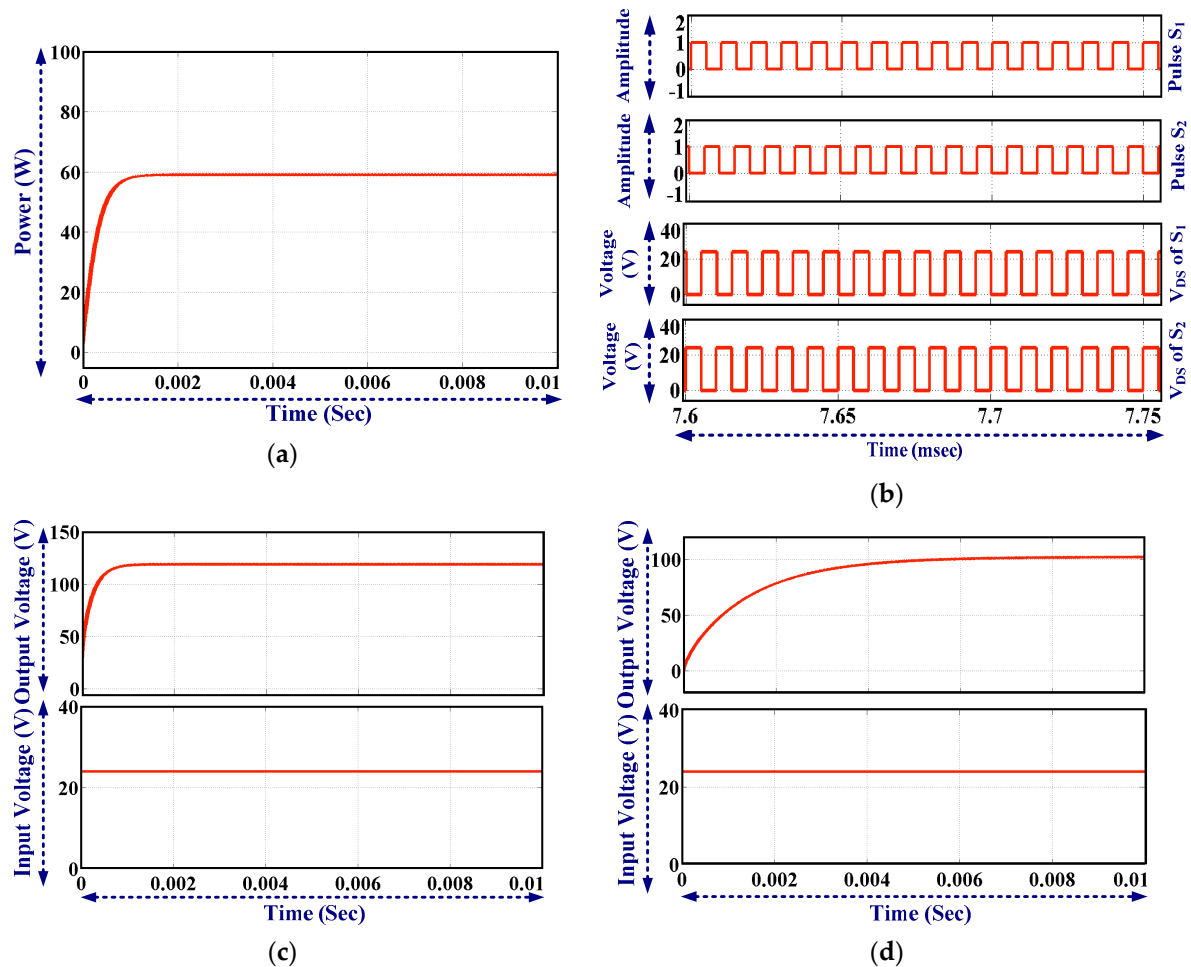
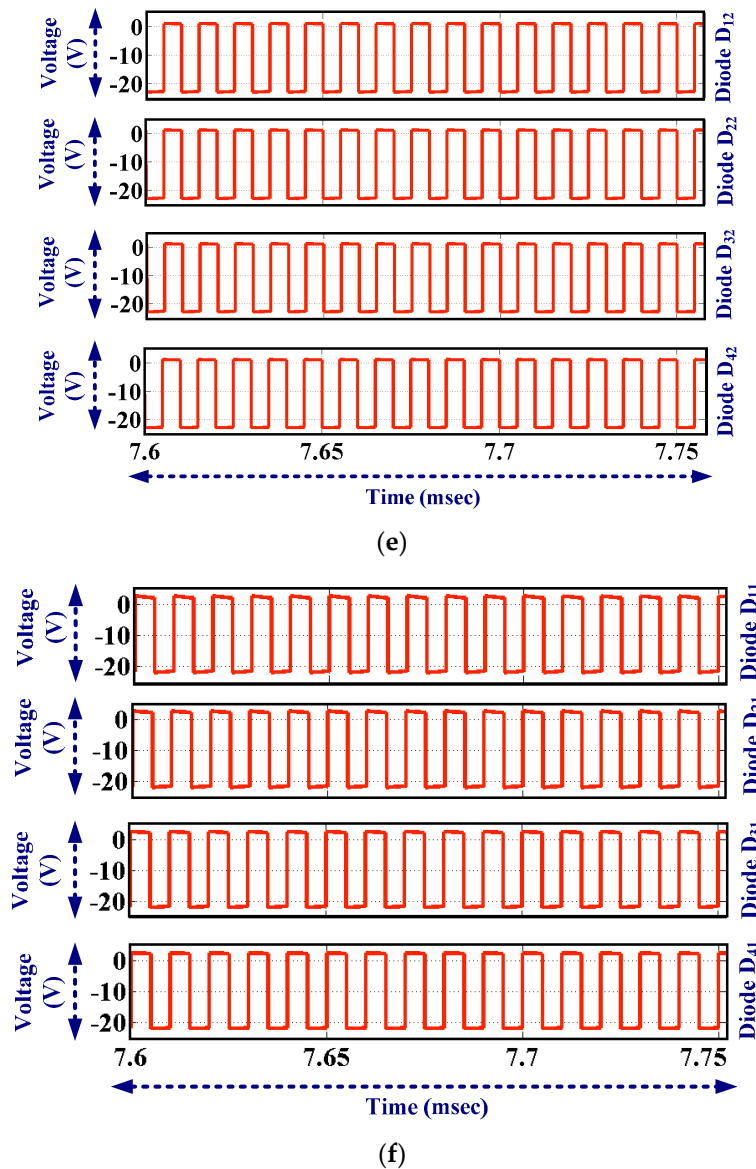



Figure 21. Simulation results **(a)** Output power of proposed converter. **(b)** Gate pulses to control switches of the converter and drain to source of the converter **(c)** Output voltage and input voltage waveform with ideal components **(e)** Output voltage and input voltage waveform with practical components **(f)** Voltage across diode D_{11}, D_{21}, D_{31} and D_{41} **(g)** Voltage across diode D_{12}, D_{22}, D_{32} and D_{42}.

The output voltage and current waveform with ideal components (voltage drop across the switch and the diode is zero) is shown in Figure 20(a). It is observed that the settling time for the output voltage of the proposed converter with ideal component (Forward resistance of the diode is 0) is less than 2msec. The effect of voltage drop across the diode is analyzed in the previous section. The output voltage and current waveform (Assume 1 V voltage drop across the switch and diode) are shown in Figure 20(b). It is observed that the settling time for the output voltage of the proposed converter with practical component is 4msec approx due to the forward resistance of the diode and switch. Thus, practical waveform is differ than ideal waveform because of time constant $(R_D+R_s)C$ as explained in section 4. The output power waveform and switch voltage is shown in Figure 21(a) and 21(b) respectively. The output voltage and input voltage waveform with ideal components (voltage drop across the switch and the diode is zero) is shown in Figure 21(c). The output voltage and input voltage waveform (Assume 1 V voltage drop across the switch and diode) are shown in Figure 21(d).

It is observed that 120V output voltage is achieved from 24V input Supply. Thus, ideally the voltage gain of the proposed converter is 5, which is equal to the number of stages+1. When the voltage drop across the diode is considered, output voltage 100V is achieved from supply 24V. The voltage across the switch is equal to the input supply voltage (24V). The voltage across all capacitors is same, which is equal to the input supply voltage (24V) if the voltage drop across the diode is not considered. The voltage across all diode is same (24 V) when the diode is reversed biased. The voltage across diodes is shown in Figure 21(f)-(g). The voltage across the capacitors is shown in Figure 22. The proposed 4-stage self balanced and magnetic DC-DC converter is investigated experimentally and the result shows a good match with the simulation results. The hardware components are listed in Table 7.

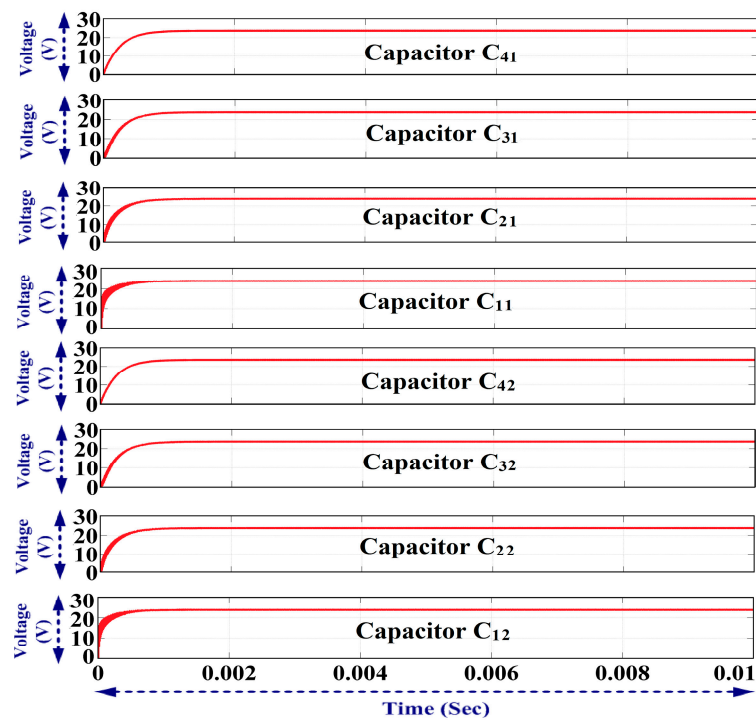



Figure 22. voltage across capacitor C_{41}, C_{31}, C_{21} C_{11}, C_{42}, C_{32}, C_{22} and C_{12} (Top to bottom in figure)

PIC18F45K20 is used to generate pulses and TLP250 is used as driver IC. The hardware prototype of proposed converter is shown in Figure 23. Pulses are generated from PIC controller and gate driver output is shown in Figure 24(a) and Figure 24(b) respectively. Output voltage and input voltage waveform are shown in Figure 24(c). It is observed that 100V output is achieved from input supply 24V.

Table 7. Hardware Component Detail of proposed converter

Sr/No	Components	Value	No. of components
1	Switch (S_1 and S_2)	IRF250 (0.085 ON sate resistance)	2
2	Diodes	BYQ28E	8
3	Capacitors	220uF, 50V	8
4	Load	168 Ω, 60W	1
5	Gate Driver IC	TLP250	2

The output current waveform is shown in Figure 24(d) and it is observed that the output current is 0.619 A. The voltage across each capacitor is shown in Figure 25(a)-(h). It is observed that the voltage across each capacitor is nearly same and slightly less than the input voltage 24V (effect of diode). Voltage stress across each diode is shown in Figure 26(a)-(h). It is observed that voltage stress across the diode is the approximately same and the peak voltage across the diode is slightly

less than the input voltage (24V) (effect of drop). Slightly voltage of all capacitors and all diodes are differs due to the forward resistance of the diode and switch. The lower stages (source side) capacitors are charges through the path which contain less number of diodes whereas as the number of stages increases the path followed for the charging of higher stage (moving towards load) capacitor of contain more number of diodes. Thus, practically slight difference is observed in the voltage of capacitors.

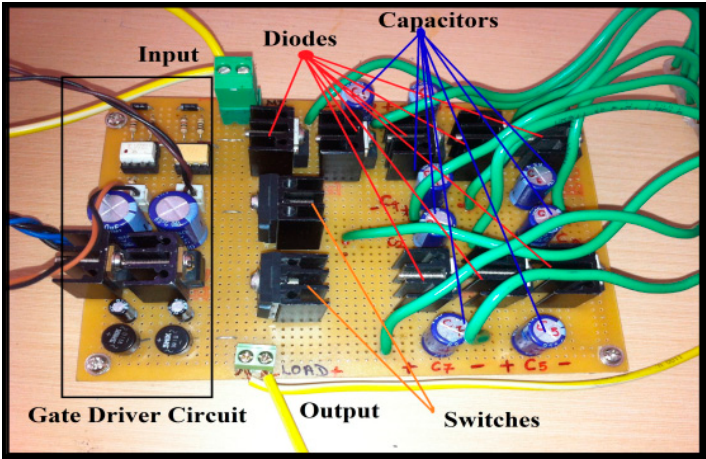



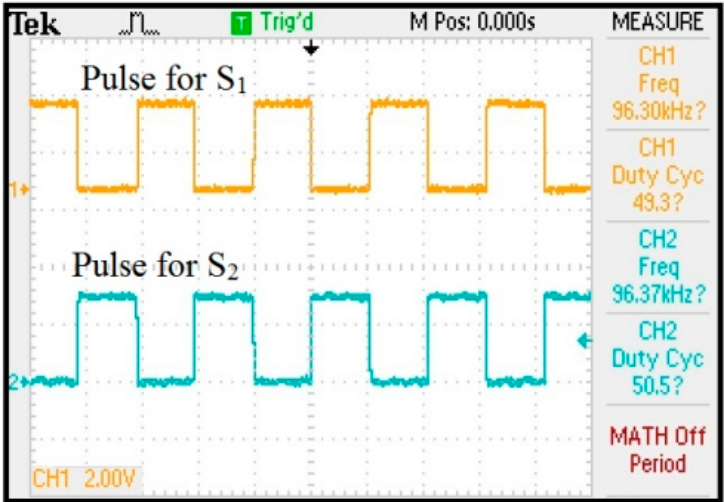
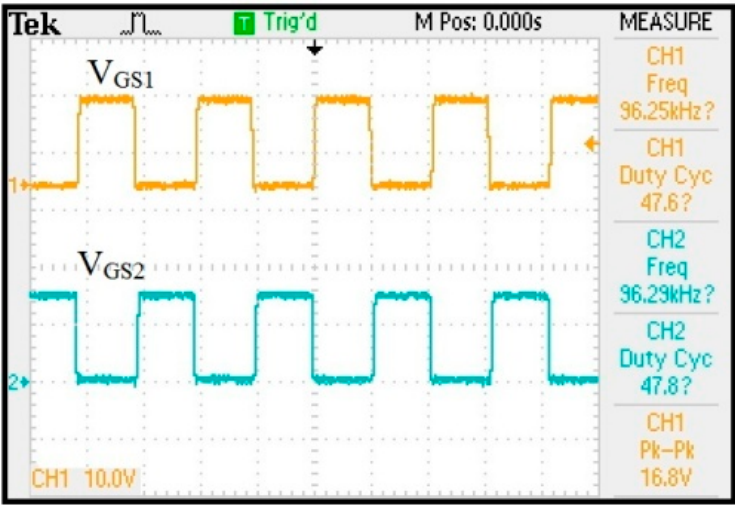
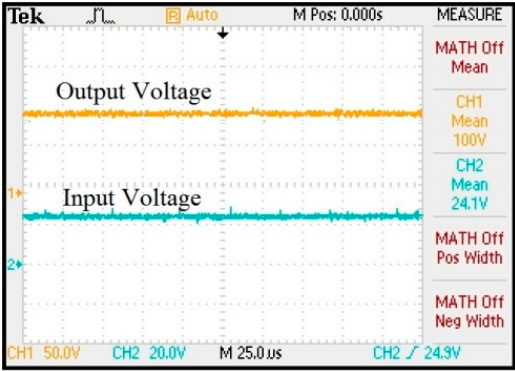
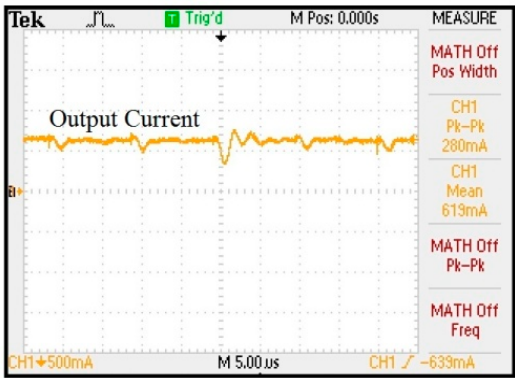
Figure 23. Hardware Prototype of Proposed DC-DC Converter

(a)

(b)

(c)	(d)

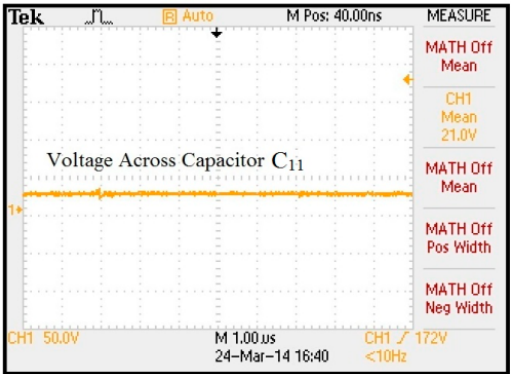
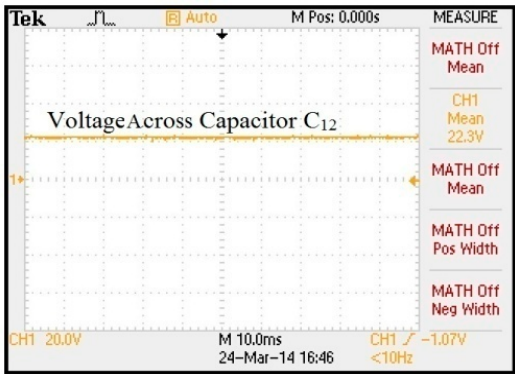
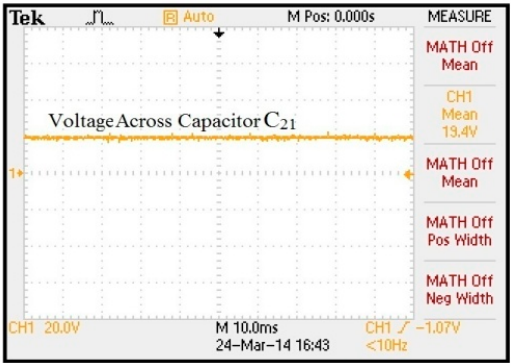
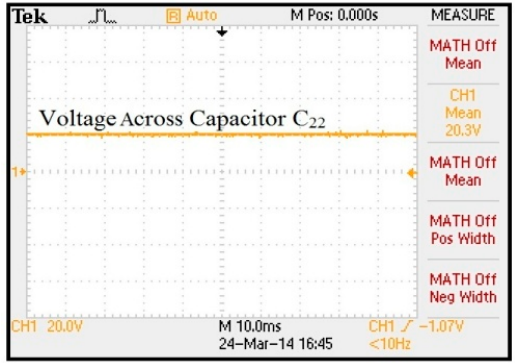
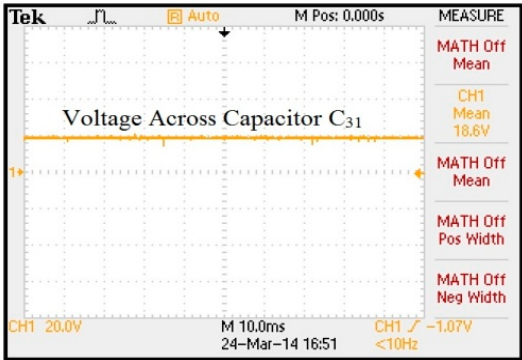
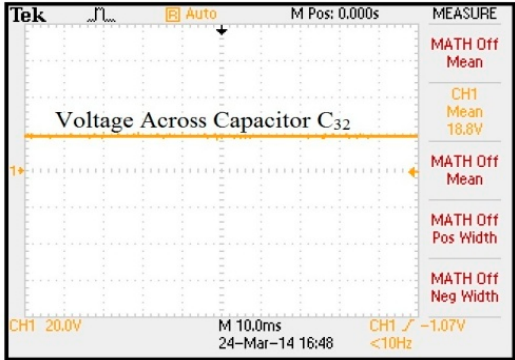
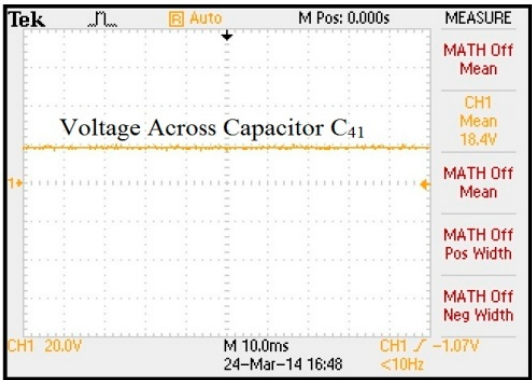
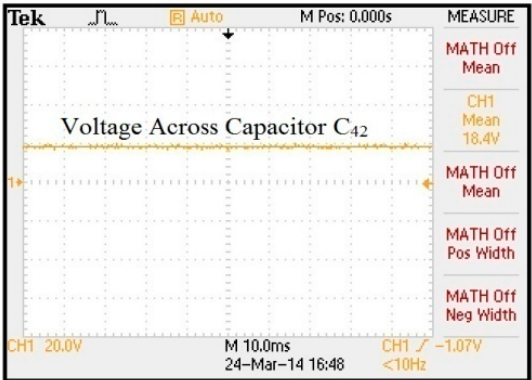
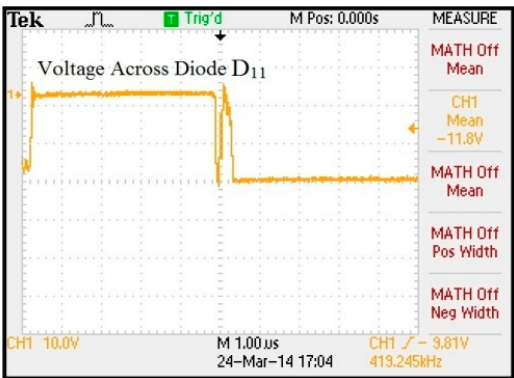
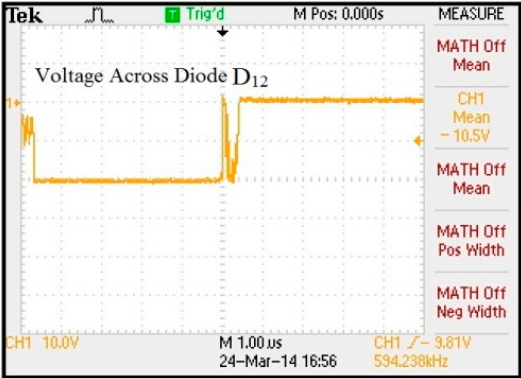
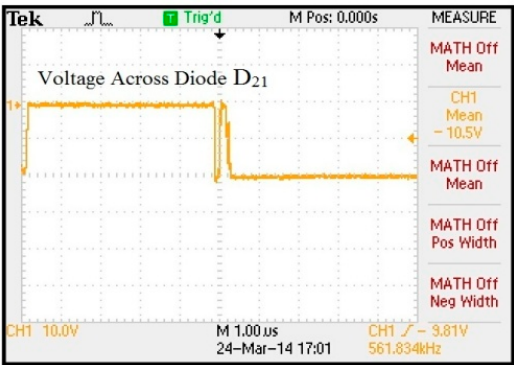
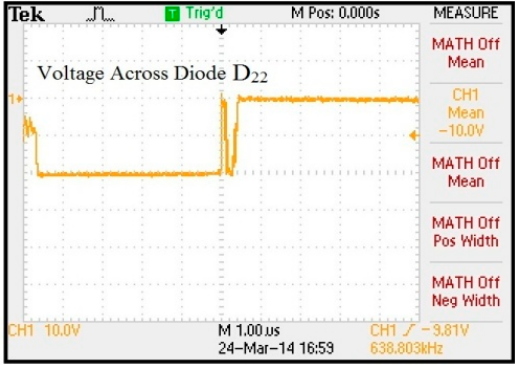
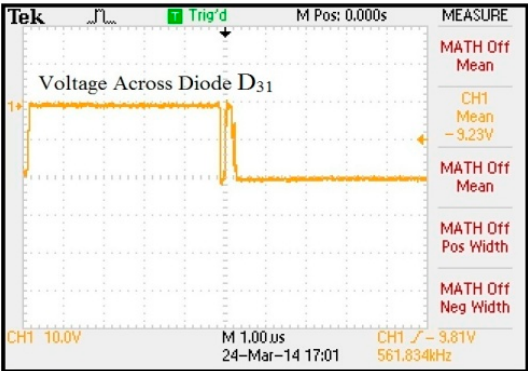
Figure 24(a) PIC controller output **(b)** TLP 250 gate driver output **(c)** Output voltage and input voltage waveform **(d)** Output current waveforms.

(a) VC$_{11}$= 21.0V **(b) VC$_{12}$= 22.3V**

(c) VC$_{21}$= 19.4V **(d) VC$_{22}$= 20.3V**

(e) VC$_{31}$= 18.6V **(f) VC$_{32}$= 18.8V**

(g) VC₄₁= 18.4V　　　　　　　　**(h) VC₄₂= 18.8V**

Figure 25. Capacitors voltage **(a)** C₁₁ **(b)** C₁₂ **(c)** C₂₁ **(d)** C₂₂ **(e)** C₃₁ **(f)** C₃₂ **(g)** C₄₁ **(h)** C₄₂

(a) MeanVD₁₁ = -11.8V　　　　　**(b) Mean VD₁₂= -10.5 V**

(c) MeanVD₂₁= -10.5V　　　　　　**(d) Mean VD₂₂= -10 V**

(e) MeanVD₃₁= -9.23V　　　　　　**(f) Mean VD₃₂= -9.69V**

(g) MeanVD$_{41}$= -8.85V   **(h) Mean VD$_{42}$= -9.24V**

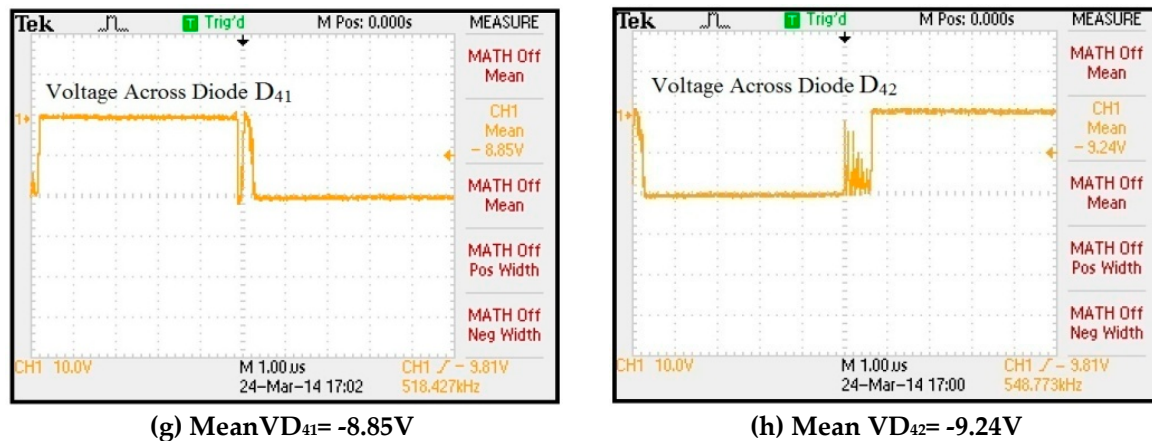



Figure 26. Voltage across diodes **(a)** D$_{11}$ **(b)** D$_{12}$ **(c)** D$_{21}$ **(d)** D$_{22}$ **(e)** D$_{31}$ **(f)** D$_{32}$ **(g)** D$_{41}$ **(h)** D$_{42}$

7. Conclusion

The self biased and magnetic free multistage step-up converter is articulated and designed for unidirectional renewable photovoltaic applications. The proposed converter is well suited for renewable photovoltaic application where voltage needs to be stepped up without using magnetic component. The proposed converter also provides a viable solution to improve the photovoltaic systems in term of modularity, cost and control. The proposed converter is suitable for the DC link application in DC-AC system where capacitor voltage balancing is the main challenge. The proposed converter also provides a viable solution to low power application, since the inductor and transformer are not required to design proposed converter. Also Maximum Power Point Tracking (MPPT) can be easily implemented to improve the efficiency of the converter. The voltage across the switch is less hence low voltage switches are used for designing high voltage converter. The conspicuous features of proposed topology are:

i)   Magnetic components free (Transformer-less and Inductorless)
ii)   Continuous input current
iii)   Low voltage rating semiconductor devices and capacitors
iv)   Modularity
v)   Easy to add a higher number of levels to increase voltage
vi)   Only two control switches with alternating operation and simple control.

The proposed converter has been designed with rated power of 60 W, input voltage is 24 V, output voltage is 100 V and switching frequency is 100 kHz. High switching frequency has been used to decrease component size. The performance of the proposed converter is verified through simulation results and experimental results.

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