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Article

Multistage DC-DC Step-Up Self Balanced and Magnetic Component Free Converter for Photovoltaic Applications – Hardware Implementation

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Abstract: This article presents a self balanced multistage DC-DC step-up converter for photovoltaic applications. Proposed converter topology is designed for unidirectional power transfer and provides a doable solution for photovoltaic applications where voltage is required to be stepped up without magnetic components. The output voltage obtained from renewable sources will be low and must be stepped up by using a DC-DC converter for photovoltaic applications. (2K-2) diodes and (2K-2) capacitors along with two semiconductor switch are used in the proposed converter to obtain an output voltage which is (K+1) times the input voltage. The conspicuous features of proposed topology are i) Magnetic components free ii) Continuous input current iii) Low voltage rating semiconductor devices and capacitors iv) Modularity v) Easy to add a higher number of levels to increase voltage gain vi) Only two control switches with alternating operation and simple control. The proposed converter has been designed with rated power of 60W, input voltage is 24V, output voltage is 100V and switching frequency is 100 kHz. The performance of the converter is verified through experimental and simulation results.

Keywords: DC-DC; Self Biased; Magnetic component Free; Multistage; Step-up; Photovoltaic application.

1. Introduction

The renewable energy resources are getting popular and trendy with the increase in demand and cost of energy. The proper utilization of energy resources is one of the most important issues of the present century. There are various renewable energy resources with zero pollution emission consisting of solar, tidal, wind, bio, nuclear and geothermal. Solar energy is free, inexhaustible source of energy and is increasingly competitive with other energy sources. This energy is utilized with the help of arrays, consisting of a number of solar panels, connected in series [1-3]. The output obtained from the photo voltaic cell/array is usually low, so before feeding this voltage to the inverter for practical application purpose, it is needed to be stepped up using conventional DC-DC boost converter [1-10]. With the increase in the duty-cycle of switch and leakage resistance of inductor, the performance of the converter degrades. Due to these practical problems, the conventional DC-DC converters are unable to provide doable solution for step up voltage applications [10]. In theory, when a duty cycle approaches 100%, infinite voltage conversion ratio is achieved from the conventional boost converter. But in practice, inductor leakage resistance of inductor limits the voltage conversion of the converter [11]. So the traditional converters cannot be used where the required conversion ratio is four or more [11]. Furthermore, to achieve a high conversion ratio by using large duty cycle compromise the utilization of high frequency for Pulse Width Modulation (PWM) because of semiconductor control devices inherent switching delay.

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Unluckily, large reactive network follows the limited switching frequency which is employed to protect the ripple condition of voltage and current [12]. Traditional Buck-Boost converter is not reliable due to discontinuous input current, which results in low utilization of input source [8], [10]. By increasing the switching frequency of the converter, the problem of leakage resistance for certain values of ripple can be overcome. The finite switching time in a normal power device limits the switching frequency if the duty ratio is either too high or too small. So, in order to abolish above crisis and simultaneously acquire essential high voltage, isolated converters can be engaged. Many isolated and non isolated converter topologies are proposed over the period of time, which makes the use of inductor, coupled inductors and transformers [11-22]. The high voltage stress occurring due to the transformer leakage inductance leads to the switching losses and electromagnetic interference (EMI) problem, resulting in the reduced efficiency of conventional converters. The hard switching converters are inconvenient to use for high voltage applications due to circuit complexity, higher voltage stress across the switch and the increased cost of the converter. Hence, for isolated topologies size, weight and losses of power transformer are limiting factors. In recent, various combinations of coupled inductors, voltage multipliers or switched capacitor multipliers [23-30] along with a Switched inductor (SI), Switched capacitor (SC), voltage lift switched inductor (VLSI) and modified VLSI principles are used to accomplish the necessity [10], [21]. Figure 1(a)-(c) shows the recent inductive network of SI, VLSI and modified VLSI. For acquiring the high boost ratio, cascaded approach is introduced. To design a Cascaded Boost Converter (CBC), a number of inductors are essential, which is the most complex part. In addition, losses and increased current ripple prove out as a barrier to achieve a high conversion ratio and better efficiency [31]-[33]. With an objective to acquire high voltage gain just by using a single switch, the Quadratic Boost converter (QBC) is proposed. Though, in Quadratic Boost converter, the higher voltage rating switches are required with higher R_{DS}-ON, as voltage stress raised across the switch is equal to the output voltage [34-36]. Multilevel converter provides a suitable solution for power conversion because of low voltage stress across each device [37]. High voltage is achieved by multilevel DC-DC converter using the capacitors and diode circuitry at output end and the output voltage level can be increased without actually disturbing the actual circuit. By varying the number of output levels and duty cycle, the voltage gain of multilevel converter can be varied [38-39]. For conventional multilevel converters, designing magnetic components like inductor is a complex task, which also induces electromagnetic emission noise. Other than these issues the inductor and transformer in the power circuit degrades the integrating capability and increases the cost, weight and size of the converter. Switched Capacitors (SC) power circuit provides a good integrating ability due to small volume and weight, since the magnetic components like transformers and inductors is not needed to design Switched Capacitors (SC) converter [28]. In this paper self balanced multistage DC-DC step up converter is proposed which provides a viable solution for renewable photovoltaic applications where voltage is needed to be stepped up without magnetic component. The proposed converter is also suitable for the DC link application in DC-AC system where capacitor voltage balancing is the main challenge. The proposed converter also provides a viable solution for low power application, since the inductor and transformer are not required to design proposed converter.

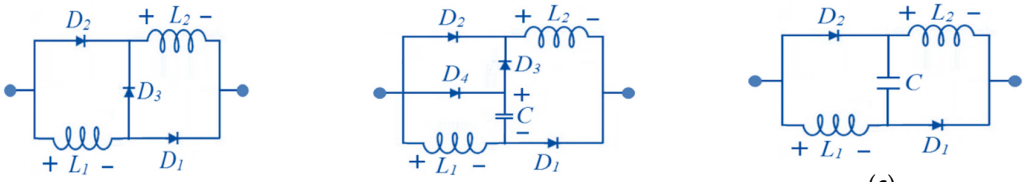

Figure 1. Inductive networks **(a)** Switched Inductor **(b)** Voltage Lift switched Inductor cell **(c)** modified voltage lift switched inductive cell

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2. Self Balanced and Magnetic Component Free Multistage DC-DC Proposed Converter

The power circuit of a proposed self balanced and magnetic component free multistage DC-DC converter for K stages is depicted in Figure 2. The conspicuous features of proposed topology are i) Magnetic components free ii) Continuous input current iii) Low voltage rating semiconductor devices and capacitors iv) Modularity v) Easy to add a higher number of levels to increase voltage vi) Only two control switches are used with alternating operation and vii) simple control. The proposed DC-DC converter topology is free from a magnetic component like inductors and is designed for unidirectional power transfer application. The proposed topology provides an output voltage higher than the input voltage without any magnetic component. The operation at high frequency permits a reduction in size of capacitor thus enabling the reduced size of the circuit without external components. In this topology the number of control switches does not depend on the number of levels. The required number of diodes and capacitors depend on the number of output levels. Two diodes and two capacitors are required to increase the level of the proposed converter by one. Thus, to design 5-level proposed step-up DC-DC converter topology, two control switches, 8 uncontrolled (power diodes) and 8-capacitors are required.

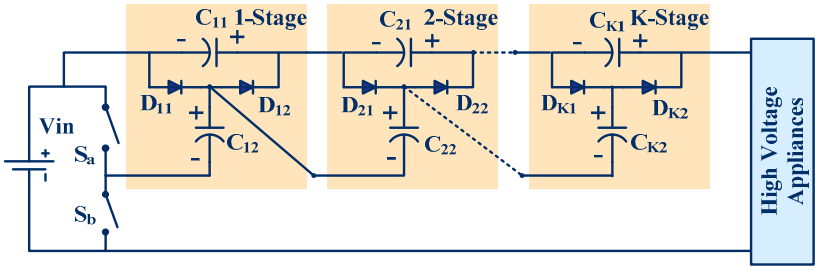

Figure 2. Self balanced and magnetic component free multistage converter for K stages

2.1. Mode of Operation

To explain the operation modes of proposed magnetic component free K-stages converter circuit is considered. The mode of operation of the converter is divided in two modes-mode one when switch S_b and S_a is act as short circuit (turned ON) and open circuit (turned OFF) respectively, and mode two when switch S_a and S_b is act as short circuit (turned ON) and open circuit (turned OFF) respectively. Hence, switch S_a and switch S_b are complementary in operation. The proposed topology has simple control and is operated at fixed duty cycle 0.5 to provide voltage to photovoltaic devices. The complex gate driver is also not required to drive the switch, instead an oscillator is also sufficient to provide gate signal.

In Mode1 (Figure 3), switch S_b is turned ON and switch S_a is turned OFF, capacitor C_{12} is charged by input voltage through diode D_{11} and switch S_b when the voltage across capacitor C_{12} smaller than the input voltage. When voltage across capacitors $C_{12}+C_{22}$ smaller than the voltage $V_{C11}+V_{in}$, then the energy stored in the capacitor C_{11} is transferred to capacitor C_{22} through D_{21} and switch S_b. Similarly capacitor $C_{(k-1)1}$ transfer its energy to C_{K2} when the voltage across capacitors $C_{12}+C_{22}+\ldots.+C_{K2}$ is smaller than voltage $V_{in}+V_{C11}+C_{C21}+\ldots..+V_{C(K-1)1}$ through diode D_{K1}. And in this mode output voltage is equal to the input voltage (V_{in}) $+V_{C11}+V_{C21}+\ldots+V_{CK1}$.

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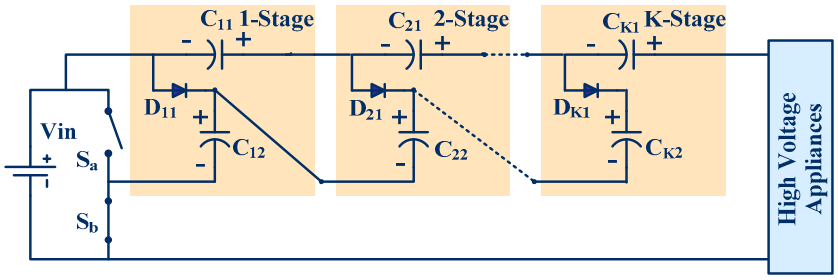

Figure 3. ON state of proposed magnetic component free multistage DC-DC converter

In Mode2 (Figure 4), control switch S_a is turned ON and switch S_b is turned OFF, when the voltage across capacitor C_{11} is smaller than capacitor C_{12}, then capacitor C_{11} is charged by capacitor C_{12} through diode D_{12} and switch S_a. When voltage across capacitor $C_{11}+C_{21}$ smaller the voltage across capacitor $C_{12}+C_{22}$, then capacitor C_{22} transfers its energy to capacitor C_{21} through diode D_{22} and switch Sa. Similarly capacitor C_{K2} transfers its energy to capacitor C_{K1} through D_{K2} when the voltage across capacitor $C_{11}+C_{21}+\ldots+C_{k1}$ is smaller than the voltage $C_{12}+C_{22}+C_{K2}$. And in this mode output voltage is equal to the input voltage(V_{in})+V_{C12}+V_{C22}+…+V_{CK2}.

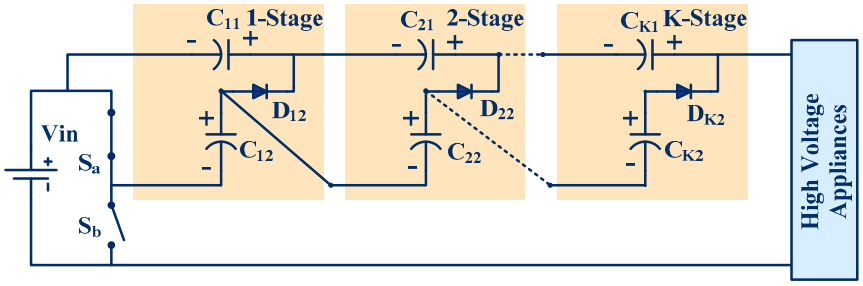

Figure 4. OFF state of proposed magnetic component free multistage DC-DC converter

2.2. Voltage Gain Analysis of Multistage Converter without Diode and Switches Loss

When the voltage drop across diodes and switches are not considered, all capacitors are subjected to the same voltage V_{in}. The voltage conversion ratio or voltage gain is equal to the (K+1) i.e. number of stages+1 and also depends on number of capacitors. Figure 5 (a)-(b) depicts the graph of required number of devices/components versus the number of stages in 2-dimensional and in 3-dimensional view respectively. In figure 5(a)-(b) it is observed that the number of devices/components are linearly increases as the number of stages are increased. Thus, with increase of each stage 2 more diodes and capacitors are needed. It is also observed that the number of diodes is equal to number of capacitors.

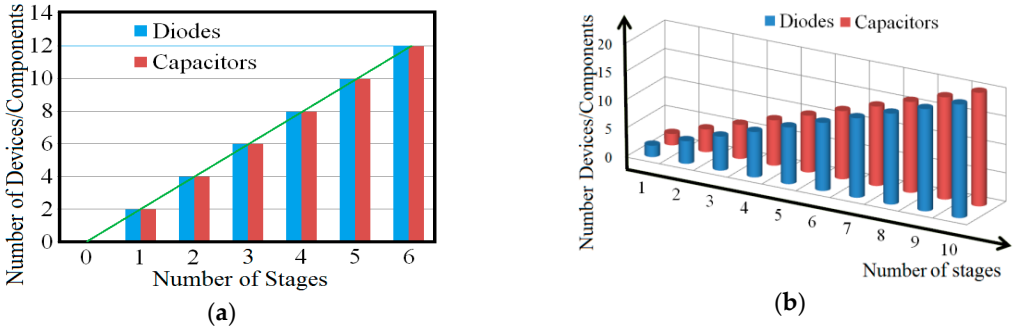

Figure 5. Number of devices/component versus number of stages **(a)** 2-dimensional view **(b)** 3-Dimensional view

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$$V_{C11} = V_{C12} = V_{C21} = V_{C22} = V_{CK2} = V_{in} \quad (1)$$

$$V_o = (K+1) \times V_{in} \quad (2)$$

$$V_o = \frac{K_C + 2}{2} \times V_{in} \quad (3)$$

$$V_o = \frac{K_D + 2}{2} \times V_{in} \quad (4)$$

$$K_C = K_D = 0.5\ \mathrm{K} \quad (5)$$

Where, K_C and K_D number of capacitor and diode used to design the proposed circuit. The graph of voltage gain versus number of stages is shown in Figure 6(a). It is observed that the proposed converter with K stages provides a K+1 voltage conversion ratio. The graph of number of stage devices/Components versus voltage gain is shown in Figure 6(b). It is observed that the number of devices/components are linearly increases as the requirement of voltage gain is increased. Thus, 2 diodes and 2 capacitors are needed to be connected to increase voltage gain by factor 1. It is also observed that the 2K-2 diodes and2K-2 capacitors are required to attain voltage gain K.

The graph of voltage gain (Vo/Vin), number of stages (K) and duty cycle (D) is shown in Figure 6 (c). It is observed that 2 capacitors and 2 diodes are required to design one stage of proposed converter. The graph of output voltage for stages 1 to 9 by considering input voltage 25V is shown in Figure 6(d). It is observed that the output voltage is increased as the number of stages is increasing. And each stage contributes the voltage equal to the input voltage (25V) to an output voltage of proposed converter.

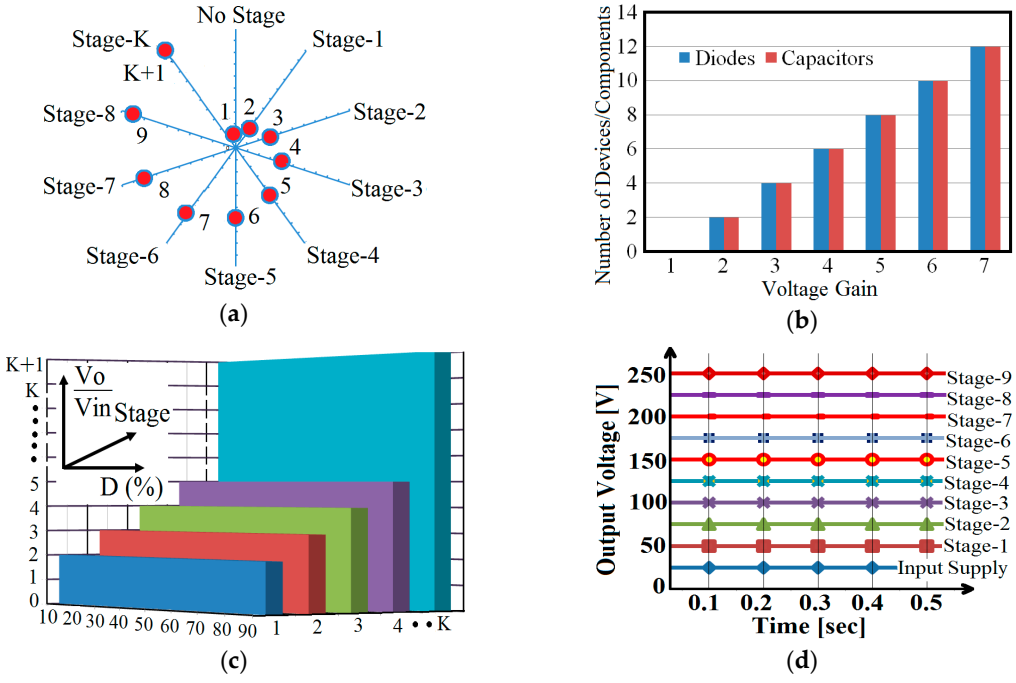

Figure 6. Relations of Converter Parameters **(a)** Graph of voltage gain versus number of stages **(b)** Graph of number of devices/component versus voltage gain **(c)** Graph of voltage gain (Vo/Vin), number of stages (K) and duty cycle (D) **(d)** Output voltage for stage 1 to 9 for 25V input voltage.

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2.3. Voltage Gain Analysis of Multistage Converter with Diode and Switches Loss

The voltage drop across power diodes and switches is ignored in medium and high power application, but in low power application it is considered. The analysis of the circuit is done with consideration of voltage drop across diodes and switches. For simplicity, the voltage drop across diodes and switches is assumed to be equal to V_d.

$$V_{C11} = V_{C12} - V_{D12} - V_{Sa} \tag{6}$$

$$V_{C11} = V_{in} - 4V_d \tag{7}$$

$$V_{C12} = V_{in} - 2V_d \tag{8}$$

$$V_{C21} = V_{C12} + V_{C22} - V_{C11} - V_{D22} - V_{Sa} = V_{in} - 4V_d \tag{9}$$

$$V_{C22} = V_{in} + V_{C11} - V_{C12} - V_{D21} - V_{Sb} = V_{in} - 4V_d \tag{10}$$

$$V_{CK1} = V_{in} - 4V_d \tag{11}$$

$$V_{CK2} = V_{in} - 4V_d \tag{12}$$

It is investigated that the voltage across each capacitor is equal to V_{in}-$4V_d$ except voltage across capacitor C_{12}. The Voltage across capacitor C_{12} is equal to V_{in}-$2V_d$. Thus, proposed topology is self balanced and magnetic component free. Thus the output voltage of the converter is limited by the devices forward voltage and number of devices. The graph of proposed converter output voltage versus number of stages with practical diode (V_d=1) and ideal diode is shown in Figure 7 (a). The graph of proposed converter output voltage versus number of diodes or capacitors with practical diode (V_d=1) and ideal diode is shown in Figure 7 (b). From Figure 7(a) and 7(b) it is observed that the difference between ideal and practical output voltage increases as the requirement of number of stages, diodes and capacitor is increased. The difference in ideal and practical output voltage is depending on the number of stages of proposed converter and it is equal to $4KV_d$ as given in equation (15)

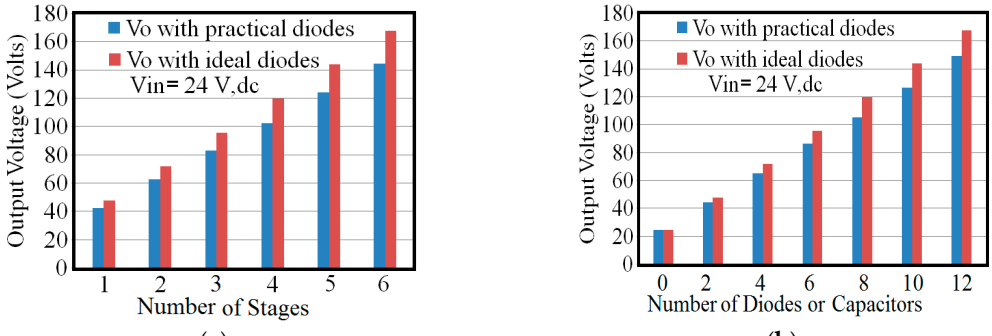

Figure 7. Comparison graph with considering Vin =24V **(a)** Graph of converter output voltage versus number of stages (practical and ideal diode) **(b)** Graph of converter output voltage versus number of diodes or capacitors (practical and ideal diode).

$$V_{C11} = V_{C21} = V_{C22} = V_{CK1} = V_{CK1} = V_{in} - 4V_d \tag{13}$$

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$$V_{C12} = V_{in} - 2V_d \tag{14}$$

$$V_0 = (K+1)V_{in} - 4KV_d \tag{15}$$

3. Design Calculation of Capacitors of Proposed Converter

To explain the designed calculation of proposed converter 1-stage proposed converter is considered. Power circuit of 1-stage proposed converter is shown in figure 8(a). ON state and OFF state equivalent circuit of 1-stage proposed converter is depicted in figure 8(b) and figure 8(c) respectively, where R_D is the forward resistance of the diode, R_S is the forward resistance of the switch, I_{Sb} is current through the switch *Sb* and I_{Sa} is current through switch *Sa*.

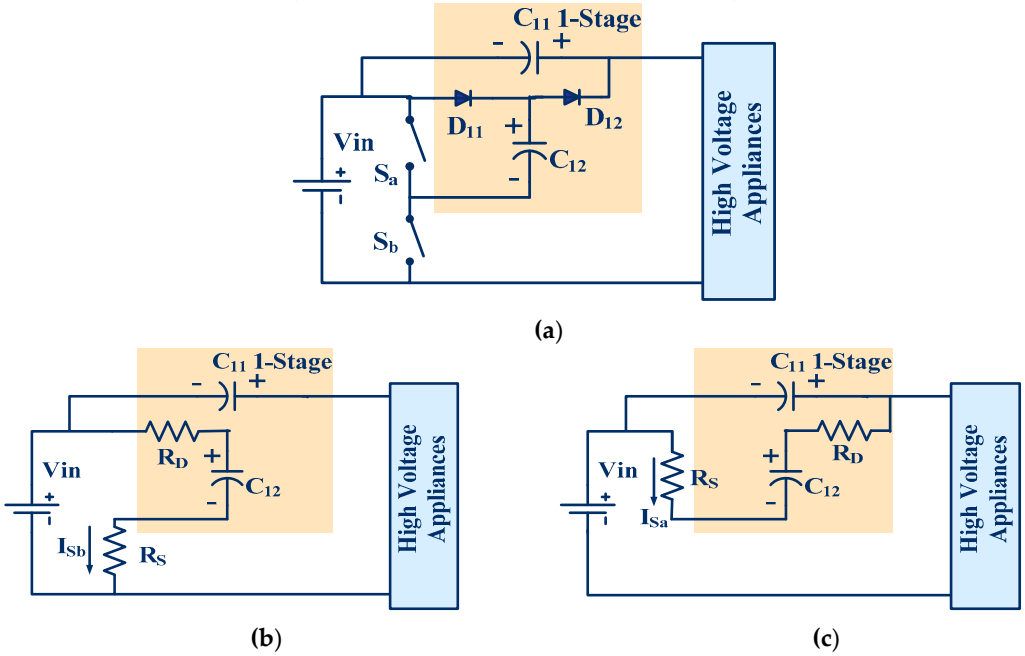

Figure 8. (a) Power circuit 1-stage of proposed converter **(b)** Equivalent circuit of ON state of 1-stage proposed converter **(c)** Equivalent circuit of OFF state of 1-stage proposed converter.

Initially voltage across capacitor C_{12} and C_{11} is zero. Capacitor C_{12} is charged through a resistance R_D and R_S from a supply voltage V_{in} when switch S_b is closed. Voltage across C_{12} does not increases to V_{in} instantaneously, but build up exponentially not a linearly.

$$V_{in} = i_{C_{12}}\left(R_D + R_S\right) + v_{C_{12}} \tag{16}$$

$$i_{C_{12}} = \frac{d(C_{12}v_{C12})}{dt} = \frac{C_{12}d(v_{C12})}{dt} \tag{17}$$

$$\left.\begin{aligned} V_{in} &= \frac{C_{12}d(v_{C12})}{dt}\left(R_D + R_S\right) + v_{C_{12}} \\ \frac{d(v_{C12})}{V_{in} - v_{C_{12}}} &= \frac{dt}{\left(R_D + R_S\right)C_{12}} \end{aligned}\right\} \tag{18}$$

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$$\left.\begin{aligned}&\int\frac{d(v_{C12})}{V_{in}-v_{C_{12}}}=\int\frac{dt}{(R_D+R_S)C_{12}}\\&\log(V_{in}-V_{C_{12}})=-\frac{t}{(R_D+R_S)C_{12}}+K,K=\log V_{in}\\&V_{C_{12}}=V_{in}(1-e^{\frac{-t}{T}}),T=(R_D+R_S)C_{12}\end{aligned}\right\}\quad(19)$$

Similarly

$$i_{Sb}=\frac{V_{in}}{(R_D+R_S)}e^{\frac{-t}{T}}\quad(20)$$

Capacitor C_{11} is charged through a resistance R_D and R_S from a capacitor C_{12} voltage when switch S_a is closed. Thus, when switch S_a is closed capacitors C_{11} and C_{12} is charging and discharging respectively.

$$\left.\begin{aligned}V_{C_{12}}&=i_{C_{11}}(R_D+R_S)+v_{C1}\\V_{C_{12}}&=i_{C_{12}}(R_D+R_S)+v_{C_{11}}\end{aligned}\right\}\quad(21)$$

$$\left.\begin{aligned}V_{C_{12}}&=\frac{C_{11}d(v_{C11})}{dt}(R_D+R_S)+v_{C_{11}}\\\frac{d(v_{C11})}{V_{C_{12}}-v_{C_{11}}}&=\frac{dt}{(R_D+R_S)C_{11}}\end{aligned}\right\}\quad(22)$$

$$\left.\begin{aligned}&\int\frac{d(v_{C11})}{V_{C_{12}}-v_{C_{11}}}=\int\frac{dt}{(R_D+R_S)C_{11}}\\&\log(V_{C_{12}}-V_{C_{11}})=-\frac{t}{(R_D+R_S)C_{11}}+K,K=\log V_{C_{12}}\\&V_{C_{11}}=V_{C_{12}}(1-e^{\frac{-t}{T}}),T=(R_D+R_S)C_{11}\end{aligned}\right\}\quad(23)$$

Similarly

$$i_{Sa}=\frac{V_{C_{12}}}{(R_D+R_S)}e^{\frac{-t}{T}}\quad(24)$$

In steady state and at high switching frequency, the voltage across capacitor C_{11} and C_{12} at any instant during charging is cycle is given in equation (25) and equation (26) where, $V_{C'11}$ and $V_{C'12}$ is the initial voltage of capacitor C_{11} and C_{12}.

If initial storage voltage of C_{11} and C_{12} is positive

$$\left.\begin{aligned}V_{C_{12}}&=(V_{in}-V_{C'_{12}})(1-e^{\frac{-t}{T}})+V_{C'_{12}}\\V_{C_{11}}&=(V_{C_{12}}-V_{C'_{11}})(1-e^{\frac{-t}{T}})+V_{C'_{11}}\end{aligned}\right\}\quad(25)$$

If initial storage voltage of C_{11} and C_{12} is negative

$$\left.\begin{aligned}V_{C_{12}}&=(V_{in}+V_{C'_{12}})(1-e^{\frac{-t}{T}})-V_{C'_{12}}\\V_{C_{11}}&=(V_{C_{12}}+V_{C'_{11}})(1-e^{\frac{-t}{T}})-V_{C'_{11}}\end{aligned}\right\}\quad(26)$$

The time required for the capacitor C_{12} to attain any value of VC_{12} during the charging cycle is given in equation (27) and equation (28).

When initial voltage across capacitor is positive

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$$t = T\log(\frac{V_{in} - V_{C'_{12}}}{V_{in} - V_{C_{12}}}) = (R_D + R_S)C_{12}\log(\frac{V_{in} - V_{C'_{12}}}{V_{in} - V_{C_{12}}}) \quad (27)$$

When initial voltage across capacitor is negative

$$t = T\log(\frac{V_{in} + V_{C'_{12}}}{V_{in} - V_{C_{12}}}) = (R_D + R_S)C_{12}\log(\frac{V_{in} + V_{C'_{12}}}{V_{in} - V_{C_{12}}}) \quad (28)$$

The time required for the capacitor C_{11} to attain any value of VC_{11} during the charging cycle is given in equation (29) and equation (30).

When initial voltage across capacitor is positive

$$t = T\log(\frac{V_{C_{12}} - V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) = (R_D + R_S)C_{11}\log(\frac{V_{C_{12}} - V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) \quad (29)$$

When initial voltage across capacitor is negative

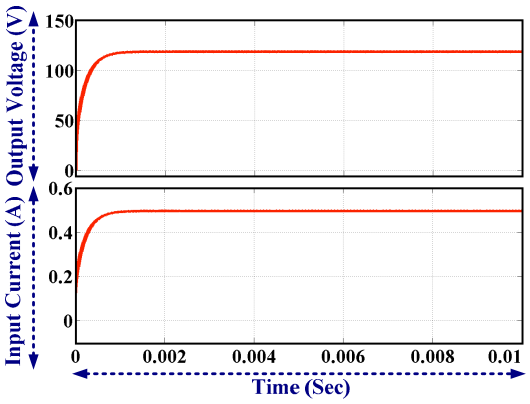
$$t = T\log(\frac{V_{C_{12}} + V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) = (R_D + R_S)C_{11}\log(\frac{V_{C_{12}} + V_{C'_{11}}}{V_{C_{12}} - V_{C_{11}}}) \quad (30)$$

$$\left.\begin{aligned} C_{12} &= \frac{1}{2\pi fsX_{C12}} = \frac{1}{2\pi fs\frac{V_{C12}}{I_{C12}}} = \frac{I_{C12}}{2\pi fsV_{C12}} \\ C_{11} &== \frac{1}{2\pi fsX_{C11}} = \frac{1}{2\pi fs\frac{V_{C11}}{I_{C11}}} = \frac{I_{C11}}{2\pi fsV_{C11}} \end{aligned}\right\} \quad (31)$$

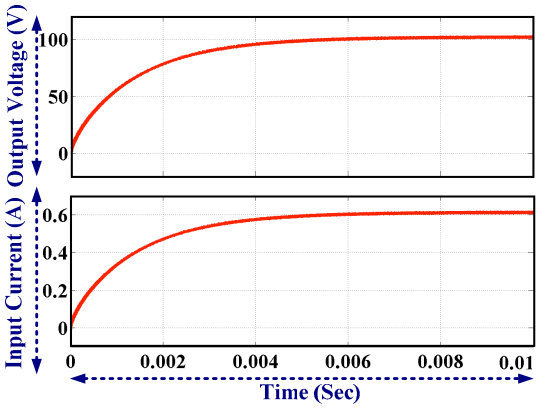
Voltage and current of all the capacitors are same during the complete switching cycle. Thus the equal rating of all capacitors is suitable to design proposed converter whose voltage rating is greater than the input voltage.

4. Experimental and Simulation Result of Self Balanced and Magnetic Component Free Multistage DC-DC Proposed Converter

The proposed self balanced and magnetic component free multistage DC-DC converter simulation and experimental result are discussed in this section. The proposed multistage converter has been designed for five levels with rated power 60W, switching frequency 100 kHz, output voltage is 100V and the supply voltage is 24V. Switches S_a (here S_1) and S_b (here S_2) are operated complementary with duty cycle 50%. High switching frequency is used to reduce the rate of the capacitor.



(a)



(b)

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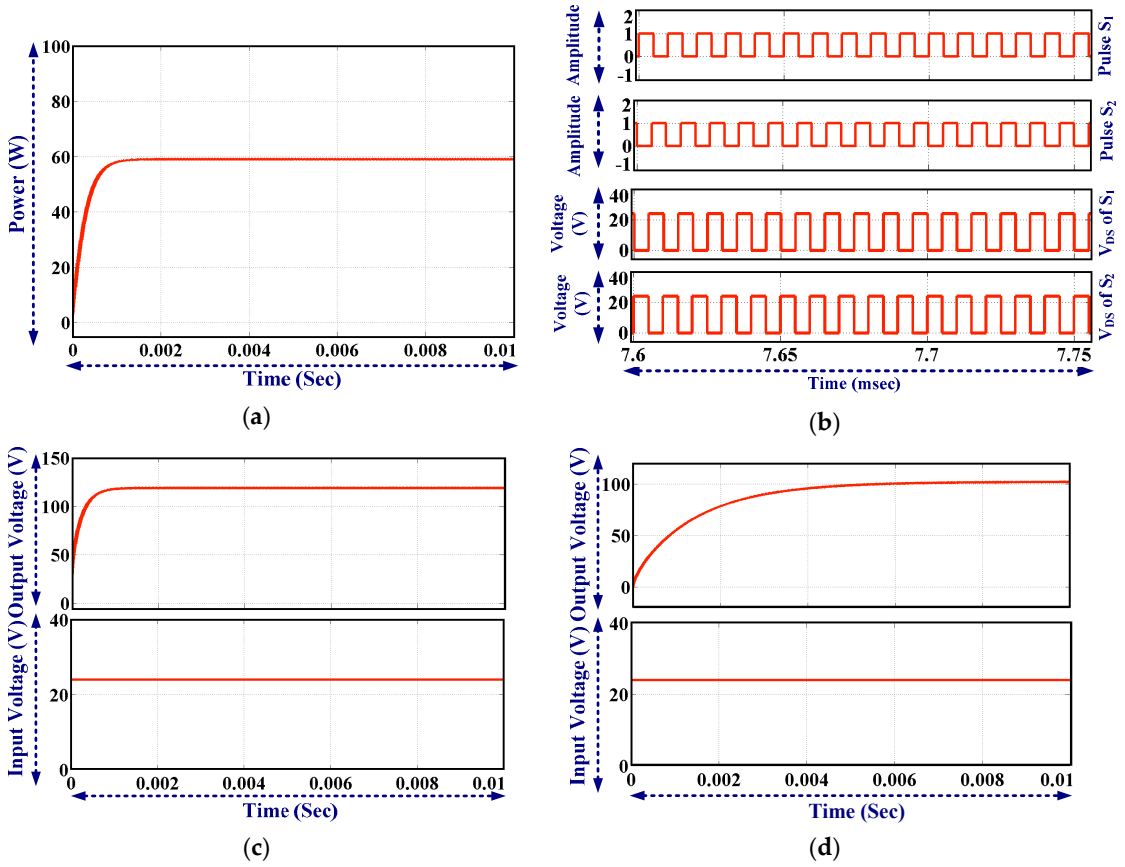
Figure 9. Simulation results **(a)** Output voltage and current waveform with ideal components and Vin =24V **(b)** Output voltage and current waveform with practical component and Vin =24V

The output voltage and current waveform with ideal components (voltage drop across the switch and the diode is zero) is shown in Figure 9(a). It is observed that the settling time for the output voltage of the proposed converter with ideal component (Forward resistance of the diode is 0) is less than 2msec. The effect of voltage drop across the diode is analyzed in the previous section. The output voltage and current waveform (Assume 1 V voltage drop across the switch and diode) are shown in Figure 9(b). It is observed that the settling time for the output voltage of the proposed converter with practical component is 4msec approx due to the forward resistance of the diode and switch. Thus, practical waveform is differ than ideal waveform because of time constant (R_D+Rs)C as explained in section 3. The output power waveform and switch voltage is shown in Figure 10(a) and 10(b) respectively. The output voltage and input voltage waveform with ideal components (voltage drop across the switch and the diode is zero) is shown in Figure 10(c). The output voltage and input voltage waveform (Assume 1 V voltage drop across the switch and diode) are shown in Figure 10(d).



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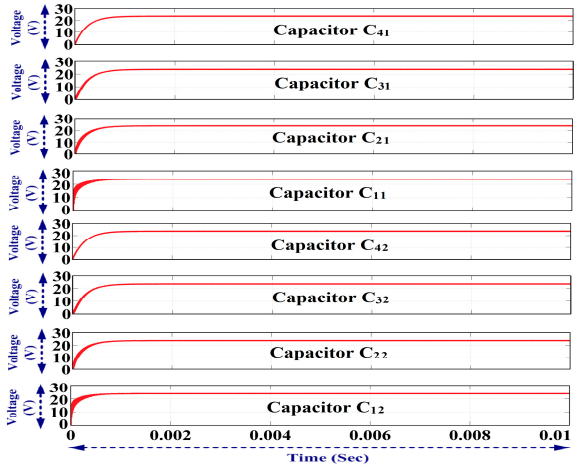
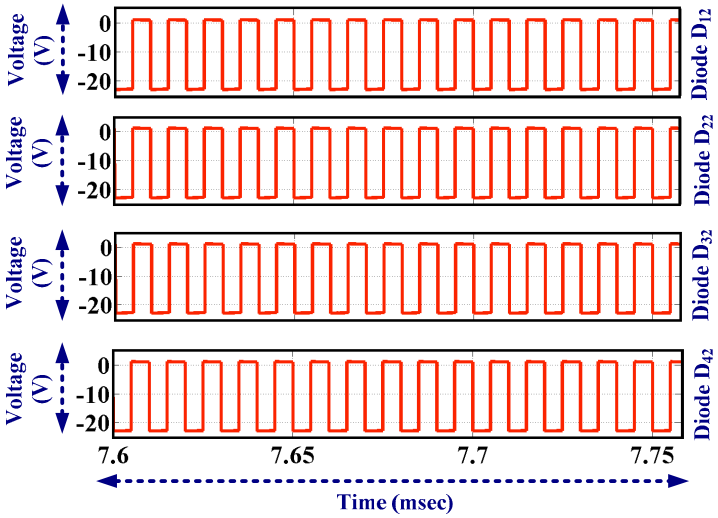
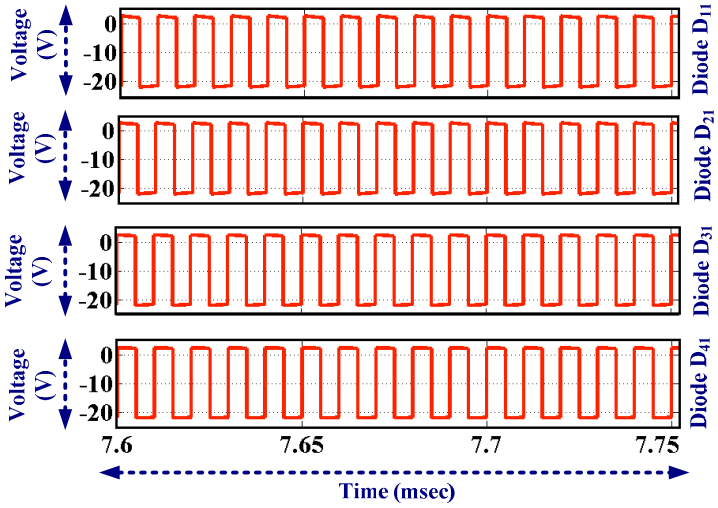


(e)



(f)



(g)

Figure 10. Simulation results **(a)** Output power of proposed converter. **(b)** Output voltage and input voltage waveform with ideal components **(c)** Output voltage and input voltage waveform with practical components **(d)** voltage across capacitor C_{11}, C_{21}, C_{31} and C_{41} **(e)** Voltage across capacitor C_{12}, C_{22}, C_{32} and C_{42} **(f)** Voltage across diode D_{11}, D_{21}, D_{31} and D_{41} **(g)** Voltage across diode D_{12}, D_{22}, D_{32} and

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D_{42}.

It is observed that 120V output voltage is achieved from 24V input Supply. Thus, ideally the voltage gain of the proposed converter is 5, which is equal to the number of levels. When the voltage drop across the diode is considered, output voltage 100V are achieved from supply 24V. The voltage across the switch is equal to the input supply voltage (24V). The voltage across all capacitors is same, which is equal to the input supply voltage (24V) if the voltage drop across the diode is not considered. The voltage across the capacitors is shown in Figure 10 (e). The voltage across all diode is same (24 V) when the diode is reversed biased. The voltage across diodes is shown in Figure 10 (f)-(g). The proposed 5-level self balanced and magnetic DC-DC converter is investigated experimentally and the result shows a good match with the simulation results. The hardware components are listed in Table 1.

PIC18F45K20 is used to generate pulses and TLP250 is used as driver IC. The hardware prototype of proposed converter is shown in Figure 11. Pulses are generated from PIC controller and gate driver output is shown in Figure 12 (a) and Figure 12 (b) respectively. Output voltage and input voltage waveform are shown in Figure 12 (c). It is observed that 100V output is achieved from input supply 24V. The output current waveform is shown in Figure 12 (d) and it is observed that the output current is 0.619 A. The voltage across each capacitor is shown in Figure 13 (a)-(h). It is observed that the voltage across each capacitor is nearly same and slightly less than the input voltage 24V (effect of diode). Voltage stress across each diode is shown in Figure 14 (a)-(h). It is observed that voltage stress across the diode is the approximately same and the peak voltage across the diode is slightly less than the input voltage (24V) (effect of drop). Slightly voltage of all capacitors and all diodes are differs due to the forward resistance of the diode and switch. The lower stages (source side) capacitors are charges through the path which contain less number of diodes whereas as the number of stages increases the path followed for the charging of higher stage (moving towards load) capacitor of contain more number of diodes. Thus, practically slight difference is observed in the voltage of capacitors.

Table 1. Hardware Component Detail

Sr/No	Components	Value	No. of components
1	Switch (S_1 and S_2)	IRF250 (0.085 ON sate resistance)	2
2	Diodes	BYQ28E	8
3	Capacitors	220uF, 50V	8
4	Load	168 Ω, 60W	1
5	Gate Driver IC	TLP250	2

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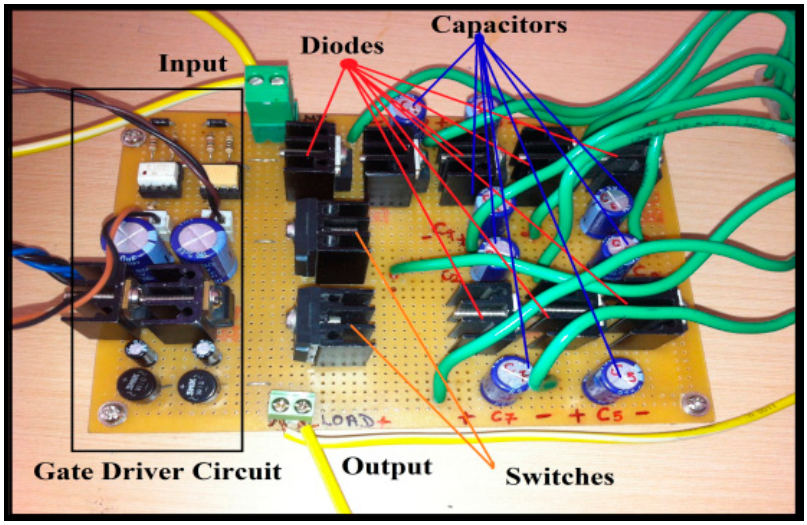
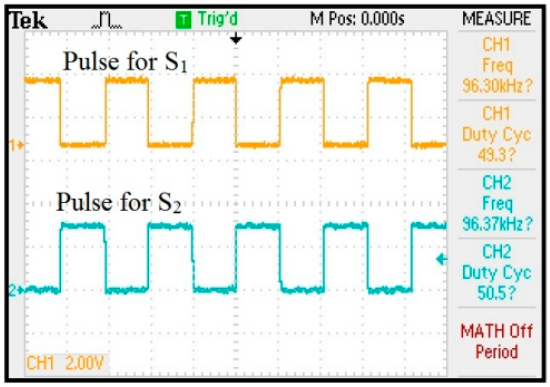
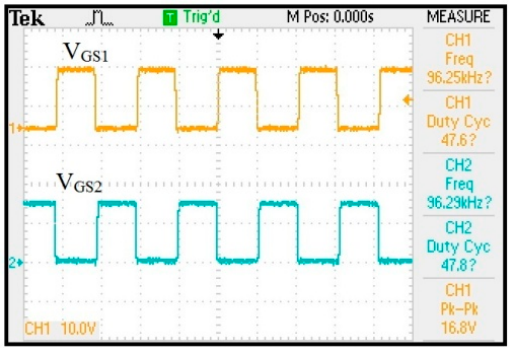


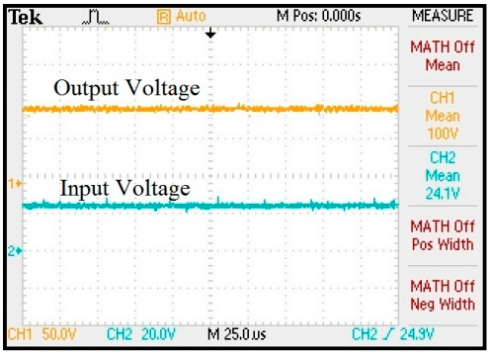
Figure 11. Hardware Prototype of Proposed DC-DC Converter



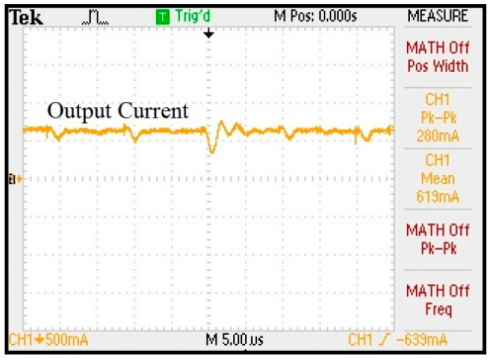
(a)



(b)



(c)



(d)

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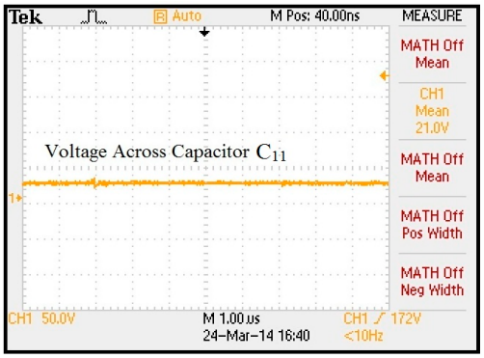
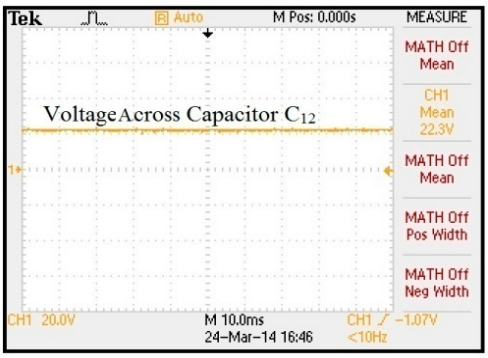
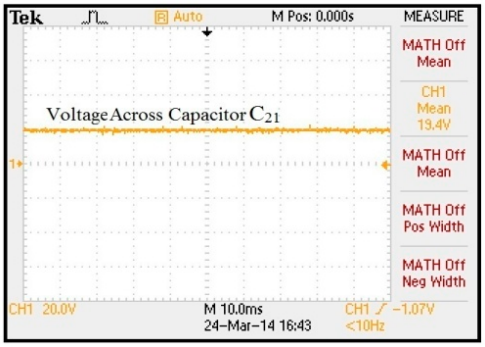
Figure 12 (a) PIC controller output **(b)** TLP 250 gate driver output **(c)** Output voltage and input voltage waveform **(d)** Output current waveforms.



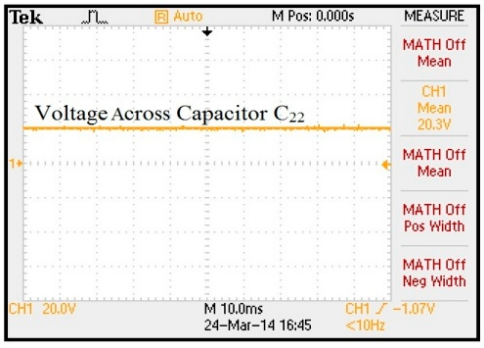
(a) VC_{11}= 21.0V



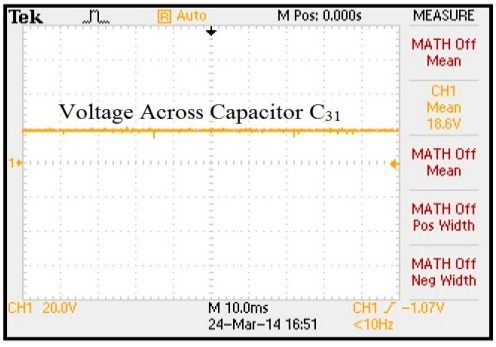
(b) VC_{12}= 22.3V



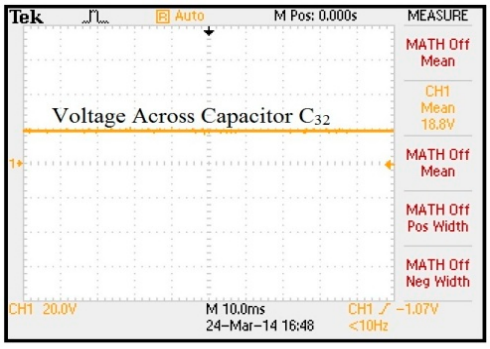
(c) VC_{21}= 19.4V



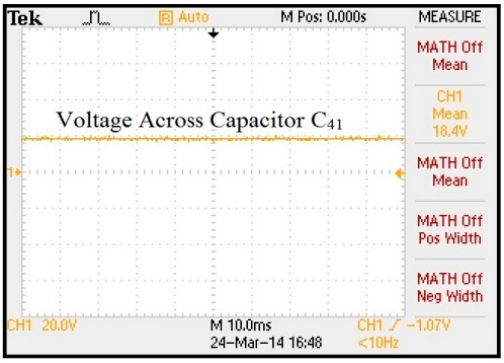
(d) VC_{22}= 20.3V



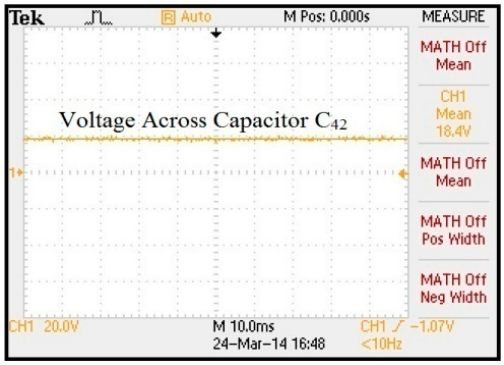
(e) VC_{31}= 18.6V



(f) VC_{32}= 18.8V



(g) VC_{41}= 18.4V



(h) VC_{42}= 18.8V

Figure 13 Capacitors voltage **(a)** C_{11} **(b)** C_{12} **(c)** C_{21} **(d)** C_{22} **(e)** C_{31} **(f)** C_{32} **(g)** C_{41} **(h)** C_{42}

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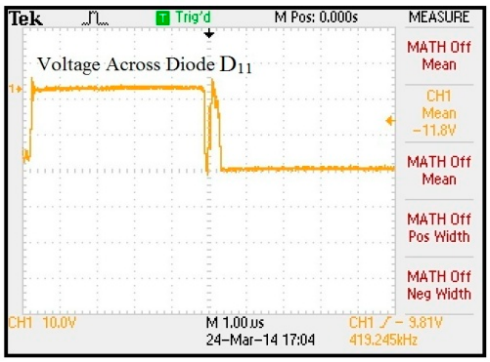
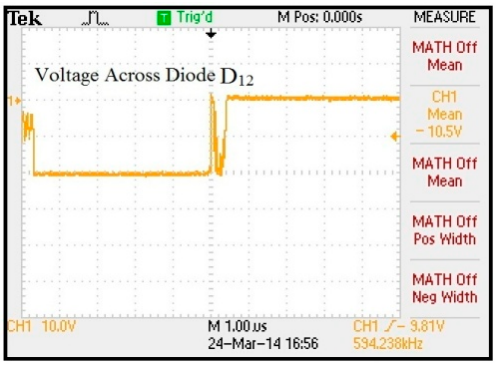
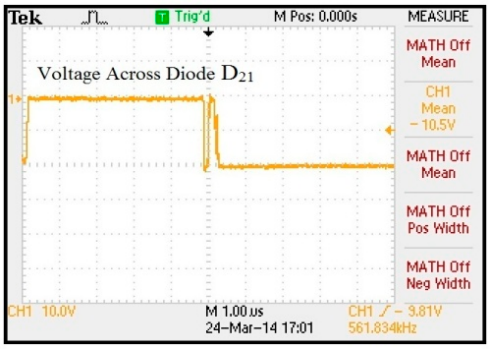


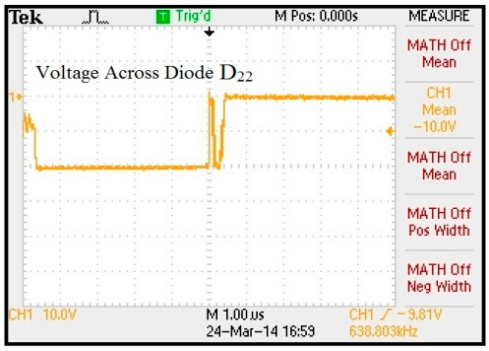
(a) MeanVD11 = -11.8V



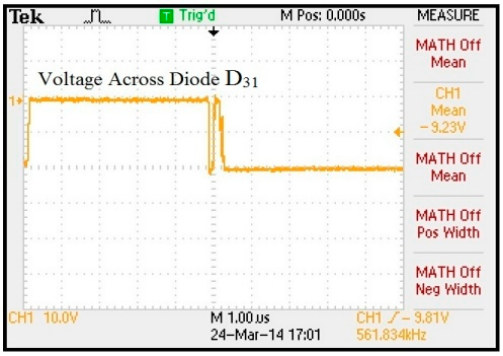
(b) Mean VD12= -10.5 V



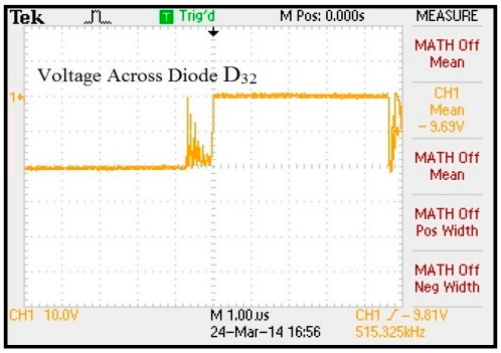
(c) MeanVD21= -10.5V



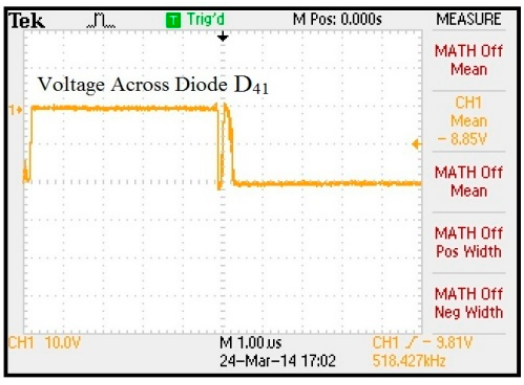
(d) Mean VD22= -10 V



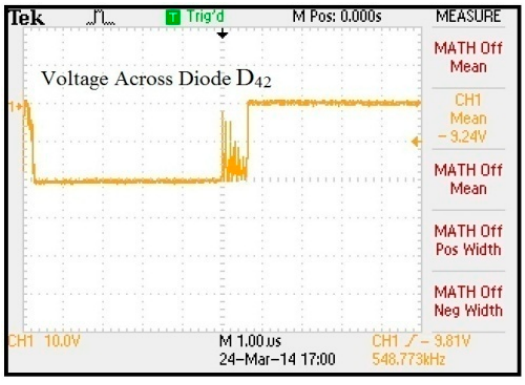
(e) MeanVD31= -9.23V



(f) Mean VD32= -9.69V



(g) MeanVD41= -8.85V



(h) Mean VD42= -9.24V

Figure 14 Voltage across diodes **(a)** D_{11} **(b)** D_{12} **(c)** D_{21} **(d)** D_{22} **(e)** D_{31} **(f)** D_{32} **(g)** D_{41} **(h)** D_{42}

5. Conclusion

The self biased and magnetic free multistage step-up converter is articulated and designed for unidirectional renewable photovoltaic applications. The proposed converter is well suited for renewable photovoltaic application where voltage needs to be stepped up without using magnetic component. The proposed converter is suitable for the DC link application in DC-AC system where capacitor voltage balancing is the main challenge. The proposed converter also provides a viable solution to low power application, since the inductor and transformer are not required to design proposed converter. Also Maximum Power Point Tracking (MPPT) can be easily implemented to improve the efficiency of the converter. The voltage across the switch is less hence low voltage switches are used for designing high voltage converter. The conspicuous features of proposed topology are:

i) Magnetic components free
ii) Continuous input current
iii) Low voltage rating semiconductor devices and capacitors
iv) Modularity
v) Easy to add a higher number of levels to increase voltage
vi) Only two control switches with alternating operation and simple control.

The proposed converter has been designed with rated power of 60 W, input voltage is 24 V, output voltage is 100 V and switching frequency is 100 kHz. High switching frequency has been used to decrease component size. The performance of the proposed converter is verified through simulation results and experimental results.

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Author Contributions: "S.B.Mahajan and P.Sanjeevikumar has developed the proposed research concept with the complete theoretical background study. Further hardware prototype implementation tasks are carried out the same authors. F.Blaabjerg has contributed his expertise to validate the proposal both theoretical background and hardware results obtained as co-author. All authors involved in framing its current format of the full research paper work".

Conflicts of Interest: Declare conflicts of interest or state "The authors declare no conflict of interest."

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