A 14-bit Hybrid Incremental Sigma-Delta/Cyclic ADC for X-ray Linear Array Sensor

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Abstract—This paper presents a two-stage ADC based on pseudo-differential operational transconductance amplifier (OTA), which is designed for the readout circuit of X-ray linear array sensor. This hybrid ADC employs an incremental sigma-delta ADC and a cyclic ADC, achieving a good trade-off between accuracy and conversion speed. The two stages share the same hardware to reduce power consumption and die area. A common-mood feedback module is used to suppress the influence of charge injection, and the effectiveness is demonstrated by detailed theoretical analysis. A test chip of 14-bit ADC is fabricated in 0.35µm CMOS technology. The measured root mean square (RMS) value of DNL is 0.254 LSB, and the maximum value of INL is -0.776/+1.56 LSB. The measured effective number of bits (ENOB) is 13.43 bits.

Keywords—hybrid ADC; sigma-delta ADC; cyclic ADC; pseudo-differential OTA; X-ray sensor

I. INTRODUCTION

X-ray imaging system is widely used in many fields such as medical, industrial, and safety monitoring areas [1]. Readout Integrated Circuit (ROIC) of the X-ray sensor has a significant effect on signal-to-noise ratio of the system [2]. Since digital signal has strong resistance to interference, ROIC integrated with Analog-to-Digital Converter (ADC) is drawing more and more attention. There are many channels in the ROIC of X-ray linear array sensor, and it is a good choice to integrate an ADC in each channel to alleviate speed requirements for ADC. The architecture of the ROIC is shown in Fig. 1. The front-end circuit of the ROIC is called Capacitive Trans-Impedance Amplifier (CTIA), which is used to convert tiny current signal generated by the X-ray linear array sensor to analog voltage signal. The ADC in each channel of the ROIC should feature small die area, low power consumption, high resolution and moderate speed to realize good performance.



Fig. 1. ROIC of the X-ray linear array sensor

Several kinds of structure have the potential to be used in the required ADC. First-order sigma-delta (Σ - Δ) ADC and single-slope ADC can achieve the required conversion accuracy easily, but it needs 2^N clock cycles for N-bit resolution which makes the

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conversion speed too slow to meet the requirement [3][4]. Although high order Σ - Δ ADC can improve conversion speed to a certain extent, the complexity of the filter is increased accordingly, which leading to important die area and power consumption [5]. Cyclic ADC and Successive approximation register (SAR) ADC need only N clock cycles for N bits conversion, but Cyclic ADC leads to limited accuracy and high accuracy SAR ADC occupies large die area [6][7]. Hybrid incremental Σ - Δ /cyclic ADC is presented to overcome the disadvantages [8]. Incremental Σ - Δ ADC acts as the first stage to achieve high resolution and cyclic ADC is the second stage to shorten conversion time.

In this paper, a new incremental Σ - Δ /cyclic ADC structure based on pseudo-differential OTA is presented. The two stages share the same hardware, and each ADC adopts the redundant signed digit (RSD) principle for a large tolerance of comparator offset. The pseudo-differential structure is used to decrease power consumption, and increase the voltage swing range. The CMFB circuit can suppress the effect of charge injection, and guarantee high conversion resolution. This hybrid ADC compromises speed and accuracy with small area and power consumption, which is suitable to be integrated in channel.

This paper is organized as follows. Section II describes the architecture and principle of the presented ADC. Section III shows the design consideration of circuit. Section IV provides the experimental results of a fabricated prototype. Finally, Section V concludes this paper.

II. ARCHITECTURE AND PRINCIPLE

A. Architecture of Hybrid ADC

Fig. 2 shows the architecture of the presented two-stage hybrid ADC. The incremental Σ - Δ ADC, as the first stage, produces a serial digital bit stream and the residue voltage V_{res} . The bit stream is translated into N-bit MSBs by a digital lowpass filter. The residue voltage is passed on to the second stage ADC (i.e. cyclic ADC) to obtain M-bit LSBs. The LSBs and MSBs are connected by the data connection module which costs 1-bit resolution to output the final (M+N-1)-bit digital signal. Σ - Δ ADC and cyclic ADC use the same integrator, 1.5-bit ADC and 1.5-bit DAC to perform conversion. Both stages adopt RSD algorithm to avoid the influence of comparator inaccuracy [9].

For the incremental Σ - Δ ADC, it takes 2^N clock cycles for N-bit resolution. For each cycle, the input voltage V_{in} is fed to the integrator in phase, and the feedback voltage $V_{DAC}(i-1)$ is integrated in anti-phase at the same time. The output of integrator is described as (1). λ is the gain of integrator in the incremental Σ - Δ ADC, and i represents the number of clock cycles.



Fig. 2. Architecture of two-stage hybrid ADC

After 2^N clock cycles, the Σ - Δ ADC exports the bit stream (2^N bits) which can be transferred to N-bit digital data. The output voltage of integrator $V_{out}(2^N)$ is the residue voltage V_{res} .

Cyclic ADC has high conversion speed for it needs only M clock cycles for M-bit resolution. In the first cycle, the residue voltage V_{res} (i.e. $V_{out}(2^N)$) is quantized by the 1.5-bit ADC. During the rest cycles, the output voltage $V_{out}(i-1)$ is fed to the integrator in phase and the feedback voltage $V_{DAC}(i-1)$ is integrated in anti-phase to get $V_{out}(i)$, as shown in (2). The gain of integrator is changed to 1 in the cyclic ADC. $V_{out}(i)$ is evaluated by the 1.5-bit ADC to get other digital data.

$$V_{out}(i) = V_{out}(i-1) + (V_{out}(i-1) - V_{DAC}(i-1))$$
⁽²⁾

B. Principle of Data Processing

Suppose the range of V_{in} is $-V_{ref} \sim V_{ref}$. The bit stream $D_1(i)D_0(i)$ is the output of the 1.5-bit ADC, as described in (3).

$$D_{1}(i)D_{0}(i) = \begin{cases} 00 & -V_{ref} < V_{out}(i) \le -\frac{1}{4}V_{ref} \\ 01 & -\frac{1}{4}V_{ref} < V_{out}(i) \le \frac{1}{4}V_{ref} \\ 10 & \frac{1}{4}V_{ref} < V_{out}(i) < \frac{1}{4}V_{ref} \end{cases}$$
(3)

The voltage $V_{DAC}(i)$ is exported from the 1.5-bit DAC which is controlled by $D_1(i)D_0(i)$, as shown in (4).

$$V_{DAC}(i) = \begin{cases} -V_{ref} & D_1(i)D_0(i) = 00\\ 0 & D_1(i)D_0(i) = 01\\ V_{ref} & D_1(i)D_0(i) = 10 \end{cases}$$
(4)

After 2^N clock cycles, use N_{00} , N_{01} and N_{10} to represent the number of $D_1(i)D_0(i)$ which is 00, 01 and 10, respectively. The total sum of N_{00} , N_{01} and N_{10} is 2^N . We can get the residue voltage V_{res} , as shown in (5).

$$V_{res} = \lambda \cdot [2^N \cdot V_{in} - (N_{10} - N_{00}) \cdot V_{ref}]$$

= $\lambda \cdot [2^N \cdot (V_{in} + V_{ref}) - (N_{10} + \frac{1}{2}N_{01}) \cdot 2V_{ref}]$ (5)

 $N_{10} + \frac{1}{2}N_{01}$ is the N-bit output data of Σ - Δ ADC, regarded as D_{inc} . Suppose D_{cyc} is the M-bit output data of cyclic ADC. Ignoring the quantization error of the cyclic ADC, we have

$$V_{res} = 2V_{ref} \cdot \frac{D_{cyc}}{2^M} - V_{ref}$$
(6)

According to (5) and (6), we can obtain

$$V_{in} = \frac{\frac{1}{\lambda} (D_{cyc} - 2^{M-1}) + 2^{M} \cdot D_{inc}}{2^{M+N}} \cdot 2V_{ref} - V_{ref}$$
(7)

In our design, the value of λ is 0.5. Equation (7) can be simplified as

$$V_{in} = [(D_{cyc} - 2^{M-1}) + 2^{M-1} \cdot D_{inc}] \cdot \frac{2V_{ref}}{2^{M+N-1}} - V_{ref}$$
(8)

We can see from (8) that the LSB of the two-stage hybrid ADC is $\frac{2V_{ref}}{2^{M+N-1}}$ and M+N-1 bits resolution can be realized.

III. CIRCUIT DESIGN

A. Implementation

The implementation of this hybrid incremental Σ - Δ /cyclic ADC is shown in Fig. 3. The integrator is of switched-capacitor type and it is symmetrical between the upper part and the lower part. The capacitor C_H is used to eliminate the input offset voltage of amplifier. The 1.5-bit ADC is composed of two latch comparators which take up small area and consume little static power. The 1.5bit DAC is made up of multiplexers and logic control circuit. The two stages share the same analog circuit block, which can decrease power and area consumption. This circuit works under the control of signal ϕ_r , ϕ_l , ϕ_2 , ϕ_3 , ϕ_{mod} , whose time sequence is shown in Fig. 4. ϕ_l is designed to be non-overlap with ϕ_l and ϕ_3 to avoid burr. There are three work modes as shown in Fig. 4. The first is reset mode, in which the amplifier and the integrating capacitors are initialized, and this mode lasts two clock cycles. Incremental Σ - Δ mode and cyclic mode take 256 and 7 clock cycles respectively. So the first stage can provide 8-bit digital data, and the second stage can provide 7 bits. The whole hybrid ADC can realize 14-bit resolution.



Fig. 4. Time sequence of control signals

B. Pseudo-Differential OTA

The OTA in this hybrid ADC is required to have small power consumption and high gain. To achieve this goal, we adopt the pseudo-differential triple telescope cascode OTA structure as shown in Fig. 5. There is no tail current source in the pseudo-differential OTA, and the positive and negative signal path is independent. Pseudo-differential OTA itself needs no common mode feedback (CMFB) circuit in principle since the common-mode input and output voltage is well-determined during the reset phase. Triple cascode structure is necessary to meet the high open-loop gain requirement. Compared to fully-differential OTA, Pseudo-differential OTA has wider output swing range [10]. Compared to folded cascode or two-stage amplifier, telescope cascode OTA has lower power consumption and splendid phase margin. This pseudo-differential OTA can fulfill the requirements of this hybrid ADC.



Fig. 5. Pseudo-differential OTA

C. CMFB Module

For high accuracy switched-capacitor circuit, the influence of charge injection cannot be ignored. Although charge injection can be suppressed by optimizing the aspect ratio of switch transistors and dummy transistors partly, there is still some charge (ΔQ), which can't be eliminated in each clock cycle. It will cause serious drift of integrator's common-mode output voltage with the accumulation of injection charge in 263 clock cycles.

Though pseudo-differential OTA itself needs no CMFB circuit, we add CMFB module to the integrator to suppress the influence of charge injection [11], as shown in Fig. 3. The capacitor C_M is discharged to common-mode ground V_{CM} at ϕ and forms a common-mode voltage detector at ϕ_2 . The difference between the common-mode voltage and V_{CM} is fed to the integrator, realizing a CMFB loop whose gain is defined as the ratio of $C_M / (C_2 + C_3)$ in sigma-delta mood or C_M / C_2 in cyclic mood.

Suppose $V_{out}^+(n)$ and $V_{out}^-(n)$ is the output voltage of integrator at n-th clock cycle, $V_{cm}(n)$ is the common-mode error of output voltage at n-th clock cycle, and $V_{DAC}^+(n)$ and $V_{DAC}^-(n)$ is the output voltage of 1.5-bit DAC at n-th clock cycle.

During the incremental sigma-delta mode, the injection charge ΔQ causes integrator's output voltage shift Δv in every clock cycle, and Δv is equal to $\Delta Q / (C_2 + C_3)$. We have (9) and (10) shown as follow.

$$V_{out}^{+}(n+1) = V_{out}^{+}(n) + \lambda \cdot (V_{in}^{+} - V_{DAC}^{+}(n)) - \frac{V_{cm}(n+1) \cdot C_{M}}{C_{2} + C_{3}} + \Delta v$$
(9)

$$V_{out}^{-}(n+1) = V_{out}^{-}(n) + \lambda \cdot (V_{in}^{-} - V_{DAC}^{-}(n)) - \frac{V_{cm}(n+1) \cdot C_{M}}{C_{2} + C_{3}} + \Delta v$$
(10)

Adding (9) and (10), we can acquire (11).

$$V_{cm}(n+1) = V_{cm}(n) - \frac{V_{cm}(n+1) \cdot C_M}{C_2 + C_3} + \Delta v$$
(11)

Equation (11) can be obtained by iteration method.

$$V_{cm}(n) = \left(\frac{C_2 + C_3}{C_2 + C_3 + C_M}\right)^n \cdot V_{cm}(0) + \frac{C_2 + C_3}{C_M} \cdot \left(1 - \left(\frac{C_2 + C_3}{C_2 + C_3 + C_M}\right)^n\right) \Delta \nu$$
(12)

There are 256 clock cycles in sigma-delta mode. The final common-mode error in sigma-delta mode V_{cm} (256) can be simplified as (13).

$$V_{cm}(256) \approx \frac{C_2 + C_3}{C_M} \cdot \Delta \nu = \frac{\Delta Q}{C_M}$$
(13)

There are 7 clock cycles in cyclic mode, and the variation Δy caused by charge injection is $\Delta Q/C_2$ in each clock cycle. We have (14) and (15) shown as follow.

$$V_{out}^{+}(n+1) = V_{out}^{+}(n) + (V_{out}^{+}(n) - V_{DAC}^{+}(n)) - \frac{V_{cm}(n+1) \cdot C_{M}}{C_{2}} + \Delta y$$
(14)

$$V_{out}^{-}(n+1) = V_{out}^{-}(n) + (V_{out}^{-}(n) - V_{DAC}^{-}(n)) - \frac{V_{cm}(n+1) \cdot C_{M}}{C_{2}} + \Delta y$$
(15)

Adding (14) and (15), we can acquire (16) and (17).

$$V_{cm}(n+1) = 2V_{cm}(n) - \frac{V_{cm}(n+1) \cdot C_M}{C_2} + \Delta y$$
(16)

$$V_{cm}(n+1) = \frac{2C_2}{C_2 + C_M} \cdot V_{cm}(n) + \frac{2C_2}{C_2 + C_M} \cdot \frac{\Delta y}{2}$$
(17)

Suppose V_{cm} (final) is the final common-mode error of output voltage.

$$V_{cm}(\text{final}) = \left(\frac{2C_2}{C_2 + C_M}\right)^7 \cdot V_{cm}(256) + \left(\left(\frac{2C_2}{C_2 + C_M}\right)^7 - 1\right) \cdot \frac{C_2}{C_2 - C_M} \cdot \Delta y$$

$$\approx \left(\frac{2C_2}{C_2 + C_M}\right)^7 \cdot \frac{\Delta Q}{C_M} + \left(\left(\frac{2C_2}{C_2 + C_M}\right)^7 - 1\right) \cdot \frac{\Delta Q}{C_2 - C_M}$$
(18)

The value of C_{M} should be much smaller than C_{2} for the limitation of system bandwidth, so (18) can be simplified as (19).

$$V_{cm}(\text{final}) \approx \left(\frac{2C_2}{C_2 + C_M}\right)^7 \cdot \left(\frac{1}{C_M} + \frac{1}{C_2 - C_M}\right) \cdot \Delta Q$$
 (19)

Take a derivative with respect to (19), we learn V_{cm} (final) is decreased with the increase of C_M in the interval of $[0, \frac{1+\sqrt{2}}{3}C_2]$. Considering the limitation of system bandwidth, we adopt $C_M = C_2/6$, which limits the value of V_{cm} (final) to $313 \cdot (\Delta Q/C_2)$. By contrast, the value of V_{cm} (final) will be greater than $16384 \cdot (\Delta Q/C_2)$ without the CMFB module. It is can also be verified by simulation. We take the common-mood ground V_{CM} (i.e. 2.5 V) as each single-ended input signal, and the output level of integrator is the common-mode output voltage. Without the CMFB module, the final common-mode output voltage of integrator drifts obviously after 256 cycles, as shown in Fig. 6. By contrast, the final common-mode output error V_{cm} (final) is well suppressed by the CMFB module, as shown in Fig. 7. The hybrid ADC will be out of work in the cyclic mode without the CMFB module.



Fig. 6. Simulation result without CMFB module



Fig. 7. Simulation result with CMFB module



A test chip of the hybrid ADC is fabricated in 0.35μ m 2P4M CMOS technology. The digital circuit used to generate control signals can be shared by all channels. The area of the analog circuit is 0.094 mm^2 . As power supply of the front-end circuit in ROIC is 5V, the analog circuit in this ADC is supplied with 5V and the digital part is supplied with 3.3V. The single-ended input voltage range is $1.2V \sim 3.8V$. The ADC works at a clock frequency of 2.5MHz.

The static and dynamic performance is measured by Ultra Flex1600 with 16-bit DAC for input voltage generation. A quasi-DC voltage ramp is used as input for static measurement. The plot of DNL is shown in Fig. 8 with the root mean square (RMS) value of 0.254 LSB. The plot of INL is shown in Fig. 9 with the maximum value of -0.776/+1.56 LSB. An 800Hz sinusoidal signal is used as the input signal to perform the dynamic test. The amplitude of sinusoidal signal is $1.3V\sim3.7V$, which is close to the full scale. Fig. 10 shows the power spectral density of the output data. The spectrum shows the pseudo-differential structure with CMFB module suppresses the even harmonic effectively. The measured ENOB achieves 13.43-bit, which is close to the theoretical resolution of 14-bit. The test results of the chip are listed in Table I.



Fig. 8. Plot of DNL



V. CONCLUSION

A 14-bit incremental Σ - Δ /cyclic hybrid ADC based on pseudo-differential OTA is designed and fabricated in 0.35 μ m CMOS process. This hybrid ADC is a good trade-off of speed and accuracy, and achieves ENOB of 13.43-bit. It is suitable for being integrated in channel of the ROIC for X-ray linear array sensor.

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