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*Article*

# A Single-Stage Buck-Boost Three-Level Neutral-Point-Clamped Inverter with Two Input Sources for the Grid-Tied Photovoltaic Power Generation

**Xuefeng Ge, Feng Gao * and Mengxing Chen**

Key Lab of Power System Intelligent Dispatch and Control (Shandong University), Ministry of Education, Jinan 250061, China; gexuefeng2013@gmail.com (X.G.); chenmx@mail.sdu.edu.cn (M.C.)

* Correspondence: fgao@sdu.edu.cn; Tel.: +86-15275138527

**Abstract:** This paper proposes a novel single-stage buck-boost three-Level neutral-point-clamped (NPC) inverter with two independent dc sources coupled for the grid-tied photovoltaic (PV) application, which can effectively solve the unbalanced operational conditions generally appeared between two coupled independent PV sources induced by the unequal irradiation and temperature distribution. The proposed control scheme can simultaneously guarantee the maximum power point (MPP) operation of both PV sources and maintain the output waveform quality. Compared to the traditional two-stage PV inverter, the proposed NPC inverter could reduce the PV array voltage requirement and dc-link capacitors' voltage rating, meanwhile show the advantage in operational efficiency. MATLAB simulations and the captured experimental results are presented to show the performance of the proposed three-level inverter.

**Keywords:** neutral-point-clamped inverter; buck-boost inverter; single stage conversion; photovoltaic inverter

## 1. Introduction

Recently, photovoltaic(PV) power generations are widely applied in the distribution network. The PV power generation system can be classified as two main categories of grid-tied and off-grid systems, where the grid-tied PV generation system dominates the PV applications in terms of the generation capacity. To date, most of the applied PV converter is two-level inverter, whose main shortcomings are the high operational current and in consequence the low operational efficiency [1-2]. For the purpose of increasing power conversion efficiency, the multilevel converters are preferably assumed as the interfacing converter between the PV array and the distribution grid due to its inherent operational characteristics [3-7], such as the reduced voltage stress, low harmonic distortion, low EMI and reduced current rating. Moreover, the mature 1500V PV panel in commercial allows the PV systems integrated into the high voltage grid (e.g. 690V) without the galvanic isolation by using the multilevel converters [8-9].Specifically, the two-stage neutral-point-clamped (NPC) inverter has been used as the interfacing converter in dozens of kW PV applications, whose topology is drawn in Figure 1, where two dc-dc boost converters directly connect to the upper and lower dc rails of the traditional NPC inverter.

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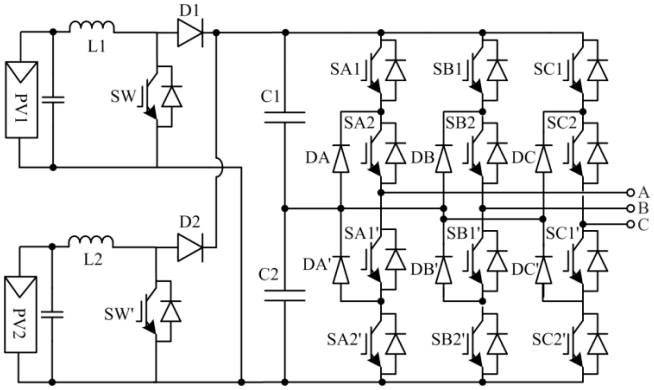



**Figure 1.** Topology of two-stage three-level NPC PV inverter.

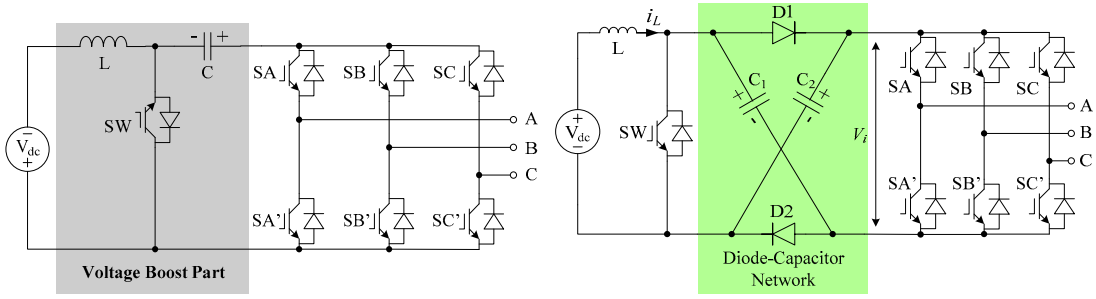
For the effort of making compact design, this paper proposes a novel single-stage buck-boost three-level neutral-point-clamped inverter as the interfacing circuit to tie the separated PV arrays, which can reduce the mandatory requirement of front-end PV array operation voltage and dc-link capacitors' voltage rating. In addition, the proposed control method can individually control the MPP per PV array and meanwhile boost the lower PV voltage to a high dc-link voltage and guarantee the output quality by adjusting the corresponding modulation states. Theoretical analysis has been done to compare the proposed inverter and traditional two-stage NPC inverter in terms of operational efficiency. MATLAB simulations and experimental prototype verified the performance of proposed three-level inverter.

## 2. Review of Single-Stage Buck-Boost Inverters

### *2.1. Single-Stage Buck-Boost Two-Level Inverters*

The Ćuk-derived buck-boost two-level inverter[10] is shown as Figure2(a), where capacitor C, switch SW, and inductor L consist of the voltage boost part. Being coupled between the negative-pole dc source and the full-bridge inverter circuitry, the voltage boost part, functioning as the energy storage and delivering intermediate, operates in particular with two distinct states defined by the ON and OFF states of SW. By carefully modulating the next connected full-bridge circuit, the whole integrated operation offers the buck-boost capability of designed inverter, whose voltage boost ratio is derived as:

$$V_g = M\frac{V_C}{2} = \frac{M}{1-k}\frac{V_{dc}}{2} \tag{1}$$




(a) (b)

**Figure 2.** Topologies of (a) Ćuk-derived and (b) diode-assisted buck-boost two-level inverter.

Where, *M* refers to the traditional modulation index and 1/(1-*k*) is the boost factor added by the voltage boost part.

The diode-assisted buck-boost voltage source converter is shown as Figure2(b) [11-12].

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Comparing with the cuk-derived single-stage inverter described above, the diode-assisted buck-boost converter assumes two capacitors and diodes and generate X-shape network to enhance the whole voltage boost ratio. Therefore, the output dc-link voltage can be derived as:

$$V_{C1} = V_{C2} = \frac{V_{dc}}{1-k}; V_{ac} = M\frac{V_{C1}+V_{C2}}{2} = \frac{MV_{dc}}{1-k} \quad (2)$$

Where, $V_{Cx}$ refers to the dc-link capacitor voltage(x=1 or 2).Figure3 shows the topology of traditional two-level Z-source inverter, where the X shape capacitor-inductor network couple the rear-end inverter circuit and PV array. The unique shoot-through state of Z-source inverter can provide the voltage boost operation characteristics[13-15]. The output voltage boost ratio can be expressed as:

$$V_g = \frac{MV_{dc}}{2(1-k)}; k = \frac{T_0}{T} \quad (3)$$

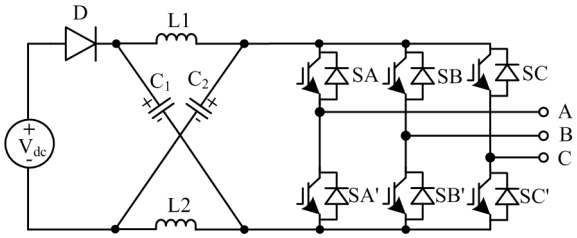


**Figure3.** Topology of two-level Z-source inverter

Where, $T$ refers to the modulation period and $T_0$ represents the shoot-through duration.

### 2.2. *Single-Stage Buck-Boost Multilevel Inverters*

Based on the single-stage buck-boost two-level converters, the buck-boost multilevel inverters were proposed in [16-19] to increase power conversion efficiency. The researches have proposed many novel topologies, and the amplitude-enhanced buck-boost NPC (AE-NPC) inverter presented in [19] can be illustrated as the typical example. Figure 4 shows the topology of AE-NPC inverter, and the voltage boost ratio can be enhanced and the dc-link voltages would be balanced by

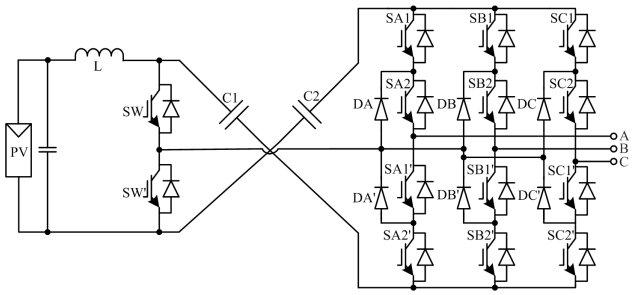


**Figure 4.** Topology of AE-NPC inverter.

controlling the two switches SW and SW′. The voltage boost ratio of AE-NPC inverter is the same as equation (2).

However, the single-stage inverters shown in Figure2-4 would only connect one PV array to power the buck-boost power generation. When implementing these inverters as the interfacing circuits in PV generation systems, they cannot effectively proceed with the power reduction

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induced by the mismatch of series-connected PV panels because of their single source nature.

To further explore the buck-boost three-level inversion techniques in the grid-tied PV implementations, this paper proposes a novel dual-source AE-NPC topology to couple two separately controlled PV sources and a NPC inversion circuit. The corresponding topological and control illustration of this novel inverter will be presented in the following sections.

## 3. Topological Illustration and Operational Principle of Dual-Source AE-NPC Inverter

The proposed dual-source AE-NPC three-level inverter with two input PV arrays is shown as Figure 5. And the voltage boost part consists of two switches and inductors. Comparing with the buck-boost inverter in Figure4, it assumes one more inductor in shunt to conduct source current in case of the unequal PV currents flowing through the circuit. The two switches SW and SW′ directly connect to the PV sources being different from Figure 4 so that two separate PV sources can be controlled independently. It is noted that the upper and lower dc conversion circuits are indeed the similar topology except for SW′ connects to the negative terminal of input source.

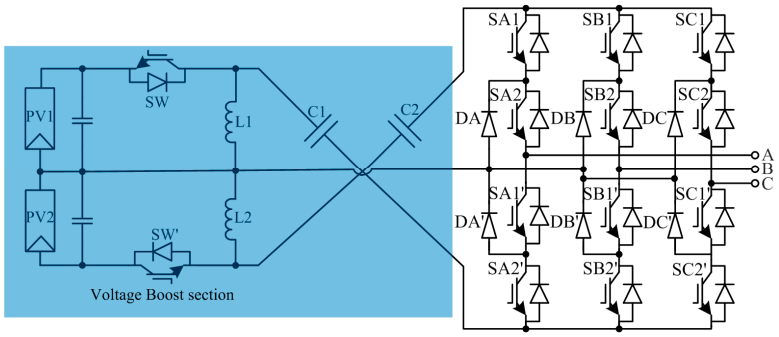


**Figure 5.** Topology of dual-source AE-NPC inverter.

The equivalent circuits are shown in Figure 6 to detailed describe operating modes of the proposed inverter. The first operating mode shown in Figure 6(a) is{ SW =ON and SW′ =OFF},where the inductor L1 is charged by the source PV1 and inductor L2 current flowing through the diodes DX and SX1 (X = A, B or C)will charge capacitor C2. Similarly, for the operating mode {SW = OFF and SW′ = ON} shown in Figure 6(b), the inductor L2 is charged by the source PV2 and the inductor L1 current flowing through diodes DX′ and SX2′ will charge the capacitor C1. According to Figure 6(a) and (b), it can be noted that when one front-end switch is ON and another is OFF, only one capacitor is charged. However the rest of NPC circuit can still work as usual. Take the operating mode {SW =OFF and SW′ = ON} for example, the NPC inverter can still output the switching states {0} and {1} of its vector diagram shown in Figure 7 since capacitor C2 and PV2 are connected in series and can power the rear-end inverter normally. Similarly, for the state SW = ON and SW′ = OFF, the NPC circuit can output the switching states {-1} and {0} of Figure 7. Figure 6(c) shows the last operating mode when SW and SW′ are both ON simultaneously, where PV1 ,C1 ,C2 and PV2 are connected in series to generate the whole dc-link sources. In this mode, the NPC inverter can freely output the three-level switching states {1}, {0} and {-1}. Therefore, when Vpv1 + Vc1 is equal to Vpv2+ Vc2, the dc-link voltages are balanced and the inverter output current is purely sinusoidal. Then the capacitor voltage can be expressed as:

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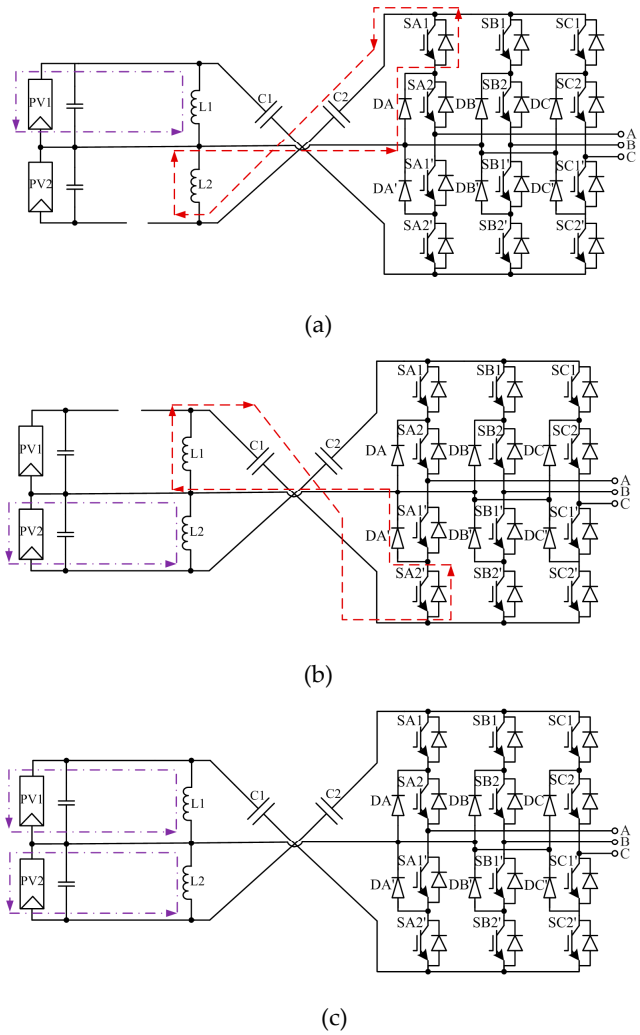


**Figure 6.** Equivalent circuits of dual-source AE-NPC inverter when (a) SW = ON and SW′ = OFF, (b) SW = OFF and SW′ = ON and (c) SW = SW′ = ON.

$$\begin{cases} \dfrac{V_{PV1}}{L_1}\times k_1 T = \dfrac{V_{C1}}{L_1}\times(1-k_1)T \Rightarrow V_{C1} = \dfrac{k_1 V_{PV1}}{1-k_1} \\ \dfrac{V_{PV2}}{L_2}\times k_2 T = \dfrac{V_{C2}}{L_2}\times(1-k_2)T \Rightarrow V_{C2} = \dfrac{k_2 V_{PV2}}{1-k_2} \end{cases} \tag{4}$$

Where $k_1$,$k_2$ represents the duty ratio of SW and SW' respectively, $V_{PVx}$ refers to the voltage of PVx (x=1,2).Therefore, the dc-link voltage is:

$$\begin{aligned} V_{up} &= V_{C2} + V_{PV2}, V_{dn} = V_{C1} + V_{PV1} \\ V_{dc} &= V_{up} + V_{dn} = \frac{V_{PV1}}{1-k_1} + \frac{V_{PV2}}{1-k_2} \end{aligned} \tag{5}$$

Where, $V_{up}$, $V_{dn}$ refers to the upper and lower dc-link voltage. If assuming $k_1 = k_2 = k$ and $V_{PV1} = V_{PV2} = V_{PV}$, the voltage boost ratio can be expressed as:

$$V_g = \frac{MV_{PV}}{1-k} \tag{6}$$

To smoothly modulate the dual-source AE-NPC inverter, this paper assumes the phase disposition (PD) modulation scheme [20]. As Figure 8 shows, the control signals of SW′ and SW is induced by two additional linear modulation references $V_U$ and $V_L$ respectively. Moreover, the NPC

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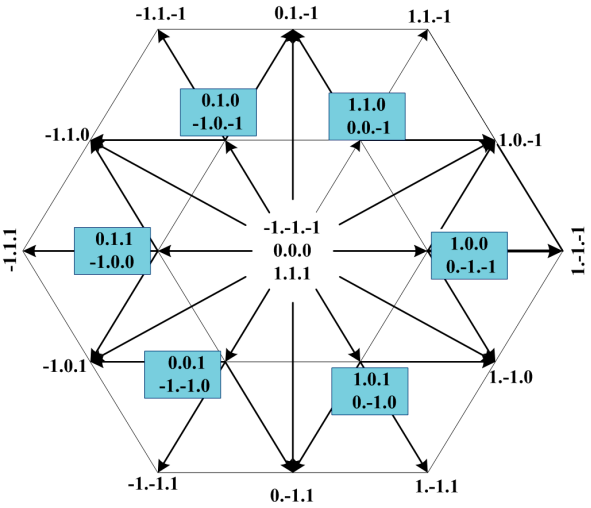


**Figure 7.** Space vector diagram of three-level inverter.

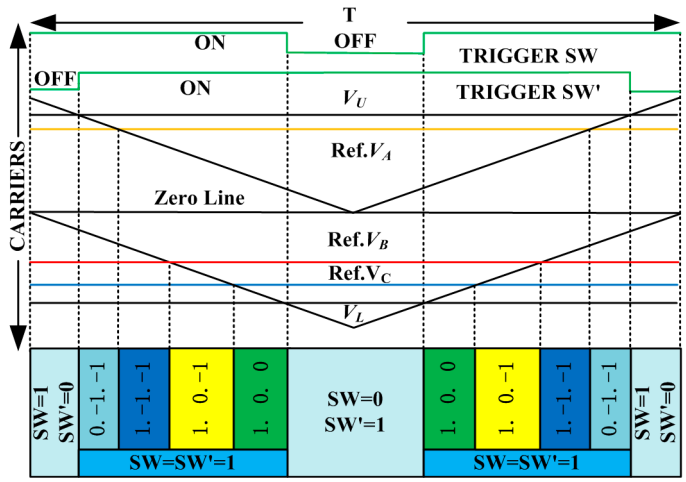


**Figure 8.** Illustration of PD modulation for dual-source AE-NPC inverter.

inverter could still output the original switching state of (0, -1, -1) or (1, 0, 0) for the operating mode{SW = 1, SW′ = 0} or {SW = 0, SW′ = 1}, which therefore coincides with the operational analysis of Figure 6(a) and (b).

## 4. Control Strategy of Dual-Source AE-NPC Inverter with the Front-End PV Sources

The main control of the dual-source AE-NPC is to maintain the MPP operation of both PV sources and meanwhile keep the output waveform quality. Figure 9 shows the control block of overall power generation system. And the two MPPT control blocks induce the modulation signals of the two switches SW and SW′, respectively. The output current reference of NPC inverter is based on the calculated active power of the PV sources. Moreover, the feedback current control would accurately control the output current and dc-link voltage. Further, the dc-link balance control is realized by modifying the PWM switching states. And the proposed control strategy will be detailed illustrated as following.

### *4.1. Maximum Power Point Control*

The perturb and observe MPPT algorithm [21-22] is assumed to maintain the MPP operation of both PV sources. The PI controller shown in (7) is adopted to precisely track the voltage reference generated by MPPT control blocks. As illustrated in Figure 9,the output of PI controller will compare

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with the triangular carriers to induce the modulation signals of SW and SW', respectively.

$$G_{PI}(s) = K_p + K_i \frac{1}{s} \tag{7}$$

*4.2. Closed-Loop Output Current Control*

The Proportional+ Resonance (PR) controller expressed in (8) is assumed to precisely trace the current reference without steady state error.

$$G_{PR}(s) = K_p + K_i \frac{s}{s^2 + w_0^2} \tag{8}$$

The ideal current reference is derived as (9), which assumes the unity power factor condition. And the power loss reference induced by dc-link voltage control is added to the current reference, which can be shown as the Figure 9.

$$I_g = \frac{2(P_{PV1} + P_{PV2})}{3V_g} \tag{9}$$

Where, $I_g$, $V_g$ represents the amplitude of ac output current and phase voltage respectively and $P_{PVx}$ refers to the output active power of *PV*x (x=*1 or 2*).

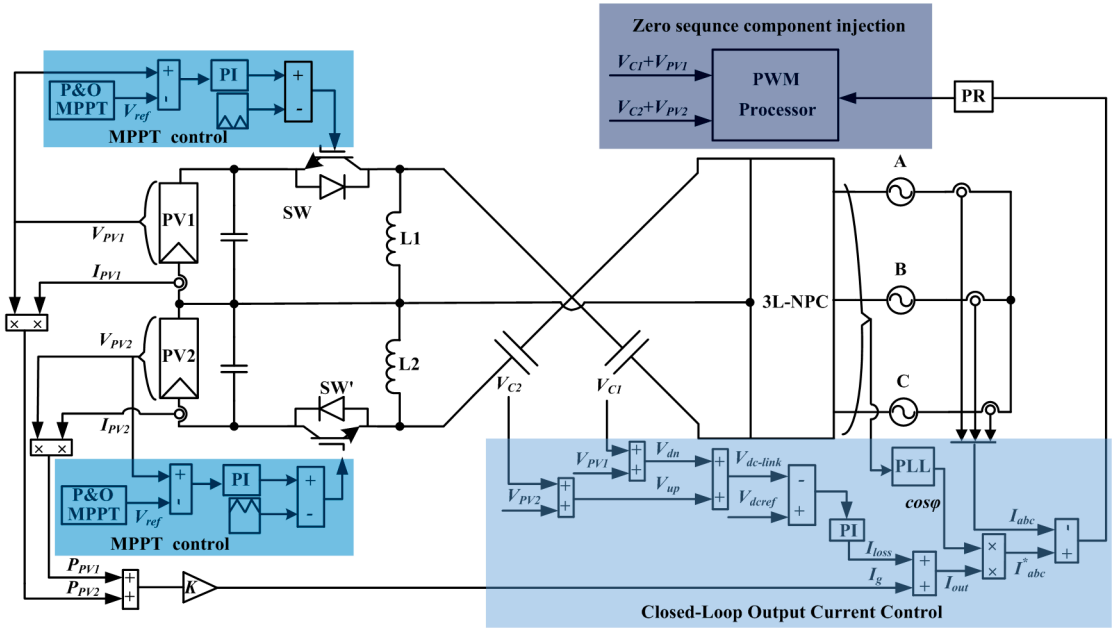


**Figure 9.** Overall control diagram of dual-source AE-NPC inverter for grid-tied PV application.

*4.3. DC-Link Voltage Balancing Control Method*

The averaged dc-link voltages can be expressed as (10) under the traditional control method when not assuming any dc-link voltage balancing control scheme.

$$V_{up\_ave} = \frac{P_{PV2} V_{dc}}{P_{PV1} + P_{PV2}}, V_{dn\_ave} = \frac{P_{PV1} V_{dc}}{P_{PV1} + P_{PV2}} \tag{10}$$

However, the PV currents in MPP condition will be different when mismatch appearing in the two input PV sources. Therefore, the charging current of dc-link capacitors would be consequently

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different under the MPP operation condition, which in turn produces the unbalanced dc-link voltages if still assuming the traditional PD modulation scheme as stated in Section III. Therefore, the possible solutions are to either balance the input power and let $P_{PV1} = P_{PV2}$, which however is not desired since the PV sources will deviate from their MPP operation, or regulate the discharging currents of dc-link capacitors. The discharging current can be modified by controlling the duration of the inner vectors in Figure 7 [23]. For example, two equivalent null states (0, -1, -1) and (1, 0, 0) per switching sequence in Figure 8 could output the same line voltage but the opposite direction neutral current. Therefore, adjusting the duration of equivalent null states can change the discharging current of dc-link capacitors and then balance the dc-link voltages. In specific, the way to realize the balanced dc-link voltages meanwhile keep the MPP operation unchanged in this paper is to use the zero-sequence component injection method to change the switching duration of equivalent null states and consequently the discharging duration of the dc-link capacitors[23-28].The illustration of the modified PD modulation strategy with zero-sequence component injection is shown in Figure 10, where the positive zero-sequence component is injected to increase the duration of state (1, 0, 0) and decrease the duration of state (0, -1, -1) and then the upper dc-link voltage can be decreased and meanwhile it will not induce the low order harmonic distortion.

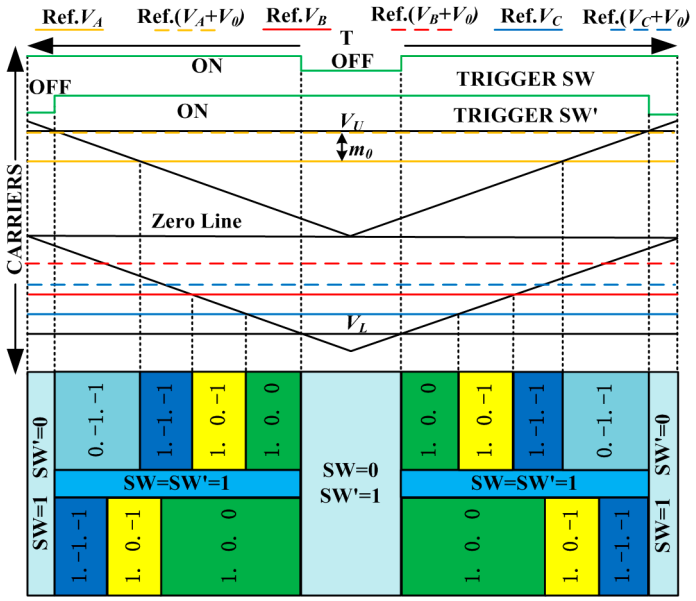


**Figure 10.** Illustration of the modified PD modulation strategy with zero-sequence component injection.

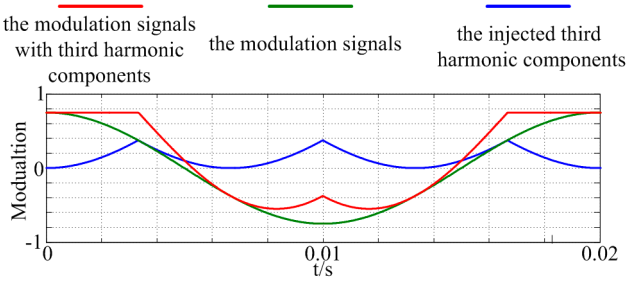


**Figure 11.** The ideal modulation references of the AE-NPC converter

When the zero-sequence voltage injection method is assumed, the neutral current can be expressed as:

$$I_0 = -|m_a + m_0| \cdot I_g \cos(\omega t) - |m_b + m_0| \cdot I_g \cos(\omega t - 2\pi/3) - |m_c + m_0| \cdot I_g \cos(\omega t + 2\pi/3) \quad (11)$$

Where, $m_x$ ($x$ =$a$, $b$ or $c$) refers to the modulation references and $m_0$ represents the zero sequence

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component, which can be written as:

$$m_0 = \begin{cases} M - \max(m_a, m_b, m_c) & \mathrm{V_{up}} \geq \mathrm{V}_{dn} \\ -M - \min(m_a, m_b, m_c) & \mathrm{V_{up}} \leq \mathrm{V}_{dn} \end{cases} \quad (12)$$

Figure 11 illustrates the modulation references with and without the zero-sequence component. In addition, the averaged neutral current $I_{0\_ave}$ can be derived as:

$$I_{0\_ave} = \frac{1}{2\pi}\int I_0(wt)d(wt) \quad (13)$$

According to (11) -(13), the averaged neutral current is not zero and the discharging current of dc-link capacitors will be controlled unequally. Moreover, the dc-link voltage can be balanced when the averaged output current of the dc-link capacitors satisfy the following equation：

$$\left.\begin{array}{l} V_{dc-link} I_{up\_ave} \big/ 2 = P_{PV2} \\ V_{dc-link} I_{dn\_ave} \big/ 2 = P_{PV1} \end{array}\right\} \Rightarrow I_{up\_ave} - I_{dn\_ave} = \frac{2(P_{PV2} - P_{PV1})}{V_{dc-link}} = -I_{0\_ave} \quad (14)$$

The zero-sequence component injection can fulfill the dc-link balance and MPP operation. However, such regulation has a limitation since the range of controlled averaged neutral current is limited. Concerning the cases, where the great difference appears between the output power of two PV sources, the positive or negative zero-sequence component should be always injected to balance the dc-link voltage. According to the aforementioned critical cases, the range of the averaged neutral current $I_{0\_ave}$ can be derived as below from (13):

$$\text{-}0.33MI_g \leq I_{0\_ave} \leq 0.33MI_g \quad (15)$$

Further, according to (14) and (15), the dc-link voltage can be balanced when the following inequality is satisfied:

$$0.64 \leq \frac{P_{PV1}}{P_{PV2}} \leq 1.56 \quad (16)$$

## 5. Efficiency Comparison

Comparing to the two-level inverter, the NPC inverter is certified owing better efficiency when both switching frequency is larger than 8 kHz [29]. Since the switching frequency in the PV application with rated power < 30kW is 10kHz or more, the two-stage three-level NPC inverter will be more efficient than the two-level converter. On the other hand, along with the mature of 1500V PV panel technology, the PV system can be integrated into a high voltage grid (e.g. 690V grid) to reduce losses. For this case, the NPC inverter could be deemed as a competitive candidate in practice. Therefore, the efficiency comparison in this paper will focus on the PV applications shown in Figure 1 and the proposed PV converter.

Before analyzing the switching losses, a fair basis for comparison is drawn by first tuning the inverters to produce the same input-to-output voltage gain. The duty ratios of front-end switches SW and SW' in dual-source AE-NPC inverter and two-stage NPC inverter can be derived as:

$$\frac{M_B}{2(1-k_B)} = \frac{M_S}{1-k_S}; 0.5 \leq k_S, k_B \leq 1 \quad (17)$$

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Where, the subscripts "*B*" and "*S*" represent two-stage NPC inverter and the proposed single-stage NPC inverter, respectively. As analyzed above, the modulation index $M_S$ of dual-source AE-NPC inverter should set to be $k_S$ to maximize the dc-link voltage utilization, while the modulation index $M_B$ of two-stage NPC inverter is independent on $k_B$, which can be set to 1. Then the relationship of dc-link voltages of both inverters can be described as:

$$V_B = k_S V_S \tag{18}$$

The dual-source AE-NPC inverter experiences a higher dc-link voltage stress and will have more switching losses in the rear-end NPC circuit. However, the blocking voltage of the front-end switches SW and SW' in dual-source AE-NPC inverter is less than the blocking voltage of switches and diodes in the front-end boost converters of two-stage NPC inverter and the dual-source AE-NPC inverter will have less switching losses in the front-end circuit. Since both NPC circuitries have the same output current and the conduction currents of both inverters will keep equal at any particular instant time, conduction dissipation of the rear-end NPC circuitry will not be discussed in this paper.

The switching dissipation and conduction dissipation of the IGBT assumed in both topologies can be derived as[30]:

$$\begin{cases} P_{switch} = \dfrac{1}{2} V_{OFF} I_{ON} t_{tr} f_{SW} \\ P_{cond} = V_{CE} I_{ON-ave} \end{cases} \tag{19}$$

Where, $P_{switch}$ refers to the total switching dissipation of single-stage or two-stage converter, $V_{CE}$ ,$V_{OFF}$ refers to forward drop voltage and turn-on or turn-off voltage of switches respectively. $I_{ON}$ represents the conducting current of the switches, $t_{tr}$ means the turn on and off transient duration of switches and $f_{SW}$ refers to switching frequency. The switching dissipation of both inverters, controlled using the switching sequence shown in Figure 8 with dc switches commutating twice and the ac bridge commutating six times per carrier cycle, can be derived as:

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$$\begin{cases} P_{switch\_dc(S)} = \dfrac{1}{2} V_S I_L t_{tr} f_{SW} \\ P_{switch\_ac(S)} = \dfrac{3}{\pi} V_S I_g t_{tr} f_{SW} \\ P_{switch(S)} = P_{switch\_dc(S)} + P_{switch\_dc(S)} = t_{tr} f_{SW} P_{in} (V_g + V_{PV}) (\dfrac{4}{\pi V_g} + \dfrac{1}{2V_{PV}}); P_{in} = P_{PV1} + P_{PV2} \end{cases} \tag{20}$$

*Two-stage NPC inverter*

$$\begin{cases} P_{switch\_dc(B)} = V_B I_L t_{tr} f_{SW} \\ P_{switch\_ac(B)} = \dfrac{3}{\pi} V_B I_g t_{tr} f_{SW} \\ P_{switch(B)} = P_{switch\_dc(B)} + P_{switch\_ac(B)} = t_{tr} f_{SW} P_{in} (\dfrac{4}{\pi} + \dfrac{V_g}{V_{PV}}) \end{cases} \tag{21}$$

Where, $I_L$ refers to input inductor current and $P_{switch\_dc}$ , $P_{switch\_ac}$ represents the dc and ac side switching dissipation. According to the equations(20) and (21),the switching dissipation difference between both topologies can be derived as:

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$$\Delta P_{switch} = P_{switch(S)} - P_{switch(B)} = t_{tr} f_{SW} P_{in} (\frac{4V_{PV}}{\pi V_g} - \frac{V_g}{2V_{PV}} + \frac{1}{2}) \quad (22)$$

It is noted from (22) that the proposed single-stage PV converter has lower switching dissipation when the boost ratio($V_g/V_{PV}$) is greater than 2.17.Moving on to analyze the conduction losses, where the forward voltage drop of the diodes and switches is assumed to be equal, then the conduction dissipation of the front-end circuits can be described as:

$$\begin{cases} P_{cond(S)} = 2\times V_{CE} I_L + 2\times 2V_{CE}(1-k_S) I_L = \frac{V_{CE}}{V_{PV}} P_{in} (1 + \frac{2V_{PV}}{V_{PV} + V_g}) \\ P_{cond(B)} = 2\times V_{CE} k_B I_L + 2\times V_{CE}(1-k_B) I_L = \frac{V_{CE}}{V_{PV}} P_{in} \end{cases} \quad (23)$$

Where, $2\times V_{CE} I_L$ and $2\times V_{CE} k_B I_L$ represent the conduction dissipations during the switch ON period and $2\times 2V_{CE}(1\text{-}k_S) I_L$ and $2\times V_{CE}(1\text{-}k_B) I_L$ represent the conduction dissipations during the switch OFF period, respectively. Similarly, the conduction dissipation difference between the front-end circuits can be derived as:

$$\Delta P_{cond} = P_{cond(S)} - P_{cond(B)} = \frac{2V_{CE} P_{in}}{V_{PV} + V_g} \quad (24)$$

According to (24), the dual-source AE-NPC inverter always produces a higher conduction loss than the two-stage NPC inverter. However, its prominence can be reduced by reasonably using the devices with a lower forward voltage drop since the blocking voltage of SW and SW' is only half of the dc-link voltage unlike the traditional two-stage NPC inverter. And the total dissipation difference between both converters can be derived from (22) and (24), whose normalized expression is written below.

$$\Delta P_{dis} / P_{in} = t_{tr} f_{SW} (\frac{4V_{PV}}{\pi V_g} - \frac{V_g}{2V_{PV}} + \frac{1}{2}) + \frac{2V_{CE}}{V_g + V_{PV}} \quad (25)$$

Where, $\triangle P_{dis}$ represents the total dissipation difference and $P_{in}$ refers to the input power. It is noted from (25) that the dissipation comparison between both converters is related to the parameters of switching frequency $f_{SW}$, input PV voltage $V_{PV}$, grid voltage $V_g$ and forward voltage drop $V_{CE}$. For the exampled illustration, the theoretical calculation assumes the IGBT of FF150R17KE4 produced by Infineon and $V_{CE}$, $t_{tr}$, $f_{SW}$ to be 1.75V, 1300ns, 20kHz, respectively. The calculation results are drawn in Figure 12. When PV voltage is below the threshold voltages shown in Figure12(a),the dual-source AE-NPC inverter will have lower dissipation than the two-stage inverter ($\triangle P_{dis}/P_{in}<0$) in the conditions that line to line grid voltage $V_{ac}$ is equal to 380V, 600V or 690V, respectively. The dissipation comparison for different PV voltages and switching frequencies is also presented in Figure12(b), where $V_{ac}$=690V.

Comparing to the two-stage NPC inverter, the proposed inverter saves two diodes and has lower voltage rating dc-link capacitors and lower voltage rating of front-end switches and also has higher efficiency in the high voltage boost ratio applications.

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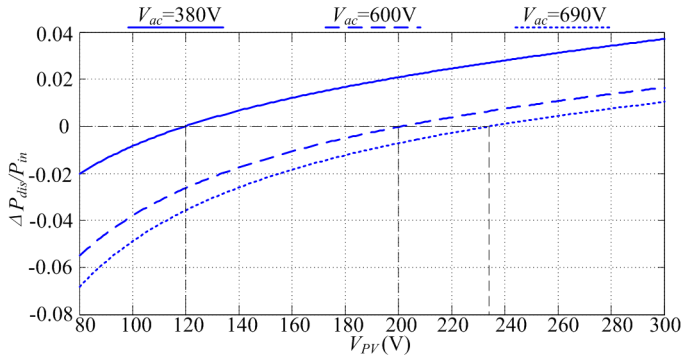
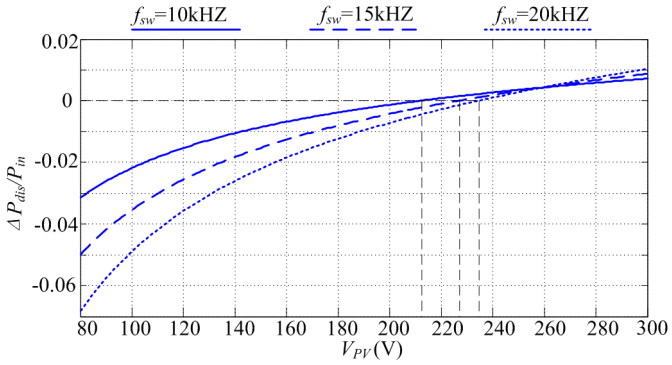



(a)




(b)

**Figure 12.** dissipation comparison under(a) different ac output voltages and (b) different switching frequencies.

## 6. Simulation and Experimental Verifications

The amplitude-enhanced neutral point clamped converter is built by MATLAB/SIMULINK. And Table 1 shows the AE-NPC circuit and two PV sources parameters. Figure 13 shows the temperature variation and irradiation effect on the output of buck-boost photovoltaic power generation. The output active power is described as Figure13(a), where the temperature of PV2 decreases from 15C° to 10C° at the time 0.07s and irradiation varies from 1000W/m² to 650W/m² at 0.05s respectively. Therefore the output power of PV1 is decreased to about 2000W at the time 0.05s with fast response and PV2 output power increases 70W at the time 0.07 because of temperature variation. Moreover the proposed control strategy can fast track the MPP variation, which can be shown as Figure13(a). Figure 13(b) shows the PV voltages under their corresponding maximum power points. Figure 13(c) shows the measured dc-link voltage and the dc-link voltage can be balanced by controlling different $k_1$, $k_2$ and meanwhile modifying the switching states of rear-end NPC circuit to compensate the mismatch of upper and lower PV array. And the PV currents under the maximum power point operation condition is shown as Figure13(d), which keep equal under the same temperature and irradiation condition. Moreover, the PV2 current almost keep unchanged when the PV2 temperature varies to 10 C°, and the PV1 current has a sharp decline because of the irradiation variation. However, different PV currents would not affect the whole operational effectiveness due to the novel topological circuit.

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**Table 1.** Simulation parameters

| | | | |
|---|---|---|---|
| dc-side inductor | 2mH | line inductor | 5mH |
| dc-link capacitor | 1000μF | grid phase voltage | 311V |
| dc-link voltage | 800V | carrier frequency | 10kHZ |
| PV array short-circuit current(1000W/m²) | 38A | PV array open circuit voltage(15C°) | 109V |

Further, the voltage and current are shown in Figure14 and 15. Figure 14 shows one switching phase voltage ,one switching line voltage and modulation signal. As the Figure14 shows, after the third harmonic component injection the modulation signal and the switching characteristics of phase voltage will be changed after 0.05s. However, such changes will not lead to the normalized volt-sec average change and the three-phase output currents are still purely sinusoidal which can be shown as Figure 15. Moreover, the FFT analysis of the grid current is shown in Figure 16 and the current THD is 1.57%.

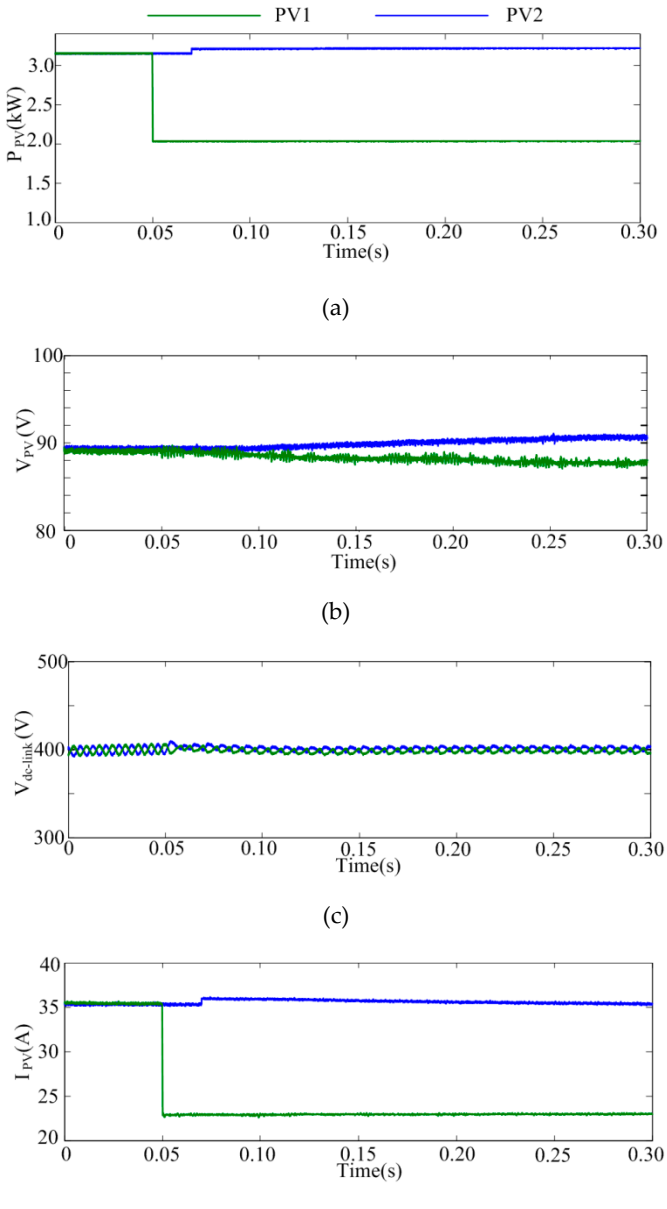


**Figure 13.** Simulated results of (a) output PV power, (b) PV voltages,

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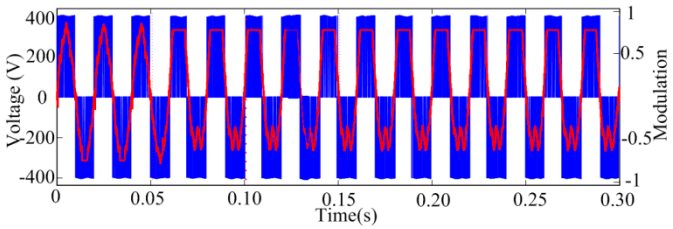
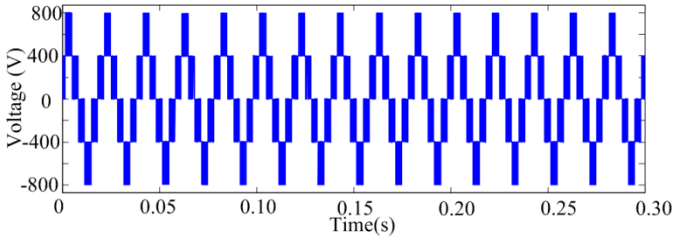
(c) dc-link voltages (Vpv+Vc) and (d) PV currents.

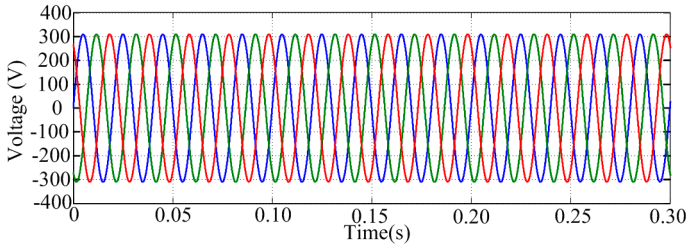



(a)

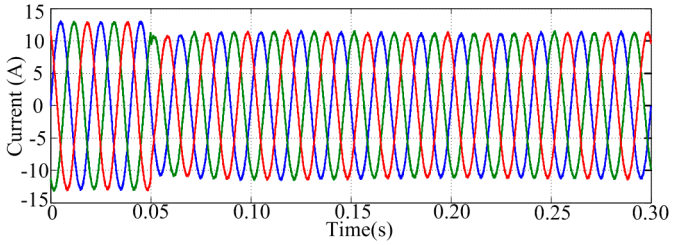



(b)

**Figure 14.** Output waveform of (a) switching phase voltage and its modulation reference and (b)switching line voltage.




(a)




(b)

**Figure 15.** Waveforms of (a) grid voltages and (b) grid currents

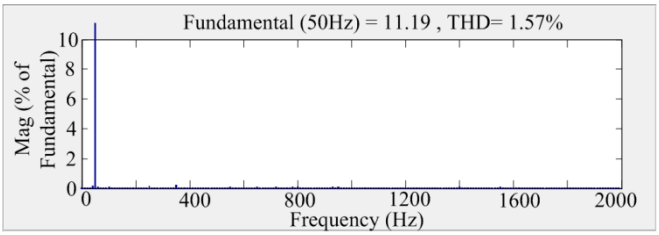



**Figure 16.** FFT analysis of the output ac current.

Next, proceeding to the experimental verification, the corresponding experimental parameters are listed in Table 2. The maximum power points of two PV arrays are both 47V and 7.4A. The output power of the whole PV arrays is about 700W, and the amplitude of output ac current is

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about 3.0A.The picture of experimental prototype is shown in Figure 17.The waveforms of grid voltage and output currents are shown in Figure 18. It is noted that the inverter can output the balanced sinusoidal currents. The harmonic spectrum of phase current is shown in Figure 19. Fortunately, the assumed zero-sequence component injection method did not produce the low order harmonic distortion and the THD of phase current is about 2.56%.

**Table 2.** Experimental parameters

| | | | |
|---|---|---|---|
| dc-side inductor | 2mH | line inductor | 5mH |
| dc-link capacitor | 550μF | grid phase voltage | 155V |
| dc-link voltage | 450V | carrier frequency | 10k HZ |
| PV array short-circuit current(1000W/m$^2$) | 7.80A | PV array open circuit voltage(0C$^o$) | 58.3V |

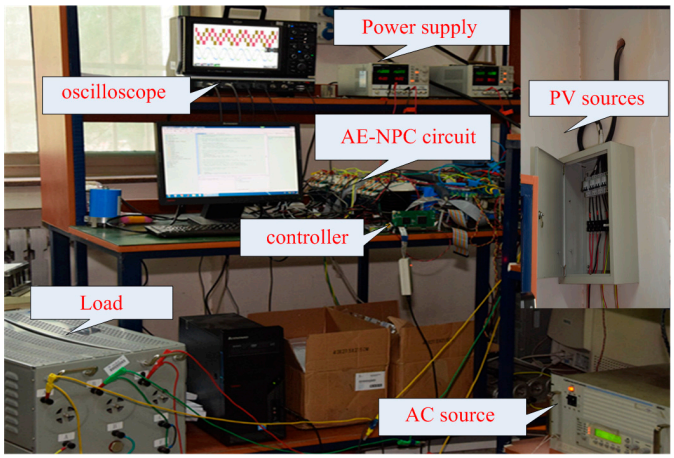


**Figure 17.** The experimental prototype of dual-source AE-NPC inverter.

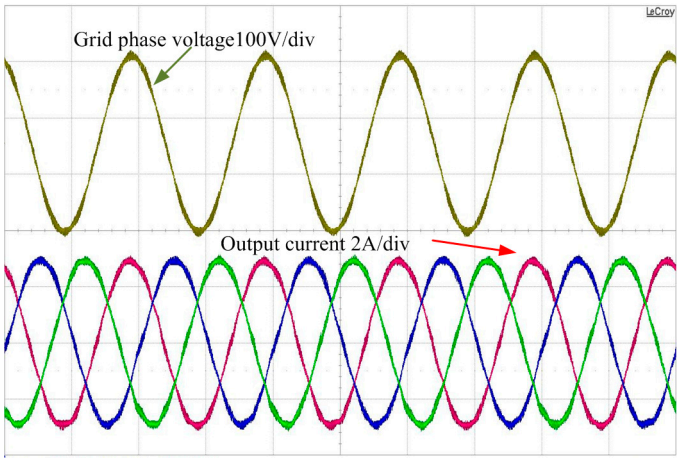


**Figure 18.** Captured grid voltages and output currents.

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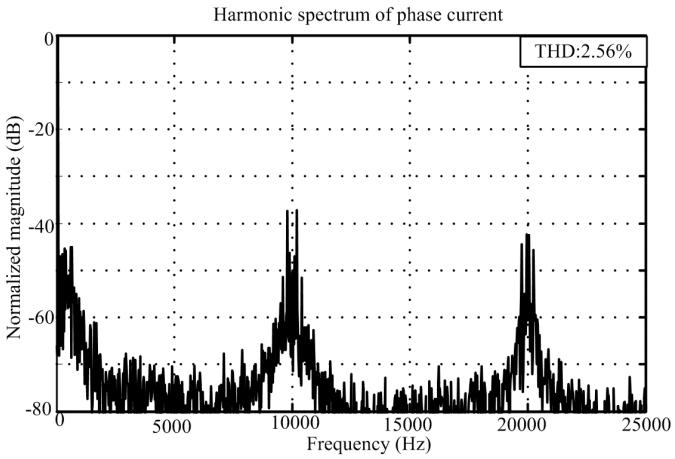


**Figure 19.** Harmonic spectrum of phase current.

As shown in Figure 20, the voltages of dc-link capacitors are about 178V and the whole dc-link voltage is about 450V.However, the dc-link voltage is not strictly balanced before operating the zero-sequence component injection function as shown in the left half of Figure 20. In specific,$V_{PV2}$+$V_{C2}$ is equal to 229V while $V_{PV1}$+$V_{C1}$ is about 221V.After assuming the zero-sequence component injection method as presented in Section IV, the dc-link voltage was balanced which can be observed from the right half of Figure 20.

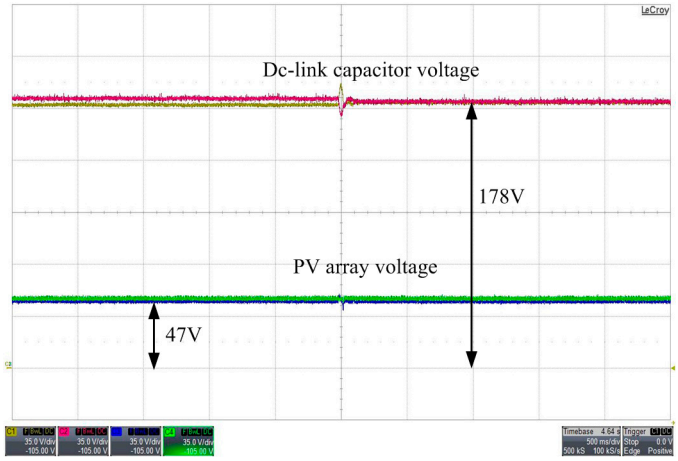


**Figure 20.** DC-link capacitor voltages and PV array voltages.

The switching phase voltages and phase B current are shown in Figure21 and Figure22 shows the switching line voltages and output currents, where the output current is almost purely sinusoidal.

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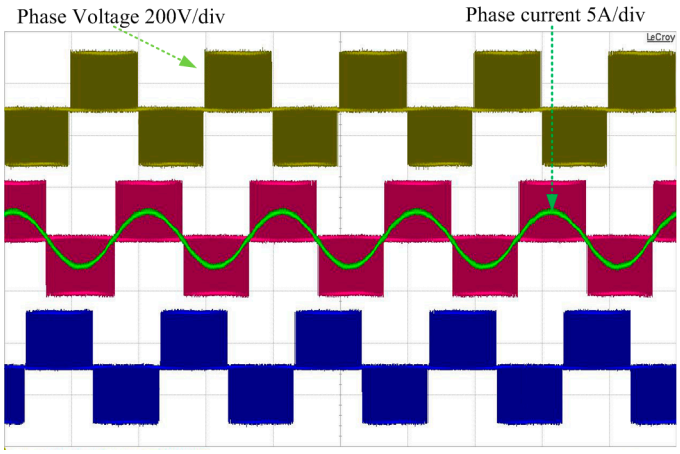


**Figure 21.** Switching phase voltages and phase B current.

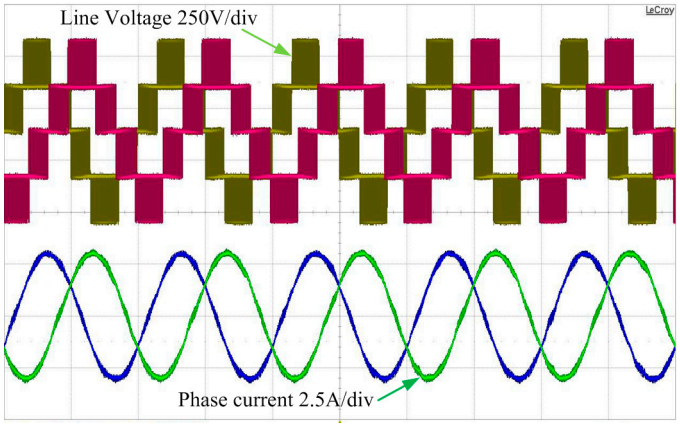


**Figure 22.** Switching line voltages and phase currents.

## 7. Conclusions

This paper proposes a novel single-stage buck-boost three-level NPC inverter, which can couple two separate dc sources in front and maintain the balance between upper and lower dc-link voltages. The corresponding operational principles are analyzed. When it is applied as the interfacing circuit between PV arrays and power grid, the zero-sequence component injection method can be employed to balance the dc-link voltage whenever the irradiation and temperature between two PV arrays are different. In addition, this paper illustrates the overall control scheme of the proposed converter for grid-tied PV application and compares the efficiency performance. MATLAB simulations and experimental results verified the performance of grid-tied PV system using the proposed converter.

**Author Contributions:** Xuefeng Ge. and Mengxing Chen conceived and designed the experiments; Xuefeng Ge wrote the paper and Feng Gao revised it.

**Conflicts of Interest:** The authors declare no conflict of interest.

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