

*Article*

# Exploring FPGA Based Lock-in Techniques for Brain Monitoring Applications

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**Abstract:** Functional Near Infrared Spectroscopy (fNIRS) systems for e-health applications usually suffer of poor signal detection mainly due to a low end-to-end signal to noise ratio of the electronics chain. Lock-In Amplifiers (LIA) historically represent a powerful technique helping to improve performances in such circumstances. In this work it has been designed and implemented a digital LIA system, based on a Zynq® Field Programmable Gate Array (FPGA), trying to explore if this technique might improve fNIRS system performances. More broadly, FPGA based solution flexibility has been investigated, with particular emphasis applied to digital filter parameters, needed in the digital LIA, and it has been evaluated its impact on the final signal detection and noise rejection capability. The realized architecture was a mixed solution between VHDL hardware modules and software ones, running within a softcore microprocessor. Experimental results have shown the goodness of the proposed solutions and comparative details among different implementation will be detailed. Finally a key aspect taken into account throughout the design was its modularity, allowing an ease increase of the input channels while avoiding the growth of the design cost of the electronics system.

**Keywords:** Digital Lock-in Amplifier (DLIA); Field Programmable Gate Array (FPGA); Near Infrared Spectroscopy (NIRS); Hardware Description Language (HDL); Light Emitting Diode (LED); Silicon Photomultiplier (SiPM); Microprocessors

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## 1. Introduction

The study of Lock-in techniques to detect and measure very small signals, usually deeply dipped into high level noise, has been investigated since the late '40 [1-2] of the last century. Quite soon it was clear the great potential, irrespective of the frequency range in which it found application, the method owned. Lock-in amplification is mainly a phase-sensitive detection technique capable to isolate a piece of the signal at a specific reference frequency and phase. Even if this signal is buried into noise sources many times larger, the system cuts down and strongly rejects noise signals, at frequencies other than a reference "locked-in" frequency, so they do not affect the signal measurement.

For long time Lock-in techniques were strongly based on analog electronics components, since the advents of powerful digital systems, namely DSP (Digital Signal Processor), 32bits microprocessors with internal DSP capabilities, ASICs and PLDs (Programmable Logic Devices or Field Programmable Gate Array), progressively replaced analog models by outperforming them in every aspect such as the allowable frequency range, the level of input noise and the stability; all of them directly related to the sampling speed of the front-end ADCs besides the available digital computing power.

Many applications have profited of Lock-in systems, spanning among very different fields. Some researchers successfully used it for low-frequency photothermal detecting systems [3] where

multiple demodulating channels, implemented within a unique FPGA, allowed compact yet simultaneous analysis of the signal of interest with multiple different frequencies. Another interesting study has been carried out for portable pulse-oxymeter applications [4] where a single CMOS chip was designed with an integrated LIA in order to reach very low power consumption.

Advantages of FPGA based LIA systems were also investigated in [5], where emphasis was given to their compactness and low-cost implementation caused by the FPGA flexibility in fulfilling more than a single digital task at the same time.

Within the e-health field, remarkable importance has been given to brain studies and recent investigations on neurology and Brain Computer Interface (BCI) have proved the benefits of functional Near-Infrared Spectroscopy (fNIRS) acquisition systems, especially when combined with simultaneous EEG, for better understanding the spectroscopy results. Various commercial products and research prototypes have been proposed in literature so far [6-10] and this work also aims to contribute to this interesting research subject. In particular in [10], the system is based on double wavelength LEDs injecting infrared light into the scalp and recovering back the light, partially diffused and partially scattered, from the same surface but at a few centimeter away from the optical source, using a lock-in technique. At a proper source-detector distance, usually ranging between 2 to 3 cm, it is possible to detect brain activities related to suitable stimuli, in the form of oxygenation variations. Of course higher number of sources-detectors couples (called fNIRS channels) lead to better volume resolution on the whole head, eventually ending up with a complete brain oxygenation mapping capability.

Since human scalp presents quite high attenuation values in the infrared region and it is not possible to increase the amount of impinging light for safety reasons, it is of great importance the choice of very sensitive detectors, capable to fully reach single photon counting performances. Silicon Photomultipliers (SiPM) have been then adopted since they fulfill these fierce requirements [11-14] and the rest of this paper will describe the system architecture that has been realized and the experimental results that evaluate the obtained performances in term of fidelity on the detecting action and the related computational loads.

The main goal of this work is to explore the possibilities of a digital implementation of LIA systems to improve fNIRS system performances and to evaluate its impact on the final signal detection and noise rejection capability.

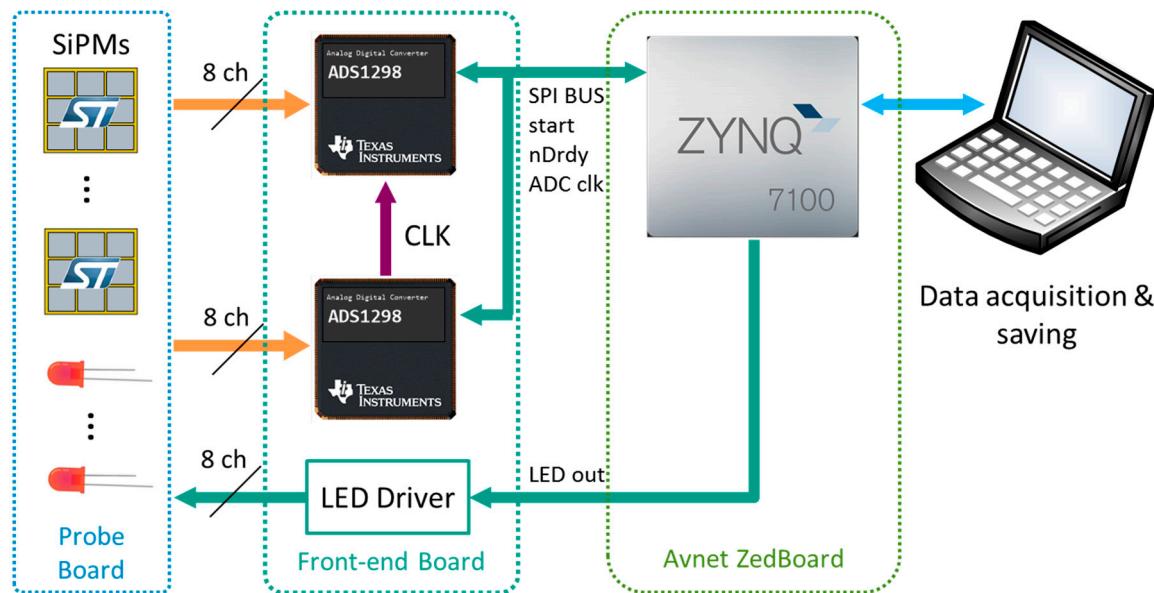
Moreover, as secondary goals, to exploit FPGA flexibility by investigating the overall latitude of the method, with particular emphasis on playing with the LIA digital filter parameters; and to predict the possibility to implement, for a limited number of channels, these algorithms on a general-purposes microcontroller.

## 2. System Architecture

In order to reach the described goals, a system able to accomplish the desired tasks and to assure a rapid prototyping has been designed, capable to leave the highest possible freedom degrees for further investigations and optimization of performances based on parameters elaboration.

The implementation of the lock-in amplifier used is the well-known dual-phase LIA [5]. It takes the input signal, modulated at a predefined and fixed frequency, and multiplies it by a generated sine and cosine reference signals, running at the same frequency of the modulated signal. The outputs are low-pass filtered with a properly designed digital filter in order to reject noise and unwanted frequency components. The obtained filtered signals from each branch represent the convolutions of the input signal and the sine and cosine reference signals. In order to find the channel output amplitude, these convolutions are then squared and summed up together, and finally the square root is calculated. Signal phase is meanwhile neglected because it isn't adding significant information in our investigations.

So, as depicted in Figure 1, it has been designed a system consisting of a probe board, a front end board, an FPGA board (Avnet ZedBoard™ in our case), and a PC for programming, data retrieving and tests.



**Figure 1.** Block diagram of the overall system architecture.

## 2.1 Probe board

The probe board contains 16 Silicon Photo Multipliers (SiPMs) and 4 dual-wavelength LEDs (850, 735 nm). It is implemented on a flexible PCB (made of Kapton™), capable to be easily adapted, as in typical fNIRS application of brain oxygenation monitoring, to the different shapes of the subject under test. A deeper description of these probe boards can be found in [11].

## 2.2 Front End Board

The front-end board is responsible of analog to digital data conversion and uses two ADS1298 analog-digital converters (ADCs), connected in daisy-chain in order to acquire a total of 16 output signals coming from the probe board. ADS1298 is a low power analog front-end (AFE) optimized for medical instrumentation systems, manufactured by Texas Instruments [15]. It performs a true simultaneous sampling of 8 channels with 24 bit delta-sigma ( $\Delta\Sigma$ ) ADCs, each containing a built-in programmable gain amplifier (PGAs). It can operate, in free run, with data rate capabilities ranging from 250 SPS up to 32 kSPS; even if at the fastest 16-32 kSPS sampling speed, resolution is limited to 16 bits. These devices can be cascaded in daisy-chain configuration; thus by sharing the same reference clock and using an external start pulse, it is possible to run a potentially very large number of simultaneous channels. Within the presented work, our system was limited to 16 channels only, but it can be easily upgraded up to 128 channels by simply cascading eight front-end boards.

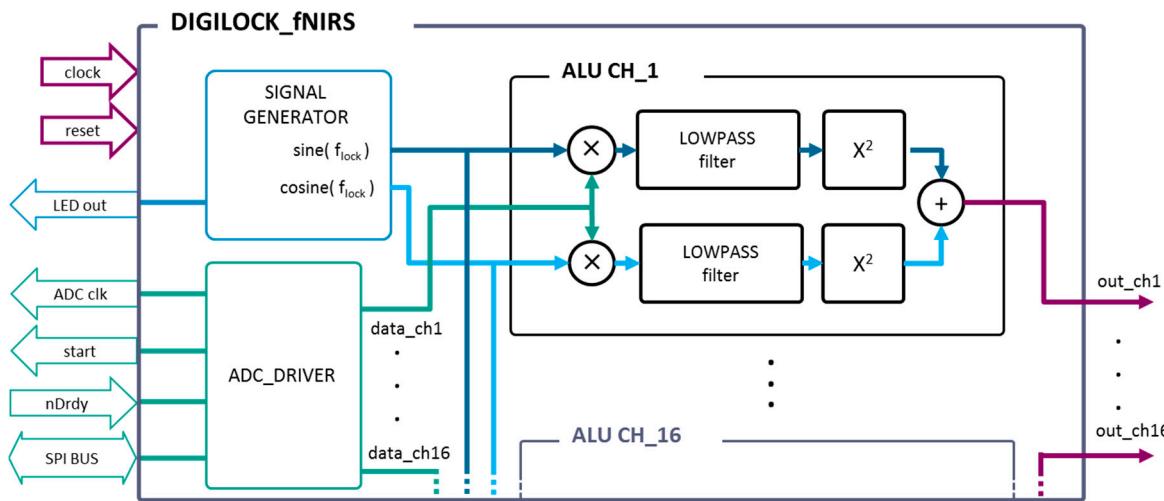
In addition, the front-end board also has some suitable circuitry needed to LEDs driving, as visible in Figure 1. For the purpose of this work a fixed value of current (about 1 mA) was necessary hence a simple circuit had been used to drive LEDs when the correspondent digital input is high.

## 2.3 Avnet Zedboard

The core of the system has been realized on an Avnet ZedBoard™ [16], a development board based on the Xilinx Zynq®-7000. All Programmable SoC. Zynq®-7000 implements a dual ARM Cortex-A9 based processing subsystem, with a large series of peripherals (Ethernet, USB, SD card, etc.), and has a large programmable logic blocks section, connected to other peripherals. Internal communication between the inner parts of FPGA is assured by high speed AXI bus. This configuration allows the realization of very fast and performing low level entities, and due to the presence of internal ARM microcontroller to easily interface the board and data with external systems. The board has been programmed using XILINX Vivado® EDA software.

Programmable logic blocks of FPGA has been extensively used, to control the Front-end board and to implement most of the entities needed to realize the lock-in amplifier; whereas some less demanding functions run in the above mentioned ARM processors.

The implemented programmable logic entities, repeated for each channel (see Figure 2) are: an ADC Driver, a signal generator and the tailored ALU.



**Figure 2.** Block diagram of the designed FPGA entities.

The *ADC DRIVER* communicates with daisy chained ADCs, using SPI protocol, providing same *ADC clock* and *Start* conversion signals. When the signal *nDrdy* is asserted, a new set of data samples are ready to be collected. The entity parses the received packet and gives an output signal for each channel. The SPI frequency is 16 MHz with a sampling rate of 16 kSPS.

The *SIGNAL GENERATOR* is mainly a look-up table working as a functions generator and it also creates a coherent square-wave digital signal at lock-in frequency named *LED out* used to properly synchronize probe's LEDs. Lock-in frequency is generated dividing sampling frequency by integer factors (8, 10, 16 or 20) selectable with switches on the FPGA board. Sine and cosine outputs are shared among all ALU entities.

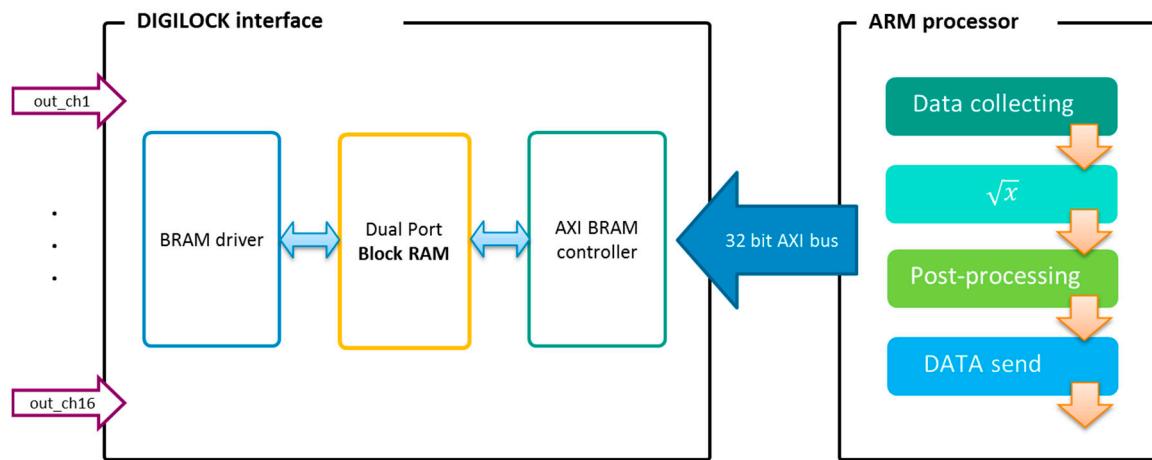
The *ALU* implements the core part of the lock-in amplifier. It performs multiplications of the input signal by reference signals, the low pass filtering, the square and the sum of the obtained signals. These output values are then stored in the internal dual port Block RAM.

Within the lock-in algorithm, a final square root operation is needed and it was decided to execute it using the softcore ARM processor of the FPGA, mainly because it was the easiest solution, even if the design of an optimized programmable logic entity executing the square root would have required a little extra effort only.

Data sharing between Programmable Logic (PL) side and the internal ARM processor goes through a dual port Block RAM. This memory resides on programmable logic and is transparently mapped into ARM memory space through the AXI Block RAM controller (see Figure 3).

The PL interrupts the ARM processor every time a new set of data samples, raw input and lock-in data output for each channel, are ready. Square root operations and needed signals post-processing to adjust voltage scale are performed, by ARM processor, before sending data to the PC for subsequent evaluation.

The ZedBoard™ is linked to a host PC through a Gigabit Ethernet connection, capable to transmit a TCP packet every data set with negligible delay. This mechanism ensures that all data samples are promptly delivered to Host PC.



**Figure 3.** Programmable Logic interface and ARM processor tasks.

#### 2.4 Filters design

The key component of lock-in chain is the way the low pass filter is designed and implemented, because it has a deep impact on the reconstruction of original input signal. Signals coming out from optical sensors have typical bandwidth ranging from DC up to 8 Hz, while the attenuation must be high enough to reject unwanted noise near the designed lock-in frequency. These constraints must be satisfied by the filter's transfer function. In order to investigate on the behavior of different filter architectures on output signals, some FIR and IIR filters have been designed and instantiated within the FPGA hardware; they have also been experimentally tested by providing with the same input data samples in order to highlight the differences.

The pass-band frequency of the filter was set slightly bigger than the maximum frequency component of the fNIRS signal, has been chosen 10 Hz. Besides, the roll-off of the transition band was chosen as a compromise between filter complexity and response characteristics.

FIR filter has been designed as two-stages cascading FIR filters, using MATLAB® Filter Designer tools. The first stage has 10 Hz pass frequency and 100 Hz stop frequency while the imposed slope provides about 80 dB of attenuation at the stop frequency. It uses equiripple filter configuration and it involves 724 taps [17]. The first stage has been internally divided in twelve parts, running in parallel with results summed together, each with a 64 serial taps block in order to properly balance computation load, using zeros coefficient padding to obtain an integer multiple of 64. The second stage has been added to eliminate the residual signal outside the band of interest. It is a 64 coefficients equiripple FIR filter, and has 150 Hz pass frequency and 1800 Hz stop frequency with an attenuation of 100 dB. Taps' coefficients are represented with signed 16 bit integers.

The designed IIR filter is a 4° order filter implemented as cascade of two identical stages of Direct Form II Biquad architecture. The selected architecture, for the IIR filter, is the well-known Biquad implementation (2° order filter with one stage), mainly for its low phase distortion and remarkable stability to truncation errors. IIR filter coefficients have been designed using a MATLAB® script, as described in [18]. Each stage has a 3dB frequency located at 10 Hz and an attenuation of 40 dB at 100 Hz. Since Zynq® FPGA doesn't implement an internal floating point unit in hardware, the hardware arithmetic of the filter uses 32bits integer numbers but, to achieve a correct computation, a 2.30 fixed point coefficients representation (2 digits for integer part and 30 for decimal part) has been used. The overall IIR filter has characteristics similar to FIR, but it only requires 10 multiplications and 12 sums per sample [19].

### 3. Experimental results

The measurement setup equipment, used to prove and verify system functionalities, includes an arbitrary function generator (AWG - Tektronix™ AFG3102) in addition to the hardware previously described.

In order to test the goodness of the implemented system, it was very useful to simulate an input signal having properties suitable to be realistic enough as a bio-signal and with clearly observable temporal and spectral behavior. A  $\text{sinc}(t)$  waveform has been selected to be the modulating signal for its spectral property and shape. The flexibility of easily selecting lock-in frequency divider has been exploited to find optimal frequency for noise rejection. The highest possible lock-in frequency ( $f_{lock-in} = 16 \text{ kHz} / 8 = 2 \text{ kHz}$ ) has been selected, for all tests.

A simple modulator has been used to generate the test signals using the reference square wave, provided by the FPGA at lock-in frequency, while the modulating signal was created by the AWG.

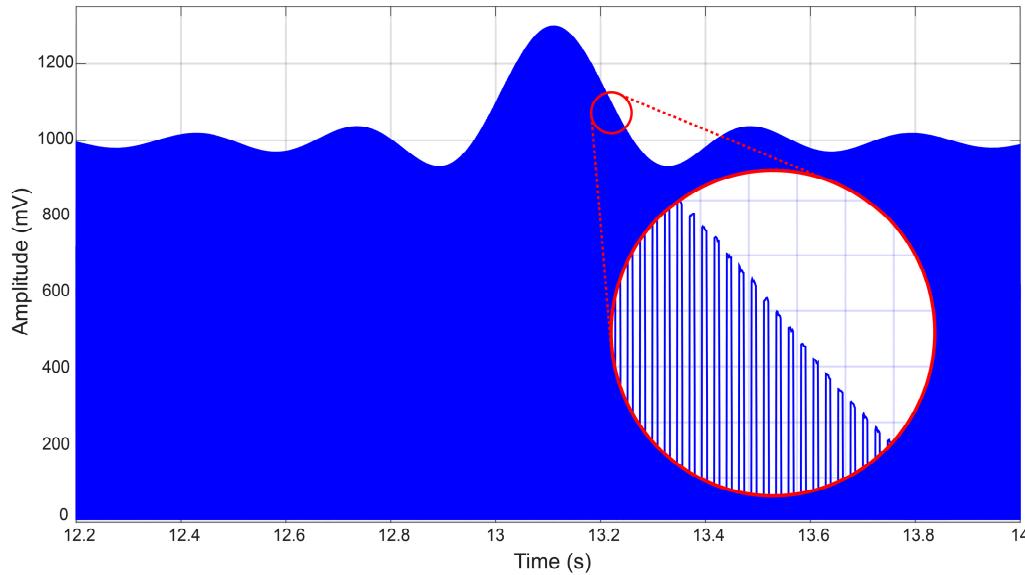
On PC side a Virtual Instrument, created with LabVIEW software, reads signals data from TCP connection and presents waveforms through some generated user-friendly charts.

### 3.1.IIR-FIR comparison

In order to properly evaluate LIA performances, to compare the results coming out from FIR and IIR filters and their fidelity level, several tests with some  $\text{sinc}(t)$  signals of suitable frequency were carried out by feeding them into the ADC input, one at a time: first a  $\text{sinc}(t)$  with a frequency bandwidth of 3.5 Hz, falling completely within the LIA's pass band; after that a second test used a  $\text{sinc}(t)$  with an extended bandwidth of 15 Hz. The equivalent formula of signal  $m(t)$ , used in the described measurements was:

$$m(t) = (0.3 \cdot \text{sinc}(2f_{sinc}t) + 1.0) \cdot \text{square}(2\pi f_{lock-in} t) [V] \quad (1)$$

The Figure 4 shows an example of the modulated signal, used as test signal and acquired by the system.

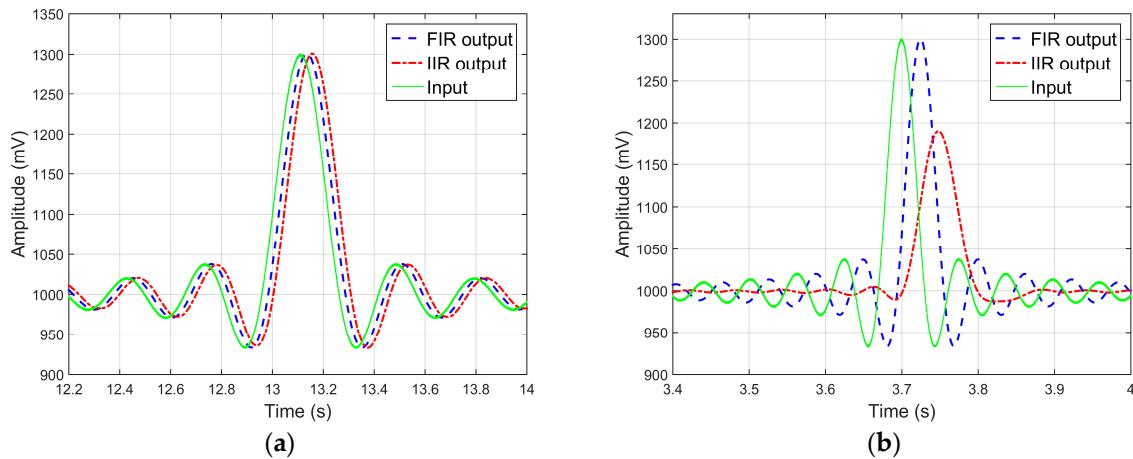


**Figure 4.** Acquired  $m(t)$  input signal, for a 3.5 Hz bandwidth  $\text{sinc}(t)$  at a  $f_{lock-in}$  of 2 kHz.  
Within the highlighted circle a zoomed portion of the modulated signal is shown.

As can be seen in figure 5.a, when the signal falls in 0 to 10 Hz range, no appreciable distortion appears on filters' outputs, not considering an obvious phase change due to the different filter's delay. With the larger spectrum  $\text{sinc}(t)$  (figure 5.b), amplitude distortion of both filters is clearly visible instead. In particular since the FIR filter achieves, in the transition band, a slope slower than the IIR, it shows less distortion and attenuation for frequency near to the pass frequency. The IIR

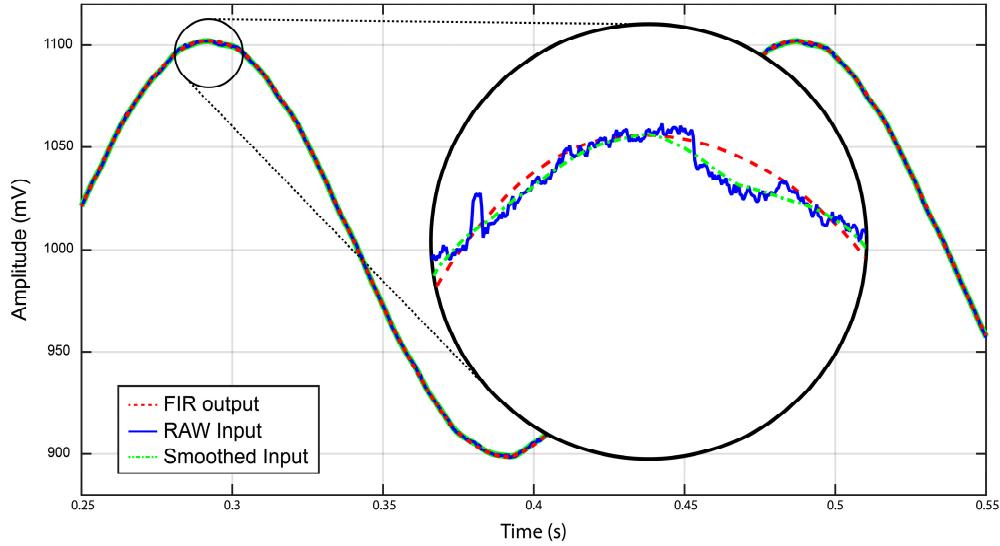
filter instead shows an asymmetrical response due to the frequency variable phase delay, and a substantial shape change of the original signal is experienced.

Moreover the signals extracted from FIR and IIR filters have specific delays and they can be evaluated at design time; in particular for IIR filter implementation, which has a non-linear phase, the estimated group delay ranges from 625 up to 760 samples, while for the FIR filter its value is constant (399 samples in this case).



**Figure 5** FIR and IIR filters responses for different input signals. (a) Response to the 3.5 Hz  $\text{sinc}(t)$ ; (b) Response to the 15 Hz  $\text{sinc}(t)$ .

To better highlight the response of LIA system, another comparative test has been carried out: a 100 mV sine test signal, at 5 Hz, has been used as modulating signal and the raw output of the ADC has been registered together with the filters outputs (see Figure 6).

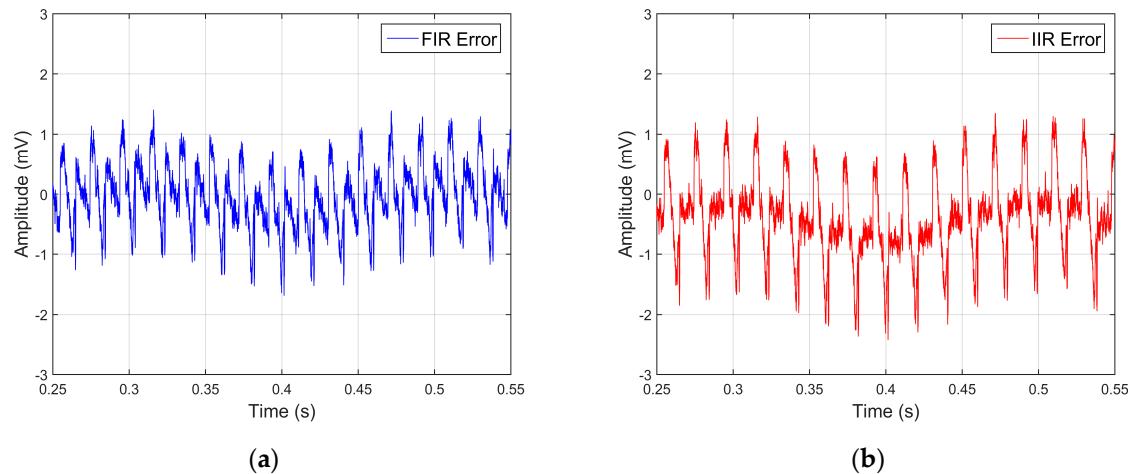


**Figure 6** FIR filter response aligned with ADC RAW input data, and smoothed input data for a 100 mV 5 Hz sine modulating signal. Within the highlighted circle a zoomed portion of the signals showing the higher noise present in the input data.

As it can be verified in the insert of figure 6, the raw input is actually a relatively noisy sine wave since it was obtained from a standard generator having a resolution of 14 bits. FIR output has been first aligned offline with the raw input data for better comparison and a smoothed input implemented with a standard 64 taps moving average filter has been also depicted. While the

smoothed input suffers of the variation of the noisy raw data, the FIR output of LIA system performs a much better reconstruction of a good 5 Hz sine wave, even showing a strong rejection of the input noise.

Figure 7.a and 7.b report the calculated signal difference between raw input signal and FIR/IIR outputs for the 5 Hz sine, respectively. In both figures, small variations and offset at modulating frequency can be observed and they are mainly due to amplitude non linearity of the filters. Finally the residual error, whose value is about  $\pm 1\text{mVpp}$ , is largely due to the noise existing in the raw input signal and removed by the LIA action.



**Figure 7** Difference between input raw data and FIR/IIR filters responses. (a) FIR response difference error; (b) IIR response difference error.

Table 1 shows a resume of the main hardware resources utilization within the Xilinx Zynq®-7000 and it's clear that, even if FIR filter performs a slightly lower signal distortion than IIR filter, it requires fourteen times the number of *Lookup tables* and almost thirty times the number of *Slices Registers*, hence exhibiting a much higher power consumption.

Moreover, among the parameters, attention must be paid to the needed *Clock cycles per sample*, since this means that IIR filters can be implemented, using pipeline elaboration, at least 4 times faster than a FIR filter with similar performances; and this can make a huge difference especially if LIA techniques would be applied in more demanding application fields.

**Table 1.** Hardware resource utilization for FIR and IIR filters from Xilinx VIVADO®

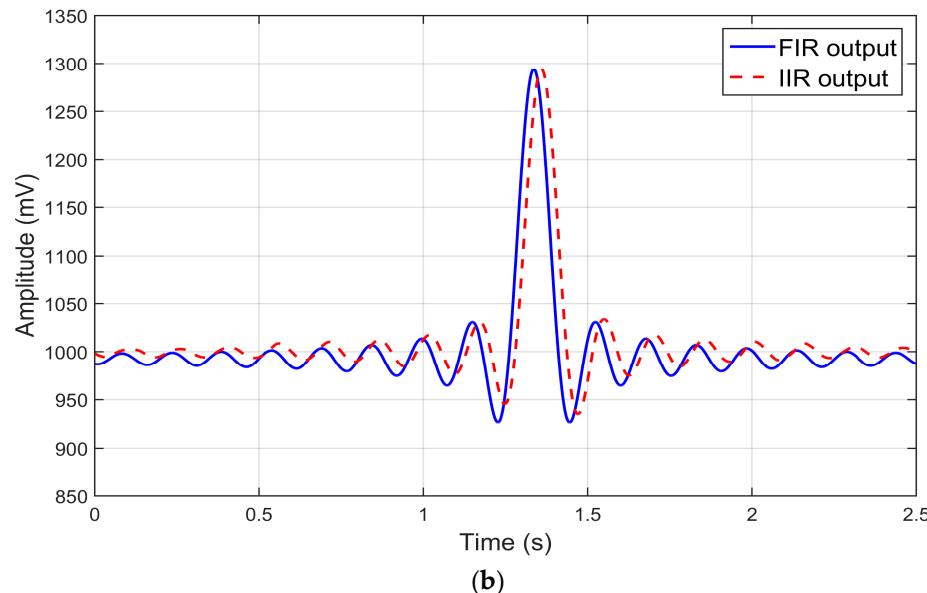
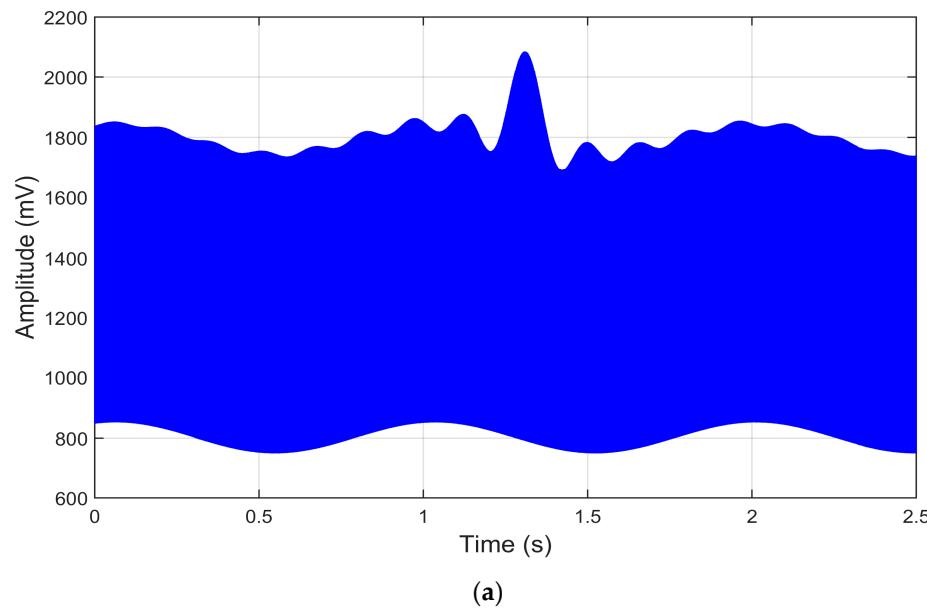
Resource	FIR	IIR
Slices Registers n°	23000	800
Lookup tables n°	8400	600
Multipliers n°	14	16
Clock cycles per sample	65	16
Power consumption	266 mW	24 mW

### 3.2 Baseline rejection

The baseline rejection test verifies the capability to remove DC offset and low frequency noise from input signal. This is a typical scenario with optical sensors affected by  $1/f$  noise and dark current indeed. The carrier is again modulated with 3.5 Hz-band  $\text{sinc}(t)$  useful signal and a DC offset of 0.8 V is summed up with a slow 0.1 V sine signal @ 0.5 Hz, acting as superimposed noise (see Figure 8a). The equivalent formula of signal  $m(t)$  is:

$$m(t) = (0.8 + 0.1 \cdot \text{sen}(2\pi 0.5t)) + (0.3 \cdot \text{sinc}(2f_{\text{sinc}} t) + 1.0) \cdot \text{square}(2\pi f_{\text{lock-in}} t) [V] \quad (2)$$

As it can be seen in Figure 8.b, baseline is completely removed by lock-in chain and FIR and IIR filters give the same envelope, each one with its own delay. The baseline noise doesn't affect output as long as it doesn't saturate ADC input. The behavior of the system, in this case, is completely different compared to systems that simply acquire ADC values [11] and perform some average filtering. In the latter case in fact, since the slow baseline variation falls within the band of the wanted signal, it would thoroughly affect the output, while the LIA system completely gets rid of this noise because both of the noise sources haven't any component near the lock-in carrier frequency.

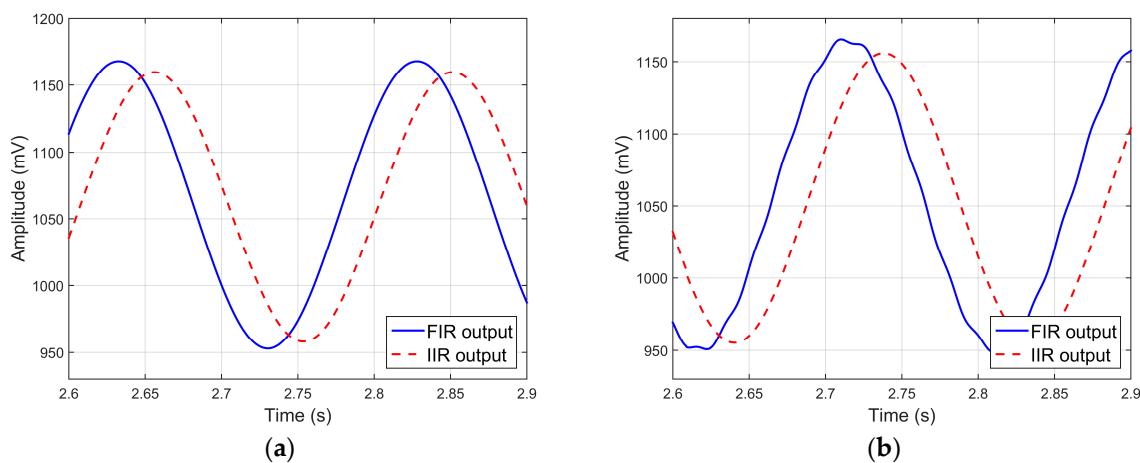


**Figure 8.** Baseline variation response. (a) input  $m(t)$  signal showing DC and slow baseline variations added to the modulated signal. (b) continuous line FIR output, dashed line IIR output.

### 3.3 Noise immunity test

In order to check lock-in chain robustness in noise rejection, some tests have been carried out using the AWG to generate typical noise sources. In normal environments one of the most awful optical noise source, that can affect fNIRS measurements, is the switching noise produced by neon lamps. This noise has a fundamental frequency of 100 Hz, so the experiments were carried out by adding to the useful test signal, represented by a 100 mV @5 Hz sine wave, a noise signal acting at 100Hz.

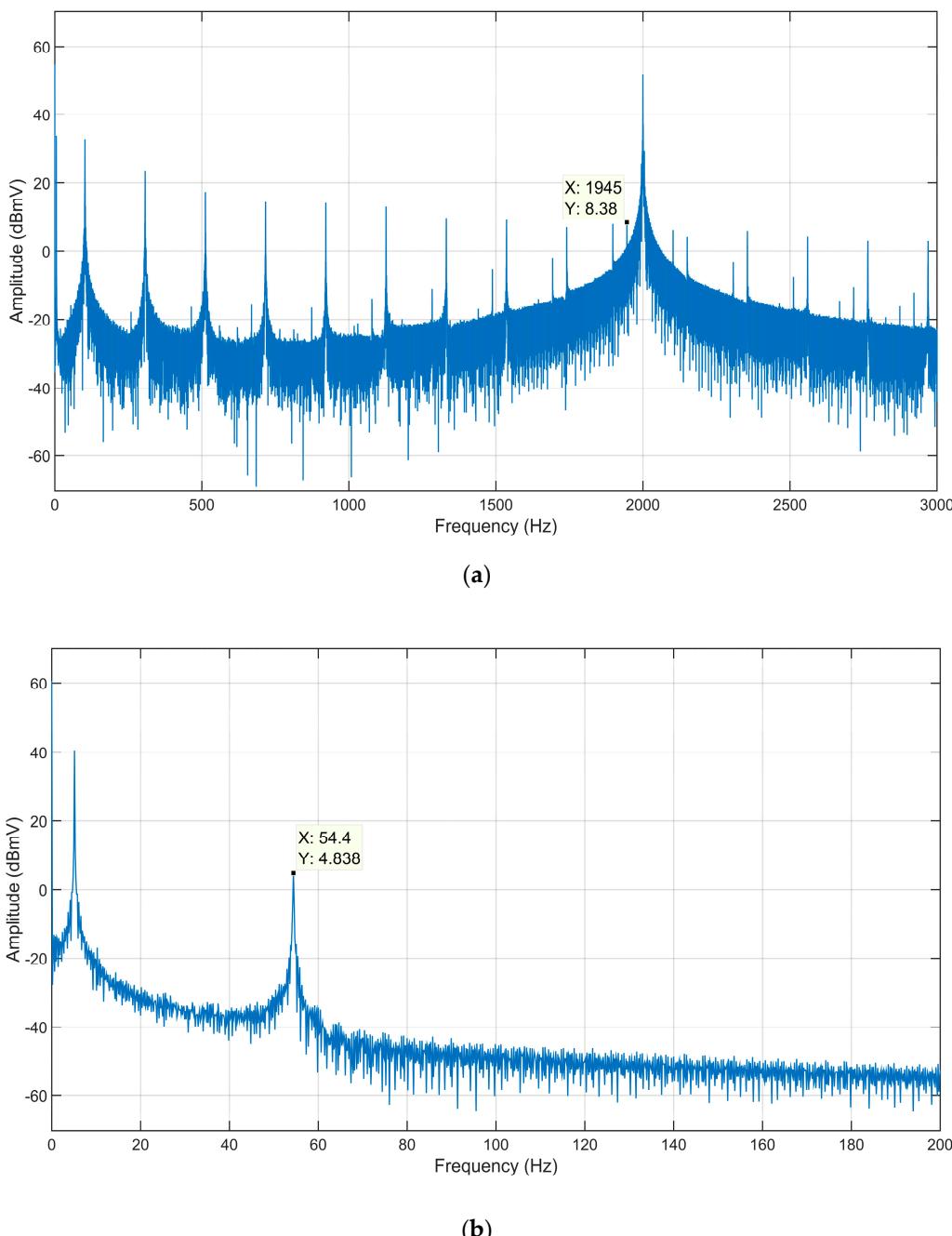
The first test (see Figure 9.a) uses a sine signal with the same amplitude of the useful one, and in both filters outputs a complete elimination of the 100 Hz component has been obtained. A second, more aggressive, test uses a 100 Hz square wave signal (see Figure 9.b) with the same amplitude of the first trial. In this case, while the IIR filter output shows, again, a complete elimination of the noise component, the FIR filter experiences a residual noise affecting its output.



**Figure 9** System responses to a 100 Hz added noise. (a) filters responses to a 100 mV @100 Hz added *sine* signal. (b) filters responses to a 100 mV @100 Hz added *square* signal.

To further investigate the last experiment, a spectrum analysis of the input signal (figure 10.a) and the corresponding FIR output (figure 10.b) has been carried out.

In particular it can be observed that, near the 2 KHz lock-in frequency carrier, the input signal also exhibits a little signal component at 1945 Hz, among the others generated by the square wave harmonics. This signal component, mainly due to the non-linearities of the modulating process, is shifted to the baseband, by the multiplication, at a frequency of about 55 Hz. Since the implemented FIR filter has a relatively slow slope in the transition band, part of this noise will pass through the filter with an amplitude of more than -30dB/Hz and then still above the noise floor (see Figure 10.b), while higher harmonics are completely attenuated by the FIR filter. The IIR filter instead has a larger slope in the transition band hence it completely removes the 55Hz component below the noise floor, together with all the other components.



**Figure 10** Frequency spectra related to the superimposed 100 Hz square wave noise. Amplitude spectrum of the input signal (a) and the corresponding FIR output (b).

#### 4. Discussion and Conclusion

In this work an FPGA based Lock-in architecture has been designed and implemented with the aim to get great flexibility on key design parameters such as sampling and lock-in frequency, together with the main characteristics of the core digital filtering action, embedded in the Lock-in chain. Besides, the design principles described in this paper may be also relevant to other research areas.

The realized system has been designed with an intrinsic level of modularity and this may bring an ease scale up of the number of acquired channels without affecting the overall architecture while, for small number of channels, the subsequent computational effort lowering may envisage a

possible implementation based on a microcontroller with suitable digital signal processing capabilities.

Extensive experimental assessments have been carried out and the obtained results show a good behavior of the developed system. In particular the action of the proposed FIR and IIR filters obtained a very strong rejection of noise affecting the baseline, particularly for signals related to fNIRS systems using SiPM as main sensors.

Moreover some noise immunity tests exhibited a quite robust behavior against possible noise sources, such as the ones generated by neon lamps, also highlighting the better performances of IIR based filter, despite its less demanding resources request.

This LIA technique employs more hardware resources than the one used in [11], based on a simple moving average filtering of a predefined number of acquired samples, but it generally leads to better results in terms of signal to noise ratio preservation, noise immunity and low amplitude signal acquisition.

The comparison between different (FIR and IIR) filtering actions, while showing both suitable results in term of rejection performances, have a substantially different impact on FPGA resources utilization and, for some tests, on the obtained results.

The goodness of the described results encourages to further investigations. The system uses a very powerful FPGA board, but in the current implementation most of the resources are not used, hence a more suitable FPGA chip could be chosen lowering overall costs of the system and power consumption. From the comparison of the filters and considering the overall computational cost, it has been evaluated that is plausible to implement the same method, to a limited number of channels (16 seems reasonable) using IIR filters without sensible degradation of the performances, on mainstream 32-bit microcontroller, especially if equipped with DSP functions.

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**Author Contributions:** C.G. Giaconia conceived the idea to apply FPGA based Lock-in technique with digital filtering actions to fNIRS systems; G. Greco and R. Rizzo designed, performed the agreed experiments; L. Mistretta provided assistance to the whole project. All authors participated to data analysis and paper writing. C. G. Giaconia is the project supervisor.

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