

Article

Study on Solar Power Charging by Flyback Converter

Guo-Shing Huang ¹, Shing-Lih Wu ^{2,*}, Pei-Siou Ding ¹

¹ Department of Electronic Engineering, National Chin-Yi University of Technology, No.57, Sec.2, Zhongshan Rd., Taiping Dist., Taichung 41170, Taiwan; hgs@ncut.edu.tw (G.-S.H.); dennis22662003@yahoo.com.tw (P.-S.D.)

² Department of Electrical Engineering, National Taitung Junior College, No.911, Jhengci N. Rd., Taitung 95045, Taiwan

* Correspondence: lihchoug@yahoo.com.tw; Tel.: +886-89-226-389; Fax: +886-89-232-871

Abstract: In this paper, a method of charging lead acid battery with solar power by flyback converter is proposed. The basic system consists of a buffer circuit, auxiliary power circuit, control circuit, voltage feedback circuit and current feedback circuit. The system is capable of monitoring battery voltage and the current, charging the coupling inductor and automatic control of output duty cycle, overcharging and over-discharging protection. The experiment proves that the charging efficiency is improved by about 83% at full load.

Keywords: Solar Power; Flyback Converter; Duty Cycle; Coupling Inductor

1. Introduction

The resource that Mother Earth can provide is depleting. Oil, the primary source of energy source, is coming to its end of supply. New alternative energy sources have to be found. Among these new energies, solar power features zero pollution. Today, many branches of industries are linked to solar power generation, and batteries are used for energy storage. Among all, lead acid battery is the most commonly used type of battery [1]-[6], as it features stable working voltage and a wide range of working temperature and current. It is capable of charging and recharging for hundreds of cycles, good energy storage performance and low cost [7]-[13]. However, batteries have to be connected in series and parallel for higher voltage and current output to meet the various demands for power. As a result, the safety of the battery during charging becomes increasingly important [13]-[19]. There are a number of studies on battery charging, most of which are focused on pulse charging. The pulse charging works by controlling the length of triggering time with a pulse width modulating controller. When the battery is low, the number of pulses increases, and so does the number of turn-ons at transistor (Q). On the other hand, as the battery is about to be fully charged, both the numbers of pulses and turn-ons at transistor (Q) decrease, so that when the battery is fully charged, the pulse width modulating controller cuts the transistor (Q) off, which completes the charging [20]-[26]. However, this easily leads to overcharging and overheating. In this study, the control circuit, combined with overcharging and over-discharging protection circuits, is capable of balancing the voltage across multiple batteries automatically, while charging multiple batteries and preventing overheating, thus achieving the protection of battery and extended service life of these batteries. The buffer circuit, auxiliary power circuit, control circuit, voltage feedback circuit and

current feedback circuit is added for better system stability. In addition, the system is able to monitor the battery voltage and the current that charged the coupling inductor, and featured automatic control of output duty cycle and over-charging/discharging protection. The experiment conducts to prove that the system’s charging efficiency is improved by about 83% at full load.

2. System chart of solar power flyback charger

The solar power flyback charging system mentioned in this study consisted of a solar panel, control system and lead-acid battery. The system architecture includes coupling inductor, auxiliary power supply, control power supply, over-voltage detection circuit and over-current detection circuit, as shown in Figure 1.

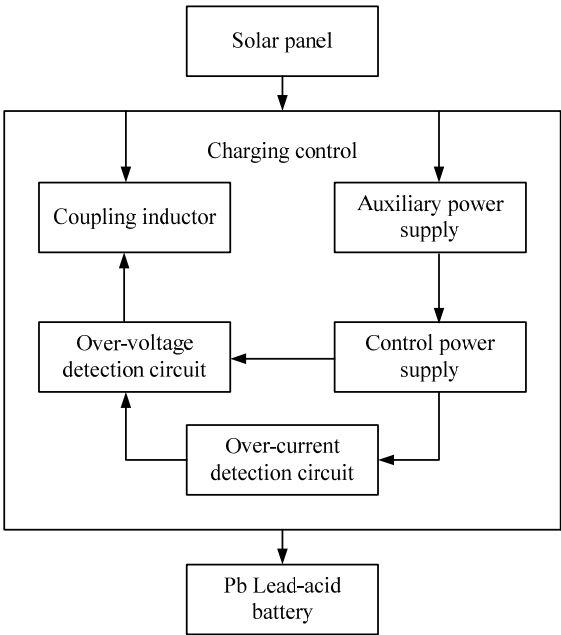


Figure 1 System chart

The flow chart is shown in Figure 2. To start, the solar panel generates 18V power which is regulated into controlled by low-ripple voltage via regulating circuit and supplied to pulse width modulating control circuit and DC converter circuit. The control circuit output pulse width is converting into signals for the control of current stored in the inductor. Then, the unstable ripple voltage of secondary output had to control the more stable 12V through the output filtering circuit to charge the lead acid battery. The overvoltage and overcurrent protection circuits are used to detect the voltage of battery, and the feedback circuit is used to control the duty cycle of pulse width modulating signals, as shown in Figure 2.

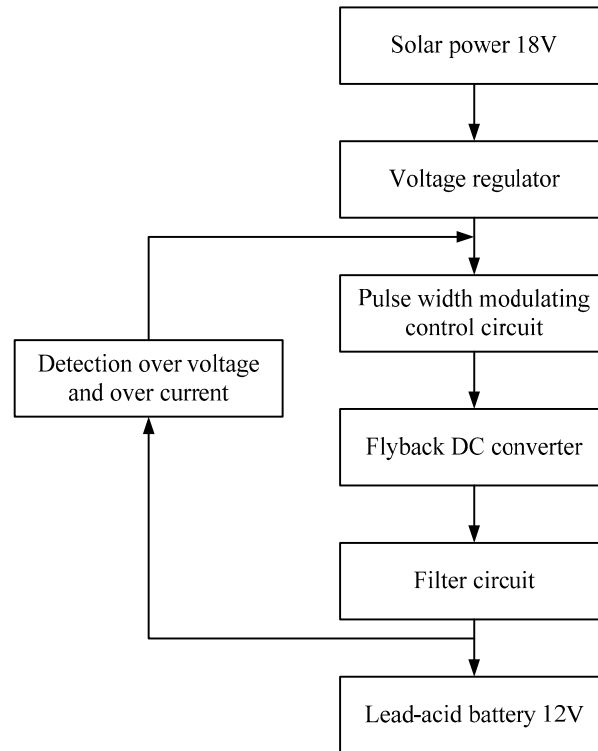


Figure 2 System block diagram

3. Working principle of system

3.1 Buffer circuit design

Figure 3 shows the buffer circuit. When the transistor is off, the capacitor C is charged through diode D1 with the voltage on the inductor as its value. When the transistor is turned on, the capacitor discharges along the path of resistor R, the power consumed by the buffer circuit is determined as Eq. (1). Eq. (2) and (3) are used to show the voltage of the capacitor, and Eq. (4) expresses the resistance.

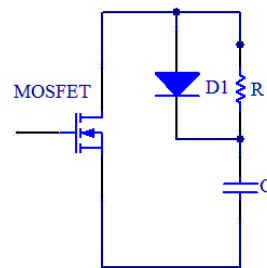


Figure 3 Buffer circuit diagram

$$E = \frac{CV_{DS}^2}{2} = \frac{I_D V_{DS}(t_r + t_f)}{2} \quad (1)$$

$$C = \frac{I_D(t_r + t_f)}{V_{DS}} \quad (2)$$

$$V_C = V_{DS} e^{-\frac{t_{on}}{RC}} \quad (3)$$

$$R = \frac{t_{on}}{3C} \quad (4)$$

$$I_{dis} = \frac{V_{DS}}{R} \quad (5)$$

where E is energy, C is the capacitance in the buffer circuit, V_{DS} is the voltage between the drain and source of MOSFET, V_C is the voltage of capacitor, t_{on} is the duration the MOSFET turn on, and Eq.(5) is the discharge current of the buffer circuit.

3.2 Pulse width regulating control circuit

The pulse width modulating signal controls the internal circuit of UC3842 and modulates the duty cycle of MOSFET through an external circuit. In this study, the partial voltage of external resistors PIN1 and PIN2 are compared to the internal 2.5V by an error amplifier. When the output voltage is greater than 2.5V, the voltage is too large and therefore, the output duty cycle is reduced. When the output voltage is smaller than 2.5V, the voltage is too low and therefore, the output duty cycle is increased, as shown in Figure 4. In case that the ideal value and error value are too large, the external compensation circuit PIN1 is conducted to fine-tune the error value and allow the circuit to stay close to the determined ideal value, as shown in Figure 5. The output frequency is determined by the R_T of PIN8 and C_T of PIN4, as shown in Figure 6. However, R_T has to be greater than 5kΩ. The frequency is determined with Eq. (6).

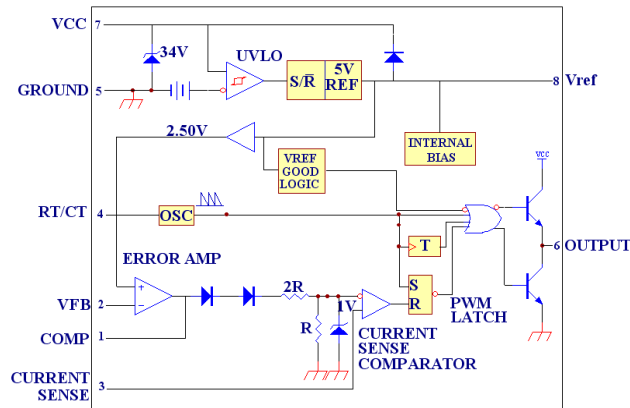


Figure 4 UC3842 block diagram

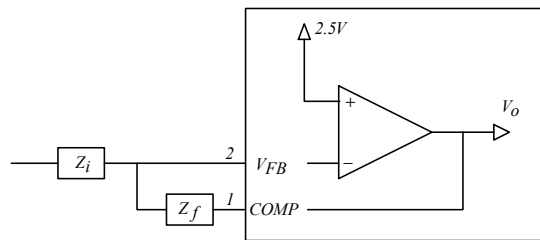


Figure 5 Internal structure of error amplifier in UC3842

$$\frac{Z_f}{Z_i} = \frac{V_o}{V_i} \quad (6)$$

where Z_f is the negative feedback output impedance in Ω , Z_i is the input impedance in Ω , V_o is the output voltage in V, and V_i input voltage in V.

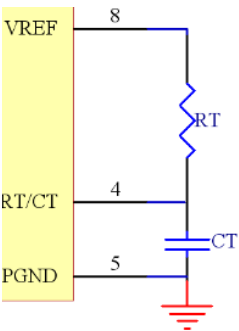


Figure 6 Design frequency circuit diagram

$$f = \frac{1.72}{R_T C_T} \tag{7}$$

where f is the frequency that determines the generated pulse width modulating signals in Hz, C_T is the capacitance that generates oscillation frequency in F, and R_T is the resistance that generates oscillation frequency in Ω .

3.3 System stability design

As mentioned above, the external compensation circuit PIN1 provides output regulation. There are a variety of feedback compensation techniques available, and the lag compensation circuit is chosen for this study. It proves the improvement of steady state errors, as the lag compensation circuit itself is a type of low-pass filter; such as it only allows low-frequency signals to pass and causes high-frequency signals to attenuate. In this study, a pair of zero-pole operational amplifier circuit is designed. The feedback is used to fix the system within a frequency range without any phase shift.

Table I Stability design parameters

Electronic component	Value
R_l	4k Ω
R_3	400k Ω
C_l	2pF
C_2	8pF

As shown in Table I, the crossover frequency is set at $f_c=10$ kHz, since the pulse width modulating signal frequency is $f=100$ kHz. The crossover frequency is designed as 10% of the pulse width modulating signal frequency for a more stable system. Then, the zero frequency is defined as $f_l=2$ kHz, pole frequency as $f_2=50$ kHz, voltage gain as $AV=100$ and $R_3=400$ k Ω . By substituting AV and R_3 into Eq. (8), it is determined that $R_l=4$ k Ω . By substituting R_3 and f_l into Eq. (9), it is determined that $C_l=2$ pF. Then by substituting f_2 , C_l and R_3 into Eq. (10), $C_2=8$ pF is determined.

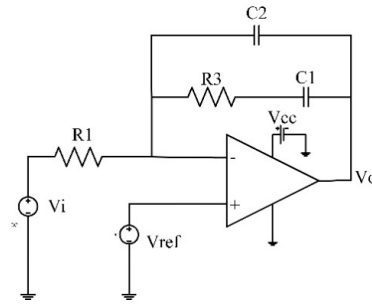


Figure 7 Circuit diagram of system stability design

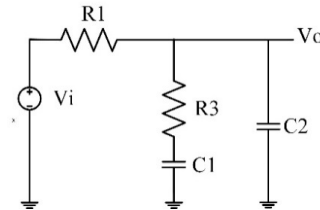


Figure 8 Circuit diagram of low-pass filter

$$\frac{R_3}{R_1} = AV \quad (8)$$

$$\frac{1}{2\pi \times R_3 \times C_1} = f_1 \quad (9)$$

$$\frac{C_1 + C_2}{2\pi \times R_3 \times C_1 \times C_2} = f_2 \quad (10)$$

where R_3 is the negative feedback resistance in Ω , R_1 is the input resistance in Ω , AV is the voltage gain, and C_1, C_2 are the capacitances that determine the frequency response in F.

3.4 Winding of coupling inductor

The winding of coupling inductor is aimed to turn ratio and the size of used enameled wire. For a flyback converter, the wire is wound in the reverse direction. As the inductor reached volt-sec balance, the turn ratio n is determined by substituting $V_{in,min}$, V_o , V_f and D_{max} (Duty Cycle) into Eq. (11). For safety reason, the D_{max} is designed at approximately 40%. For the size of the used enameled wire of windings, Eq. (14)-(18) are used to determine the radius of the wire for the inductor windings. Using Eq. (19), the volume of coupling inductor is determined and substituted into Eq. (20) and (21) to determine the number of windings at the primary and secondary sides. The iron core used in this study is EE30. The B_m value is substituted into the range of $1500 G_{uess}$ empirically.

$$\frac{V_{i_{min}} \times D_{max}}{(V_o + V_f)(1 - D_{max})} = n \quad (11)$$

where $V_{in,min}$ is the minimum of initial voltage imposed in V, D_{max} is the maximum duty cycle in %, V_o is output voltage in V, V_f is the different voltage across the diode in V, and n is the turn ratio between primary and secondary windings in turns.

$$\frac{P_i}{V_i} = I_i \tag{12}$$

P_i is the input power in W and V_i is the input voltage in V.

$$\frac{P_o}{V_o} = I_o \tag{13}$$

P_o is output power in W, I_i is input current in A, and I_o is output current in A.

$$\frac{3.13 \times P_o}{V_{in,max}} = I_p \tag{14}$$

$$\frac{I_s}{I_p} = n \tag{15}$$

$V_{in,max}$ is the maximum initial voltage imposed in V, I_p is the primary side current in A, I_s is the secondary side current in A, and n is the turn ratio between primary and secondary windings in turns.

$$4\pi r^2 = I \tag{16}$$

$$\sqrt{\frac{I_p}{4 \times \pi}} = r_p \tag{17}$$

$$\sqrt{\frac{I_s}{4 \times \pi}} = r_s \tag{18}$$

r_p is the wire radius at the primary side in mm and r_s is the wire radius at the secondary side in mm.

$$\frac{P_o \times 10^9}{1.16 \times B_{max} \times f} = A_e \times A_c \tag{19}$$

$$\frac{V_{in,max} \times 10^8}{4 f B_{max} \times A_e} = N_p \tag{20}$$

$$\frac{N_p}{n} = N_s \tag{21}$$

4. Experiment

The waveform of inductor and current are measured and efficiency of those are compared. Modification is made based on experiment results and the optimized value is obtained. The measurement flowchart is provided in Figure 9.

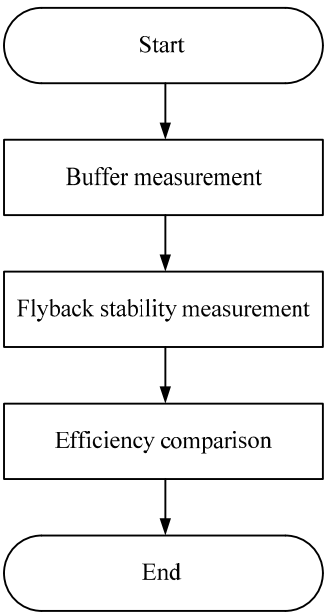


Figure 9 Measurement flowchart

4.1 Waveform measurement

The V_{DS} of MOSFET is measured for waveforms. A comparison is made between the presence and absence of buffer. The input voltage and load were varied for measurement.

4.2 Efficiency comparison

The voltage measurements yielded the input and output powers, which were used to calculate the conversion efficiency. The experiment result suggests the impact of increase and decrease of input voltage on the conversion efficiency.

5. Experiment results

It is clear in Figure 10 that the conversion efficiency of the solar panel was at its highest between 10:00 am and 3:30 pm. Shading caused decrease of conversion efficiency in this period of time. The feedback circuit is designed to change the magnitude and increase the stability of power supply. With a load of 100Ω, the input voltage is 18V and output voltage is 13.3V, as shown in Figure 13. The idea to add a buffer circuit in the system is to avoid damage of elements due to instability of input voltage or even unwanted oscillations. These oscillations led to very high voltage at the V_{DS} end. The 18V input can increase the oscillation voltage up to 80V as shown in Figure 11. However, the addition of buffer circuit reduced the oscillation voltage significantly, as the voltage amplitude dropped from 80V to 20V. This demonstrates effective reduction of power loss on MOSFET and in turn the protection of MOSFET, as shown in Figure 12.

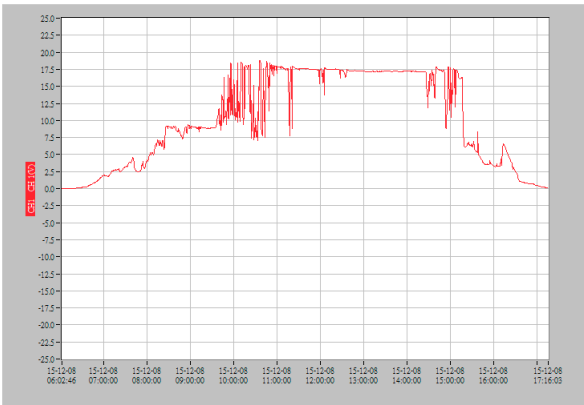


Figure 10 Voltage waveform of solar panel

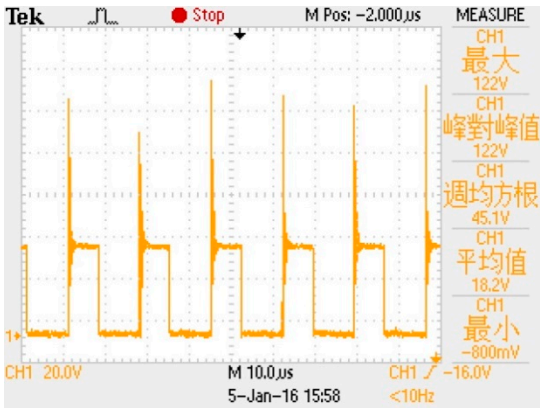


Figure 11 V_{DS} without buffer

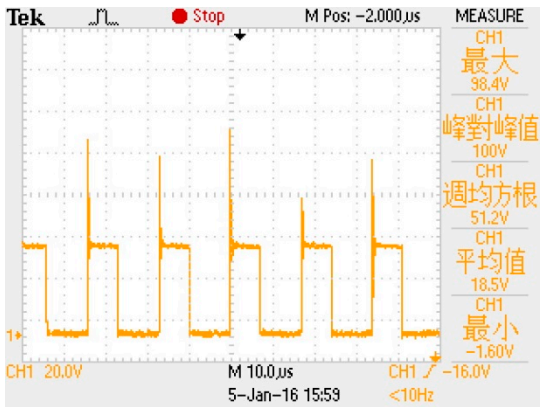


Figure 12 V_{DS} with buffer

The stability of power supply is improved by regulating the magnitude of duty with the feedback circuit designed. With a load of 100Ω, the input voltage is 18.2V, the output voltage is 13.3V and the duty is 21%, as shown in Figure 13. With a load of 10Ω, the input voltage is 17.8V, the output voltage is 12.9V, and the duty is 43%, as shown in Figure 14.

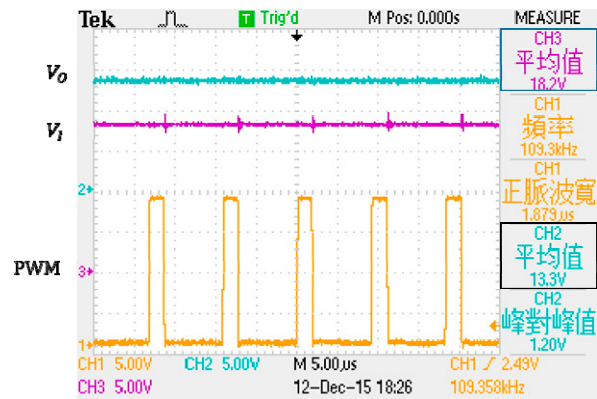


Figure 13 With a load of 100Ω

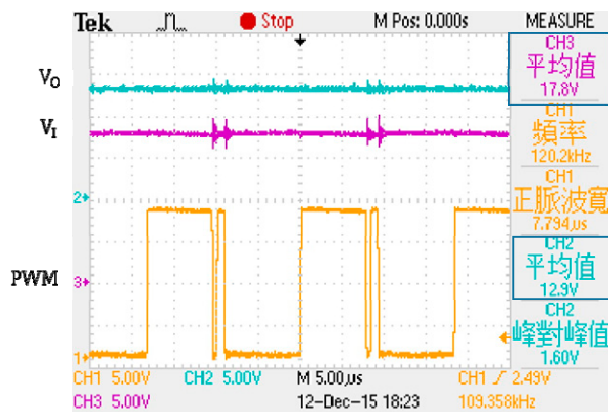


Figure 14 With a load of 10Ω

As indicated in Table II, the output power reaches as high as 16.6W at the same voltage by only changing the loading. Due to the addition of feedback circuit, the larger the load, the greater the duty cycle; whereas the smaller the load, the smaller the duty cycle.

Table II Load and duty cycle

V_{DS}	18V	18V	18V	18V	18V	18V
Duty (%)	11.3	12.8	20.8	27.6	29.8	43.3
V_O (V)	13.3	13.3	13.3	13.2	13.1	12.9
P_O (W)	3.5m	215m	1.77	3.48	8.58	16.6
Load (Ω)	50k	820	100	50	20	10

When the input voltage is 14.1V, the output voltage is 12V, the load is 10Ω and the duty cycle is 43%, as shown in Figure 15. When the input voltage is 18.1V, the output voltage is 13V, the load is 10Ω and the duty cycle is 43%, as shown in Figure 16. It is found that the output voltage dropped by 1V and the duty cycle remained the same when the output voltage decreased from 18.1 to 14.1V. PWM decreased with the input voltage.

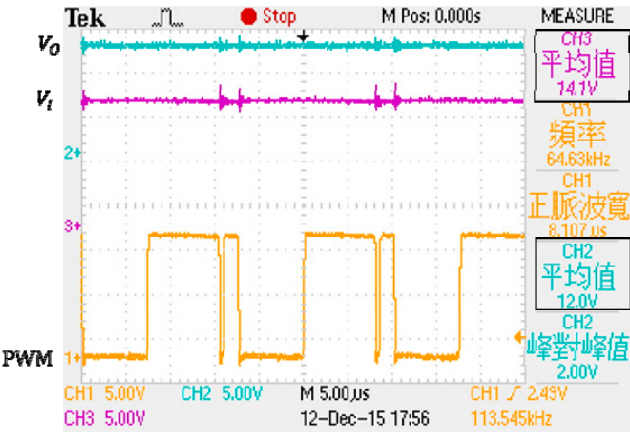


Figure 15 With an input of 14V

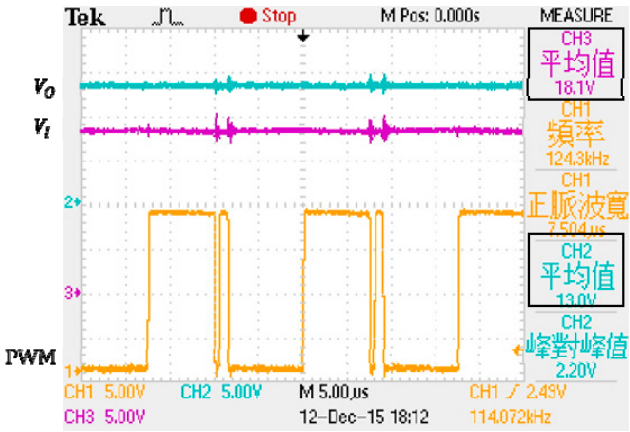


Figure 16 With an input of 18V

It is clear in Table III that the efficiency decreased with the input voltage as the battery is being charged. The reason is the power loss due to the internal resistance of MOSFET r_{DS} and leakage inductance. The leakage inductance loss increased as the input voltage is close to the output voltage. It becomes difficult to drive the MOSFET when the PWM voltage is decreased, and the internal resistance r_{DS} is increased, which causes power loss.

Table III Input voltage vs efficiency

v_I (V)	I_I (A)	P_I (W)	v_O (V)	I_O (A)	P_O (W)	η (%)
10.5	2.04	21.42	10.4	1.04	10.82	50.51
11	2.08	22.88	10.5	1.05	11.03	48.21
12	1.86	22.32	11.7	1.17	13.69	61.34
13	1.72	22.36	11.9	1.19	14.16	63.33
14	1.63	22.82	12	1.2	14.4	63.1
15	1.52	22.8	12.2	1.22	15.13	66.36
16	1.35	21.7	12.6	1.26	15.88	73.17
17	1.26	21.42	12.8	1.28	16.38	76.47
18	1.13	20.34	13	1.3	16.9	83.10

The solar power battery chargers available in the market sometimes experience unstable current. As indicated in Figure 17, it is clear that a current up to 4A is generated when the PWM switch is turned on and off. When a lead acid battery is charged under such a maximum instantaneous current, the battery’s service life is reduced as the charging time increases. The output voltage provided by the design presented in this study is much more stable than that by market-available products for lead acid battery charging. The maximum instantaneous current generated is smaller when the PWM is switched on and off as indicated in Figure 18.

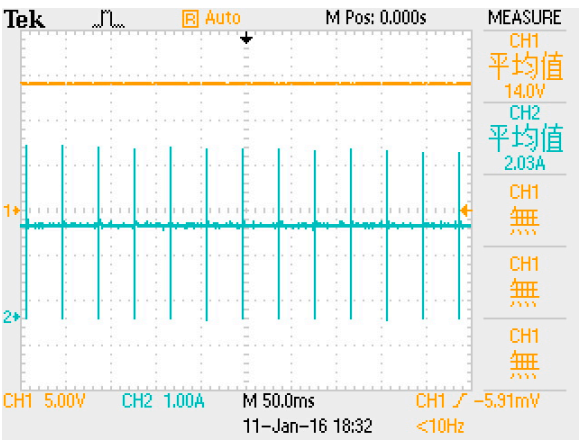


Figure 17 Output voltage and current of market available solar panel

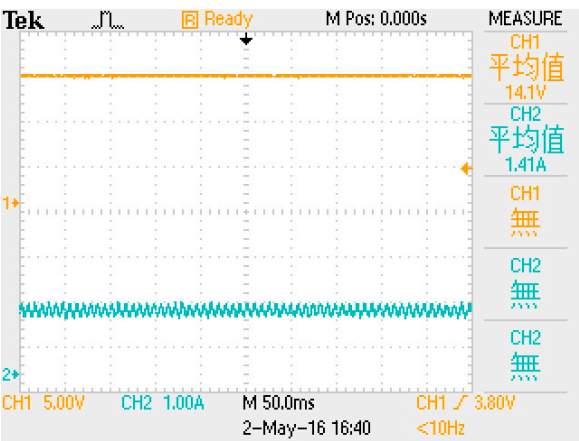


Figure 18 Output voltage and current of the paper available solar panel

6. Conclusion

This study is motivated by the instability of solar power generation. A flyback charged is used to convert sunlight into electric energy to store in lead acid battery. Over-charge/discharging protection is added to detect the battery charging. The experiment results suggest 6.6% of error between the ideal value and practical value. The design presented in this study is capable of fast charging with the standard test condition of the sunshine intensity of 1000W/m². The design is capable of monitoring the battery charging, thus contributing to the longevity of battery. In addition, the unstable current output commonly seen in market-available products is improved.

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