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Article

Design of Mixed-Mode Analog PID Controller with CFOAs

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Abstract: The design of a mixed-mode proportional-integral-derivative (PID) controller circuit using current-feedback operational amplifiers (CFOAs) as active components is proposed. With the same circuit topology, the proposed configuration of three CFOAs, four resistors, and two capacitors is capable of performing the PID controller in all four operation modes: namely voltage mode, trans-admittance mode, current mode, and trans-impedance mode. Numerous mathematical analyses are conducted to determine the controller performance under ideal and non-ideal conditions. Additionally, the mixed-mode second-order lowpass filter is suggested, and also used to examine the workability of the proposed mixed-mode PID controller in a feedback control structure. The proposed PID controller is implemented with the commercially available IC-type CFOA AD844, and the simulation results are presented to illustrate the functionality of the controller and its closed-loop control system.

Keywords: current-feedback operational amplifier (CFOA); proportional-integral-derivative (PID); analog controller; mixed-mode circuits

1. Introduction

The proportional-integral-derivative (PID) controllers are the most significant control components used in numerous industrial processes [1]. It is estimated that PID controllers are utilized in over 90% of all dynamical control systems [2]. With its three-term functionality involving proportional, integral, and derivative actions, the PID controller handles the treatment of transient and steady-state responses and adjusts the level of system stability, which are effective solutions for a wide range of real-world control problems [3]. It also offers simplicity, robustness, wide applicability, and simple parameter tuning. Consequently, the prevalence of PID control has increased considerably.

Literature review reveals that the PID controller implementation includes a wide variety of designs based on the use of different active elements [4–17]. In [4], voltage-feedback operational amplifiers (OAs) are extensively used to implement conventional voltage-mode (VM) PID controllers. The realized controller, however, requires a significant number of active and passive components. Its response time is also limited by the constant gain bandwidth product and low slew rate of the OA. To overcome these limitations, some current-mode (CM) active components, such as operational transconductance amplifier (OTA), current differencing buffered amplifier (CDBA), operational transresistance amplifier (OTRA), second-generation current conveyor (CCII), voltage differencing current conveyor (VDCC), and current-feedback operational amplifier (CFOA), are suggested for PID controller implementations. The OTA-based PID controller in [5] uses two grounded capacitors and eight OTAs. It supplies the output voltage signal at the high-impedance terminal, which is incompatible with cascading in VM. The PID controller designed with CDBAs

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requires four active and ten passive components, and lacks high input impedance [6]. In [7], the VM PID controller circuit is constructed with two OTRAs, four floating resistors, and three floating capacitors, but it does not have both high input and low output impedances. Based on CCIIs, the PID controller circuits are proposed in [8–10]. The works of [8,9] present two distinct configurations for VM and CM operations, while [10] only discusses CM operation. However, none of the CCII-based VM PID designs have low output impedance, and neither of the CM PID designs have low input impedance. As described in [11], a single VDCC-based VM PID controller circuit with a single input and two output terminals is realized with four resistors and two capacitors. It can simultaneously implement non-inverting and inverting control signals. However, the configuration does not fully utilize the differential input property of the VDCC because one of the differential inputs is not employed. This could be the result of input noise injection. Also, a recent VM PID controller using a single active component was reported in [12], but its limitations are the same to those in [11]. Three DDCCs and five passive elements are used in the construction of VM PID controllers [13]. At the inputs of all DDCCs, the high input impedance and capability of arithmetic operations are not fully utilized. Some earlier works do not exhibit high-input and low-output impedances for VM [14,15], or low-input and high-output impedances for CM [16]. In addition, all of the proposed PID controllers in [4–16] are capable of operating in either VM or CM. In real-world process control applications, mixed-signal processing PID controllers are required to interact between CM and VM circuits. To satisfy this requirement, the trans-admittance-mode (TAM) and trans-impedance-mode (TIM) PID controller circuits are also used to interface between CM and VM units without any distortion. Only one of those controllers suggests a transconductor-capacitor-based mixed-mode PID design [17]. The active blocks used in the design are not commercially available. Note that implementing the controller with commercially available elements is advantageous from both a practical and a simplicity aspect.

This work describes a mixed-mode PID controller circuit that utilizes three CFOAs as active components in addition to four resistors and two capacitors as passive components. In a single topology, the proposed controller can implement mixed-mode PID control responses, i.e., VM, CM, TAM, and TIM. Table 1 provides a detailed comparison between the proposed circuit and earlier PID controllers [4–17].

2. Proposed Mixed-Mode PID Controller Configuration

The CFOA is a four-terminal active device represented symbolically in Figure 1. Its ideal characteristic is defined by $i_y = 0$, $v_x = v_y$, $i_z = i_x$, and $v_w = v_z$. In addition, the characteristics of the CFOA with non-ideal transfer gains can be defined by the following terminal relations:

$$i_y = 0, \quad v_x = \beta v_y, \quad i_z = \alpha i_x, \quad \text{and} \quad v_w = \gamma v_z, \tag{1}$$

where $\beta = (1 - \varepsilon_\beta)$, $\alpha = (1 - \varepsilon_\alpha)$, and $\gamma = (1 - \varepsilon_\gamma)$. Further, ε_β ($|\varepsilon_\beta| << 1$) is the input-voltage tracking error, ε_α ($|\varepsilon_\alpha| << 1$) is the input-current tracking error, and ε_γ ($|\varepsilon_\gamma| << 1$) is the output-voltage tracking error. All of the parameters β, α, and γ should ideally equal one.

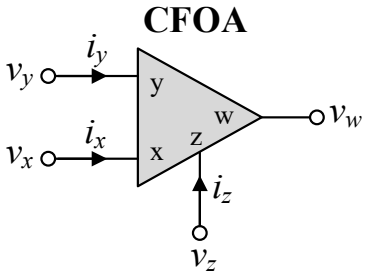

Figure 1. CFOA circuit representation.

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Table 1. Comparison features of the proposed controller circuit with the earlier PID controllers [4–17].

Ref.	Active component	Passive component	Mixed-mode operation	Operating modes				Technology	Supply voltage (V)
				VM	CM	TAM	TIM		
[4]	OA = 4	R = 8, C = 2	no	yes	no	no	no	NA	NA
[5]	OTA = 8	C = 2	no	yes	no	no	no	0.8-µm CMOS	±5, (-2 ~ 4)
[6]	CDBA = 4	R = 8, C = 2	no	yes	no	no	no	0.8-µm CMOS	±2.5, ±1
[7]	OTRA = 2	R = 4, C = 3	no	yes	no	no	no	0.18-µm CMOS	±1.5
[8]	CCII = 2	R = 4, C = 2	no	yes	yes	no	no	AD844	NA
[9]	CCII = 1, DO-CCII = 1	R = 3, C = 2	no	yes	yes	no	no	0.35-µm CMOS	±1.5, +0.5
[10]	DO-CCII = 1	R = 2, C = 2	no	no	yes	no	no	0.13-µm CMOS	±1, +0.4
[11]	VDCC = 1	R = 4, C = 2	no	yes	no	no	no	0.18-µm CMOS	±0.9
[12]	DVCCTA = 1	R = 3, C = 2	no	yes	no	no	no	0.25-µm CMOS	±1.5, -1
[13]	DCCC = 3	R = 3, C = 2	no	yes	no	no	no	0.13-µm CMOS	±0.75, +0.37
[14]	ZC-CFTA = 1	R = 2, C = 2	no	yes	no	no	no	0.35-µm CMOS	±1
[15]	CCTA = 1	R = 2, C = 2	no	yes	no	no	no	0.35-µm CMOS	±1.5
[16]	CFOA = 2	R = 3, C = 2 for VM, R = 5, C = 2 for CM	no	yes	yes	no	no	AD844	±12
[17]	Transconductor = 6	C = 2	yes	yes	yes	yes	yes	0.18-µm CMOS	±0.9
Proposed controller	CFOA = 2	R = 4, C = 2	yes	yes	yes	yes	yes	AD844	±9

Abbreviations:
R = Resistor, C = Capacitor, NA = Not Available,
OA = operational amplifier, OTA = operational transconductance amplifier,
CDBA = current differencing buffered amplifier, OTRA = operational transresistance amplifier,
CCII = second-generation current conveyor, DO-CCII = dual-output CCII, VDCC = voltage differencing current conveyor,
CCTA = current conveyor transconductance amplifier, DVCCTA = differential voltage CCTA, DDCC = differential difference current conveyor,
ZC-CFTA = z-copy current follower transconductance amplifier, CFOA = current feedback operational amplifier

Figure 2 depicts the configuration of the proposed mixed-mode PID controller, which consists of two input terminals (v_{ic} and i_{ic}), and two output terminals (v_{oc} and i_{oc}). For the VM signal, the circuit provides high input and low output impedance, while for the CM signal, it provides low input and high output impedance. By appropriately employing the relevant input signals via v_{ic} and i_{ic}, the proposed PID controller can realize all four possible modes of operation, VM, TIM, CM, and TAM, in a single topology. Consequently, it is a mixed-mode PID controller.

The general transfer function of the PID controller can be expressed as:

$$G_V(s) = K_P + \frac{K_I}{s} + sK_D \quad (2)$$

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where the parameters K_P, K_I and K_D are the proportional gain, integral gain, and derivative gain of the controller, respectively.

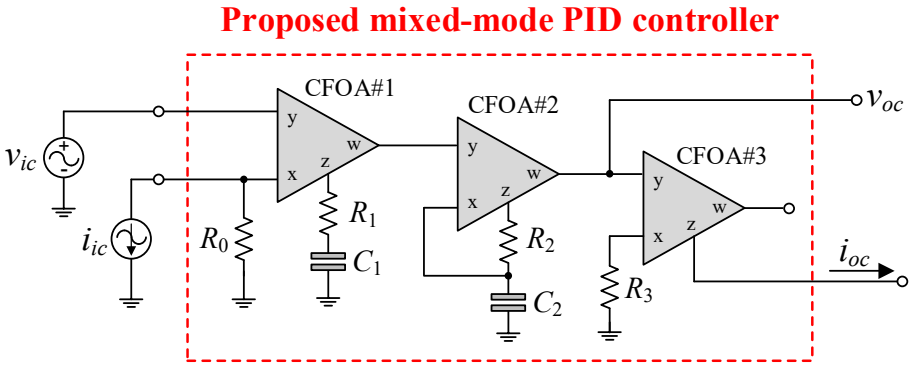

Figure 2. Proposed mixed-mode PID controller configuration using CFOAs.

2.1. VM and TAM Operations

From Figure 2, if $i_{ic} = 0$, one can derive the following generalized transfer function for VM:

$$G_V(s) = \frac{v_{oc}}{v_{ic}} = \frac{R_1}{R_0}\left(1+\frac{R_2C_2}{2R_1C_1}\right)+\left(\frac{1}{sR_0C_1}\right)+\left(\frac{sR_1R_2C_2}{2R_0}\right) \quad . \tag{3}$$

Comparing Equation (3) to Equation (2), the important gain coefficients of the proposed VM PID controller are obtained as follows:

$$K_{PV} = \frac{R_1}{R_0}\left(1+\frac{R_2C_2}{2R_1C_1}\right) \quad , \tag{4a}$$

$$K_{IV} = \frac{1}{R_0C_1} \quad , \tag{4b}$$

and

$$K_{DV} = \frac{R_1R_2C_2}{2R_0} \quad . \tag{4c}$$

In Equation (4), the parameters K_{PV}, K_{IV} and K_{DV} are the gains K_P, K_I, and K_D for VM, respectively.

Similarly, the transfer function of the proposed TAM PID controller is also obtained as:

$$G_Y(s) = \frac{i_{oc}}{v_{ic}} = \frac{R_1}{R_0R_3}\left(1+\frac{R_2C_2}{2R_1C_1}\right)+\left(\frac{1}{sR_0R_3C_1}\right)+\left(\frac{sR_1R_2C_2}{2R_0R_3}\right) \quad , \tag{5}$$

where

$$K_{PY} = \frac{R_1}{R_0R_3}\left(1+\frac{R_2C_2}{2R_1C_1}\right) \quad , \tag{6a}$$

$$K_{IY} = \frac{1}{R_0R_3C_1} \quad , \tag{6b}$$

and

$$K_{DY} = \frac{R_1R_2C_2}{2R_0R_3} \quad . \tag{6c}$$

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Since the primary objective of this communication is to design an analog PID controller with all four modes of operation in a single configuration, orthogonal adjustment of the control gain parameters $K_{PV(Y)}$, $K_{IV(Y)}$, and $K_{DV(Y)}$ derived from Equations (4) and (6) is not anticipated. However, independent tuning of $K_{IV(Y)}$ and $K_{DV(Y)}$ is possible via R_0 and C_2, respectively, by adjusting R_0, R_1, C_1, and C_2 simultaneously in order that R_1/R_0 and C_2/C_1 remain constant.

2.2. CM and TIM Operations

Furthermore, by applying i_{in} while connecting v_{ic} to ground (v_{ic} = 0), the proposed circuit in Figure 2 can be used for CM PID control. As a consequence, the realized transfer function of the CM PID controller is

$$G_I(s) = \frac{i_{oc}}{i_{ic}} = \frac{R_1}{R_3}\left(1+\frac{R_2C_2}{2R_1C_1}\right)+\left(\frac{1}{sR_3C_1}\right)+\left(\frac{sR_1R_2C_2}{2R_3}\right) \quad . \tag{7}$$

For $R_0 = R_3$, the gain parameters K_{PI}, K_{II}, and K_{DI} of the CM PID controller in Equation (7) are the exact same as K_{PV}, K_{IV}, and K_{DV} in Equation (4).

It is also observed that the transfer function of the proposed TIM PID controller is found as:

$$G_Z(s) = \frac{v_{oc}}{i_{ic}} = \left(R_1+\frac{R_2C_2}{2C_1}\right)+\left(\frac{1}{sC_1}\right)+\left(\frac{sR_1R_2C_2}{2}\right) \quad , \tag{8}$$

where

$$K_{PZ} = R_1+\frac{R_2C_2}{2C_1} \quad , \tag{9a}$$

$$K_{IZ} = \frac{1}{C_1} \quad , \tag{9b}$$

and

$$K_{DZ} = \frac{R_1R_2C_2}{2} \quad . \tag{9c}$$

According to Equations (4), (6), and (9), it can be observed that the relative element sensitivities of the control coefficients are low, in that their values are all less than unity, as given below:

$$S_{R_0}^{K_{PV}} = S_{R_0,R_3}^{K_{PY}} = S_{R_3}^{K_{PI}} = -1 \quad , \tag{10}$$

$$S_{R_1}^{K_{PV},K_{PY},K_{PI},K_{PZ}} = \frac{1}{\left(1+\frac{R_2C_2}{2R_1C_1}\right)} < 1 \quad , \tag{11}$$

$$S_{R_2,C_2}^{K_{PV},K_{PY},K_{PI},K_{PZ}} = -S_{C_1}^{K_{PV},K_{PY},K_{PI},K_{PZ}} = \frac{1}{\left(1+\frac{2R_1C_1}{R_2C_2}\right)} < 1 \quad , \tag{12}$$

$$S_{R_0,C_1}^{K_{IV}} = S_{R_0,R_3,C_1}^{K_{IY}} = S_{R_3,C_1}^{K_{II}} = S_{C_1}^{K_{IZ}} = -1 \quad , \tag{13}$$

and

$$S_{R_0}^{K_{DV}} = S_{R_0,R_3}^{K_{DY}} = S_{R_3}^{K_{DI}} = -S_{R_1,R_2,C_2}^{K_{DV},K_{DY},K_{DI},K_{DZ}} = -1 \quad . \tag{14}$$

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3. Non-Ideality Effects of CFOA Parasitic Gains

In practice, the CFOA may take into account the non-ideal transfer gains β, α, and γ. According to Equation (1), when $\beta \neq \alpha \neq \gamma \neq 1$, the following are the practical gain parameters of the proposed PID controller in Figure 2.

For VM operation, the control parameters K_{PV}, K_{IV}, and K_{DV} are nonideally obtained as:

$$K_{PV} = \frac{\beta_1\beta_2\alpha_1\gamma_1\gamma_2 R_1}{R_0}\left[1+\frac{\alpha_2 R_2 C_2}{(1+\alpha_2)R_1 C_1}\right], \tag{15a}$$

$$K_{IV} = \frac{\beta_1\beta_2\alpha_1\gamma_1\gamma_2}{R_0 C_1}, \tag{15b}$$

and

$$K_{DV} = \frac{\beta_1\beta_2\alpha_1\alpha_2\gamma_1\gamma_2 R_1 R_2 C_2}{(1+\alpha_2)R_0}, \tag{15c}$$

where the multiplication coefficients β_i, α_i, and γ_i (i = 1, 2, 3) denote the non-ideal gains β, α, and γ of the i-th CFOA, respectively.

For TAM operation, the non-ideal control parameters K_{PY}, K_{IY}, and K_{DY} can be expressed as:

$$K_{PY} = \frac{\beta_1\beta_2\beta_3\alpha_1\alpha_3\gamma_1\gamma_2 R_1}{R_0 R_3}\left[1+\frac{\alpha_2 R_2 C_2}{(1+\alpha_2)R_1 C_1}\right], \tag{16a}$$

$$K_{IY} = \frac{\beta_1\beta_2\beta_3\alpha_1\alpha_3\gamma_1\gamma_2}{R_0 R_3 C_1}, \tag{16b}$$

and

$$K_{DY} = \frac{\beta_1\beta_2\beta_3\alpha_1\alpha_2\alpha_3\gamma_1\gamma_2 R_1 R_2 C_2}{(1+\alpha_2)R_0 R_3}. \tag{16c}$$

For CM and TIM operations, the non-ideal control parameters can be determined, respectively, as follows:

$$K_{PI} = \frac{\beta_2\beta_3\alpha_1\alpha_3\gamma_1\gamma_2 R_1}{R_3}\left[1+\frac{\alpha_2 R_2 C_2}{(1+\alpha_2)R_1 C_1}\right], \tag{17a}$$

$$K_{II} = \frac{\beta_2\beta_3\alpha_1\alpha_3\gamma_1\gamma_2}{R_3 C_1}, \tag{17b}$$

$$K_{DI} = \frac{\beta_2\beta_3\alpha_1\alpha_2\alpha_3\gamma_1\gamma_2 R_1 R_2 C_2}{(1+\alpha_2)R_3}, \tag{17c}$$

and

$$K_{PZ} = \beta_2\alpha_1\gamma_1\gamma_2\left[R_1+\frac{\alpha_2 R_2 C_2}{(1+\alpha_2)C_1}\right], \tag{18a}$$

$$K_{IZ} = \frac{\beta_2\alpha_1\gamma_1\gamma_2}{C_1}, \tag{18b}$$

$$K_{DZ} = \frac{\beta_2\alpha_1\alpha_2\gamma_1\gamma_2 R_1 R_2 C_2}{(1+\alpha_2)}. \tag{18c}$$

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According to Equations (15)-(18), the gain parameters of the proposed PID controller differ slightly owing to the non-ideal transfer gains β_i, α_i, and γ_i. Inspecting these equations implies that all sensitivities of the PID control coefficients with respect to non-ideal transfer gains of the CFOA are not greater than unity in absolute value.

4. Non-Ideality Effects of CFOA Parasitic Impedances

Figure 3 shows the non-ideal behavior model of the practical CFOA, including the typical parasitic impedances. In accordance with this model, R_x and R_w are the low-level parasitic resistances, R_z is the high-level parasitic resistance, and C_z is the parasitic capacitance, associated with the corresponding terminals. For example, the parasitic element values for the commercially available integrated circuit (IC) AD844 CFOA are as follows: R_x = 50 Ω, R_w = 15 Ω, R_z = 3 MΩ, and C_z = 4.5 pF [18].

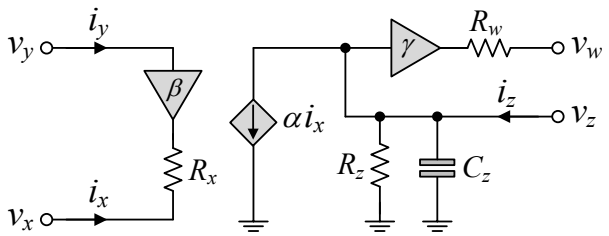

Figure 3. Non-ideal behavior model of the CFOA.

Considering the dominant parasitic effects of the CFOA on the performance of the proposed mixed-mode PID controller in Figure 2, the following additional assumptions can be defined under the conditions that $\beta \cong \alpha \cong \gamma \cong 1$:

$$\left| R_1 + \frac{1}{j\omega C_1} \right| << \left| R_{z1} // \frac{1}{j\omega C_{z1}} \right| , \tag{19}$$

and

$$\left| R_2 + \left(R_{x2} // \frac{1}{j\omega C_2} \right) \right| << \left| R_{z2} // \frac{1}{j\omega C_{z2}} \right| . \tag{20}$$

It is important to note that, in practice, the impact of the parasitic resistances R_{x1} and R_{x3} is negligible due to the fact that $R_0 >> R_{x1}$ and $R_3 >> R_{x3}$. The expression in Equation (19) can be rewritten as:

$$\sqrt{1+\left(\omega R_1 C_1\right)^2} << \frac{\omega R_{z1} C_1}{\sqrt{1+\left(\omega R_{z1} C_{z1}\right)^2}} . \tag{21}$$

When the parasitic capacitance C_{z1} is minimal, the operating frequency is limited to the following range:

$$f >> \frac{1}{2\pi\left(\sqrt{R_{z1}^2 - R_1^2}\right)C_1} \Rightarrow f_1 . \tag{22}$$

Additionally, from Equation (21), if R_{z1} is negligible, the range of applicable frequency is as follows:

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$$f << \frac{\sqrt{\left(\frac{C_1}{C_{z1}}\right)^2 - 1}}{2\pi R_1 C_1} \Rightarrow f_2 \quad . \tag{23}$$

For instance, if the commercially available IC AD844 CFOA is employed with R_1 = 5 kΩ, and C_1 = 1 nF, the useful operating frequencies found from Equations (22) and (23) are around $f_1 \cong$ 53 Hz, and $f_2 \cong$ 7.07 MHz.

Assuming that $R_2 >> R_{x2}$, Equation (20) can be rearranged as:

$$\sqrt{1+\left(\omega R_{z2} C_{z2}\right)^2} << \frac{R_{z2}}{R_2} \quad . \tag{24}$$

In the same manner, the practical frequency range in this case is limited to

$$f << \frac{\sqrt{\left(\frac{R_{z2}}{R_2}\right)^2 - 1}}{2\pi R_{z2} C_{z2}} \Rightarrow f_3 \quad . \tag{25}$$

By utilizing R_2 = 5 kΩ, R_{z2} = 3 MΩ, and C_{z2} = 4.5 pF, it is possible to determine the frequency location of $f_3 \cong$ 7.07 MHz.

By combining Equations (22), (23), and (25), the proposed mixed-mode PID controller shown in Figure 2 can be effectively utilized over the following frequency range:

$$max\{f_1\} << f << min\{f_2, f_3\} \quad . \tag{26}$$

5. Functional Simulation and Discussion

In order to validate the theoretical analysis presented in the previous section, the proposed mixed-mode PID controller circuit depicted Figure 2 was investigated using PSPICE program with model parameters of the commercial CFOA IC-type AD844 available from Analog Devices company [18]. All the AD844 ICs were biased with symmetrical power supplies of ±9 V. The passive components for the controller were set as: R_0 = 1 kΩ, $R_1 = R_2 = R_3$ = 5 kΩ, and $C_1 = C_2$ = 1 nF. For the specified component values, the controller parameters were calculated as follows:

- K_{PV} = 7.5, K_{IV} = 1 Ms^{-1}, and K_{DV} = 12.5 μs for VM;
- K_{PY} = 1.5 m, K_{IY} = 200 s^{-1}, and K_{DY} = 2.5 ns for TAM;
- K_{PI} = 1.5, K_{II} = 0.2 Ms^{-1}, and K_{DI} = 2.5 μs for CM;
- K_{PZ} = 7.5 k, K_{IZ} = 1 Gs^{-1}, and K_{DZ} = 12.5 ms for TIM.

Figure 4 illustrates the time-domain simulation responses of the VM, TAM, CM and TIM PID controllers in comparison to the ideal responses. As shown in Figure 4, the controller was applied with a 100-mV triangular input signal with a frequency of 1 MHz. Figure 5 additionally illustrates the ideal and simulated frequency-domain characteristics of the proposed mixed-mode PID controller with the exact same components. It is evident from these responses that the gain-frequency limitation of the controller occurs predominantly at more than 5 MHz. This phenomenon can be attributed to the dominant pole frequencies of parasitic impedances, as expected in the previous section. The total power consumption of the controller is approximately 0.348 W.

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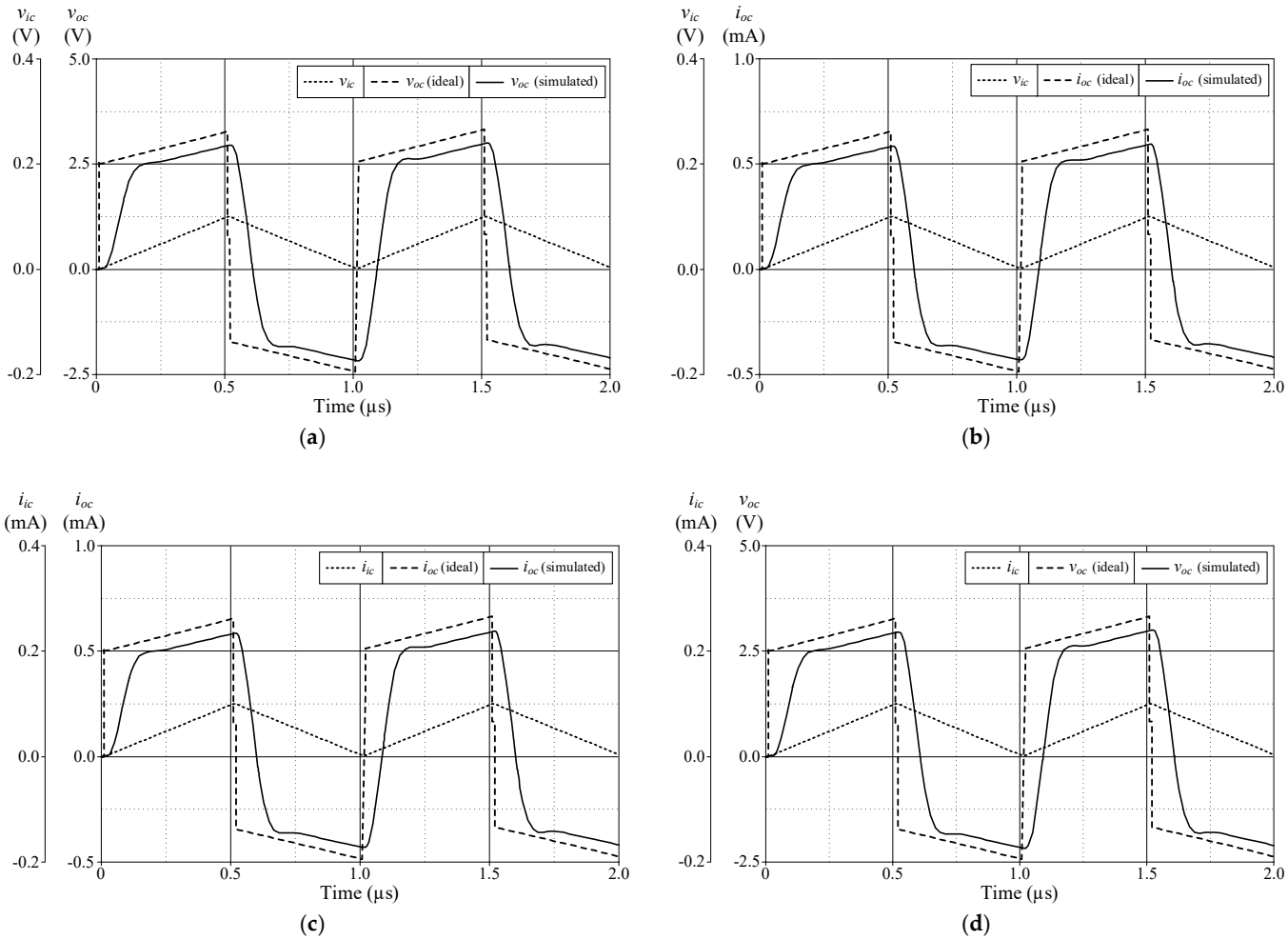

Figure 4. Ideal and simulated time-domain responses of the proposed controller in Figure 2: (**a**) VM; (**b**) TAM; (**c**) CM; (**d**) TIM.

A further analysis was conducted on the gain response variation in the proposed VM PID controller with respect to ambient temperature. The temperature analysis was performed at the following temperatures: T = 0°C, 25°C, 50°C, 75°C, and 100°C. The simulation results of the analysis of ambient temperature are illustrated in Figure 6, while Table 2 provides the controller gain values for various temperatures. Based on the data given in Table 2, the controller gain change with respect to temperature variation (ΔdBV/ΔT) is determined to be 0.137%, 0.138%, and 0.179% at f = 10 kHz, 100 kHz, and 1 MHz, respectively.

Additionally, Monte Carlo statistical analysis has been performed to demonstrate the robustness of the proposed controller. The analysis was conducted using 200 simulation runs in which the resistor and capacitor values were subject to a 5% Gaussian deviation. The Monte Carlo analysis results are shown in Figure 7. The results indicate that a change in the passive component has no significant effect on the phase or gain responses of the controller.

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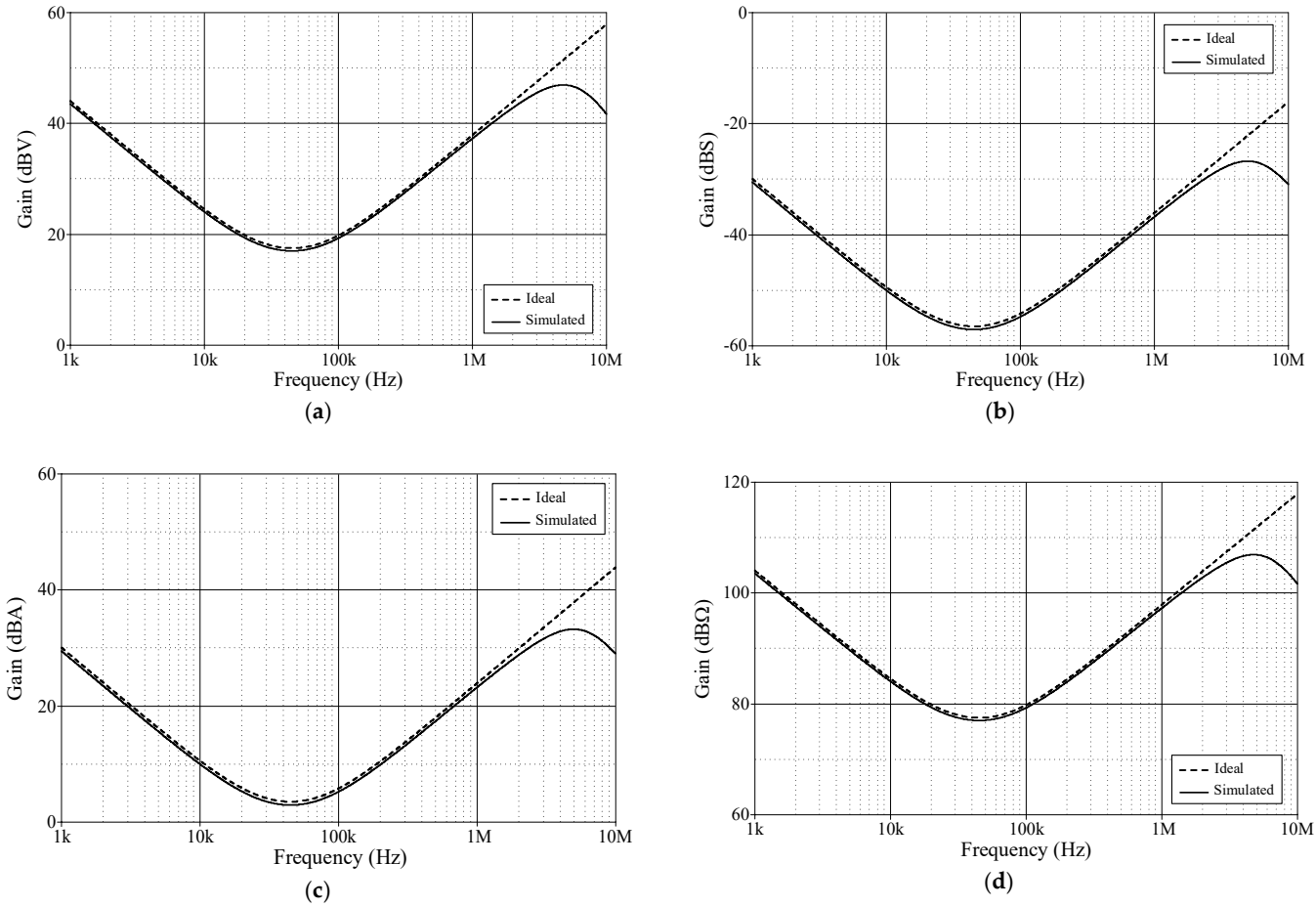

Figure 5. Ideal and simulated frequency-domain responses of the proposed controller in Figure 2: (**a**) VM; (**b**) TAM; (**c**) CM; (**d**) TIM.

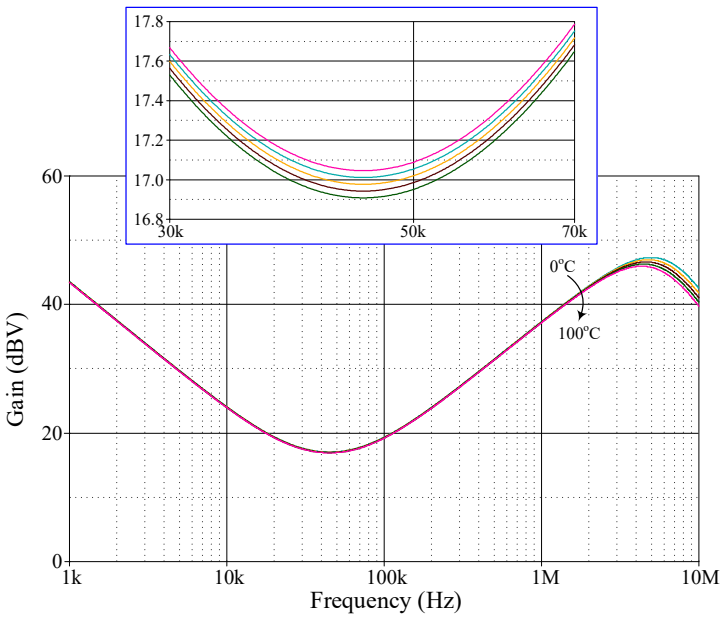

Figure 6. Simulated frequency responses of the proposed VM PID controller with ambient temperature variation.

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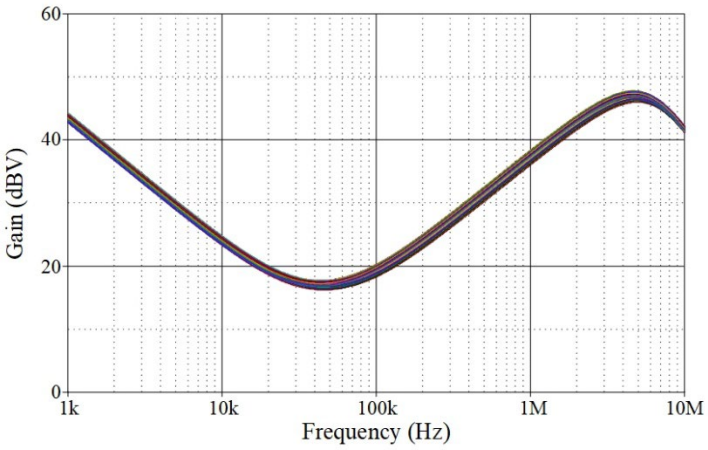
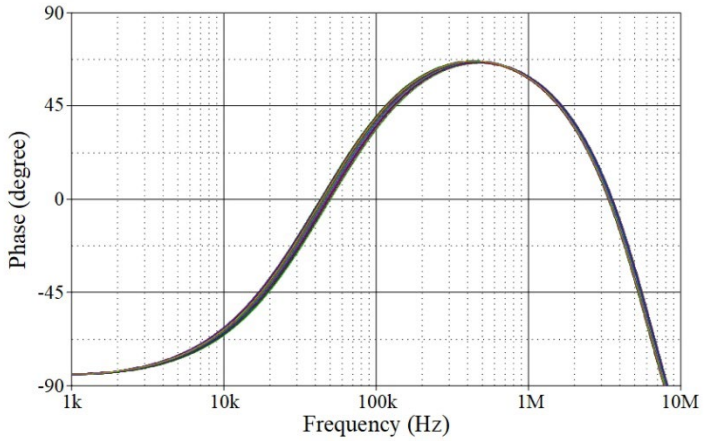
Table 2. Temperature dependence of the gain value for the proposed VM PID controller.

Temperature (°C)	Controller VM gain (dBV)		
	f = 10 kHz	f = 100 kHz	f = 1 MHz
0	24.090	19.350	37.336
25	24.056	19.315	37.293
50	24.021	19.281	37.249
75	23.987	19.246	37.204
100	23.953	19.212	37.157



(**a**)



(**b**)

Figure 7. Monte Carlo statistical analysis results of the proposed VM PID controller: (**a**) gain response; (**b**) phase response.

In order to evaluate of the tuning performance, the simulations have been carried out by varying the coefficients K_{PV}, K_{IV} and K_{DV} of the VM controller. For our first tuning example, the values of various controller components for the variation in controller coefficient K_{PV}, while holding K_{IV} and K_{DV} constant, are given in Table 3. As evident in Figure 8, the parameter K_{PV} influences the entire operational range as it appears from the gain response of the controller. The variations in the K_{IV} and K_{DV} values resulting from the use of different component values are also provided in Tables 4 and 5. For the specified set parameters, the gain responses of the VM PID controller with tuning K_{IV} and K_{DV} are illustrated in Figures 9 and 10, respectively.

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Table 3. Different component values for the variation in controller coefficient K_{PV}.

K_{PV}	K_{IV} (Ms^{-1})	K_{DV} (µs)	R_0 (kΩ)	$R_1 = R_2 = R_3$ (kΩ)	C_1 (nF)	C_2 (nF)
8.25			2.5	5	0.40	2.5
10.05	1	12.5	3.5	5	0.29	3.5
15.54			6.0	5	0.17	6.0

Table 4. Different component values for the variation in controller coefficient K_{IV}.

K_{PV}	K_{IV} (Ms^{-1})	K_{DV} (µs)	R_0 (kΩ)	$R_1 = R_2 = R_3$ (kΩ)	C_1 (nF)	C_2 (nF)
	0.89		2.5	5	0.45	2.5
7.5	0.70	12.5	3.5	5	0.41	3.5
	0.44		6.0	5	0.38	6.0

Table 5. Different component values for the variation in controller coefficient K_{DV}.

K_{PV}	K_{IV} (Ms^{-1})	K_{DV} (µs)	R_0 (kΩ)	$R_1 = R_2 = R_3$ (kΩ)	C_1 (nF)	C_2 (nF)
		5.61	3.5	5	0.72	1.57
3	0.4	4.52	6	5	0.42	2.17
		3.13	10	5	0.25	2.50

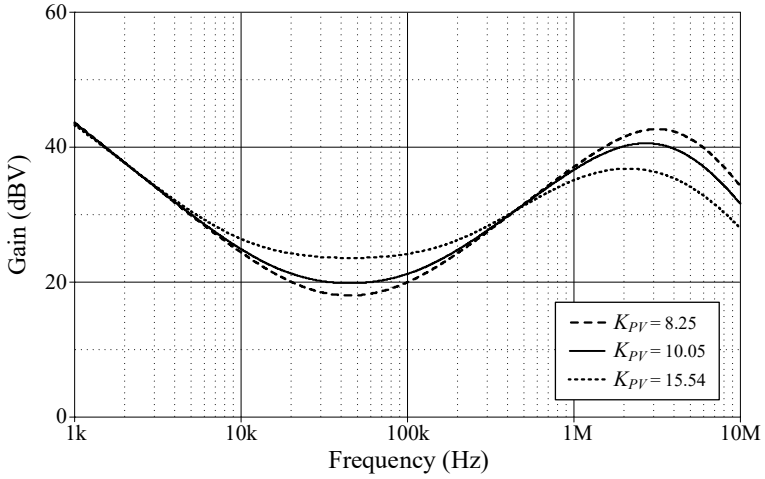

Figure 8. Gain-frequency responses of the proposed VM PID controller when adjusting K_{PV} while keeping K_{IV} and K_{DV} constant.

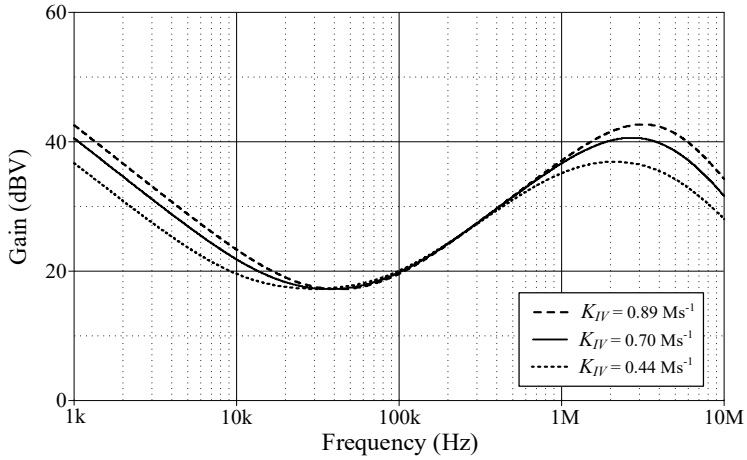

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Figure 9. Gain-frequency responses of the proposed VM PID controller when adjusting K_{IV} while keeping K_{PV} and K_{DV} constant.

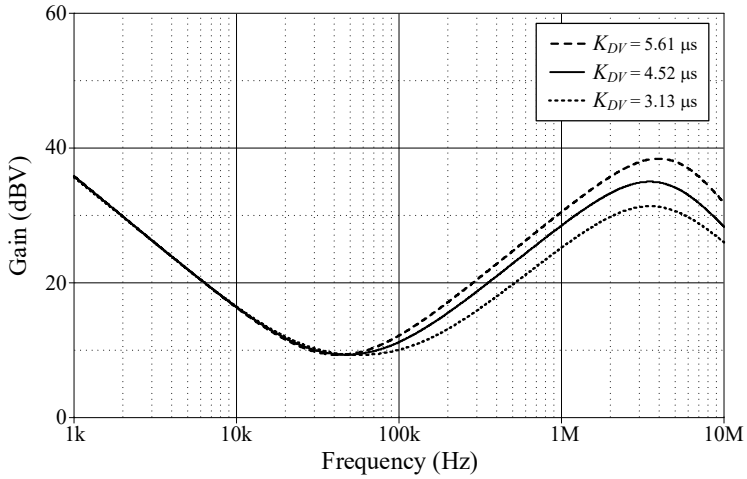

Figure 10. Gain-frequency responses of the proposed VM PID controller when adjusting K_{DV} while keeping K_{PV} and K_{IV} constant.

6. Performance Verification with Closed-Loop Control Implementation

In order to assess the effectiveness of the proposed mixed-mode PID controller in Figure 2, the mixed-mode second-order lowpass (LP) filter depicted in Figure 11 is suggested as a plant for implementing a closed-loop control system. The suggested LP filter can be realized for all four-mode LP filters with the following transfer functions:

VM:
$$T_V(s) = \frac{v_{op}}{v_{ip}} = \frac{\left(\frac{1}{R_{p0}R_{p2}C_{p1}C_{p2}}\right)}{D(s)}, \tag{27}$$

TAM:
$$T_Y(s) = \frac{i_{op}}{v_{ip}} = \frac{\left(\frac{1}{R_{p0}R_{p2}R_{p3}C_{p1}C_{p2}}\right)}{D(s)}, \tag{28}$$

CM:
$$T_I(s) = \frac{i_{op}}{i_{ip}} = \frac{\left(\frac{1}{R_{p2}R_{p3}C_{p1}C_{p2}}\right)}{D(s)}, \tag{29}$$

TIM:
$$T_Z(s) = \frac{v_{op}}{i_{ip}} = \frac{\left(\frac{1}{R_{p2}C_{p1}C_{p2}}\right)}{D(s)}, \tag{30}$$

where

$$D(s) = s^2 + s\left(\frac{1}{R_{p1}C_{p1}} + \frac{1}{R_{p2}C_{p2}}\right) + \left(\frac{1}{R_{p1}R_{p2}C_{p1}C_{p2}}\right). \tag{31}$$

From Equations (27)-(31), the natural angular frequency (ω_n) and the quality factor (Q) for the filter are respectively obtained as:

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$$\omega_n = 2\pi f_n = \frac{1}{\sqrt{R_{p1}R_{p2}C_{p1}C_{p2}}} \quad , \tag{32}$$

and

$$Q = \frac{\sqrt{R_{p1}R_{p2}C_{p1}C_{p2}}}{R_{p1}C_{p1} + R_{p2}C_{p2}} \quad . \tag{33}$$

The implemented closed-loop systems, as depicted in Figure 12, utilize the mixed-mode PID controller proposed in Figure 2 and the filter plant suggested in Figure 11. The configurations depicted in Figures 12a–d were constructed for the performance assessment of VM, TAM, CM, and TIM controllers, correspondingly. The component values for the filters are as follows: $R_{p0} = R_{p1} = R_{p2} = R_{p3} = 1$ kΩ and $C_{p1} = C_{p2} = 1$ nF; thus, $f_n = 159$ kHz and $Q = 0.5$ are obtained. All implemented controllers utilized $R_1 = R_3 = 5$ kΩ and $C_1 = C_2 = 200$ pF.

Figures 13–16 illustrate the step responses of the uncontrolled filter and PID-controlled filter systems for Figures 12a–d, respectively. The controller parameters employed to evaluate the step response, along with the characteristics derived from the responses for each of the four modes, are also documented in Tables 6–9. It is evident from the tables that the proposed PID controllers improve the time response of the closed-loop control filter systems, particular for t_d, t_r, t_p, and t_s. Additionally, the controlled filters enter the steady-state faster than the uncontrolled filters, and track the step-input with a reduced stead-state error.

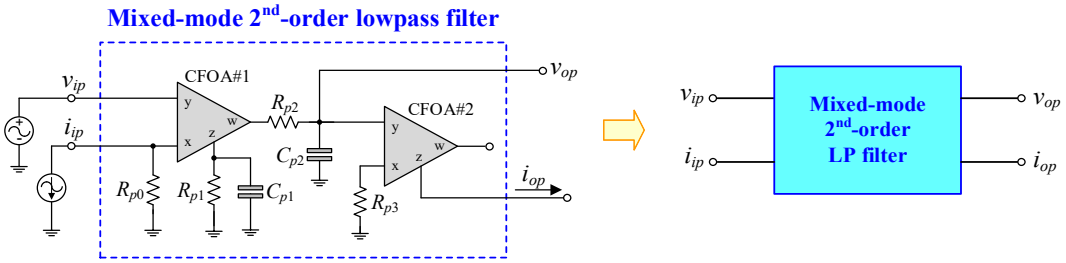
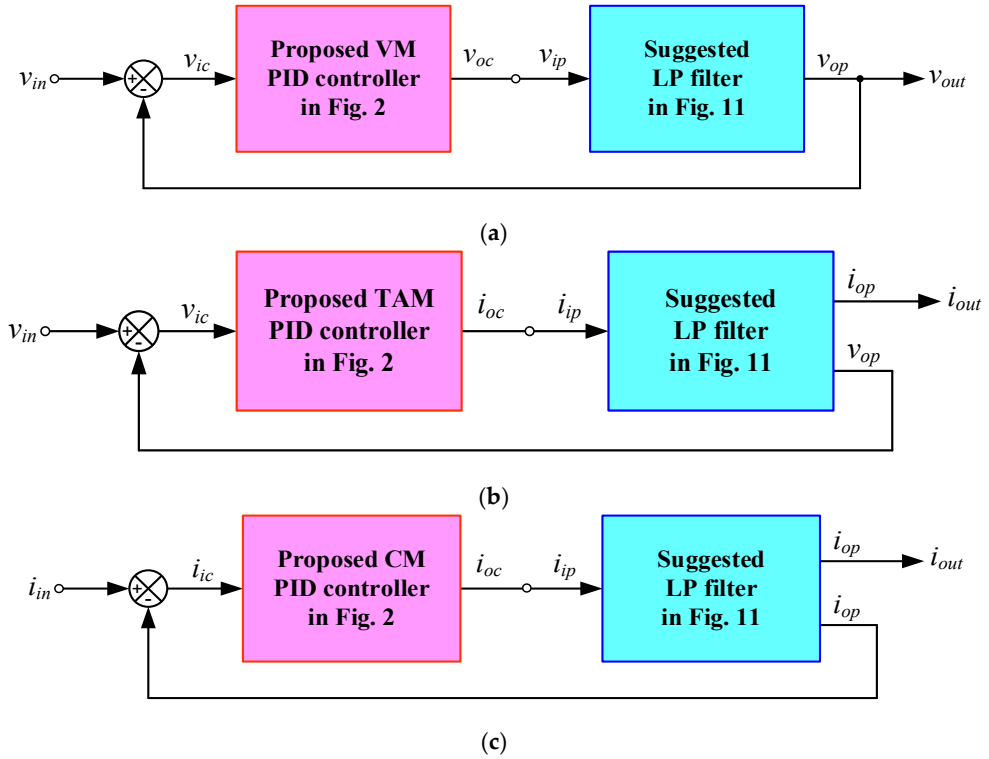


Figure 11. Suggested mixed-mode lowpass filter.



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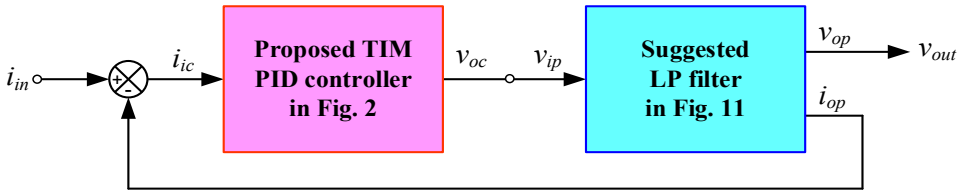

(**d**)

Figure 12. Closed-loop control system implementation: (**a**) VM; (**b**) TAM; (**c**) CM; (**d**) TIM.

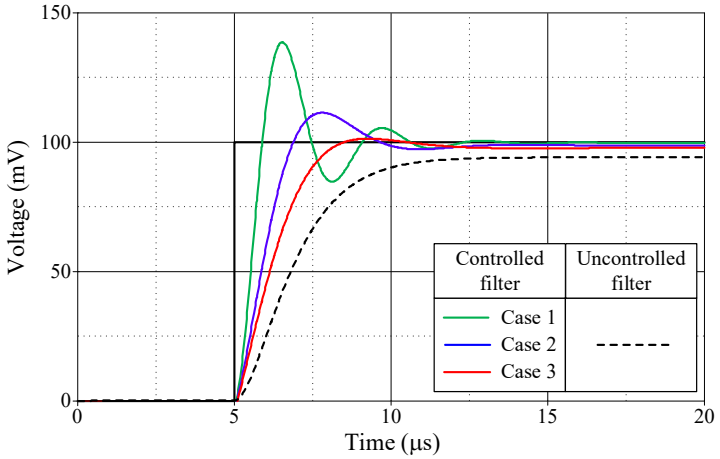

Figure 13. Step-responses of the uncontrolled and controlled filters in Figure 12(a).

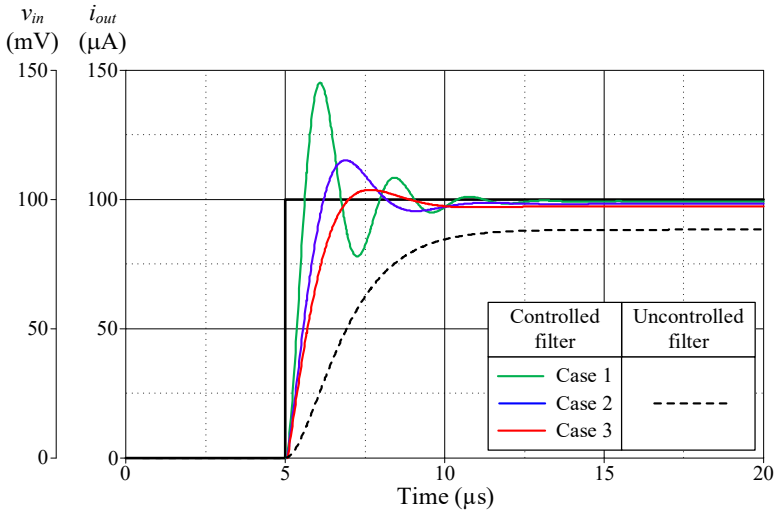

Figure 14. Step-responses of the uncontrolled and controlled filters in Figure 12(b).

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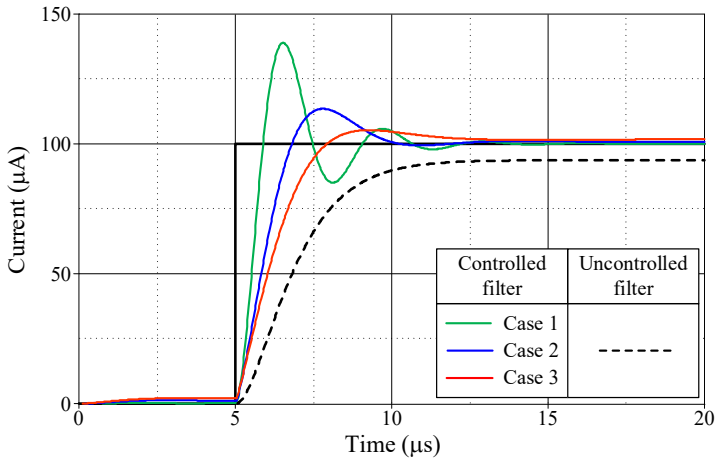

Figure 15. Step-responses of the uncontrolled and controlled filters in Figure 12(c).

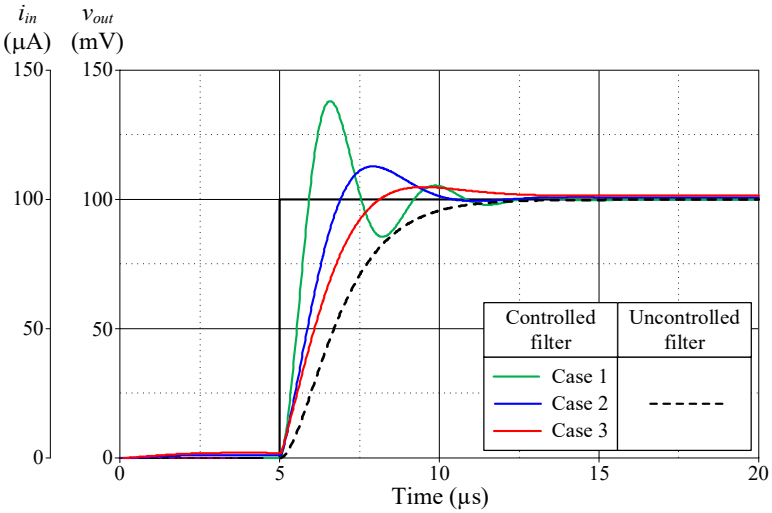

Figure 16. Step-responses of the uncontrolled and controlled filters in Figure 12(d).

Table 6. Controller parameters and the resulting characteristics of the uncontrolled filter and controlled filter systems shown in Figure 12(a).

		$R_0 = R_2$ (kΩ)	K_{PV}	K_{IV} (Ms^{-1})	K_{DV} (μs)	Delay time, t_d (μs)	Rise time, t_r (μs)	Peak time, t_p (μs)	Settling time, t_s (μs)		Maximum overshoot, M_p (mV)	Steady-state error (mV)
									5%	2%		
PID-controlled filter	**Case 1**	1	5.50	5.00	0.5	5.52	5.89	6.53	9.97	11.52	138.63	0.20
	Case 2	3	2.17	1.67	0.5	5.86	6.88	7.81	9.06	9.52	111.43	1.19
	Case 3	5	1.50	1.00	0.5	6.12	8.50	9.28	7.66	10.66	101.40	2.19
Uncontrolled filter						6.79	11.69	11.69	9.72	10.83	94.19	5.81

Table 7. Controller parameters and the resulting characteristics of the uncontrolled filter and controlled filter systems shown in Figure 12(b).

		$R_0 = R_2$ (kΩ)	K_{PY}	K_{IY} (Ms^{-1})	K_{DY} (μs)	Delay time, t_d (μs)	Rise time, t_r (μs)	Peak time, t_p (μs)	Settling time, t_s (μs)		Maximum overshoot, M_p (μA)	Steady-state error (μA)
									5%	2%		
PID-	**Case 1**	1	11	10	1	5.36	5.61	6.09	8.83	10.04	145.23	0.72

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controlled filter	**Case 2**	3	4.33	3.33	1	5.56	6.21	6.89	7.92	9.64	115.20	1.68
	Case 3	5	3	2	1	5.69	6.98	7.68	8.28	9.09	103.76	2.63
Uncontrolled filter						6.92	14.30	14.30	9.64	10.76	88.36	11.64

Table 8. Controller parameters and the resulting characteristics of the uncontrolled filter and controlled filter systems shown in Figure 12(c).

		$R_0 = R_2$ (kΩ)	K_{PI}	K_{II} (Ms^{-1})	K_{DI} (μs)	Delay time, t_d (μs)	Rise time, t_r (μs)	Peak time, t_p (μs)	Settling time, t_s (μs)		Maximum overshoot, M_p (μA)	Steady-state error (μA)
									5%	2%		
PID-controlled filter	**Case 1**	1	1.1	1	0.1	5.52	5.89	6.53	9.99	11.45	138.92	0.10
	Case 2	3	1.3	1	0.3	5.83	6.81	7.80	9.06	9.51	113.53	0.90
	Case 3	5	1.5	1	0.5	6.03	7.98	9.26	7.66	10.66	105.29	1.71
Uncontrolled filter						6.81	11.63	11.63	9.72	10.83	93.74	6.26

Table 9. Controller parameters and the resulting characteristics of the uncontrolled filter and controlled filter systems shown in Figure 12(d).

		$R_0 = R_2$ (kΩ)	K_{PZ}	K_{IZ} (Ms^{-1})	K_{DZ} (μs)	Delay time, t_d (μs)	Rise time, t_r (μs)	Peak time, t_p (μs)	Settling time, t_s (μs)		Maximum overshoot, M_p (mV)	Steady-state error (mV)
									5%	2%		
PID-controlled filter	**Case 1**	1	5.50	5	0.5	5.54	5.92	6.59	10.06	11.62	138.03	0.001
	Case 2	3	6.5	5	1.5	5.87	6.91	7.91	9.19	9.67	112.82	0.782
	Case 3	5	7.5	5	2.5	6.09	8.13	9.51	7.81	10.79	104.79	1.579
Uncontrolled filter						6.70	11.81	11.81	9.79	10.91	99.92	0.085

7. Conclusions

This work presents the tunable mixed-mode PID controller implemented with commercially available integrated circuits (ICs), the current-feedback operational amplifiers (CFOAs). The presented PID controller circuit employs three CFOAs, four resistors, and two capacitors. All four operational mode PID controllers, namely VM, TAM, CM, and TIM, can be performed with a single proposed circuit topology. The important parameters of the proposed PID controllers, namely, K_P, K_I, and K_D, are modifiable as desired. Since the proposed controller is designed using only off-the-shelf ICs together with some passive components, it has advantages in terms of practicality and simplicity. Analyses of non-ideal transfer gain and parasitic effects on the controller performance have also been examined in detail. In addition, to evaluate the practical applicability of the proposed mixed-mode PID controller, the mixed-mode second-order lowpass filter is designed to be a testing plant for a mixed-mode closed-loop control system. A simulation study demonstrates the performance of the circuits.

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Conflicts of Interest: The authors declare no conflict of interest.

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