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Article

Design of Three Phase Solid State Transformer Deployed within Multi-Stage Power Switching Converters

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Abstract: This paper presents a symmetrical topology for the design of solid-state transformer, made up of power switching converters, to replace conventional bulky transformers. The proposed circuitry not only reduces the overall size but also provides power flow control with the ability to be interfaced with renewable energy resources (RESs) to fulfill the future grid requirements at consumer end. Solid state transformer provides bidirectional power flow with variable voltage and frequency operation and has the ability to maintain unity power factor, and current total harmonic distortion (THD) for any type of load within defined limits of IEEE standard. Solid State Transformer offers much smaller size as compared to that of the conventional iron core transformer. MATLAB/Simulink platform is adopted to test the validity of the proposed circuit for different scenarios by providing the simulation results evaluated at 25 kHz switching frequency.

Keywords: Decoupled controller; ferrite material; proportional integral (PI); solid state transformer (SST); space vector pulse width modulation (SVPWM); voltage source converter (VSC); voltage source inverter (VSI).

1. Introduction

Main consideration, nowadays is to supply cheap, clean and sustainable supply of power to end consumers in future. To meet this goal, the most significant and required change is the design of distribution transformer. Traditional transformers are heavy, occupy a large volume and possess fix voltage and frequency operation. Traditional transformers are sensitive to transients, voltage disturbances, harmonics and inter harmonics due to non-linear and unbalanced loads [1], [2]. This creates power quality issues, as effects of load from consumer side travel to power distribution network. Distribution transformers have poor transformer utilization factor as magnetic core saturates due to harmonic nature of load. The presence of harmonic current due to nonlinear and unbalanced loads also influences the primary side current, thus creating power quality issues [3]. Besides power quality improvement and continuous supply of power to the customers, advanced type of transformer needs to be introduced to cope with the future grid requirement.

Over the past decade, power electronic converters have played a vital role in the well-known High Voltage Direct Current Transmission (HVDC) and Flexible Alternating Current Transmission

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(FACT) Systems in the form of static var compensators (SVCs), static synchronous compensators (STATCOMs) and unified power flow controllers (UPFCs), and so on [4]. Since renewable energy resources (RESs) such as wind, fuel cells and solar have penetrated into the industry, so power electronic converters also find their applications in them [5], [6]. Energy resources like natural coal or gas are limited and use of RESs are growing constantly with the aim to exchange electric power with the grid by net metering. Owing to the fact that the conventional transformer cannot be interfaced with RESs and the progress made in the field of power electronics, have led to the evolution of another power electronic converter named Solid State Transformer, also known as power electronic transformer, that has grabbed a lot of attention [7]-[11].

With the progress made in the field of semiconductor industry, high-frequency controlled switches with high-power ratings have been developed. With these advancements and to cope with the future requirement of distributed energy sources integration, research is being carried out in the field of power electronics which targets the use of SSTs in applications of high-power level. One of the key interests of researchers is to develop a dynamic architecture of SST acquiring minimum controlled switches; the other approach is integration of SSTs with RESs and other power applications [19].

Solid State Transformers respond to control signals but their designs are not simple due to the presence of power electronic converters. The basic principle of operation of SST is that it first transforms low-frequency (50 Hz) AC voltage to high-frequency (frequency more than 20 kHz) voltage. After that isolated dual active DC-DC high frequency converter regulates secondary dc voltage, whose size is much smaller because of high frequency operation. The multi-stage power electronic converters use controlled power electronic switches in series. In the first stage active rectifier is used which converts and controls grid voltage to dc grid voltage and provides extended control of active and reactive power [12]. Thus, it provides control of power and power factor. One of the most important benefits provided by SST is that it isolates both primary and secondary side, thus eliminating the coupling effects. Ride through capabilities, and compatibility between RESs and grid make SST superior to conventional transformers [12]. The ability of SSTs to generate any variable frequency voltage enables it to perform better and efficient in industry applications as it removes the requirement of using variable frequency drives (VFDs). SSTs, in future, will not only replace the conventional bulky transformers dominating at charge stations, locomotive and traction applications, smart grids and at secondary distribution sides, but also provide additional functions, such as control of active-reactive power and distribution source integration. Reduced-volume SST with aforementioned features also plays a key role in improving the power quality [13], [14].

Various two-level and multilevel switching converter topologies can be employed in SSTs as discussed in [15]. Some recent configurations of SST are also reported in [16]-[19]. SSTs in the form of Direct AC to AC Matrix Converters directly convert three phase alternating current to three phase alternating voltage [20]. SSTs without dc link are impossible to be interfaced with RESs and fuel cells [21]. However, SST with a dc link [22] offers advantages such as availability of dc port, and much reduced size due to high frequency operation over [20], [21]. But all aforementioned topologies involve large number of converter valves. The isolated type topology, presented in this paper with least possible controlled switches, completely isolates grid and load, and provides independent control of voltage, frequency, power flow and power factor. The suggested topology of SST also can maintain clean voltage and current waveforms of utility supply irrespective of type and nature of the load. This is what that has been stressed upon in this paper.

2. Proposed SST Circuit, Specifications and Control Layout

Vector control (decoupled controller) is used for three phase rectification purpose. Vector control employing controlled switches such as IGBTs maintains THD of input current within IEEE defined limits and provides ripple free dc output voltage. Obtained dc voltage $V_{DC,mes}$ is converted to high frequency square wave using full-bridge inverter which is stepped down using ferrite core high

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frequency transformer. This stepped down voltage is rectified again with the help of full-bridge converter as shown in Fig. 1. In the last stage, dc voltage V_x is converted back to variable three phase

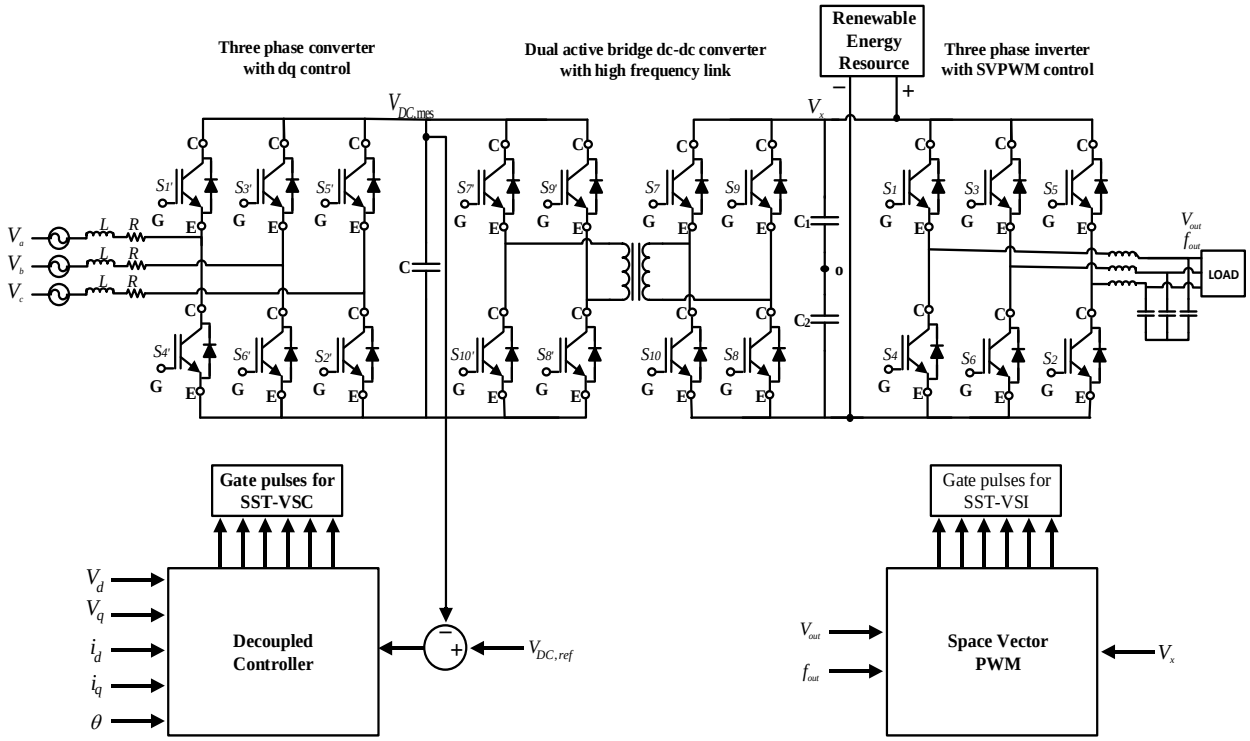

Figure 1. Proposed circuit diagram of Solid State Transformer.

voltage with frequency and voltage control using Space Vector Pulse Width Modulation (SVPWM) technique.

2.1. Control Layout Of SST-Voltage Source Convereter

Flux-oriented vector current control (VOC), based on two control layers: outer current control layer (OCC) and inner current control layer (ICC), is used to control the operation of voltage source converters (VSCs) [23]. The outer layer satisfies the dc voltage, active power and reactive power demands of the VSCs while the inner layer uses decoupling control method to regulate the q-axis and d-axis currents. Both control loops have a proportional and integral (PI) controller as common element in them. DC link voltage $V_{DC,mes}$ is regulated using voltage droop control [24]. Through the investigation of bi-layer control architecture deployed within multi-input multi-output (MIMO) voltage source converter, it can be realized that the operation of SST-VSC becomes a bit complex [25]. This complex control architecture has many variables which need to be controlled precisely using PI controllers [26]. Therefore, it is requirement of the system that PI controllers should be optimally tuned to provide both transient and steady state desired responses. But, tuning PI parameters of the nonlinear system like voltage source converter, is a challenging task within itself [27].

Vector current control is used at point of common coupling, which regulates the dc voltage control at VSC and power flow control with ac voltage regulation [28]. In this technique, ac voltage and current of the VSC are converted into rotating d-q reference frame, which is synchronized with ac grid voltages using phase locked loop (PLL). This methodology not only regulates dc and ac voltage but also provides the decoupled control of both active and reactive power. The layout of d-q control architecture-based SST-VSC is shown in Fig. 2. The outer control loop produces reference currents for inner current loop, which then provides the reference voltage for the d-q reference frame.

By taking d-q control frame into consideration, internal control loop uses PI controllers which generate reference current and maintain required voltage for the VSCs. Voltage expression at the point of common coupling (p_c) and voltage source converter side (v_s) can be given as:

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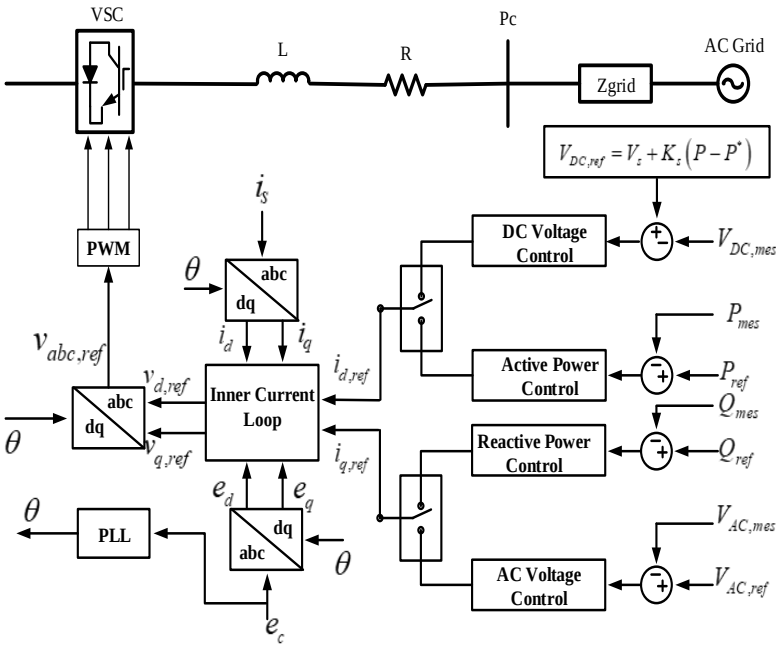

Figure 2. The d-q control architecture of SST-VSC.

$$e_C - v_S = R \times i_S + L\frac{di_S}{dt} \tag{1}$$

where R and L represent resistance and inductance between SST-VSC and PCC, while i_S is the current from grid to the SST-VSC.

From Park's transformation:

$$e_d - v_d = Ri_d - \omega Li_q + L\frac{di_d}{dt} \tag{2}$$

$$e_q - v_q = Ri_q + \omega Li_d + L\frac{di_q}{dt} \tag{3}$$

Here ω represents the angular frequency at PCC of ac system. Based on (2) and (3), ICC control layout is shown in Fig. 3. The reference signals (V_{d_ref} and V_{q_ref}) are transformed back to *abc* frame, which are used to generate switching pulses for IGBTs of VSC.

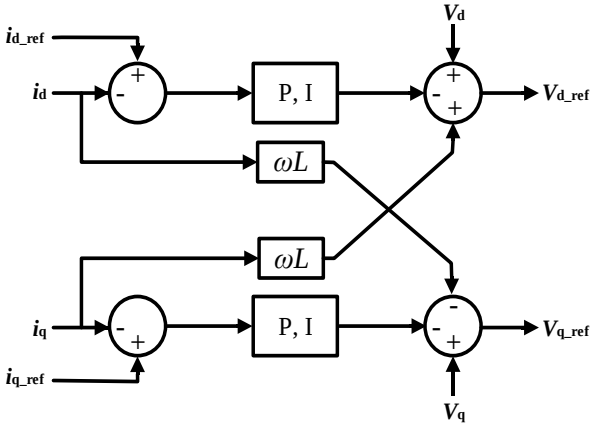

Figure 3. Inner current control loop of SST-VSC.

In this research, classical tuning method is used to tune the PI controller parameters. The transfer function of simple PI controller is:

$$F(s)=k_p+\frac{k_i}{s} \tag{4}$$

According to internal model control (IMC) method as presented in [29], we can write:

$$F(s)=k_p+\frac{\alpha_{ICC}}{s}\hat{G}^{-1}(s)=\frac{\alpha_{ICC}}{s}(R+sL)$$

$$F(s)=\alpha_{ICC}L+\alpha_{ICC}\frac{R}{s} \tag{5}$$

Here α_{ICC} (rad/s) represents the bandwidth of the current controlled system; $\hat{G}(s)$ is the estimation of $G(s)$. Comparison of (4) and (5) yields the range of PI controller coefficients for ICC as:

$$k_{p,ICC}\le\alpha_{ICC}L \tag{6}$$

$$k_{i,ICC}\le\alpha_{ICC}R \tag{7}$$

The bandwidth α_{ICC} for the ICC must be selected such that it is ten times lesser than the switching frequency [30], [31]. That is to say:

$$\alpha_{ICC}\le\frac{2\pi Fs}{10} \tag{8}$$

The PI controller parameters for the OCC can also be tuned using the same procedure as for ICC but with a constraint that OCC must be ten times slower than the ICC to achieve the non-oscillatory response of the closed loop system. This is achieved by selecting bandwidth of the OCC such that it is 10 times smaller than the bandwidth of the ICC. As presented in [32], the OCC PI controller parameters are given as:

$$k_{p,OCC}\le\alpha_{OCC}C \tag{9}$$

$$k_{i,OCC}\le\alpha_{OCC}{}^{2}C \tag{10}$$

$$\alpha_{OCC}\le\frac{\alpha_{ICC}}{10} \tag{11}$$

Outer control loop is responsible for controlling ac and dc voltage, both active and reactive powers at PCC. As shown in Fig. 2, *d-channel* controls dc link voltage or active power control, while the *q-channel* regulates ac voltage or controls the reactive power. These relations are mathematically represented as:

$$P=V_d i_d+V_q i_q \tag{12}$$

$$Q=V_q i_d-V_d i_q \tag{13}$$

Using PLL, d-axis of vector control is synchronized with phasor voltage of the ac system. So, $V_q=0$. This reduces (12) and (13) to:

$$P=V_d i_d \tag{14}$$

$$Q=-V_d i_q \tag{15}$$

From (14) and (15), active power and reactive power is regulated by controlling *d-q* axis currents. At PCC, ac voltage is regulated by *q*-axis current or can also be controlled by injecting required

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reactive power to the system. Likewise, dc link voltage is maintained via exchange of real power with ac system or by modifying the *d*-axis current.

The specifications of the VSC used within SST are given in Table 1:

Table 1. VSC Specifications for SST.

	Nominal Voltage	Specifications	Impedance
Ac grid	11 kV	200 kVA	$R = 1\ \Omega$ $L = 100$ mH
dc-link	20 kV		
dc-Capacitor	20 kV	Single 880 μF	

2.2. Control Layout Of SST-Voltage Source Inverter

Three phase two level voltage source inverters (VSIs), consisting of two power electronic switches in each leg, have penetrated in the industry as they provide various speed control demands of induction motor drives. Two level VSI has six active states and two null states. Various PWM techniques are proposed in [33], [34] to reduce the VSI output waveform distortions at given switching frequency. The most popular one is Space Vector PWM as it provides low output current ripple and provides maximum utilization of the dc-link voltages [35], [36]. It provides 15% higher ac voltage, lower current and voltage harmonics distortions as compared to conventional PWM [37]. This is the reason that SVPWM as modulation technique is employed in this research. The active states divide the space vector plane into six sectors of equal magnitude as shown in Fig. 4. Switching states for all eight (six active and two null) vectors are shown in Table 2.

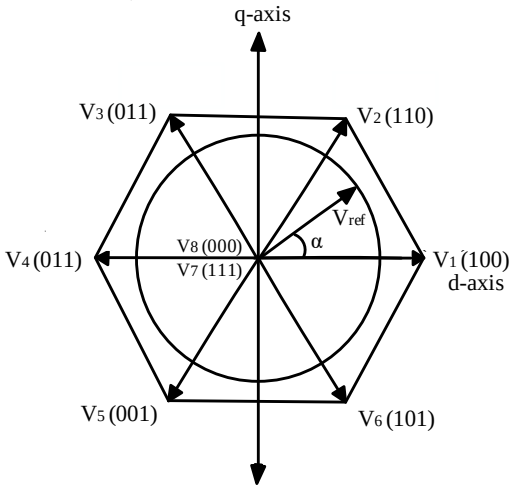

Figure 4. Vector representation of SVM signal.

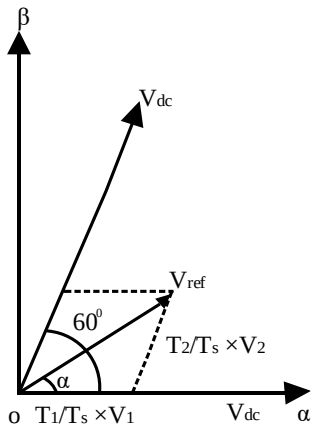

Figure 5. Vector representation of SVM signal in sector 1.

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Table 2. Space Vectors State and Switching Sequence.

Vector	Sector & Vector Combination		Line to Line Voltage			State
			V_{ab}	V_{bc}	V_{ca}	
V_0 (000)			0	0	0	Zero
V_1 (100)	I	V_0, V_1, V_2, V_7	$+V_d$	0	$-V_d$	Active
V_2 (110)	II	V_7, V_2, V_3, V_0	0	$+V_d$	$-V_d$	Active
V_3 (010)	III	V_0, V_3, V_4, V_7	$-V_d$	$+V_d$	0	Active
V_4 (011)	IV	V_7, V_4, V_5, V_0	$-V_d$	0	$+V_d$	Active
V_5 (001)	V	V_0, V_5, V_6, V_7	0	$-V_d$	$+V_d$	Active
V_6 (101)	VI	V_7, V_6, V_1, V_0	$+V_d$	$-V_d$	0	Active
V_7 (111)			0	0	0	Zero

Using SVPWM, desired three phase voltages are provided by the voltage vector controlled in *d-q* rotating frame as shown in Fig. 4, whose rotation is sampled in every sub-cycle T_s. Fig. 5 shows the component of reference voltage vector of magnitude V_{ref} along α and β-axis in sector I whereas, T_1, T_2 and T_z are dwell times for which active voltage vector V_1, active voltage vector V_2 and null vectors are applied in a sub-cycle T_s, such that the following relation is always satisfied.

$$T_S = T_1 + T_2 + T_Z \tag{16}$$

Consequently, the applied gating sequence of sector I is depicted in Fig. 6.

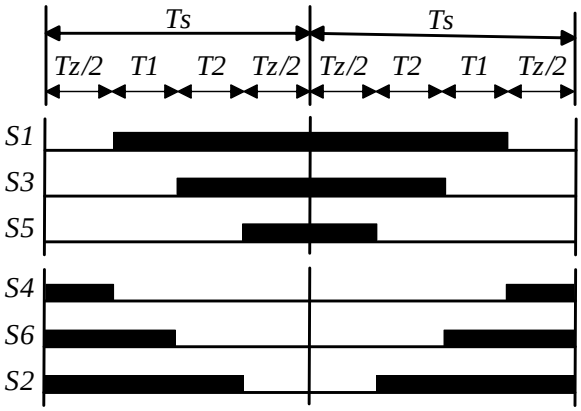

Figure 6. Gating sequence for the switches.

Volt-second balance equations along α-axis and β-axis are given as:

$$V_{ref} \times T_S \times \cos(\alpha) = \frac{2}{3} V_{dc} \left\{ T_1 + T_2 \times \cos(\frac{\pi}{3}) \right\} \tag{17}$$

$$V_{ref} \times T_S \times \sin(\alpha) = \frac{2}{3} V_{dc} \times T_2 \times \sin(\frac{\pi}{3}) \tag{18}$$

Solving (17) and (18) gives dwell time for each vector as:

$$T_1 = m \times \frac{\sin(\pi/3 - \alpha)}{\sin(\pi/3)} \times \frac{1}{f_s} \tag{19}$$

$$T_2 = m \times \frac{\sin(\alpha)}{\sin(\pi/3)} \times \frac{1}{f_s} \tag{20}$$

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206 $$T_Z = T_S - (T_1 + T_2) \quad (21)$$

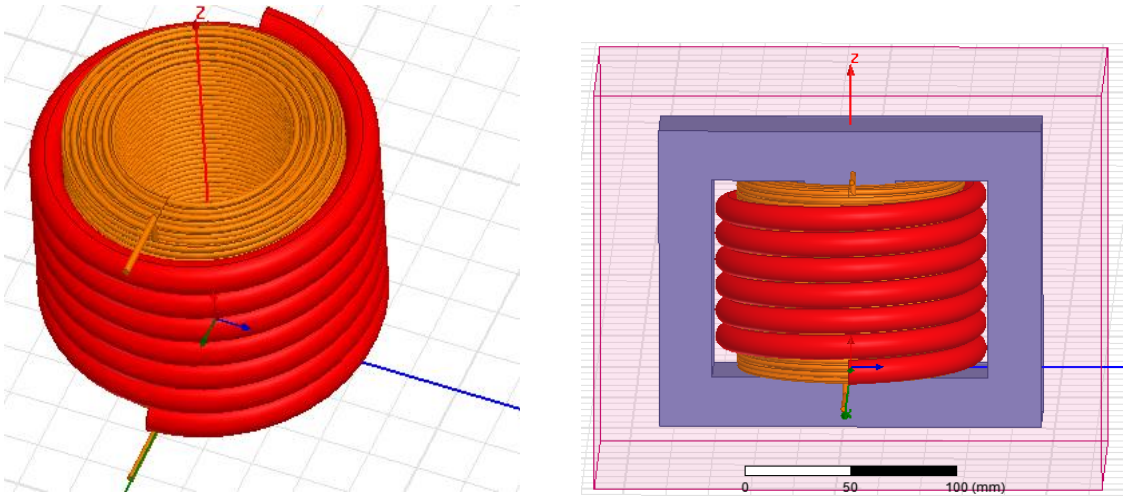
207 where '*m*' represents modulation index which is equal to $V_{ref}/(2/3V_{dc})$ and $f_s = 1/T_s$
208 represents the switching frequency.
209 The specifications of the VSI used within SST are given in Table 3.

210 **Table 3.** VSI Specifications for SST.

	Quantity	Specifications
dc- link	Input DC Voltage	500 V
dc- Capacitors	2-dc capacitors in series	Each 250 V & 20 mF
V_{out}	Output Voltage	Variable
F_{out}	Output Frequency	Variable

211 *2.3. Ferrite Core High Frequency Transformer Design*

212 The importance of ferrite materials is worth mentioning in modern power and industrial
213 electronics application. Design constraints of ferrite materials and losses incorporated in soft
214 magnetic materials due to high switching frequency are already discussed in literature [38], [39].
215 More elaborate models which discuss the modelling and dependence of ferrite losses at high flux
216 densities and high frequencies are also discussed in [40].
217 The operation of ferrites at square waves with 50% duty cycle offer 0-15% smaller losses as
218 compared to sinusoidal signals of same peak and frequency [41]-[44]. These properties and
219 performance make ferrite materials suitable for many switching applications where square wave
220 switching is desired without using any auxiliary filter circuits.
221 In this research work ferrite medium, operated at 50% duty cycle within DAB, is used not only
222 to provide galvanic isolation but also to decrease voltage levels. ANSYS/Maxwell platform is chosen
223 to design the high frequency ferrite core transformer. The specified design parameters of simulated
224 Maxwell model, as shown in Fig. 7, are tabulated in Table 4.



(**a**) (b)

225 **Figure 7.** High frequency ferrite core transformer. (**a**) Primary and secondary coil. (b) Complete
226 transformer model placed within air medium.

227 The parameters of high frequency transformer, simulated using ANSYS/Maxwell software,
228 tabulated in Table IV, are used in MATLAB/Simulink to carry out the simulation of SST.

Table 4. Parameters of High Frequency Ferrite Transformer.

Units	Quantity	Values
3F3	Ferrite (MnZn), P-Type	9997 (nH/T^2)
B	Magnetic flux density	3200 Gauss (core losses < 100 mW/cm^3)
W_aA_c	Product of Core Area and Window Winding Area	1006.7857 cm^4
A_c	Core Area	25cm^2
W_a	Window Winding Area	40.271429 cm^2
P_o	Power	200 kVA
F	Frequency	25 kHz
J	Current Density	3.5 A/mm^2
K	Filling Factor	0.6
V_p	Primary Voltage	20 kV
I_p	Primary Current (with 5% increase in input power to cover losses)	10.5 A
V_s	Secondary Voltage	500 V
I_s	Secondary Current	400 A
N_p	Primary Turns	250 Turns
N_s	Secondary Turns	7 Turns
R_p	Primary Winding Resistance	0.299947 Ω
L_p	Primary Winding Inductance	26676.98 μH
R_s	Secondary Winding Resistance	0.34242 mΩ
L_s	Secondary Winding Inductance	400.904 μH
A_{pw}	Primary Winding Wire Area (with skin effect compensation)	4.399 mm^2
A_{sw}	Secondary Winding Wire Area (with skin effect compensation)	122.23 mm^2

3. Simulation Results

The SST-VSC incorporated within inner-outer control loops and voltage droop control maintains both active and reactive power requirements while the SST-VSI fulfills variable frequency control requirements at the consumer end. The SST-VSC connected with 11 kV grid, maintains dc-link $V_{DC,mes}$ at 20 kV whose specifications are already given in Table I, while the SST-VSI, specifications given in Table 2, generates variable voltage and variable frequency at the load end.

Since the proposed circuit is symmetric, so the bidirectional power flow can be achieved just by changing the gate pulses only without any amendment in the circuit. To assess the flexibility and validity of the proposed circuit, simulations using MATLAB/Simulink environment are carried out for four different test cases: SST to deliver active power, SST as a variable frequency drive, bidirectional power flow interfacing RES, and SST as a power factor improvement (PFI) device.

3.1. Case 1: Active Power Flow

Simulation results are presented at various stages of the proposed SST based on multi-stage power switching converters after the transient period is elapsed. Three phase voltage and current at grid side are shown in Fig. 8. As can be observed from Fig. 9, SST input voltage (phase A) and current

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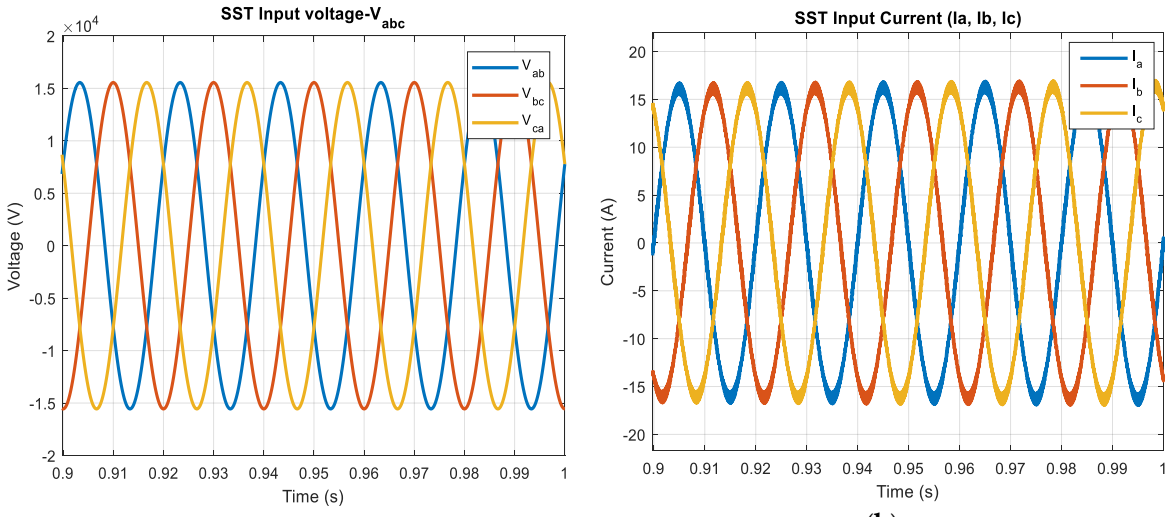
(phase A) at grid side remain in-phase even active power demand is varied from 0.0 p.u. to 1.0 p.u, thus delivering power at unity power factor. Results show that presented SST model draws balanced three phase current from the grid. Input current (phase A) has very less harmonic content (THD = 2.16%) as shown in Fig. 10. Same results are valid for other phases as well.



(**a**) (**b**)

Figure 8. (**a**) SST input voltage at grid side. (b) SST input current at grid side.

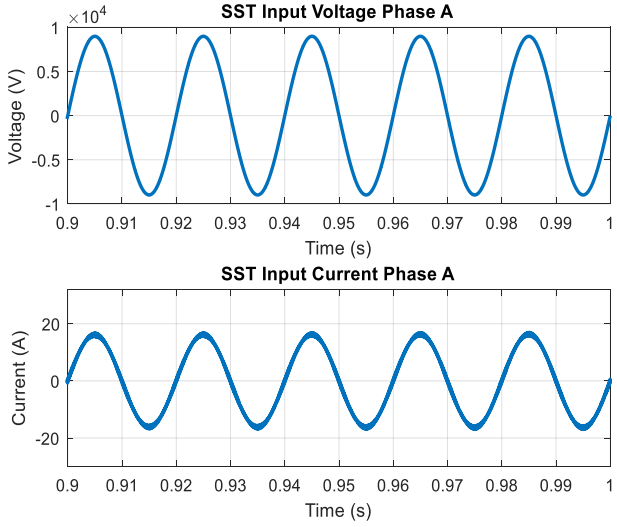
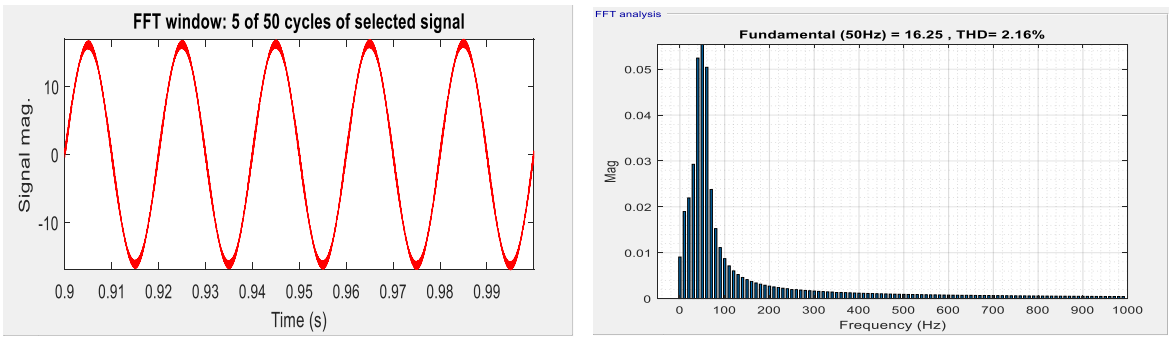


Figure 9. Result displaying that phase A voltage and current are in phase with each other.



(**a**) (**b**)

Figure 10. (a) Phase A current drawn from utility (b) THD analysis of phase A current.

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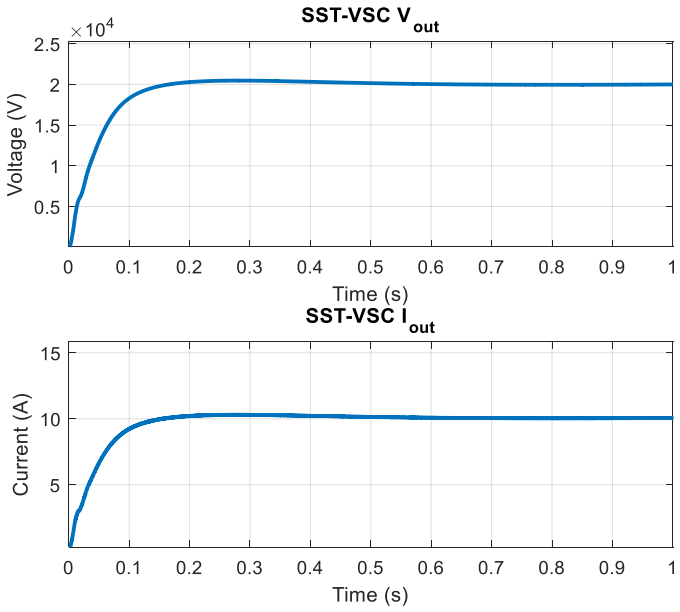

FIGURE 11. SST-VSC voltage and current at dc-link

In dual active bridge (DAB) circuit, the full bridge square wave inverter cascaded at SST-VSC generates square wave voltage of 25 kHz for the high frequency transformer (HFT), which reduces voltage level. The other full bridge square wave converter used within DAB, rectifies the voltage at secondary side of HFT. The voltage and current response of the SST-VSC at dc-link $V_{DC,mes}$ side is given in Fig. 11. Voltage at primary and secondary side of HFT are shown in Fig. 12.

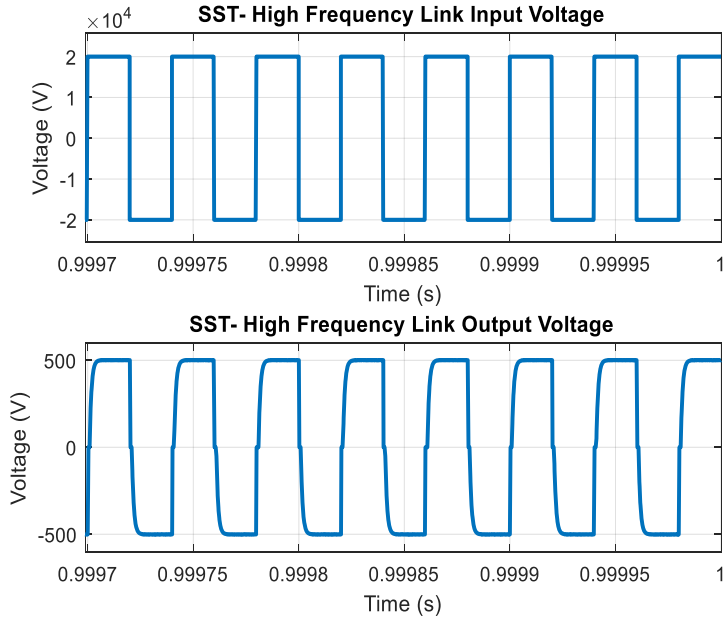

FIGURE 12. Primary and secondary voltage of high frequency transformer.

At the DAB end, dc-capacitor decreases the ripple content while the SST-VSI cascaded uses SVPWM pulses to generate three phase voltage with variable frequency and amplitude for the consumer end. When generated frequency is 50 Hz, the SST-VSI output L-N voltage before and after filter circuits are shown in Fig. 13.

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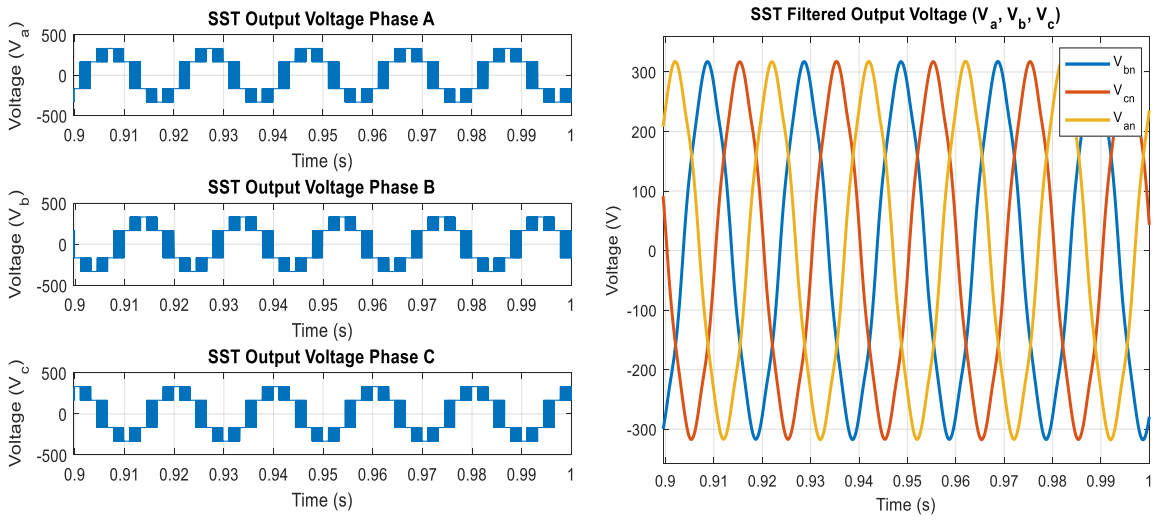

Figure 10. (a) SST-VSI output voltage without filter. (b) Filtered SST output Voltage.

3.2. Case 2: SST as Variable Frequency Drive

When the operation of SST as VFD is evaluated for the case when SST delivers power to an induction motor with 1.0 p.u mechanical loading, the obtained results show satisfactory results. SST maintains unity power factor. The grid side current harmonic contents are within IEEE defined THD limits. With induction motor at rated loading, settling time of SST-VSC at dc-link increases by 0.15 s, as shown in Fig. 14. SST-VSC takes a little bit more (0.32 s) time to settle for the inductive load.

For the case when SST generates voltage signal of 50 Hz for the inductive load, it can be observed from Fig. 15 that SST input current and the voltage are in phase, thus ensuring unity power factor. For this case, filtered SST output voltage is show in Fig.16.

When SST generates 60 Hz voltage signal for the load, same parameters are evaluated, as in for previous case, and are displayed in Fig. 17. Similarly, a voltage signal of other frequencies can be generated using the proposed SST for the resistive as well as the inductive load.

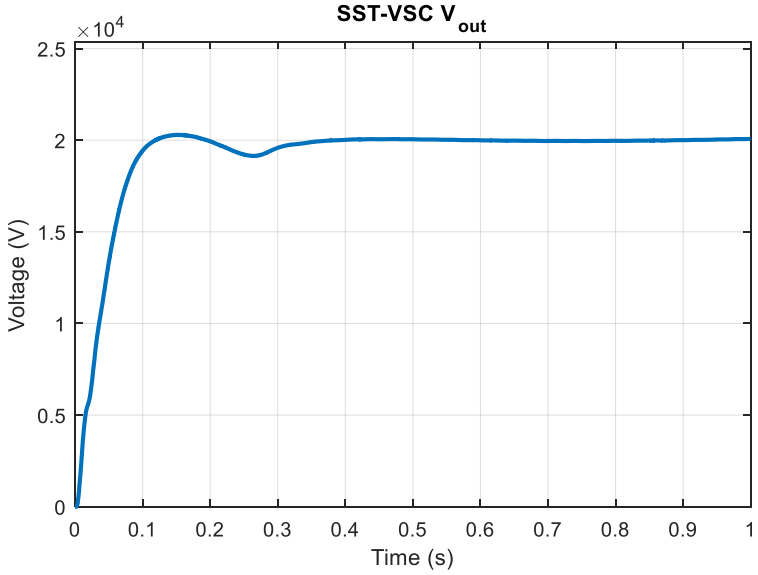

FIGURE 14. SST-VSC response with induction motor loading.

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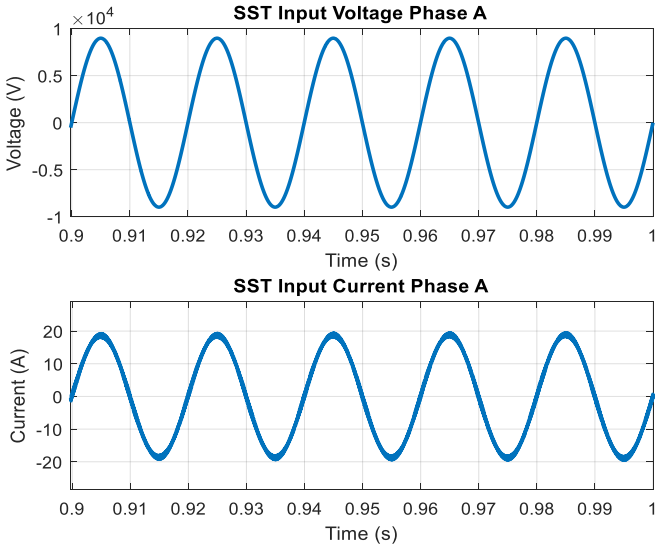

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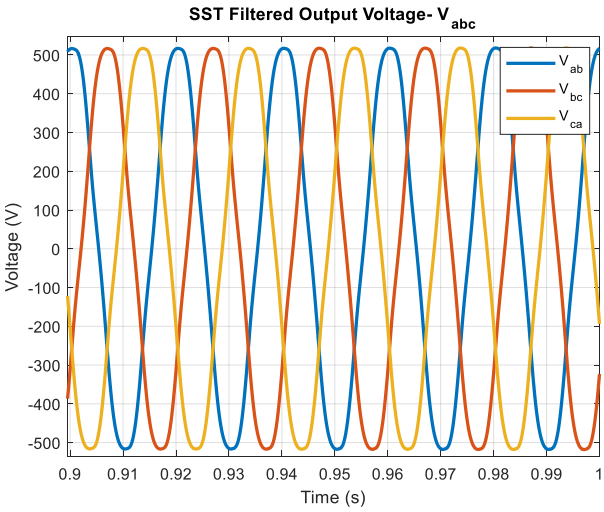
285 **FIGURE 15.** Result displaying that phase A voltage and current are in phase.



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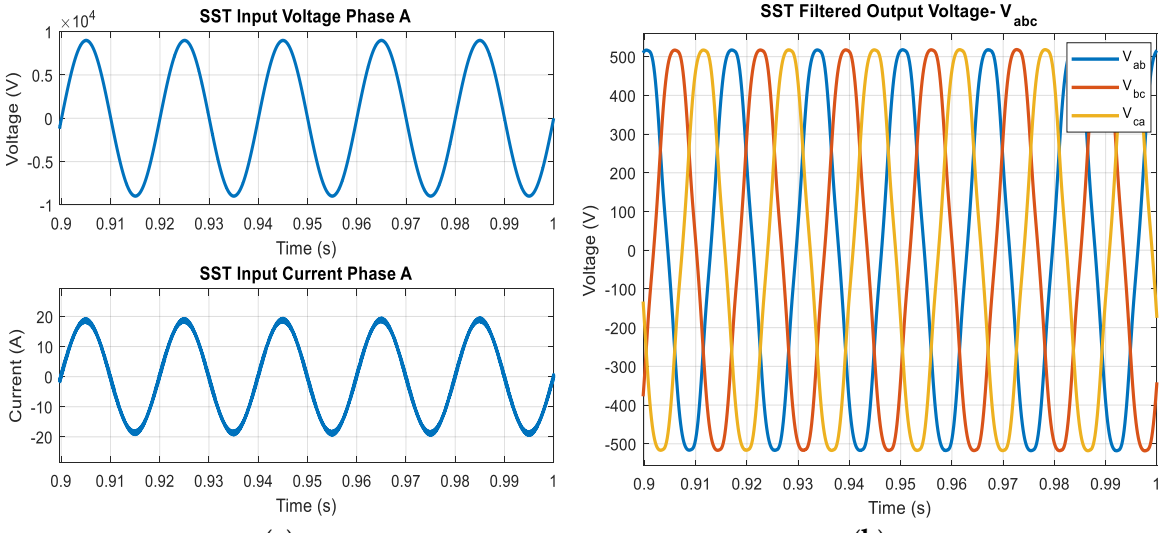
287 **FIGURE 16.** SST 50 Hz filtered output voltage.



(a) (b)

288 **FIGURE 17.** SST simulation results for 60 Hz output. (a) Phase A voltage and current in phase. (b)
289 SST 60 Hz filtered output voltage.

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3.3. Case 3: SST with a Renewable Interface

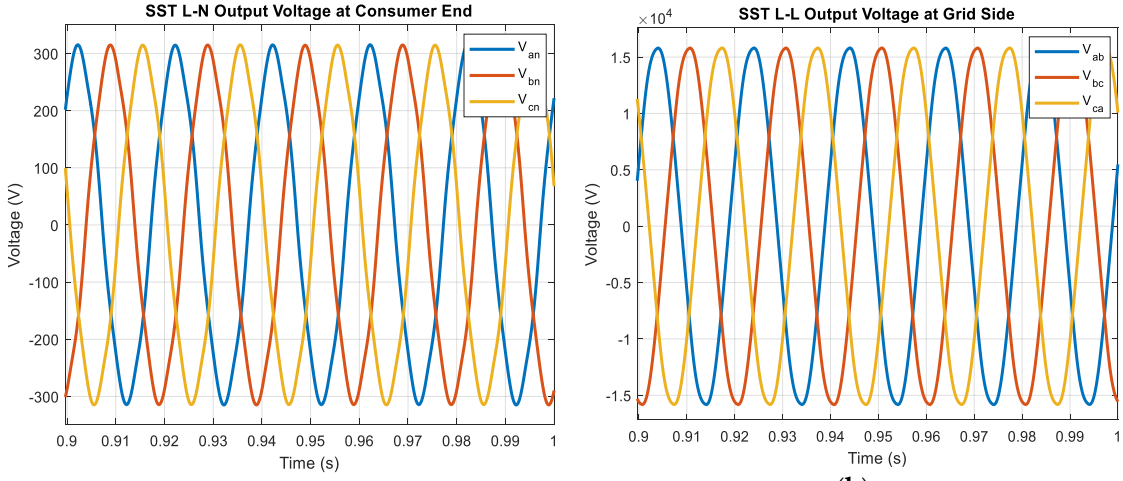
To cope with the increasing trend of using RESs, SST provides a very handy infrastructure. RES integrated with SST, as shown in Fig. 1, can be used solely to provide power to consumer, making SST working as stand-alone system. The proposed topology also makes bidirectional power flow possible just by changing the gate pulses of the SST-VSC to make it perform as SST-VSI.

High frequency transformer, which in previous cases was used to reduce the voltage level, now in this scenario, is working as step up HFT. DAB, in this case, will maintain dc-link for the SST-VSC. The SST-VSC, now working as SST-VSI, uses SVPWM pulses to generate three phase voltage. In this scenario SST is working as grid-tied inverter, feeding power to the utility.

The RES block, represented in Fig. 1, would be any single RES or the hybrid-RES incorporating batteries as well. In this research work, only the design of controlled multi-input multi-output circuitry of SST is under investigation. So, no specific constraints regarding the RESs are taken into consideration.

When a constant dc source is used as RES, simulations show that SST provides power not only to consumer but also to the utility as well, as shown in Fig. 18.

So, this architecture provided by SST would be a solution to all problems, that will be faced in the future when smart and super grids will be kicked in the power system.



(a) (b)

FIGURE 18. SST simulation results when integrated with renewable energy resource (a) SST line to neutral voltayge at consumer end. (b) SST line to line voltage at grid end.

3.4. Case 4: SST as a Power Factor Improvement Device

In the ICC of SST-VSC, quadrature component of current is maintained at zero using PI regulation, which forces SST not to draw reactive power from the grid, thus maintaining unity power factor at the grid side. When the q-component of current in ICC is maintained at any positive value, SST draws leading VAR from the grid, making SST as a PFI device, and at the same time maintaining its own feature of transformer.

When the current at grid side was set to 45° leading, simulation result shows that SST maintains its function of PFI device when it is delivering power to a 1 p.u. rated inductive load. As compared to the conventional transformers, this is remarkable achievement of the proposed SST design. Proposed circuit as a part of interconnected system has the ability to improve the overall power factor of the system while meeting the lagging reactive power requirement of the load. However, the current at the grid side increases as expected. Fig. 19 shows voltage and current of phase A at grid side, and filtered output voltage of the SST.

When SST as a PFI device is investigated by the pre-tuned PI controller parameters, simulation results show that SST-VSC takes more time (0.7 s) to settle its steady state value (see Fig. 20). Voltage

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droop control at the outer layer of the SST-VSC can be re-tuned to reduce the settling time of the SST-VSC.

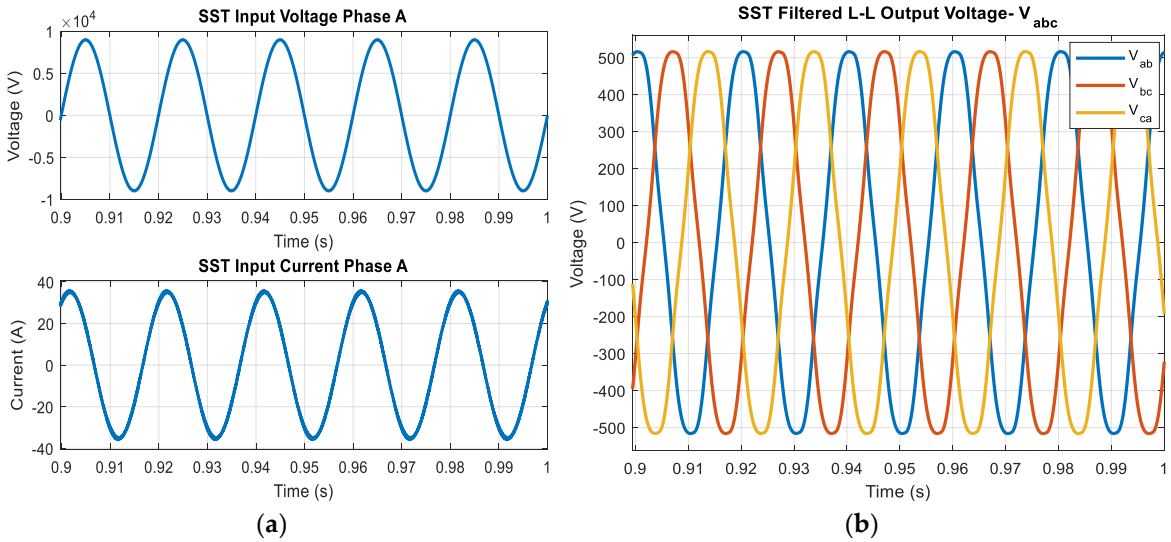

FIGURE 19. SST simulation results as PFI device (a) Input current leads input voltage. (b) SST filtered output voltage.

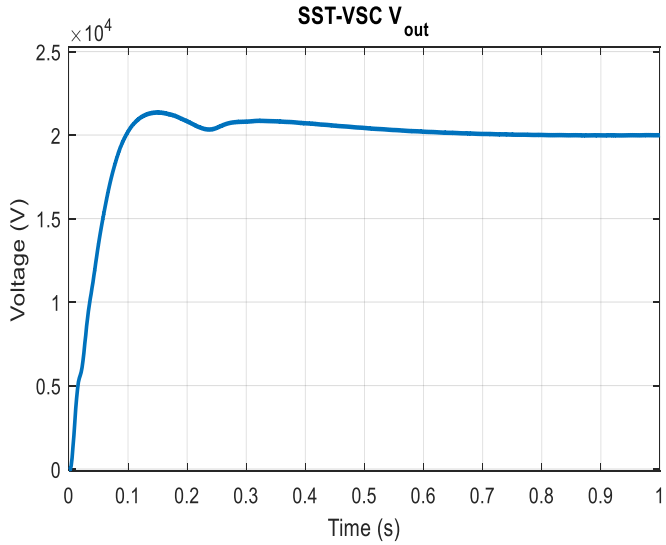

FIGURE 20. SST-VSC response working as PFI device with induction motor loading.

4. Conclusions

To replace conventional bulky transformers, reduced-size 'isolated' SST is proposed in this research. Either the source is single phase or three phase or dc source, proposed SST model can generate single phase or three phase or dc voltage for any type of resistive or inductive load. When interfaced with RES, symmetric configuration of SST makes it working as a stand-alone system at consumer end as well as grid-tied inverter at grid side. Simulation results are assessed for scenarios where SST acts as a variable frequency drive and as a power factor improvement device. In addition, when interfaced with RES, SST ensures bidirectional power flow as well. Simulation results validate the performance of the proposed SST for all the scenarios. Working of SST as VFD and PFI device with renewable interface makes it ideal for industrial applications where the proposed SST topology may eliminate the requirements of bulky conventional transformer especially for motor drive applications. This justifies the role of SST as VFD. The four quadrant operation of controlled switches with dc port within SST enables it to be integrated with micro/super grids. Proposed SST design has the ability to reject grid side disturbances, and regulate VAR at grid side and voltage levels for the

consumer end. The presented topology of SST can easily support the wide range operation of distribution system. The future work would be development of hardware setup for the proposed SST topology, thus to check the validity of the proposed SST model on real time industrial applications. Apart from SST design, optimized integration of SST with hybrid-RES would be a design worth of importance.

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References

1. J. S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in *Proc. IEEE Industry Applications Conference*, 2-6 Oct. 2005, pp. 1893-1899.
2. E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537-543, 2002.
3. U. Tahir, S. A. Ali, O. Azeem, O. Khan and R. Muzzammel, "THD improvement of phase voltages via injection of voltage in neutral conductor for three phase four wire distribution system," *2018 International Conference on Computing, Mathematics and Engineering Technologies (iCoMET)*, Sukkur, 2018, pp. 1-5.
4. N.G. Hingorani, *Understanding FACTs: concept and technology of flexible AC transmission systems*. New York: IEEE press, 2000.
5. Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A review of state of art power electronics for wind turbines," *IEEE Trans. Power Electron.*, vol.23, no.8, pp.1859-1875, Aug.2009.
6. J. M .Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P .Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power Electronic Systems for the Grid integration of Renewable Energy Sources: A survey," *IEEE Trans.Ind.Electron.*, vol.53, no.4, pp.1002-1016, June 2006.
7. S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. C. Clare, "Advanced power electronic conversion and control system for Universal and Flexible Power Management," *IEEE Trans.smart grid.*, vol.2, no.2, pp.231-243, June 2011.
8. T. F. Zhao, L. Y. Yang, J. Wang, and A. Q. Huang, "270kVA Solid State Transformer Based on 10kV SiC Power Devices," in *Proc.IEEE.Electric Ship Tech. Symp.*, 2007, pp.145-149.
9. G. Y. Wang, S. Baek, J. Elliott, A. Kadavelugu, F. Wang, X. She, S. Dutta, Y. Liu, T. F. Zhao, W. X. Yao, R. Gould, S. Bhattacharya, and A. Q. Huang, "Design and hardware implementation of Gen-I silicon based solid state transformer," in *Proc.IEEE.Appl.Power Electron.Conf.*, 2011, pp.1344-1349.
10. X. She, A. Q. Huang, and G. Y. Wang, "3-D space modulation with voltage-balancing capability for a cascaded seven-level converter in a solid state transformer," *IEEE Trans.Power Electron.*, vol.26, no.12, pp.3778-3789, Dec.2011.
11. D. Grider, M. Das, A. Agarwal, J. Palmour, S. Leslie, J. Ostop, R. Raju, M. Schutten, and A. Hefner, "10kV/120A SiC DMOSFET Half-bridge Power Modules for 1MVA Solid State Power substation," in *Proc.IEEE.Electric Ship Tech. Symp.*, 2011, pp.131-134.
12. A. Al-Hafri, H. Ali, A. Ghias and Q. Nasir, "Transformer-less based solid state transformer for intelligent power management," *2016 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA)*, Ras Al Khaimah, 2016, pp. 1-4.
13. P. Drabek, Z. Peroutka, M. Pittermann, and M. Cedl, "New configuration of traction converter with medium-frequency transformer using matrix converters", *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041-5048, Nov. 2011.
14. X. She, A. Q. Huang, F. Wang, and R. Burgos, "Wind energy system with integrated active power transfer, reactive power compensation, and voltage conversion functions", *IEEE Trans. Ind. Electron*, vol. 60, no. 10, pp. 4512-4524, Oct. 2013.
15. S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE Power and Energy Society General Meeting*, 25-29 Jul. 2010, pp. 1-8.

16. K. Basu and N. Mohan, "A single-stage power electronic transformer for a three-phase PWM AC/AC drive with source-based commutation of leakage energy and common-mode voltage suppression," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5881-5893, Nov. 2014.
17. S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid state transformer and MV Grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3343-3360, Jul.-Aug. 2015.
18. L. Wang, D. Zhang, Y. Wang, B. Wu, and H. S. Athab, "Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3289-3301, Apr. 2016.
19. Xu She, Alex Q. Huang and Rolando Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 1, No. 3, pp.-186-198, Sept. 2013.
20. R. Muzzammel and U.Tahir, "Maximization of Transfer Ratio and Minimization of Harmonics in Three Phase AC/AC Matrix Converter," *British Journal of Applied Science & Technology*, ISSN: 2231-0843,Vol.: 21, Issue. 2, 2017
21. H. Chen and D. Divan, "Design of a 10-kV·A Soft-Switching Solid-State Transformer (S4T)," in *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5724-5738, July 2018.
22. Reddy, B. Dheeraj, Dr. Sahoo, Sarat Kumar,"Design of Solid State Transformer," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 4, Issue 1, January 2015.
23. G. Wu *et al.*, "Analysis and design of vector control for VSC-HVDC connected to weak grids," *CSEE J. Power Energy Syst.*, vol. 3, no. 2, pp. 115-124, Jun. 2017.
24. K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "A generalized voltage droop strategy for control of multiterminal DC grids," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 607-618, Jan./Feb. 2015.
25. K. Rouzbehi, W. Zhang, J. I. Candela, A. Luna, and P. Rodriguez, "Unified reference controller for flexible primary control and inertia sharing in multi-terminal voltage source converter-HVDC grids," *IET Gener., Transmiss. Distrib.*, vol. 11, no. 3, pp. 750-758, Feb. 2017.
26. A. Raza, X. Dianguo, L. Yuchao, S. Xunwen, B. W. Williams, and C. Cecati, "Coordinated operation and control of VSC based multiterminal high voltage DC transmission systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 1, pp. 364-373, Jan. 2016.
27. Z.-L. Gaing, "A particle swarm optimization approach for optimum design of PID controller in AVR system," *IEEE Trans. Energy Convers.*, vol. 19, no. 2, pp. 384-391, Jun. 2004.
28. L. Xu, "Modeling, analysis and control of voltage-source converter in microgrids and HVDC," M.S. thesis, Univ. South Florida, Tampa, FL, USA, Nov. 2013.
29. OTTERSTEN ROLF. "*On Control of Back-to-Back converters and Sensorless Induction Machine Drives*". PhD Thesis, Department of Electric Power Engineering, Chalmers University of Technology, Göteborg, Sweden. 2003. 165p. ISBN: 91-7291-296-0.
30. K. Rouzbehi, A. Miranian, A. Luna, and P. Rodriguez, "Optimized control of multi-terminal DC grids using particle swarm optimization," *Eur. J. Power Electron.*, vol. 24, no. 2, pp. 38-49, 2014.
31. R. T. Pinto, P. Bauer, S. F. Rodrigues, E. J. Wiggelinkhuizen, J. Pierik, and B. Ferreira, "A novel distributed direct-voltage control strategy for grid integration of offshore wind energy systems through MTDC network," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2429-2441, Jun. 2013.
32. S. Rodrigues, "A multi-objective optimization framework for the design of offshore wind farms," Ph.D. dissertation, Delft Univ. Technol., Delft, The Netherlands, 2016.
33. J. Holtz, "Pulse width modulation for electronic power conversion", *Proc. IEEE*, vol. 82, no. 8, pp. 1194-1214, Aug, 1994.
34. D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Hoboken, *NJ:Wiley*, 2003.
35. J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls, and applications", *IEEE Trans. Ind. Electr.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
36. A. C. Binojkumar, J. S. Siva Prasad, and G. Narayanan, "Experimental investigation on the effect of advanced bus-clamping pulse width modulation on motor acoustic noise," *IEEE Trans. Ind. Electr*, vol. 60, no. 2, pp. 433-439, Feb. 2013.
37. A. Kumar and D. Chatterjee, "A survey on space vector pulse width modulation technique for a two-level inverter," *2017 National Power Electronics Conference (NPEC)*, Pune, 2017, pp. 78-83.

38. G. Bertotti, 'Hysteresis in magnetism', Academic Press, San Diego, USA, 1998, pp. 225-429.
39. R. Boll, 'Soft Magnetic Materials', The Vacuumschmelze Handbook, Heyden&Son Ltd., London, UK, 1979, pp. 13-108.
40. C.R. Sullivan, "Winding loss calculation with multiple windings, arbitrary waveforms and 2-D field geometry," IEEE IAS Annual Meeting,1999, pp. 2093-2099.
41. J. Li, T. Abdallah and C. Sullivan, "Improved calculation of core loss with non-sinusoidal waveforms," IEEE, IAS 36-th Annual Meeting, Chicago, USA, September 30 – October 4, 2001, pp. 2203-2210.
42. E. C. Snelling, "Soft Ferrites Properties and Applications", 2nd edition, London, UK., Butterworth, 1988.
43. A. V. Bossche, V. C. Valchev, G. B. Georgiev, "Measurement and Loss Model of Ferrites with Non-sinusoidal Waveforms", PECS'04, Aachen, Germany, 24-28 June, 2004.
44. V. C. Valchev, A. P. Van den Bossche and D. M. Van de Sype, "Ferrite losses of cores with square wave voltage and DC bias," *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005.*, Raleigh, NC, 2005, pp. 837-841.