A Cascade Fractional-N Synthesizer Topology of DLL and Frequency Multiplier for 5G+ Communication Systems

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Article

A Cascade Fractional-N Synthesizer Topology of DLL and Frequency Multiplier for 5G+ Communication Systems

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Abstract: This study presents a synthesizer topology based on a DLL and programmable frequency multiplier for 5G+ communication systems. The proposed synthesizer comprises a 512-phase DLL, an intermediate frequency generator (IFG), and an RF frequency multiplier (RFFM). The 512-phase DLL provides 512 delayed pulses through a chain of 256 delay units and single-to-differential complementary converters (S2DCs). The IFG comprises I/Q-multiplexers, I/Q-accumulators, an XOR, and an S2DC. The I/Q-multiplexer outputs switch to the phase lag or lead waveforms at every rising or falling edge of the outputs, which makes the I/Q-multiplexer output frequency, f_{MX}, programmable. The IF, f_{IF}, is two times f_{MX}, and f_{IF} is up-converted to RF, f_{RF}, through the RFFM. When reference clock frequency, f_{ref} is 156.25 MHz, the f_{IF} range is 156.863–312.5 MHz and the f_{RF} dynamic range is approximately 1.89–9.96 GHz. The channel resolution range is 3.698–38.609 MHz. Consequently, the proposed synthesizer provides a wide 134 % output frequency bandwidth and a finer channel resolution smaller than f_{ref}. The presented synthesizer is fabricated in a 65-nm CMOS process. The total power consumption is 15 mW, and the rms jitter integrated from 12 kHz to 20 MHz measured as 83 fs.

Keywords: 5G synthesizer; CMOS integrated circuits; delay-locked loop (DLL); harmonic suppression; integrated rms jitter; programmable frequency multiplier; phase locked loop (PLL)

1. Introduction

The quality factors of inductor (L) and capacitor (C) are small at the millimeter wave (mmWave). Therefore, designing an ultra-low phase noise (PN) LC voltage-controlled oscillator (VCO) that adheres to the stringent integrated jitter specification for the beyond 5G communication systems is tough. The cascade local oscillator (LO) generator structures of a lower-frequency synthesizer and a frequency multiplier (FM) have been recently published [1–5] to accomplish the jitter performance. The main goals of the lower-frequency synthesizer are to provide the best in-band phase noise (PN) and the finest channel resolution performances.

A multiplying delay-locked loop (MDLL), a subsampling phase-locked loop (SSPLL), and an injection-locked PLL (ILPLL) are good candidate topologies to achieve ultra-low in-band PN. Figure 1(a) shows a phase edge combined (EC)-based MDLL block diagram. Output frequency (f_{out}) can be expressed as $N \times f_{in}/2$, where N is an even integer number of delay cells in a voltage-controlled delay line (VCDL). Therefore, the MDLL channel resolution would be f_{in}. The biggest advantage of the MDLL is that it is free from jitter accumulation, which will improve the in-band PN. However, N is strictly difficult to program because the delay unit number in a VCDL must be changed. Therefore, its channel programmability is limited [6–9].

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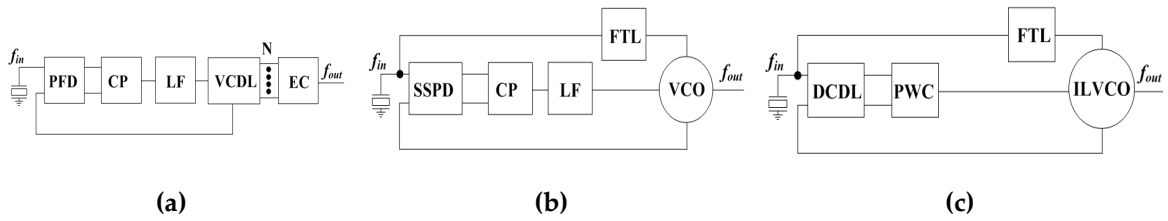

(a) **(b)** **(c)**

Figure 1. Block diagrams: (**a**) MDLL; (**b**) SSPLL; (c) ILPLL.

Both the SSPLL and ILPLL (Figure 1(b) and Figure 1(c)) have the same channel resolution (f_{in}) but require extra frequency tracking loops (FTLs) for locking the output frequency as N×f_{in}. After the target frequencies are tuned, the FTLs are turned off, and their lock states are maintained by a subsampling phase detector (SSPD) for the SSPLL and cascade connection of a digitally-controlled delay line (DCDL) and a pulse width controller for the ILPLL. Therefore, their in-band PNs will be improved because in-band PN sources are no longer multiplied by N^2 when transferred to the PLL outputs [10–12]. However, neither the SSPLL nor the ILPLL is suitable for high-magnitude multiplication, N, because it is difficult to design a reliable SSPD and DCDL as N is increased [13–16]. Consequently, the number of possible programmable channels is also restricted.

This paper presents a new cascade topology of a DLL-based synthesizer and an FM for a lower-frequency synthesizer. The DLL-based synthesizer consists of a 512-phase DLL and an intermediate frequency generator (IFG), providing a wide IF band. The IF band is up-converted to the RF band by the programmable high-frequency multiplication factor (FMF) RFFM. Therefore, the proposed synthesizer can provide ultra-low in-band PN, a channel resolution that is finer than the input frequency (f_{in}), ultra-low out-band PN, and a wide frequency band. The proposed synthesizer is fabricated in a 65-nm CMOS process, and the active die area is 0.6 mm^2. The total power consumption is 15 mW without counting a 50 Ω driving amplifier (DA) power consumption. Recent 5G LO research papers have achieved their rms jitter performances while using signal generators as reference clocks. However, our main purpose is to implement the optimum LO module solution for 5G+ wireless communication systems composed of the proposed synthesizer and currently available state-of-the-art reference external oscillators. When a 156.25 MHz micro-electro-mechanical systems (MEMS) differential oscillator (SiT9501) is applied as the reference clock, the LO module output frequency range is 1.88–9.96 GHz, and its channel resolution range is 3.698–38.609 MHz. The integrated rms jitter from 12 kHz to 20 MHz is 83 fs.

The rest of this paper is organized as follows: In section II, a new synthesizer topology is introduced. Its components are explained as well as their functionalities. Then, the proposed synthesizer output frequency range and channel resolution equations are presented. Finally, the synthesizer's phase noise analysis and the benefits are presented. Section III shows core building block schematics. The core circuitries are analyzed and verified through simulations. Also, the design procedure for the target output frequency range is talked about in detail. Furthermore, the synthesizer's adjacent harmonic rejection ratio analysis and simulation are presented last. The proposed synthesizer chip fabrication and printed circuit board (PCB) environment for testing the chip are shown in Section IV. Moreover, the synthesizer's power consumption is summarized, and the DA output matching and capacitor bank (C_{bank}) calibration are discussed. Finally, the test measurements of core specifications are reported. The summary and comparative analysis with recently published synthesizers are presented in Section V.

2. Topology, Analysis, And Frequency Range

2.1. Synthesizer Topology, RF Range, and Channel Resolution

The proposed synthesizer consists of three subsidiary blocks (blue-color boxes): a 512-phase DLL, an IFG, and an RFFM as shown in Figure 2. In terms of functionality, the synthesizer can be divided into two blocks. One is an IF synthesizer consisting of the 512-phase DLL and IFG, and the other is a programmable RFFM.

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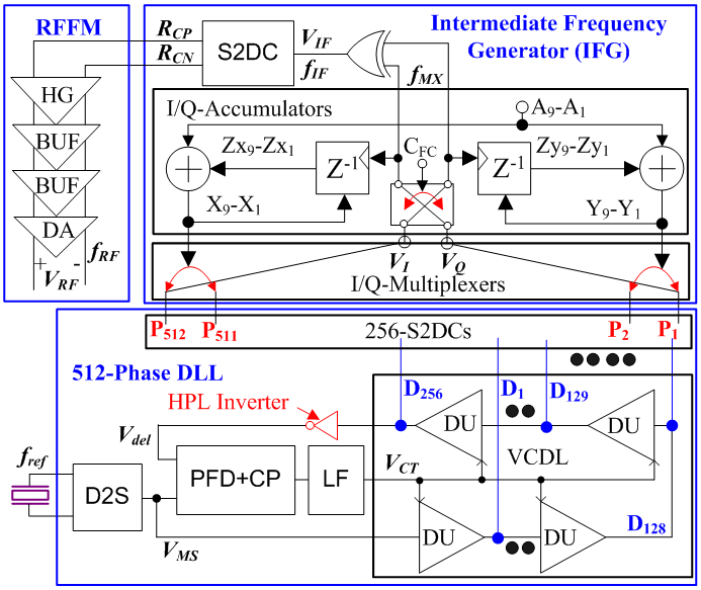

Figure 2. The proposed synthesizer block diagram.

The DLL's components are a differential-to-single (D2S) buffer, a phase frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled delay line (VCDL), and 256-phase single-to-differential complementary converters (256-S2DCs). The external oscillator frequency is denoted by f_{ref}, and its differential outputs are converted to V_{MS} through the D2S. The frequency of V_{MS} is f_{MS} (= f_{ref}), driving the PFD and VCDL. And, the VCDL is composed of a cascade chain of 256 delay units (DUs). An inverter (red) is inserted at the VCDL output to make it half-period locked, and its output (V_{del}) is fed to the other PFD input. The phase difference between V_{MS} and V_{del} is manipulated by the PFD+CP, which adjusts V_{CT} to control the delay of all the DUs simultaneously. When the phases of V_{MS} and V_{del} are locked, V_{del} is delayed by $T_{MS}/2$ from the rising edge of V_{MS}, where T_{MS} (= $1/f_{MS}$) is the period of V_{MS}. Therefore, each DU's delay, t_d, is uniformly equal to $T_{MS}/512$. An S2DC comprises two XORs: one XOR input is connected to a power supply, and the other XOR input is connected to a ground as shown in the dotted box of Figure 3(a). Figure 3(b) shows that the 256 different phase (D_1–D_{256}) pulses are expanded to 512 different phase (P_1–P_{512}) pulses through the 256-S2DCs.

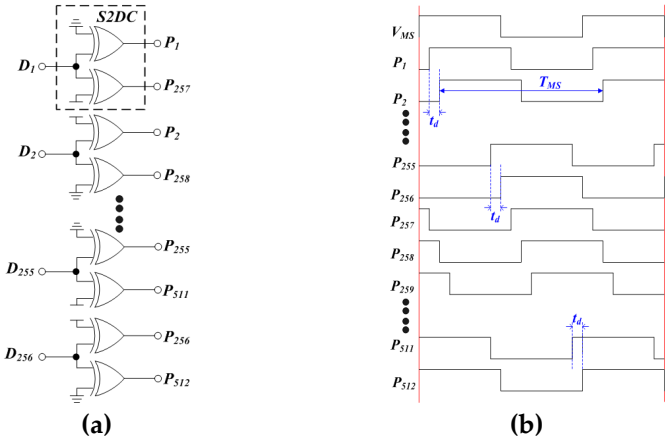

Figure 3. 256-S2DCs (a) Schematic. (b) Output waveforms.

The IFG consists of I/Q-multiplexers, I/Q-accumulators, an XOR, and an S2DC. All digital bits of A_9–A_1, Zy_9–Zy_1, and Zx_9–Zx_1 are programmable. After the DLL is locked, the accumulators add or subtract the input magnitude (A_9–A_1) from the previous values (Zy_9–Zy_1 or Zx_9–Zx_1). Depending on the accumulator output state of Y_9–Y_1 (or X_9–X_1), V_Q (or V_I) is switched to the P_M multiplexer input,

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where M is equal to the magnitude of Y_9–Y_1 (or X_9–X_1). For example, when the magnitude of Y_9–Y_1 = 1, V_Q is connected to P_1. V_Q and V_I drive the I/Q-accumulator's D-flip-flops (DFFs) and XOR gate of generating V_{IF}. Depending on a feedback clock control (C_{FC}) state, V_Q (or V_I) is connected to either the left or right accumulator's DFF. By applying the appropriate initial states of Zy_9–Zy_1 and Zx_9–Zx_1, the time delay between V_Q and V_I can be either $T_{MX}/4$ or $(T_{MX}/4)$–t_d. T_{MX} is the V_Q (or V_I) pulse period. The consequent V_{IF}'s fundamental frequency (f_{IF}) = $2\times f_{MX}$, where $f_{MX} = 1/T_{MX}$.

To visualize simple examples of how to vary f_{IF}, the multiplexer input phases are set to 16. As shown in Figure 4(a), P_1–P_{16} waveforms are uniformly delayed by t_d (= $T_{MS}/16$). When the magnitude (AC_M) of A_9–A_1 is programmed as 6, and V_Q (or V_I) is switched to the phase lead signal at its rising and falling edges, the shift of V_Q (or V_I) would follow as the sequence P_{16}, P_{10}, P_4, P_{14}, P_8, P_2, P_{12}, P_6, and P_{16}. By combining the sequence, the high and low state durations of V_Q are reduced by $6t_d$, which results in a 50% duty cycle $4t_d$ period pulse as indicated by the purple pulse at the bottom of Figure 4(a).

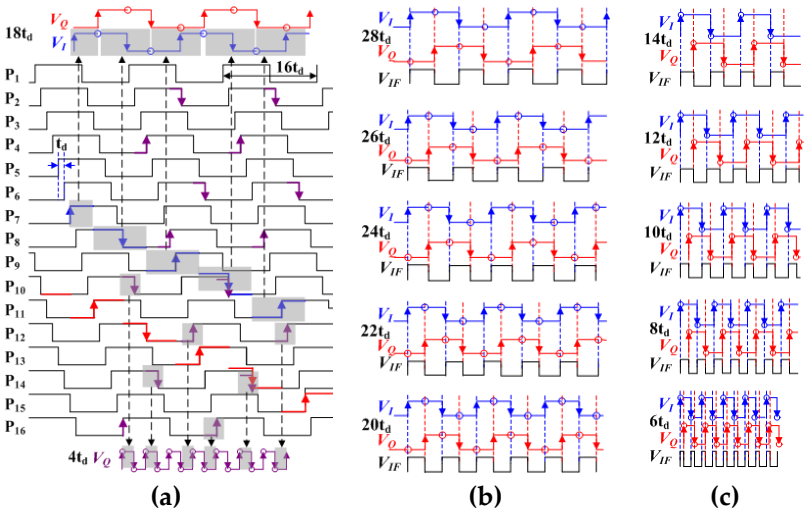

Figure 4. (a) P_1-P_{16}, V_Q and V_I ($18t_d$ period), and V_Q ($4t_d$ period) pulses. (b) V_Q, V_I, and V_{IF} pulses when AC_M = 2-6 and switching to phase lag. (c) V_Q, V_I, and V_{IF} pulses when AC_M = 1-5 and switching to phase lead.

Unlike the previous phase shift pattern, V_Q and V_I might be switched to the phase lag signal. In addition, V_Q might be updated by V_I, and V_I might be updated by V_Q. Figure 4(a) shows V_Q and V_I shift sequences (blue and red) when AC_M = 1. Initially, V_I and V_Q are connected to P_7 and P_{10}. V_Q is switched to P_{11} at the first rising edge of V_I, while V_I is switched to P_8 at the first rising edge of V_Q. The second phase shift of V_Q from P_{11} to P_{12} happens at the first falling edge of V_I. Moreover, V_I is switched to P_9 at the first falling edge of V_Q. By continuously updating in the just mentioned method, the phase shift sequence of V_I (V_Q) would be P_7 (P_{10}), P_8 (P_{11}), P_9 (P_{12}), P_{10} (P_{13}), and P_{11} (P_{14}). The final pulses of V_I and V_Q are 50% of the duty cycle and their period would be $18t_d$ because high and low state durations are increased to $9t_d$ at each rising and falling edge from $8t_d$.

Figure 4 (b) shows all waveforms of V_Q and V_I for AC_M = 2, 3, 4, 5, and 6 when V_Q and V_I are shifted to the phase lag signal. The waveforms of V_Q and V_I shifting to the phase lead signal waveforms for AC_M = 1, 2, 3, 4, and 5 are shown in Figure 4(c). All V_Q and V_I waveforms are 50% duty cycle pulses. However, V_{IF}s are 50% duty cycle pulses (Figure 5(a)) when the period of V_Q and V_I (T_{MX}) is $4t_d$, $8t_d$, $12t_d$, $16t_d$, $20t_d$, $24t_d$, and $28t_d$. Otherwise, the duty cycle (D_{cycle}) of V_{IF} would be expressed as

$$D_{cycle} = \frac{0.25T_{MX} \pm 0.5t_d}{0.5T_{MX}} = \frac{1}{2} \pm \frac{t_d}{T_{MX}}, \quad (1)$$

as shown in Figure 5(b). If t_d is reduced and T_{MX} is increased, the duty cycle offset (t_d/T_{MX}) would be close to zero.

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Considering the previous example (P_1–P_{16}), T_{MX} would be t_d × (512±2AC_M). Because T_{MS} = 512×t_d, T_{MS}/T_{MX} can be expressed as 512/(512±2AC_M). Therefore, f_{IF} can be derived as

$$f_{IF} = 2f_{MX} = 2f_{MS}\frac{512}{512 \pm 2AC_M}, \quad (2)$$

where AC_M can be programmed to any integer between 0-254. The proposed synthesizer output frequency can be expressed as

$$f_{RF} = RF_{FMF}f_{MS}\frac{1024}{512 \pm 2AC_M}, \quad (3)$$

where RF_{FMF} is the RFFM's FMF. Replacing AC_M as AC_M+1 in (3) and subtracting it from (3), RF channel resolution (Δf_{RF}) between AC_M and AC_M + 1 is expressed as

$$\Delta f_{RF} = RF_{FMF}f_{MS}\frac{2048}{(512 \pm 2AC_M)(512 \pm 2AC_M + 2)}. \quad (4)$$

The Δf_{RF} would be finer as the denominator of (4) is increased.

Applying f_{MS} = 156.25 MHz for AC_M = 1–254, the f_{IF} range is simulated as 156.86–311.28 MHz when V_I (V_Q) switches to the phase lag pulse. For V_I (V_Q) shifting to the phase lead pulse, the f_{IF} span will range from 313.73 MHz to 40 GHz. However, f_{IF} is intentionally limited to 311.28 MHz for a fine channel resolution in this paper. RF_{FMF} can be programmed as any even number among 12-32. By setting RF_{FMF} = 32 and AC_M = 1, f_{RF} will be 9.96 GHz. A 1.88 GHz f_{RF} can be generated by programming RF_{FMF} = 12 and AC_M = 254. The consequent Δf_{RF} range is 3.698 -38.609 MHz according to (4).

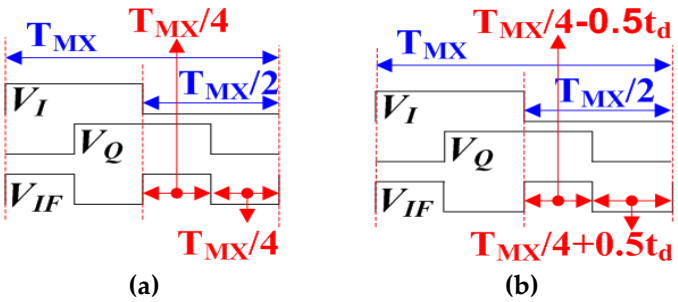

Figure 5. V_{IF}, V_I, and V_Q waveforms. (a) V_{IF} is 50% duty cycle. (b) V_{IF} are ±0.5t_d duty cycle offsets from the 50 % duty cycle.

2.2. Phase Noise Analysis and no Jitter Accumulation

The proposed synthesizer PN sources are shown in Figure 6, where θ_{XO}, θ_{PC}, and θ_{DL} are the PN spectral densities (PNSDs) of the reference clock, the PFD+CP, and the VCDL, respectively. K_{PC} (= $I_{cp}/(C_LS)$) and K_{DL} are the PFD+CP and VCDL gains. K_{SYN} is the total FMF from f_{ref} (= f_{MS}) to f_{RF} as shown in Figure 2. T_{MS} (= 1/f_{MS}) is much less than the DLL time constant such that exp(-ST_{MS}) = 1 [17]. Therefore, the proposed synthesizer output PNSD, θ_{SYN}, can be derived as

$$\theta_{SYN}(s) = \{\theta_{XO} + \theta_{PC}[H_l(s)]^2 + \theta_{DL}[H_h(s)]^2\}K_{SYN}^2, \quad (5)$$

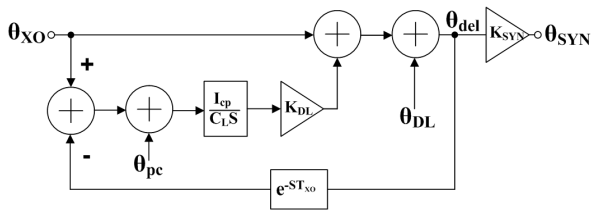

Figure 6. Phase noise sources of the proposed synthesizer.

where

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$$H_l(s) = \frac{I_{CP}K_{DL}}{I_{CP}K_{DL} + SC_L} \; and \;\; H_h(s) = \frac{SC_L}{I_{CP}K_{DL} + SC_L}. \quad (6)$$

According to (5), the proposed synthesizer has no low-pass filter effect on θ_{XO}. Therefore, the integrated rms jitter of θ_{XO} should be less than the target jitter such as 100 fs from 12 kHz to 20 MHz of the 28 GHz carrier frequency [18]. The target 100 fs integrated rms jitter is translated as 0.005625° at a 156.25 MHz crystal oscillator, which was stringent to achieve a decade ago. Fortunately, ultra-low jitter oscillator products have been recently released with a few hundred frequency range MHz. For example, SiT9501 yields a 70.629 fs rms jitter integrating a 12 kHz–20 MHz offset bandwidth when the operation frequency is 156.25 MHz.

As noted in (6), the noise transfer function (NTF) of the θ_{PC}, $H_l(S)$, is a low-pass filter (LPF). Unlike other synthesizers such as the CPPLL, SSPLL, and ILPLL, both values of I_{cp} and C_L can be freely selected because the presented DLL has no stability constraint. Therefore, the effect of θ_{PC} on the presented synthesizer output can be minimized by manipulating I_{cp} and C_L as much as possible. On the contrary, $H_h(S)$, the NTF of θ_{DL} is a high-pass filter (HPF) so that lower-frequency PN sources such as flicker noise would be filtered out.

While VCO output jitters in all other PLLs are accumulated until they are fixed by the reference clock as shown in Figure 7, the proposed synthesizer has no jitter accumulation because of no oscillator. Furthermore, a good design FM output's integrated jitter would be close to the input jitter. In contrast, a typical synthesizer's integrated jitter is severely degraded by a VCO out-band PN, particularly, for wide data bands.

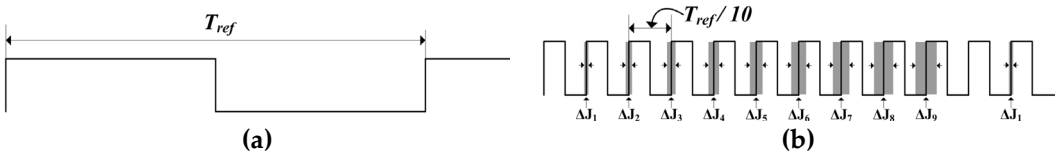

Figure 7. Clock waveforms of (a) Ideal reference. (b) Jitter accumulated VCO.

The absence of a loop stability constraint and VCO makes the proposed synthesizer provide a relatively wide output frequency range, comparable jitter, and a finer channel resolution than f_{ref}, compared with the state-of-the-art synthesizers proposed in recently published papers [19–23] and [28].

3. Design of the Proposed Synthesizer and Spur Analysis

3.1. Low Phase Noise PFD and CP

To operate a high-frequency phase synchronization, a true single-phase clocking (TSPC)-based PFD is implemented (Figure 8). Following the PN optimization design procedure described in [24], a small 40 ps on-time (T_L) is confirmed by simulations when 156.25 MHz input signals are locked.

Figure 9 shows the presented CP schematic with noise sources, which is the same topology described in [25]; however, BJTs are replaced by CMOS transistors. All channel current noises are included but all flicker voltage noises at the transistor (M_1–M_5) gates are omitted for simplicity. Because M_n and M_p are used for switches, their noise contributions are trivial. Most of the noises due to M_3–M_5 are filtered by R_{G1}–C_{G1} and R_{G2}–C_{G2} LPFs. The current noises of M_1 and M_2, $\overline{I_{M1}^2} = 4kT\gamma g_{m1}$ and $\overline{I_{M2}^2} = 4kT\gamma g_{m2}$ can be degenerated by R_{dn} and R_{dp}, respectively. However, some portions of R_{dn} and R_{dp} noises are added. Therefore, the equivalent current noise ($\overline{I_{m1-dg}^2}$) flowing through the M_1 channel is expressed as

$$\overline{I_{M1-dg}^2} = \frac{\overline{I_{M1}^2}}{(1 + R_{dn}g_{m1})^2} + \frac{4kTR_{dn}{g_{m1}}^2}{(1 + R_{dn}g_{m1})^2}. \quad (7)$$

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According to (7), the equivalent current noise would be close to $4kT/R_{dn}$ if $R_{dn}g_{m1}$ is big enough. As R_{dn} is increased, $\overline{I_{M1-dg}^2}$ is decreased. Therefore, the maximum possible R_{dn} must be used to minimize the equivalent current noise as long as guarantees an appropriate output tuning DC range.

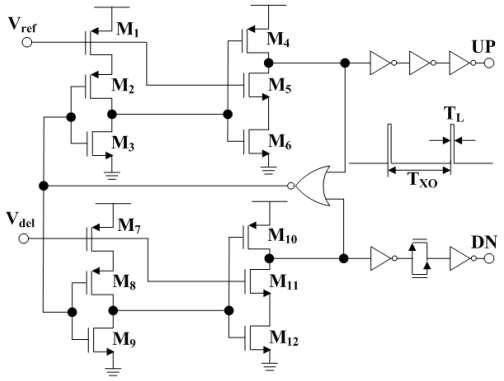

Figure 8. TSPC PFD schematic.

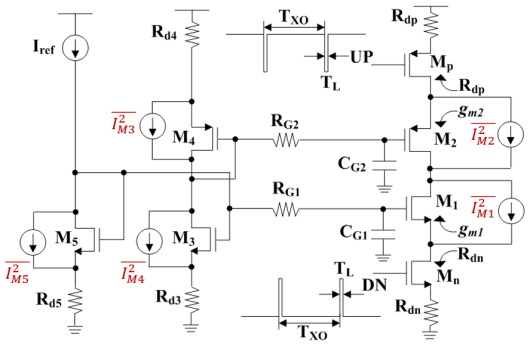

Figure 9. Charge pump schematic.

To secure the degeneration R_{dn} benefit, $\overline{I_{M1-dg}^2}$ should be less than $\overline{I_{M1}^2}$, which can be expressed as

$$\frac{4kTR_{dn}{g_{m1}}^2}{(1+R_{dn}g_{m1})^2-1} < \overline{I_{M1}^2}. \tag{8}$$

When $R_{dn}g_{m1} \gg 1$, (8) can be simplified as

$$\frac{1}{\gamma g_{m1}} < R_{dn}, \tag{9}$$

which defines the minimum required degeneration resistance to reduce the CP output noise due to $\overline{I_{M1}^2}$.

Moreover, the flicker noises of M_1 and M_2, $\overline{V_{M1}^2}$ and $\overline{V_{M2}^2}$, can be individually alleviated by $g_{m1}R_{dn}$ and $g_{m2}R_{dp}$. Consequently, the equivalent output current noise, $\overline{I_{nc}^2}$, can be expressed as

$$\overline{I_{nc}^2} = \overline{I_{ot1}^2} + \overline{I_{ot2}^2} + \overline{I_{of1}^2} + \overline{I_{of2}^2} + \overline{I_{or1}^2} + \overline{I_{or2}^2}, \tag{10}$$

where $\overline{I_{ot1}^2} = \overline{I_{M1}^2}\left(\frac{1}{1+g_{m1}R_{dn}}\right)^2$, $\overline{I_{ot2}^2} = \overline{I_{M2}^2}\left(\frac{1}{1+g_{m2}R_{dp}}\right)^2$, $\overline{I_{of1}^2} = \overline{V_{M1}^2}\left(\frac{g_{m1}}{1+g_{m1}R_{dn}}\right)^2$, $\overline{I_{of2}^2} = \overline{V_{M2}^2}\left(\frac{g_{m2}}{1+g_{m2}R_{dp}}\right)^2$, $\overline{I_{or1}^2} = \frac{4kTR_{dn}{g_{m1}}^2}{(1+R_{dn}g_{m1})^2}$ $\overline{I_{or2}^2} = \frac{4kTR_{dp}{g_{m2}}^2}{(1+R_{dp}g_{m2})^2}$.

Figure 10 shows the PN simulations of the PFD+CP when the degeneration resistance (both magnitude of R_{dn} and R_{pn}) is 62.5, 125, 250, 500, 1k, 2k, and 4k ohm. The smallest simulated PN at 1 kHz offset is –135 dBc/Hz which is 21 dB lower than that of SiT9501. However, the lowest PN at 10 kHz offset is –141dBc/Hz, which is close to that of SiT9501. Therefore, the DLL 3-dB loop bandwidth

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must be lower than 10 kHz to force the dominant in-band PN source for the proposed synthesizer to be the external reference clock. The best PN floor is -143 dBc/Hz.

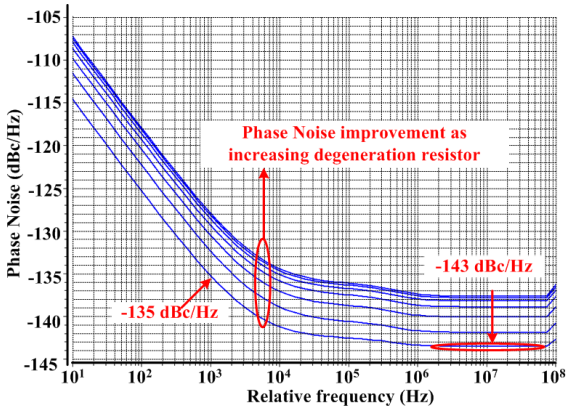

Figure 10. The proposed PFD+CP PN simulations increase R_{dn} and R_{dp} as 62.5, 125, 250, 500, 1000, 2000, and 4000 Ω.

3.2. Delay Unit

As shown in Figure 2, the VCDL is the chain of 256 DU cells. Each DU output drives DU input, but the last DU drives the inverter for a half-period lock. Therefore, to make all nodes (D_1–D_{256}) an identical capacitive load, the last DU should be different from the other DUs.

The DU schematic shown in Figure 11(a) is used for the first 255 DUs in the chain, which consists of two delay unit inverters (I_{DU}s), two varactors (V_{ar}s), and two 3-bit C_{bank}s. The DU output drives the multiplexer through the inverter buffer (I_B). Adding a dummy buffer inverter (I_B) at the DU_X node makes the same capacitive load for the DU_X and DU_{out} nodes. In addition, another dummy inverter (I_H) is applied to both DU_X and DU_{out} nodes, where I_H is the last DU's load inverter for the half-period lock shown in Figure 2. Figure 11(b) shows the last DU schematic. The only difference is that the dummy inverter (I_H) is replaced by I_{DU} at the DU_{out} node. Consequently, all nodes of the DU inverter (I_{DU}) in the VCDL have the same capacitive load, which leads to the same delay for each DU inverter. The reason for the 3-bit C_{bank} is to reduce K_{DL} to make the DU less sensitive to the power supply and delay line noises as well as to minimize the DU PN.

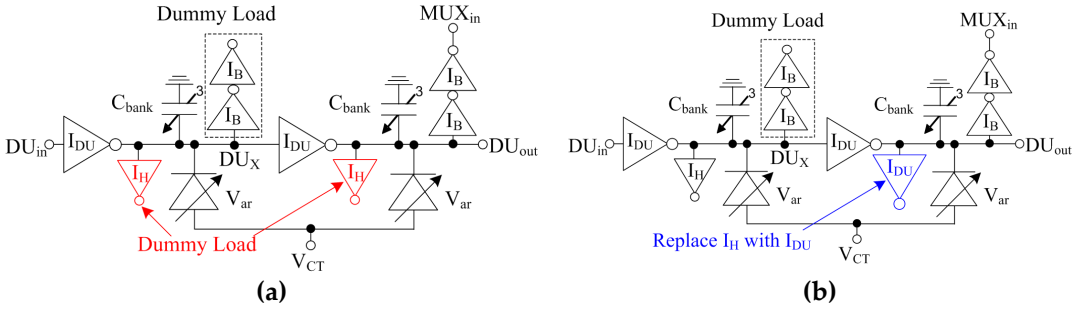

Figure 11. Proposed schematic. (a) The first 255 DUs. (b) The last DU in the VCDL DU chain.

The delay, D_T, from DU_{in} to DU_{out}, can be varied by adjusting the capacitance of V_{ar}, which is inversely proportional to the V_{CT} magnitude. Figure 12 shows the simulated D_T versus V_{CT} when two extreme process/temperature variations of FF/–20 ºC and SS/100 ºC are applied. The delay curves of FF/–20 ºC (blue) and SS/100 ºC (red) should be overlapped to overcome the variations of the ±3σ process and the −20 to 100 ˚C temperature range. The overlapped delay must include T_{MS}/512 to make DLL locked, which would be 12.5 ps when f_{MS} = 156.25 MHz. The V_{CT} node would converge to either 1.2 V or 0.9 V for both FF/-20 ºC/ '111' C_{bank} state and SS/100 ºC/ '000' C_{bank} state, respectively.

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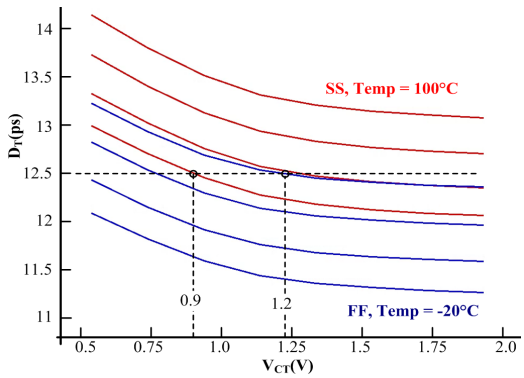

Figure 12. DU SS/100ºC and FF/−20ºC simulation.

The DU chain PN simulations on DU_{16}, DU_{32}, DU_{48}, DU_{64}, and DU_{80} outputs have been completed, as shown in Figure 13 (blue curves). Beyond the DU_{80} output, PN simulation cannot be accomplished owing to the convergence problem in Cadence. Therefore, PN beyond the DU_{80} output is induced by linearly expanding from the PN simulations on DU_{16}, DU_{32}, DU_{48}, DU_{64}, and DU_{80} outputs. The average PN degradations between DU_{X+16} and DU_X outputs for flicker and thermal noise regions are 1 and 0.25 dB, respectively. As a result of expansion, PN degradations of approximately 11 and 2.75 dB are estimated between DU_{256} and DU_{80} outputs (the red curve in Figure 13).

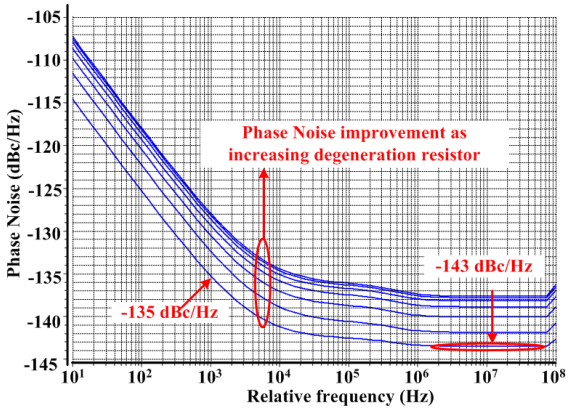

Figure 13. PN simulations on DU_{16}, DU_{32}, DU_{48}, DU_{64}, and DU_{80} (blue curves) and estimated PN curve (red) on DU_{256}.

The PN contribution of S2DC (Figure 3) is trivial so the PN on P_{512} is close to that on DU_{256}. Because V_Q or V_I in Figure 2 is continuously switched among P_1–P_{512}, the average PN on either V_Q or V_I is always better than that on P_{512}. Rather, the average PN for all possible pulses programming A_9–A1 would be close to the PN on P_{128}, where the estimated PN on P_{128} is approximately equal to 3 dB and 0.75 dB PN degradations from the P_{80} PN as shown in the black curve in Figure 13.

To prove the above statement, the jitter-added P_1–P_{16} pulses on rising and falling edges are shown in Figure 14(a). The single DU's jitter (J_1) is added on P_1. The jitter on P_2 would be double as $2J_t$, and $15J_t$ will be accumulated finally on P_{15}. However, the jitter on P_{16} is fixed by PFD+CP such that no jitter exists on P_{16}. For A_4–A_1 = 1, the period of V_{IF} is adjusted to $9t_d$ (the bottom in Figure 14(b)). The accumulated jitter at the rising edge of V_{IF} is varied as the sequence of $7J_t$, $8J_t$, $9J_t$, $10J_t$, $11J_t$, $12J_t$, $13J_t$, $14J_t$, $15J_t$, 0, J_t, $2J_t$, $3J_t$, 4Jt, 5Jt, and $6J_t$. Moreover, the accumulated jitter at the falling edge of V_{IF} is varied as the sequence of $11J_t$, $12J_t$, $13J_t$, $14J_t$, $15J_t$, 0, J_t, $2J_t$, $3J_t$, 4Jt, 5Jt, $6J_t$, $7J_t$, $8J_t$, $9J_t$, and $10J_t$. Therefore, the average jitter at both rising and falling edges of V_{IF} would be $8J_t$. When A_4–A_1 = 6 (the $14t_d$ period waveform in Figure 14(b)), the accumulated jitter sequence at the rising edge of V_{IF} would be $7J_t$, $13J_t$, $3J_t$, $9J_t$, $15J_t$, 5Jt, $11J_t$, and J_t. The jitter sequence at the falling edge of V_{IF} would be $14J_t$, $4J_t$, $10J_t$, 0, $6J_t$, $12J_t$, $2J_t$, and $8J_t$. The resulting accumulated average jitter would be $8J_t$ and $7J_t$ at the rising and falling edges of V_{IF}, respectively.

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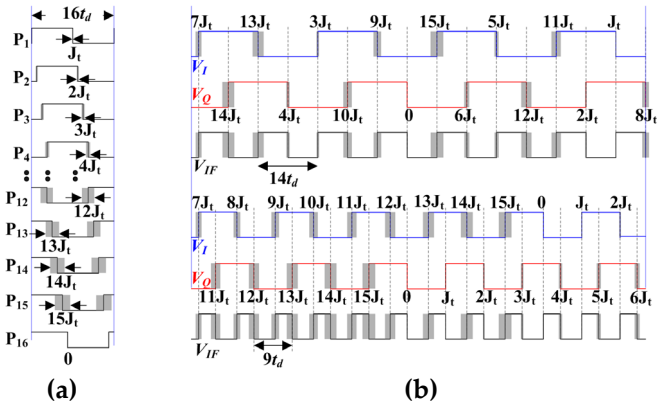

Figure 14. (a) Jitter added P1-P16 waveforms. (b) Jitter added VPSP VPSN, and VXOR pulses for 14t_d (top) and 9t_d (bottom).

3.3. Programmable RFFM

As shown in Figure 2, RFFM is composed of an HG, two buffers (BUFs), and a drive amplifier (DA). The proposed HG schematic is shown in Figure 15, which has been recently published in [25,26]. [26] has implemented it as a frequency quadrupler and [25] has applied it as a programmable FM for 8–16 FMF range. The HG in this paper has been optimized for the programmable 12–32 FMF range.

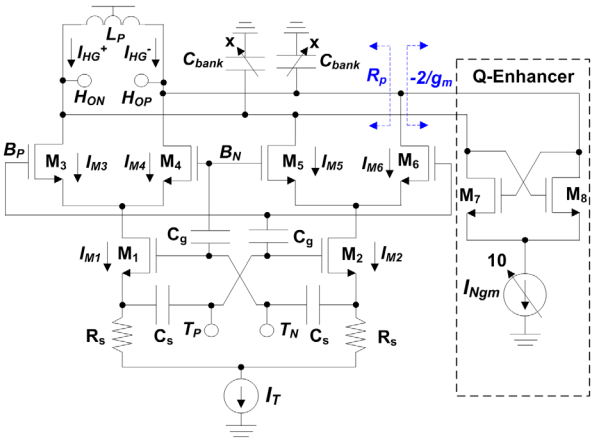

Figure 15. Harmonic generator schematic.

All the transistors of M1–M6 in Figure 15 are fully turned on and off periodically by applying enough amplitude at (T_P–T_N). Figure 16(a) shows the ideal HG's important internal voltage and current pulses. The corresponding output currents are illustrated in Figure 16(b). The delay time (T_w) between the differential signals of (T_P–T_N) and (B_P–B_N) is intentionally introduced by adjusting C_s and C_g. The current (I_{M4}) flows only for the duration of both T_N and B_N in the high state. Because $I_{M1} = I_{M3} + I_{M4}$, the high state pulse width of I_{M3} is T_w but that of I_{M4} is $T_{IF}/2 - T_w$, where $T_{IF} = 1/f_{IF}$. Similarly, I_{M5} and I_{M6} can be generated by applying the complementary pulses (T_P and B_P) of (T_N and B_N). The fundamental frequency of I_{M3}–I_{M6} is still f_{IN} (= $1/T_{IN}$), but their summation (I_{HG^+} and I_{HG^-}) fundamental frequency is 2×f_{IN}. Figure 16(b) shows the HG differential current ($I_{HG^+} - I_{HG^-}$) pulse (purple), which would provide strong even current harmonics.

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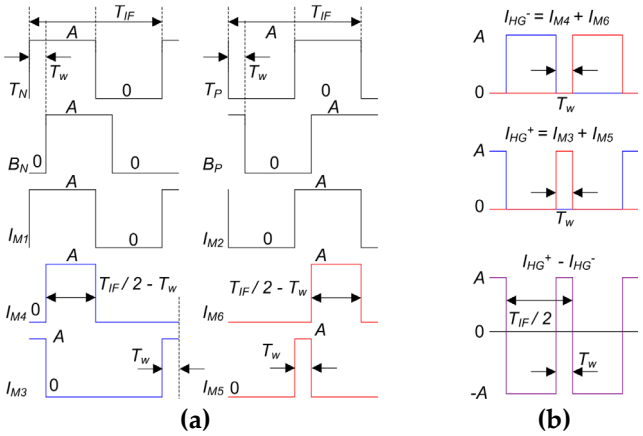

Figure 16. Proposed HG ideal. (a) Internal voltage and current pulses. (b) Single and differential output current pulses.

According to (2), f_{IF} is equal to f_{MS}×(1024/1020) by programming AC_M as 254. Since f_{MS} is 1/(512×t_d), the corresponding period of V_{IF} would be 510×t_d. When t_d is 12.5-ps, the V_{IF} period is 6.375-ns and the period of ($I_{HG}^+ - I_{HG}^-$) is 3.1875-ns. Figure 17(a) shows the 3.1875-ns fundamental period pulse with a 20-ps pulse width, 20-ps rising delay, and 20-ps falling delay. Its power spectrum is also shown in Figure 17(b). The power difference between 0.3137 and 10.04 GHz is only 2.8 dB, which means that the power is more balanced and distributed over a 0.3–10 GHz frequency band compared with a 50 % duty cycle pulse.

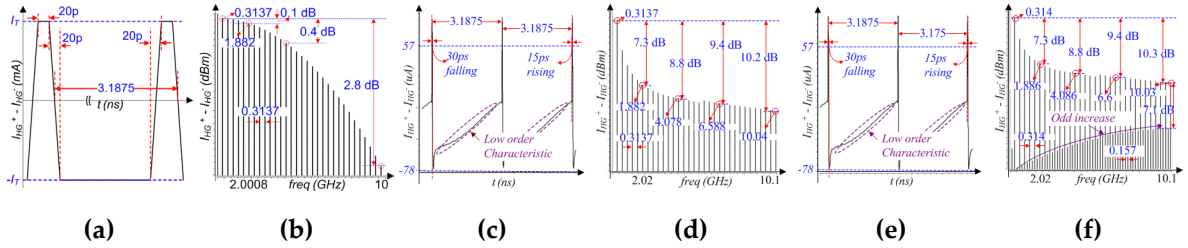

Figure 17. Ideal ($I_{HG}^+ - I_{HG}^-$). (a) Pulse. (b) Spectrum. For AC_M = 254, simulated ($I_{HG}^+ - I_{HG}^-$). (c) Pulse. (d) Spectrum. For AC_M = 253, simulated ($I_{HG}^+ - I_{HG}^-$). (e) Pulse. (f) Spectrum.

Unfortunately, the ideal current pulse of the above example cannot be produced because all active devices have limited bandwidth. Instead, it is more likely to draw the differential output current ($I_{HP}^+ - I_{HP}^-$) as shown in Figure 17(c), which is the simulation result when AC_M is set to 254. Figure 17(d) shows the Fourier transform of ($I_{HP}^+ - I_{HP}^-$). Because of the slew rate, the low-order harmonic characteristic would be expressed as highlighted with the purple dotted ellipse, which leads to more power concentration on 2×f_{IF}, 4×f_{IF}, and 6×f_{IF}. Consequently, the power spectrum difference between those at the lowest and the highest harmonics is now 10.2 dB, which is 7.4 dB bigger than that of the ideal ($I_{HP}^+ - I_{HP}^-$) spectrum. However, the power spectrum difference between those at 1.882 and 10.04 GHz is 2.9 dB, which is only 0.2 dB bigger than that of the ideal pulse (2.7 dB power difference between those at 1.882 GHz and 10.04 GHz as shown in Figure 17(b)). As shown in Figure 15, the wanted high-order current harmonic can be conserved by programming the resonant frequency of parallel L_P and C_{bank}. The corresponding HRR performance would be much better than the HRR when the output current is a 50 % duty cycle pulse.

When AC_M is programmed as 253, the duration difference between the low and high states of V_{IF} would be t_d, as described in Figure 5(b). Consequently, the differential output current ($I_{HP}^+ - I_{HP}^-$) is the sequence of 3.1875-ns and 3.175-ns periods as shown in Figure 17(e). Its spectrum appears to be close to that shown in Figure 17(d), but the noticeable adjacent harmonic happens at ±f_{IF} around the wanted harmonic. As shown in Figure 17(f), odd harmonics appear as 3×f_{IF}, 5×f_{IF}, ..., and 33×f_{IF}. The odd harmonic power is increased as frequency is increased. The worst adjacent harmonic rejection

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ratio (HRR) is 7.1 dB between the power levels at 10.03 and 10.187 GHz. Each DU's delay (t_d) would be decreased as the number of DU is increased, which leads to the power spectrum reduction of odd harmonics.

The proposed HG L_P-C_{bank} output load schematic is shown in Figure 18(a), where M_1–M_x act as digitally controllable switches. R_{LP} is the equivalent parallel parasitic resistor of the inductor (L_P). The output load capacitor of summing all parasitic capacitors due to M_3–M_8 in Figure 15 and the following building block input capacitor is expressed as C_{PR}. The sizes of C_x and M_x are binary-weighted.

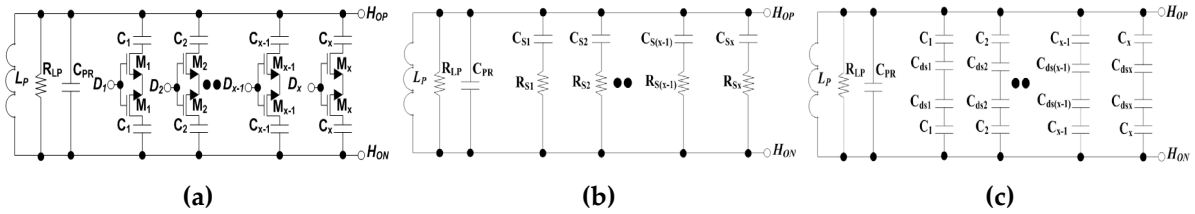

Figure 18. (a) HG output L_P-C_{bank}. (b) Equivalent parallel L_P-C_{bank}. (b) When all M_1–M_{10} are turned on. (c) When all M_1-M_{10} are turned off.

The minimum sizes of C_1 and M_1 are intentionally used to attain a wide tuning range and fine resonant frequency resolution, which results in implementing 9.64-fF C_1 and 200-nm (width)-60-nm (length) M_1 in the 65-nm CMOS technology. Figure 18(b) and Figure 18(c) show the equivalent L_P-C_{bank} circuitries when all M_1–M_x are turned on and off, respectively. C_{S1} is the equivalent capacitance of two C_1s in series and is equal to $C_1/2$. However, $R_{S1} = 2 \cdot R_{ON1}$, where R_{ON1} is the turn-on resistance of the M_1 switch. C_{ds1} is the parasitic capacitance between the drain and the source of the turned-off M_1.

When all switches are turned off, the highest resonant frequency can be expressed as

$$f_{rs-max} = \frac{1}{2\pi\sqrt{L_P(C_{PR} + \sum_{k=1}^{x} C_{OFFk})}}, \tag{11}$$

where

$$C_{OFFk} = \frac{C_{Sk}C_{dsk}}{2(C_{Sk} + C_{dsk})}. \tag{12}$$

The corresponding equivalent parallel resistance would be close to R_{LP}.

On the contrary, the lowest resonant frequency occurs when all M_1–M_x are turned on. Therefore, it can be expressed as

$$f_{rs-min} = \frac{1}{2\pi\sqrt{L_P(C_{PR} + \sum_{k=1}^{x} C_{Pk})}}. \tag{13}$$

C_{Pk} is transformed from C_{Sk} as the following equation:

$$C_{Pk} = C_{Sk}\frac{Q_C^2}{1+Q_C^2}, R_{Pk} = R_{Sk}(1+Q_C^2), \tag{14}$$

where $Q_C = Q_S$ $(=1/\omega C_{Sk}R_{Sk}) = Q_P$ $(=\omega R_{Pk}C_{Pk})$ and R_{Pk} is the transformed resistor. The corresponding equivalent parallel resistor ($R_{P\text{-}min}$) would be

$$R_{P-min} = \frac{R_{LP}}{\left[1 + R_{LP}\sum_{k=1}^{x}\left(\frac{1}{R_{Pk}}\right)\right]}, \tag{15}$$

which is the minimum resistance at the lowest resonant frequency.

To achieve the target output frequency band, $f_{rs\text{-}max}$ in (11) should be bigger than 10 GHz but $f_{rs\text{-}min}$ in (13) should be less than 2 GHz. The ratio of (11) to (13) should be greater than five and can be derived as

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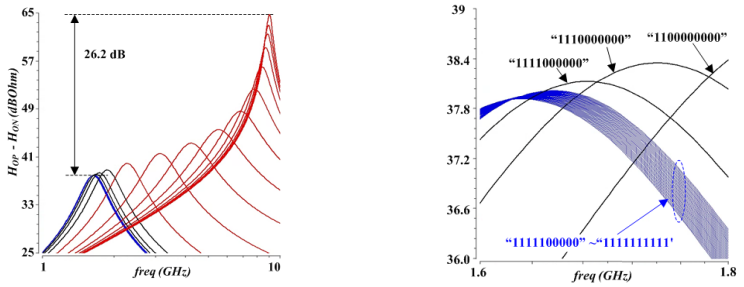
$$\frac{f_{rs-max}}{f_{rs-min}} = \sqrt{\frac{C_{PR} + \sum_{k=1}^{x} C_{Pk}}{C_{PR} + \sum_{k=1}^{x} C_{OFFk}}} > 5. \quad (16)$$

As C_{Pk} is binary weighted, that is $C_{Px} = 2\times C_{P(x-1)} = \ldots. = 2^{(x-2)} \times C_{P2} = 2^{(x-1)} C_{P1}$, so is C_{OFFk}, (16) can be rewritten as

$$\frac{C_{PR} + (2^x - 1)C_{P1}}{C_{PR} + (2^x - 1)C_{OFF1}} > 25 \quad (17)$$

By inserting C_{PR}, C_{P1}, and C_{OFF1} as 68-fF, 4.6585-fF, 0.09675-fF (confirmed by simulations) results in $2^x > 356$. Therefore, the minimum number of C_{bank} bits, x, is 9. Inserting x in (11) as 9 leads to 2.159-nH L_P for 10 GHz f_{rs-max}. By applying L_P = 2.159-nH in (13), f_{rs-min} becomes 2.191 GHz. Trying x = 10 in (11) to get 10 GHz (f_{rs-max}) results in 1.517-nH L_P. The corresponding f_{rs-min} is 1.859 GHz, which adheres to the initial output frequency target range of 2–10 GHz.

The AC simulations (TT-process and 25 ˚C) are shown in Figure 19(a). The impedance dB difference between the highest and lowest resonant frequencies is 26.2 dB. The red curves are simulation results when the C_{bank} states are "0000000000", "0000000010", "0000000100", ..., and "1000000000". The blue curves represent simulation results for programming the C_{bank} states from "1111100000" to "1111111111" in integer one step. The magnified curves from 1.6 GHz to 1.8 GHz are shown in Figure 19(b).



(a) (b)

Figure 19. HG differential output ($H_{OP} - H_{ON}$) impedance simulations. (a) TT process at 25°C. (b) Zoomed simulations.

The 26.2 dB output impedance variation can be compensated by adding a negative-g_m pair (M_7–M_8 inside a Q-enhancer dotted rectangular in Figure 15). By setting $KR_P = 2/g_m$, the equivalent parallel impedance, R_{EQ}, of R_P and $-2/g_m$ is derived [25] as

$$R_{EQ} = \left(\frac{K}{K-1}\right) R_P, \quad (18)$$

where g_m is the transconductance of M_7 and M_8. If $g_m < 2/R_P$ and $K > 1$, it leads to no oscillation owing to the positive feedback pair of M_7–M_8. The tail current of the negative-g_m pair (I_{Ngm} in Figure 15) can be appropriately adjusted by 10-bit digital control bits such that all HG output impedances at the wanted resonant frequencies can be equalized close to 65 dBOhm.

Figure 20(a) shows process corner simulations at 27 °C. Nine different AC simulations on the HG output for SS (red), TT (black), and FF (blue) processes at the highest, amid, and lowest resonant frequencies are plotted. As expected, the impedance magnitudes at the lowest are about 26.2 ~ 30.3 dB lower than those at the highest. The impedances at the lowest and amid are equalized close to 65 dBOhm by applying I_{Ngm} properly as shown in Figure 20(b). The gap frequency between the lowest FF and the highest SS processes is 2–10 GHz, which might be defined as the synthesizer output frequency band overcoming ±3σ process variations.

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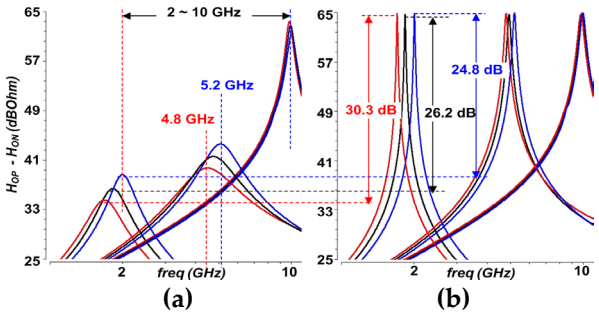

Figure 20. HG differential output ($H_{OP} - H_{ON}$) AC simulation for FF, TT, and SS processes. (a) Without negative-g_m. (b) With negative-g_m compensation.

To further improve the HRR performance of the RFFM, the HG is followed by two buffers (BUFs) whose schematic is shown in Figure 21. The BUF core is a parallel connection of a differential cascade buffer and a negative-g_m pair. The output load of L_P-C_{bank} is the same as that of the proposed HG. As proven in [25,26], an automatic constant amplitude control loop (ACACL) not only prevents it from oscillation but also maintains the constant output amplitude for the best performance of the following blocks. The negative-g_m pair plays the main role of the ACACL. The output amplitude is detected by a peak detector. If peak magnitude $V_{PK} > V_R$, the negative-g_m pair current is reduced to make its g_m lower. According to (18), the equivalent impedance (R_{EQ}) would be reduced because K is increased. Therefore, the BUF output magnitude would be decreased. On the contrary, the BUF output amplitude would be increased when $V_{PK} < V_R$. The negative-g_m pair current is varied until V_{PK} converges to V_R.

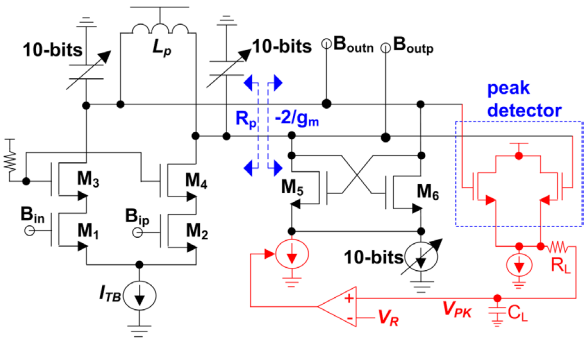

Figure 21. Schematic of a buffer with an ACACL.

3.4. Adjacent HRR Simulation and Analysis

When the MASH 1-1-1 ΔΣ modulator is applied to the feedback path of a classical fractional-N PLL (CFNPLL), the CFNPLL's total division (N) is not fixed. Instead, N keeps changing to any integer number between N-3 and N+4. The average N over a relatively long duration can be expressed as a fractional number as N + (K/M), where K and M are integers. This is the reason causing fractional spurs. In contrast, f_{IF} is the product of a fixed fractional number and f_{MS} because AC_M in (2) does not vary. Therefore, there are no fractional spurs.

Even though every I_{DU} output has the same capacitive load as shown in Figure 11, each DU in the VCDL might have a different delay because of a mismatch. Similar to an MDLL, any mismatch among DUs directly translates into a duty cycle error of V_{IF} (Figure 2). The duty cycle error causes odd harmonics in addition to even harmonics of f_{IF} like the spectrum shown in Figure 17(f). Therefore, the worst HRR often happens at the ± f_{IF} offset from the wanted harmonic.

The output L_P-C_{bank} loads of the HG and BUF are identical and would be expressed as a parallel of R_{EQ}, L_P, and C_P equivalently for all C_{bank} states. The corresponding HRR (dB) at ± $\Delta\omega$ from the resonant frequency ω_0 can be derived as

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$$HRR_{\pm\Delta\omega}\big|_{dB} = 20\log(R_{EQ}) + 10\log\left(\frac{1}{R_{EQ}^2} + W^2\right), \tag{19}$$

where

$$\mathrm{W} = \frac{1}{\omega_0 \pm \Delta\omega} - (\omega_0 \pm \Delta\omega). \tag{20}$$

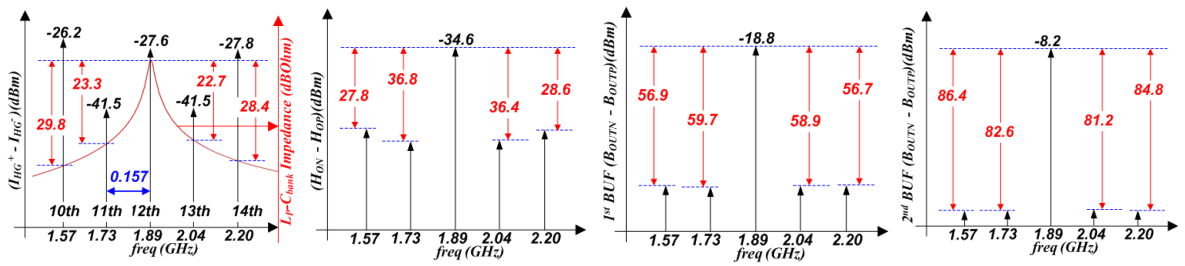
For all C_{bank} states, R_{EQ} is maintained close to 65 dBOhm by adjusting the negative-g_m pair current as shown in Figure 20(b).

As expected from (2), f_{IF} = 157.17 MHz when AC_M = 253. L_P-C_{bank} is programmed to resonate at the 12th harmonics of f_{IF} to distinguish 1.886 GHz (≈ 12×157.17 MHz). Recalling Figure 17(f), the dominant adjacent spurious tones of ($I_{HP^+} - I_{HP^-}$) are located at the 10th and 14th harmonics, and their HRRs of the 12th harmonic are –1.4 and 0.2 dB, respectively. Furthermore, there are noticeable spurious tones at $\pm f_{IF}$ offsets due to the sequence of 3.1875-ns and 3.175-ns periods of ($I_{HP^+} - I_{HP^-}$) as shown in Figure 17(e). The HRR at the 11th and the 13th harmonics of the 12th harmonic are identical and easily calculated as 13.9 dB (= −27.6 + 41.5).

The HG differential output current ($I_{HP^+} - I_{HP^-}$) is filtered by the L_P-C_{bank}. By simply applying $\omega_0 = 2\pi$ (12×157.17 MHz) in (19), the HRRs are calculated as 29.8, 23.3, 22.7, and 28.4 dB at $\pm 2\pi\times f_{IF}$ and $\pm 4\pi\times f_{IF}$ offsets. If the HG is perfectly linear, the HRRs of ($H_{ON} - H_{OP}$) at the 10th, 11th, 13th, and 14th harmonics should be 28.4 dB (= 29.8 – 1.4), 37.2 dB (= 23.3 + 13.9), 36.6 dB (= 22.7 + 13.9), and 28.6 dB (= 28.4 + 0.2), respectively.

Figure 22(a) shows the simulated spectrum of ($I_{HP^+} - I_{HP^-}$) along with the L_P-C_{bank} load impedance (red curve) resonated at the 12th harmonic of f_{IF} when AC_M is programmed as 253. The HG output spectrum simulation is shown in Figure 22(b). The simulated HRRs are 27.8, 36.8, 36.4, and 28.6 dB, which is degraded compared with the estimation. The HRR degradation is due to the HG nonlinearity emphasized in [26]. The simulated output harmonics of the 1st and 2nd BUFs are shown in Figure 22(c) and Figure 22(d). There are also HRR degradations due to the BUF nonlinearity.

The simulated 2nd BUF output harmonics for AC_M =127 and AC_M = 1 are individually shown in Figure 23(a) and Figure 23(b). Their f_{IF}s are 0.209 GHz and 0.3111 GHz, and their resonant frequencies are tuned to the 28th and 32th harmonics, respectively. Considering Figure 22(d) and Figure 23, it degrades HRR performance as the resonant frequency is increased. This is exactly the expected result because increasing C_P while maintaining R_{EQ} and L_P to reduce the resonant frequency results in improving the quality factor of parallel R_{EQ}-C_P-L_P.



(a) **(b)** **(c)** **(d)**

Figure 22. For AC_M = 253. (a) ($I_{HG^+} - I_{HG^-}$) spectrum. (b) HG output spectrum. (c) First BUF output spectrum. (d) Second BUF output spectrum.

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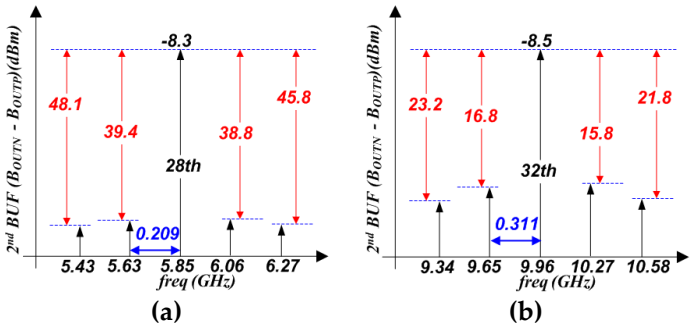

Figure 23. The second BUF output spectrum. (a) AC_M = 127. (b) AC_M = 1.

4. Fabrication and Measurement

The proposed synthesizer is fabricated in a 65-nm CMOS technology and its active die size is approximately 0.6 mm² as shown in Figure 24 (yellow-dotted box). Almost 35 % of the die area is occupied by the 512-phase DLL (blue-dotted boundary), and the RFFM occupies roughly 40 % (red-dotted boundary). The last 15 % of the active die area is for the IFG (purple-dotted boundary). The total die area is 1 mm² including central reference current, SPI, IQ-offset, and I/O pads.

As described in [27], about 42 dB substrate isolation within 100-μm apart two points with only one 30-μm width guard ring is reported. Since each building block has a wider than 30-μm guard ring width in Figure 24, the substrate isolation within 100-μm apart would be expected to be more than 42 dB due to multilateral isolations. This is why we try to assign separate power supply, ground, and guard ring (GR) for each building block as much as possible even though GR occupies an extra die area.

Three separate pairs of power supply and ground are allocated for the building blocks in the 512-phase DLL. The power supply voltage is 2.5 V for the PFD+CP to obtain enough headroom. However, the power supply voltage for VCDL and the 256-S2DC is 1.2V for the smallest die area and the lowest average power consumption in the 65-nm process. There is no level shifter required between the CP and VCDL because the CP drives the DU's varactor, whose maximum potential difference can be bigger than 2.5 V. Each pair of power supply and ground is separated by an individual GR, preventing mutual interference with one another.

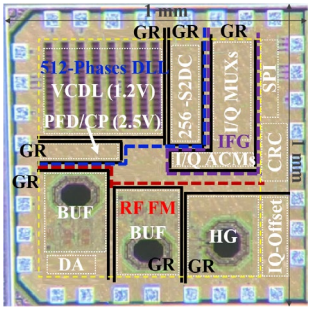

Figure 24. Photograph of the proposed synthesizer.

The IFG has one pair of power supply and ground for its building blocks of I/Q-multiplexers and I/Q-accumulators and has wide a GR to prevent especially the reference clock harmonics (N×f_{ref}) from interfering.

A separate pair of 1.2 V power supply and ground is individually applied for the HG and the BUFs in the RFFM because the mutual interferences through the power supply and ground are so sensitive to the HRR performance. While the DA shares the ground with the 2nd BUF, the DA power supply is separated from the BUF power supply to distinguish the DA power consumption from that of the BUF.

The laboratory test environment is shown in Figure 25. An external MEMS differential oscillator (SiT9501) is used as a 156.25 MHz reference clock, and its integrated rms jitter from 12 kHz to 20 MHz is as low as 70.629-fs according to the datasheet. Applying a Keysight E3631A as the power supply,

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the fabricated chip can be evaluated by programming the CPU to control the device under test through SPI. A Keysight E4446A spectrum analyzer measures the presented synthesizer output.

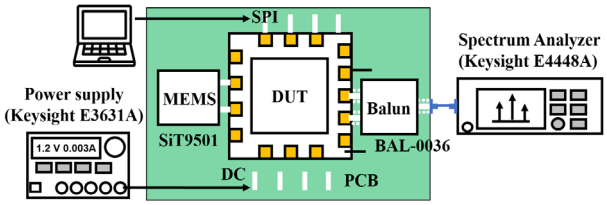

Figure 25. Test environment block diagram.

The proposed synthesizer consumes 15 mW. More than 50 % of the total power consumption is allocated to the 512-phase DLL. Even though they are digital circuitries, the average power consumption of the VCDL is approximately 35 % of the total power consumption to perform low PN. However, the 256-S2DCs power consumption is 15 % because it is less sensitive to PN contribution. The power consumption of PFD+CP is 5%. The IFG and RFFM power consumptions are 1.3 and 6.2 mW, respectively. The power consumption of each building block is summarized as shown in Figure 26.

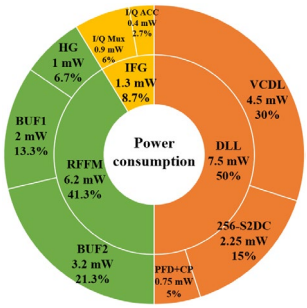

Figure 26. Test environment block diagram.

As mentioned in Section I, the proposed synthesizer is the first building block of the recent cascade LO chain for a 5G+ wireless communication system. Therefore, the synthesizer will drive the mmWave FM, whose impedance is normally bigger than 50 Ω. For only driving 50 Ω, a simple differential push-pull topology DA for wideband output matching is integrated. As shown in Figure 27, the DA is matched to 50 Ω through external balun (BAL-0036) and two cascade stages of the C-L-C pi-match. Figure 28(a) shows the simulation plot of the DA output (V_{OUT}) versus input (V_{IN}). The DA power gain is 9.5 dB and the output 1-dB compression point (OP1dB) is 1.6 dBm when it consumes 6 mW, which is enough to set the -8 dBm balun output without causing the significant signal distortion by the DA.

Five sample chips (Chip#1–Chip#5) have been mounted on a PCB by chip-on-board and successfully tested for evaluating performances. The DA output is placed as close to the PCB pad as possible so that the bonding wire inductor (0.35 nH L_{BW} in Figure 27) would be the smallest. Figure 28(b) shows the S22 measurements of the sample chips, whose worst S22 is less than −10 dB for the target measurement frequency band of 1.8–10 GHz.

The C_{bank} magnitude of programming the resonant frequency would be shifted over the process variation. Therefore, the auto-calibration of C_{bank} is required to promote an efficient mass production yield. Figure 29 shows the proposed calibration block diagram. As soon as calibration starts, all building blocks are turned off, except those highlighted in the shaded boxes of the digital 256-FD, digital 4096-FD, CMOS differential-to-single (D2S), and the negative-g_m pair of the second BUF. Applying enough current of I_{ng} forces the positive feedback to oscillate, and its frequency, f_{osc}, can be expressed as

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$$f_{osc} = 1/2\pi\sqrt{L_P(C_P + C_{pa})}, \tag{21}$$

where C_{pa} is the all-parasitic capacitance between v_p and v_n. C_P is expressed as

$$C_P = \sum_{k=1}^{10}\left(D_k C_{Pk} + \overline{D_k} C_{OFFk}\right). \tag{22}$$

D_k and $\overline{D_k}$ are complement binary bits. C_{OFFk} and C_{Pk} are defined in (12) and (14). f_{osc} is down-converted to CK_B by 4096-FD and 2048-FD, and the external MEMS frequency, f_{MS}, is down-converted to CK_{MS} by 256-FD. The counter output in the CPU is updated at the CK_{MS} rate for the CK_B period. The final counted value, $Cal_{1\text{-}12}$, for each C_{bank} state is stored in a look-up table.

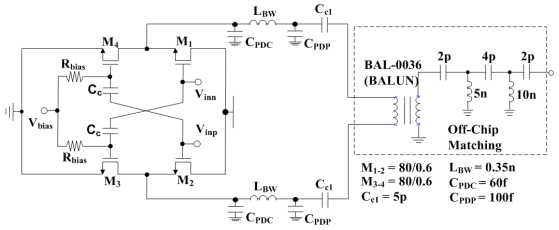

Figure 27. Driver amplifier with external output matching.

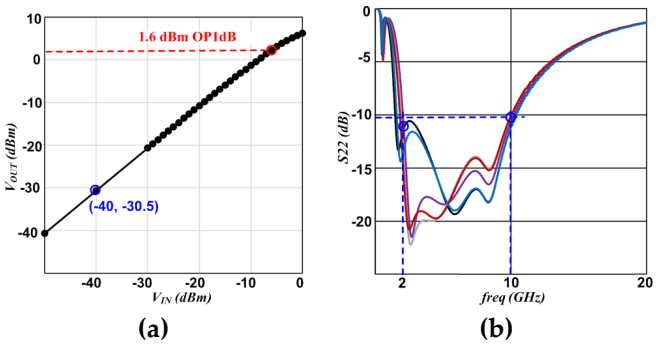

Figure 28. DA. (a) OP1dB simulation. (b) S22 measurements of chip#1 ~ chip#5.

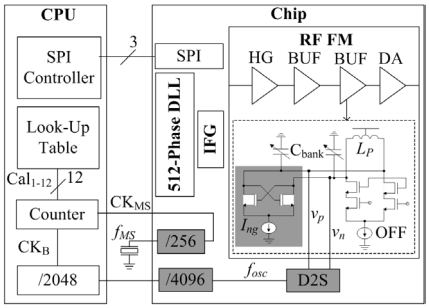

Figure 29. Capacitor bank (C_{bank}) calibration block diagram.

Unfortunately, the CMOS D2S would be a complicated topology to handle the wide frequency band of 1.8–10 GHz, which leads to a huge die area. Therefore, the calibrated frequency band is limited up to 2.2 GHz to minimize the D2S die area.

Table 1 shows the calibrated Cal_{12}-Cal_1 magnitudes in decimals (Cal_{dec}) when the C_{bank} states are intentionally set to oscillate at approximately 2.0, 2.05, 2.10, 2.15, and 2.20 GHz for Chip#1. The oscillation frequency can be estimated from the calibrated Cal_{dec} as

$$f_{c-osc} = \frac{(2048)(4096)}{(256)Cal_{dec}} f_{MS}. \tag{23}$$

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Figure 30 shows the graph of the frequency difference (Δf_{osc}) between measured (f_{osc}) and calibrated ($f_{c\text{-}osc}$) frequencies versus f_{osc} for all five test chips. The maximum frequency deviation is less than 0.2 % (= 2MHz / 2GHz × 100%), meaning all the tested five chips have an approximately equal C_{bank} value.

Table 1. Counter Output.

C_{bank}	Cal_{12}-Cal_1 Magnitude in decimal (Cal_{dec})				
D_{10}-D_1	Chip#1	Chip#2	Chip#3	Chip#4	Chip#5
1101010101	2561	2562	2561	2560	2560
1100101011	2499	2498	2499	2499	2499
1100000101	2400	2400	2439	2438	2439
1011100001	2382	2383	2382	2382	2383
1011000000	2328	2328	2328	2329	2327

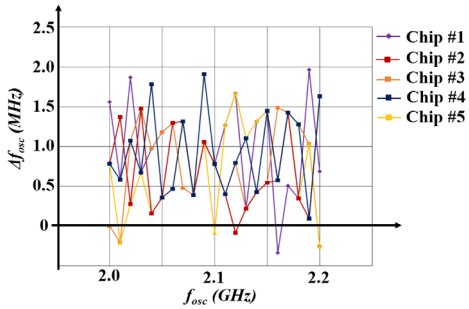


Figure 30. Oscillating frequency calibration error.

Assuming that the L_P-process variation is trivial and that all capacitances are changed linearly in the same direction over process variations, (21) can be rewritten as

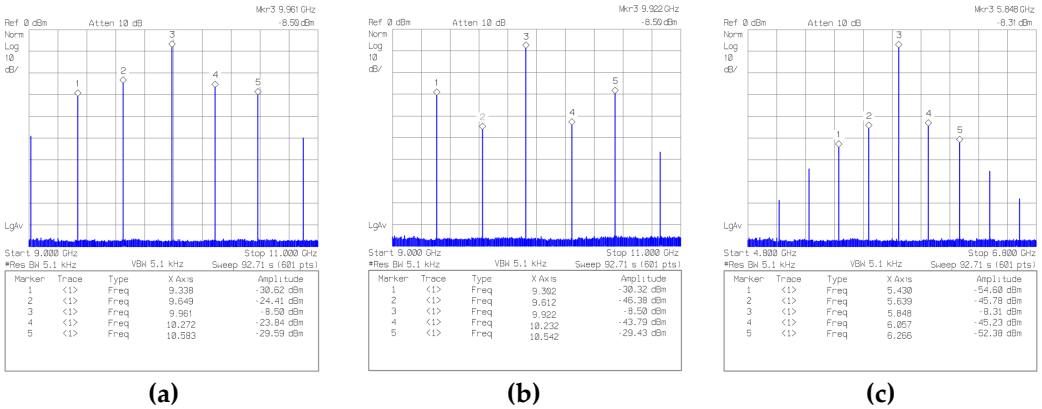
$$f_{c-osc} = {}^{1}\Big/{}_{2\pi\sqrt{L_P\alpha_C(C_{P-TT}+C_{pa-TT})}}. \tag{24}$$

The capacitive process coefficient(α_C) can be calculated by deriving (24) as

$$\alpha_C = \frac{1}{4\pi^2 f_{c-osc}^2 L_P (C_{P-TT}+C_{pa-TT})}, \tag{25}$$

where $C_{P\text{-}TT}$ and $C_{pa\text{-}TT}$ are the capacitances at the TT process. Therefore, α_C represents how much the capacitance deviates from that at the TT process. If α_C is bigger than 1.2, the tested chip is close to the SS process. On the contrary, it is close to the FF process if α_C is smaller than 0.8. Using α_C the required SPI C_{bank} state of the resonant frequency greater than 2.2 GHz can be estimated.

The output spectral measurements for Chip#1, when ACM is programmed as 1, 2, 127, 128, 253, and 254, are shown in Figure 31. The output frequency range is 1.882–9.961 GHz, which is close to the simulated range of the TT process.



(a) **(b)** **(c)**

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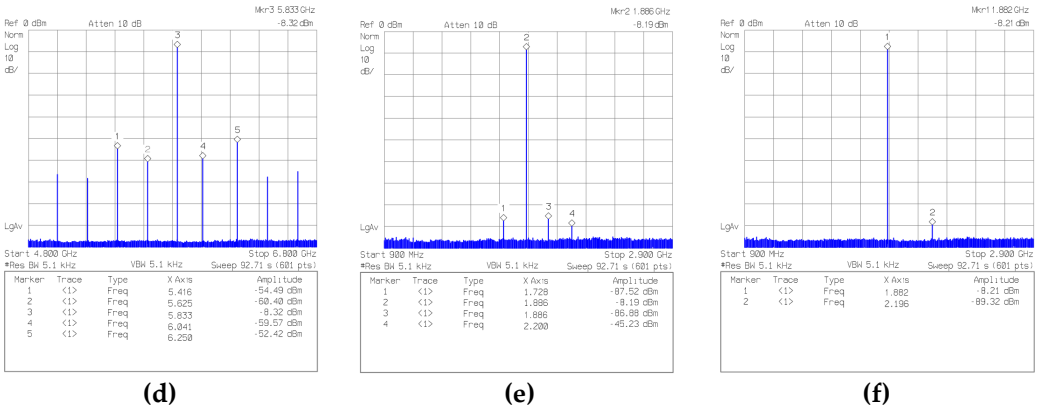

Figure 31. The synthesizer output spectrum waveform. (a) AC_M =1 and RF_{FMF} =32. (b) AC_M =2 and RF_{FMF} =32. (c) AC_M =127 and RF_{FMF} =28. (d) AC_M =128 and RF_{FMF} =28. (e) AC_M =253 and RF_{FMF} =12. (f) AC_M =254 and RF_{FMF} =12.

The worst adjacent HRRs happen when AC_M = 1 (Figure 31(a)) and AC_M = 2 (Figure 31(b)) resonating with the L_P-C_{bank} on the 32nd harmonic of f_{IF}. Unlike the HRR for AC_M = 1, the dominant HRR when AC_M = 2 happens at ±2×f_{IF} because the duty cycle offset of V_{IF} is zero. Nonetheless, there are noticeable spurious tones at ±f_{IF} from the wanted harmonic. The main cause of these spurious tones is the HG differential mismatches. Intentionally introducing the current mismatch between the positive and negative paths of the HG might reduce the HG differential mismatch, but the detailed schematic and analysis are omitted in this article.

The proposed synthesizer output spectra resonating the L_P-C_{bank} on the 28th and 12th harmonics when AC_M = 127 and AC_M = 253 are shown in Figure 31(c) and Figure 31(e), respectively. As expressed in (2), f_{IF} decreases as AC_M increases. The adjacent offset frequencies are 208.877 and 157.171 MHz for AC_M = 127 and AC_M = 253, respectively. The corresponding output frequencies are 5.848 GHz (= 28×208.877 MHz) and 1.886 GHz (= 12×157.171 MHz). For AC_M = 128 and AC_M = 254, the HRRs at ±f_{IF} are better compared with the HRRs for AC_M = 127 and AC_M = 253 as shown in Figure 31(d) and Figure 31(f).

Figure 32 (a) and Figure 32(b) show all the measured worst HRRs of the sampled chips for AC_M = 1, 127, and 253 and AC_M = 2, 128, and 254, respectively. The HRR performance tendency is maintained as explained in the previous section, which leads to the HRR at a lower resonant frequency being better than that at a higher one. However, all the measured HRRs are slightly deteriorated compared with those from HRR simulations. These HRR gaps are considered owing to all the harmonics of the fundamental tone coupled to the synthesizer output through the same substrate in addition to the HG differential mismatch.

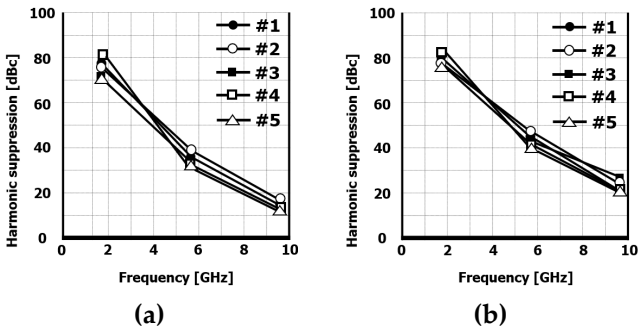

Figure 32. The synthesizer output worst HRRs. (a) AC_M = 1, 127, and 253. (b) AC_M = 2, 128, and 254.

The synthesizer PN measurements (PN_{SYN-1} and $PN_{SYN-253}$) are shown in Figure 33 for AC_M = 1 and AC_M = 253, with corresponding FMFs between f_{MS} and f_{RF} of 63.751 (=9.96/0.15625) and 12.071 (=1.89/0.15625). All the dotted curves are simulated PNs. The measured MEMS oscillator PN (PN_{MS})

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is drawn to distinguish the PN degradation between f_{MS} and f_{ref}. The integrated rms jitter of f_{MS} from 12 kHz to 20 MHz is 72 fs, which is 1.4 fs degraded compared with the jitter in the SiT9501 datasheet.

When AC_M = 1, the estimated synthesizer PN (PN_{EST-1}) is simply the multiplication of FMF^2 and PN_{SUM}. $PN_{SUM} = PN_{MS} + PN_{LP}H_l^2(s) + PN_{HP}\times H_h^2(s)$, where $H_l(s)$ and $H_h(s)$ are LPF and HPF NTFs as defined in (6). Also, PN_{LP} is the PN simulation of PFD+CP (Figure 10), and PN_{HP} is the PN simulation of DU_{128} shown in Figure 13. Since PN_{LP} is bigger than PN_{HP}, the 3-dB DLL loop bandwidth is set low enough for optimizing the synthesizer rms jitter from 12 kHz to 20 MHz. PN_{SYN-1} green curve is PN measurement when the DLL 3-dB bandwidth is 100 Hz.

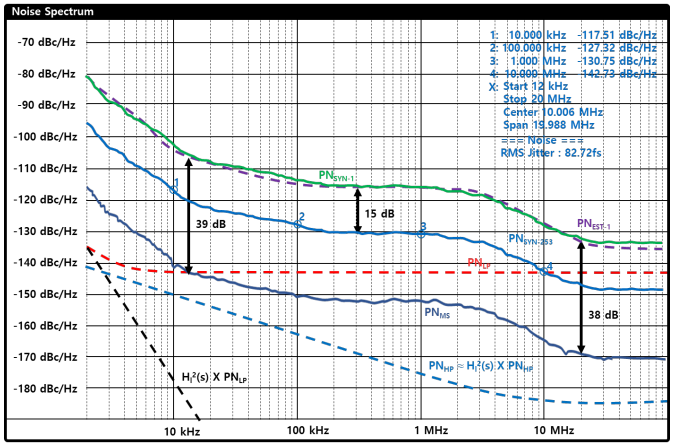

Figure 33. The synthesizer PN curves of 1.89 and 9.96 GHz.

As shown in Figure 33, the estimated PN (PN_{EST-1}) is close to the measured PN (PN_{SYN-1}), proving that the most dominant noise sources are PFD+CP and VCDL. Moreover, the PN differences between PN_{SYN-1} and PN_{MS} are approximately 39 and 38 dB at 12 kHz and 20 MHz offsets, respectively, which are only 3 and 2 dB bigger than the mathematical PN degradation due to frequency multiplication between f_{RF} and f_{MS}. The PN difference between PN_{SYN-1} and $PN_{SYN-253}$ is 15 dB, close to the mathematical PN degradation (20 log (9.96/1.886)). The measured rms jitters of PN_{SYN-1} and $PN_{SYN-253}$ integrated from 12 kHz to 20 MHz are 82.65 and 82.72 fs, which is a jitter degradation of approximately 10.7 fs compared with the measured integrated jitter of PN_{MS} (72 fs). In other words, more than 87 % of the presented synthesizer's rms jitter comes from the reference clock. Table 2 shows the rms jitter measurements of 12k-20MHz for all five test chips. Also, the rms integrated for 1k-100MHz have been measured, and which average rms jitters are 107.606 and 107.634 fs at 1.89 and 9.96 GHz, respectively. The jitter degradation is only 9.2 fs compared with the integrated PN_{MS} (98.0 fs) of 1k-100MHz.

Table 2. RMS jitter measurement.

	Chip#1	Chip#2	Chip#3	Chip#4	Chip#5
RMS Jitter [fs] @ 1.89 [GHz]	82.65[1]	83.12[1]	82.14[1]	81.84[1]	83.74[1]
	107.6[2]	107.9[2]	107.43[2]	107.12[2]	107.98[2]
RMS Jitter [fs] @ 9.96 [GHz]	82.72[1]	83.54[1]	82.34[1]	82.21[1]	84.13[1]
	107.57[2]	107.83[2]	107.48[2]	107.24[2]	108.05[2]

[1] Integrated from 12k to 20M. [2] Integrated from 1k to 100M.

5. Summary and Conclusion

To achieve the stringent jitter performance of a beyond 5G LO generator, the cascade structures of a low-frequency synthesizer and FM have been actively researched in the recent decade. If an mmWave FM is noiseless, the FM output jitter equals the lower synthesizer jitter. Therefore, the lower-frequency synthesizer integrated rms jitter must be less than the LO generator target

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specification. Otherwise, without a PN filter function, the FM output integrated rms jitter cannot achieve the jitter specification.

ILPLL and SSPLL have been successfully developed for the lower-frequency synthesizer to enhance in-band PN by removing the frequency divider in the feedback path. However, VCO jitters in both ILPLL and SSPLL are still accumulated over the injection and subsampling clock periods. Therefore, the output PNs are degraded enough to affect the integrated rms jitter performance, particularly for a wide integrated frequency band. Moreover, their channel resolutions and frequency ranges are poorer than those of the classical Integer-N PLL (CINPLL). In addition, they normally require extra circuitries to program the output frequency and prevent them from losing lock states.

In this article, a new DLL-based synthesizer topology is introduced. The 512 phases (P_1-P_{512}) are equally spaced by a 512-phase DLL (Figure 2). The I/Q multiplexer outputs (V_I and V_Q) are initially connected to P_I and P_Q. Next, V_I and V_Q switched to $P_{I\pm ACM}$ and $P_{Q\pm ACM}$, where AC_M is the programmable input magnitude of the I/Q accumulator. As keeping switch by AC_M, the period of V_I and V_Q would be $(512 \pm 2AC_M)\times t_d$, where $t_d = T_{MS}/512$. Therefore, the fundamental frequency (f_{IF}) of the XOR output (V_{IF}) can be derived as (2).

If V_I and V_Q switch only to the phase lag signal, equation (2) can be rewritten as

$$f_{IF} = f_{MS}\left(\frac{1024}{512 + 2AC_M}\right) = f_{MS}\left(1 + \frac{512 - 2AC_M}{512 + 2AC_M}\right). \quad (26)$$

Equation (26) shows that f_{IF} can be programmed as a fractional multiple of f_{MS} (= f_{ref}) similar to CFNPLL output frequency, f_{CFN}, as

$$f_{CFN} = f_{ref}\left(N + \frac{K}{M}\right), \quad (27)$$

where K and M are integers. And, its channel resolution is f_{ref}/M which is normally smaller than the proposed synthesizer channel resolution defined in (4). On the contrary, the proposed synthesizer provides a finer channel resolution than ILPLL, SSPLL, and CINPLL by setting

$$RF_{FMF}\frac{512 - 2AC_M}{512 + 2AC_M} < 1. \quad (28)$$

Normally, a CFNPLL provides fractional spurs close to an output frequency, which degrades integrated jitter somewhat. In addition, the ΔΣ modulator in the feedback path of CFNPLL contributes a quite bit of integrated jitter. However, the proposed synthesizer removes the above-mentioned penalties for fractional multiplication due to the fixed fractional multiplication.

Recently, injection-locked frequency multipliers (ILFMs) have proven to be an efficient topology for unwanted harmonic suppression. However, ILFMs suffer from a narrow injection-locked frequency range. Moreover, they may require additional circuitries to maintain the lock state, particularly for high-order harmonic injections.

The synthesizer implemented in this paper has the same FM topology as the one reported in [26], but the presented FM is optimized to achieve the maximum frequency range using the smallest switch and capacitor sizes. The output resonant frequency is tuned by varying the C_{bank} magnitude while keeping the same parallel inductor (L_P) and equivalent resistance (R_{EQ}). Therefore, the highest quality factor (Q) of the L_P-C_{bank} load can be achieved at the lowest resonant frequency because Q is proportional to the square root of the total capacitance magnitude. Consequently, the HRR performance is degraded as the wanted frequency is increased.

Table 3 shows the specification comparison of state-of-the-art synthesizers with the proposed synthesizer. While [23] and [28] provide the rms jitter integrated from 10 kHz to 30 MHz, the other references including this work have measured rms jitter integrated from 1 kHz to 100 MHz. The active die area of [19] and [21] is the smallest (0.2 mm^2). Synthesizers proposed in [19] and [22] consume a relatively low power. The jitter performance of [21] is only 58.2 fs, which is the smallest. The synthesizer proposed in [28] provides the widest frequency bandwidth.

Table 3. Comparison with state-of-the-art synthesizer.

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Parameter	[19]	[20]	[21]	[22]	[23]	[28]	This work
Tech.	65mm CMOS	28mm CMOS	28mm CMOS	65mm CMOS	65mm CMOS	65mm CMOS	65mm CMOS
f_{ref} [MHz]	50.0	125.0	500.0	150.0	200.0	10	156.3
f_{out} [GHz]	12–14.5	18.9–22.3	11.9–14.1	3–3.7	24–28.2	0.1–5	1.88–9.96
Frequency Bandwidth [%]	18.9	16.5	16.9	20.9	16.1	192.2	136.5
rms jitter [fs]	83.0 (1k-100M)	71.8 (1k-100M)	58.2 (1k-100M)	135.0 (1k-100M)	65.4 (10k-30M)	960[1] (10k-30M)	107.6 (1k-100M)
Active Die area [mm²]	0.2	0.5	0.2	0.4	0.5	1.44	0.6
Power consumption [mW]	7.7	36.0	18.0	9.5	14.5	21	17.0
FoM1[2]	-252.8	-247.3	-252.1	-247.6	-252.1	-227.1	-246.9
FoM2[3]	-265.5	-259.5	-264.4	-260.8	-264.1	-250.0	-268.25

[1] Referred from phase noise plot. [2] $FoM_1 = 20\log(rms\ jitter) + 10\log(power\ consumption)$. [3] $FoM_2 = FoM_1 - 10\log(\frac{FW}{1\%})$.

For fair performance comparison, two figure-of-merits (FoMs) are introduced. FoM1 and FoM2 are defined at the bottom of Table 3. FoM1 includes integrated rms jitter and power consumption, which are used for all the references. FoM2 is added to include frequency bandwidth percentage in the comparison metric. As a result, the synthesizer implemented in [19] accomplishes the best FoM1. Still, this work achieves the best FoM2, which might mean the proposed synthesizer performs outstanding overall compared with the other state-of-the-art synthesizers.

Author Contributions: Conceptualization, K.N., N.H. and J.P.; methodology, K.N., N.H. and J.P.; validation, K.N. and N.H.; formal analysis, K.N. and J.P.; investigation, K.N., N.H. and J.P.; data curation, K.N. and N.H.; writing—original draft preparation, K.N., N.H. and J.P.; visualization, K.N. and N.H.; supervision, J.P.; project administration, J.P.; funding acquisition, J.P. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data are contained within the article.

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References

1. W. El-Halwagy.; A Nag.; P Hisayasu.; F Aryanfar.; P Mousavi.; M Hossain. A 28-GHz quadrature fractional-N frequency synthesizer for 5G transceivers with less than 100-fs jitter based on cascaded PLL architecture. *IEEE Trans. Microw. Theory Techn.* **2017,** *65*, 396–413.
2. T. Siriburanon et al. A 28-GHz fractional-N frequency synthesizer with reference and frequency doublers for 5G cellular. ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference, Graz, Austria, 14–18 September 2015.
3. J. Kim et al. A 76fs$_{rms}$ jitter and –40dBc integrated-phase-noise 28-to-31GHz frequency synthesizer based on digital sub-sampling PLL using optimally spaced voltage comparators and background loop-gain optimization. 2019 IEEE International Solid-State Circuits Conference, San Francisco, USA, 17–21 February 2019.

 doi:10.20944/preprints202410.0173.v1

4. H. Yoon et al. A −31dBc integrated-phase-noise 29 GHz fractional-N frequency synthesizer supporting multiple frequency bands for backward-compatible 5G using a frequency doubler and injection-locked frequency multipliers. 2018 IEEE International Solid-State Circuits Conference, San Francisco, USA, 11–15 February 2018.
5. D. Shin.; K. -J. Koh. An injection frequency-locked loop-autonomous injection frequency tracking loop with phase noise self-calibration for power-efficient mm-wave signal sources. *IEEE J. Solid-State Circuits*. **2018**, 53, 825–838.
6. P. C. Maulik.; D. A. Mercer. A DLL-based programmable clock multiplier in 0.18-µm CMOS with -70 dBc reference spur. *IEEE J. Solid-State Circuits*, **2007**, 42, 1642–1648.
7. J. Choi.; S. T. Kim.; W. Kim.; K. Kim.; K. Lim.; J. Laskar. A low power and wide range programmable clock generator with a high multiplication factor. *IEEE Transaction on Very Large Scale Integration (VLSI) Systems* **2011**, 19, 701–705.
8. J. Koo,; S. Ok,; C. Kim. A low-power programmable DLL-based clock generator with wide-range antiharmonic lock. *IEEE Trans. Circuits Syst. II, Exp. Briefs* **2009**, 56, 21–25.
9. F. Liao.; S. Lu. A programmable edge-combining DLL with a current-splitting charge pump for spur suppression. *IEEE Trans. Circuits Syst. II, Exp. Briefs* **2010**, 57, 946–950.
10. X. Gao.; E. A. M. Klumperink.; M. Bohsali.; B. Nauta.; A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2," *IEEE J. Solid-State Circuits* **2009**, 44, 3253–3263.
11. X. Gao. Sub-sampling PLL for millimeter wave applications: An overview. 2019 IEEE MTT-S International Microwave Conference on Hardware and Systems for 5G and Beyond (IMC-5G), Atlanta, USA, 15–16 August 2019.
12. K.-C. Peng.; C.-H. Lee.; D.-G. Wong.; F.-K. Wang.; T.-S. Horng.; An injection- and frequency-locked loop for reducing phase noise of wideband oscillators. *IEEE Trans. Microw. Theory Techn.* **2018**, 66, 1374–1383.
13. X. Jin.; D.-S. Kang.; Y. Ko.; K.-W. Kwon.; J.-H. Chun. A 4-GHz sub-harmonically injection-locked phase-locked loop with self-calibrated injection timing and pulsewidth. *IEEE J. Solid-State Circuits* **2020**, 55, 2724–2733.
14. M.-S. Choo.; Y. Song.; S.-Y. Cho.; H.-G. Ko.; K. Park.; D.-K. Jeong.; A 15-GHz, 17.8-mW, 213-fs injection-locked PLL with maximized injection strength using adjustment of phase domain response. *IEEE Trans. Circuits Syst. II, Exp. Briefs* **2019**, 66, 1932-1936.
15. H. Wang,; O. Momeni,; Low-power and low-noise millimeter-wave SSPLL with subsampling lock detector for automatic dividerless frequency acquisition. *IEEE Trans. Microw. Theory Techn.* **2021**, 69, 469–481.
16. J. Kim et al. A 104fsrms-Jitter and -61dBc-Fractional Spur 15GHz Fractional-N Subsampling PLL Using a Voltage-Domain Quantization-Error Cancelation Technique. 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, USA, 13–22 February 2021.
17. B. Razavi. The Delay-Locked Loop [A Circuit for All Seasons]. *IEEE Solid-State Circuits Magazine* **2018**, 10, 9–15.
18. X. Lil et al.; A 3.84 GHz 32 fs RMS Jitter Over-Sampling PLL with High-Gain Cross-Switching Phase Detector. 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, USA, 21–25 May 2023.
19. Y. Lim.; J. Kim.; Y. Jo.; J. Bang.; J. Choi. A wide-lock-in-range and low-jitter 12–14.5 GHz SSPLL using a low-power frequency-disturbance-detecting and correcting loop. *IEEE J. Solid-State Circuits* **2022**, 57, 480–491.
20. F. Buccoleri et al. A 72-fs-Total-Integrated-Jitter Two-Core Fractional-N Digital PLL With Digital Period Averaging Calibration on Frequency Quadrupler and True-in-Phase Combiner. *IEEE J. Solid-State Circuits* **2023**, 58, 634–646.
21. M. Mercandelli et al. A 12.5-GHz Fractional-N Type-I Sampling PLL Achieving 58-fs Integrated Jitter. *IEEE J. Solid-State Circuits*, **2022**, 57, 505–517.
22. Y. Jo et al.; A Wideband LO Generator for 5G FR1 Bands Using a Single LC-VCO-Based Subsampling PLL and a Ring-VCO-Based Fractional-Resolution Frequency Multiplier. *IEEE J. Solid-State Circuits* **2023**, 58, 3338–3350.
23. X. Geng.; Z. Ye.; Y. Xiao.; Y. Tian.; Q. Xie.; Z. Wang. A 25.8-GHz Integer-N CPPLL Achieving 60-fs rms Jitter and Robust Lock Acquisition Based on a Time–Amplifying Phase–Frequency Detector. *IEEE Trans. Microw. Theory Techn.* **2023**, 71, 4869–4881.
24. A. Homayoun.; B. Razavi. Analysis of phase noise in phase/frequency detectors. *IEEE Trans. Circuits Syst. I, Reg. Paper* **2013**, 60, 529–539.
25. N. -P. Hong.; K. -H. Nam.; J. -S. Park.; A Fractional-N Synthesizer Based on Programmable Frequency Multiplier for 5G+ Communication System. *IEEE Trans. Microw. Theory Techn.* **2023**, 71, 1518–1535.
26. K.-H. Nam.; N.-P. Hong.; J.-S. Park. A 16-times frequency multiplier for 5G synthesizer. *IEEE Trans. Microw. Theory Techn.* **2021**, 69, 4961–4976.

 doi:10.20944/preprints202410.0173.v1

27. H. Lan.; T. W. Chen.; C. O. Chui.; P. Nikaeen.; J. W. Kim.; R. W. Dutton. Synthesized Compact Models and Experimental Verifications for Substrate Noise Coupling in Mixed-Signal ICs. *IEEE J. Solid-State Circuits* **2006**, 41, 1817–1829.
28. Zhang, Zhao et al. 0.1–5 GHz wideband ΔΣ fractional-N frequency synthesizer for software-defined radio application. IET Circuits, Devices & Systems **2019**, 13, 1071–1077.