Communication

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On-Chip Transformer Based Isolation Driver Chip Using PCB Technology

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Abstract: Isolation driver chips are widely used for reliable communication between low and high voltage levels, with on-chip transformers serving as the core devices for magnetic isolation. In this study, we designed, simulated, and tested an on-chip transformer that can be manufactured using PCB technology. This transformer uses copper as the conductive material and FR4 as the dielectric, theoretically achieving an insulation level of up to 3KV, making it suitable for mass production and showing significant industrial application potential. Based on this on-chip transformer, we designed corresponding encoding and decoding circuits and implemented the circuit structure through System in Package (SIP). Simulation results indicate that this isolation driver chip can reliably support communication across different voltage levels.

Keywords: isolation driver; on-chip transformer (OCT); Printed Circuit Board (PCB); CMOS

1. Introduction

Isolation driver chips are widely used in fields such as photovoltaic inverters [1], energy storage systems [2,3], electric drive system [4,5]. They effectively prevent voltage spikes and ground loops between low-voltage areas (e.g., microcontrollers) and high-voltage regions (e.g., gate drivers) through isolation shielding, ensuring reliable and safe communication between different voltage levels within a system [6–9]. The development of isolation driver chips primarily focuses on reducing manufacturing costs (such as processes, area, and packaging) while improving performance (such as power consumption, delay, and isolation level) [10,11]. Optocoupler typically require larger volumes [12,13], while capacitive isolator is mainly suitable for data communication [14,15]. In contrast, transformer based isolator is more suitable for power transmission, offering higher isolation levels, more compact integration, faster transmission speeds, and lower power consumption [16,17].

On-chip transformers (OCT) are key devices for achieving magnetic inductive coupling, and their development has received considerable attention [10,18]. Silicon-based OCTs have a dielectric breakdown strength of up to 850 V/μm but occupy a relatively large area [19]. Methods such as self-assembly are also research directions for on-chip transformers [20], while using mature Printed Circuit Board (PCB) technology can achieve both high isolation levels and low costs. Common Mode Transient Immunity (CMTI) is an important parameter for assessing isolation driver chips, referring to the ability of an isolator to maintain correct signal output during rapid voltage changes (dV/dt) [21]. This parameter is particularly crucial for rapidly switching power devices.

Therefore, this paper designs and manufactures an on-chip transformer compatible with PCB technology, incorporating a grounding shield layer to enhance CMTI, and designs a driver circuit based on this transformer. The wafer processing is completed under a fabless model, and the isolation driver function is realized through System in Package (SIP). This work primarily employs mature PCB and CMOS processes, demonstrating promising commercial prospects.

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2. Design and Fabrication

Figure 1a shows the basic structure of the on-chip transformer. The primary and secondary coils are separated by FR4 material, with copper used as the coil material. Each coil consists of two layers, interconnected through copper plating in the Vias, allowing the formation of a three-dimensional structure of the transformer through stacked planar processing. Typical coil shapes include circular, elliptical, and rectangular [22]. Although complex winding or stacking structures can enhance the inductance [23], they increase the number of variables in the design and manufacturing processes, resulting in a significant increase in simulation workload. Therefore, this paper only selects equidistant rectangular coil patterns, as shown in Figure 1b.

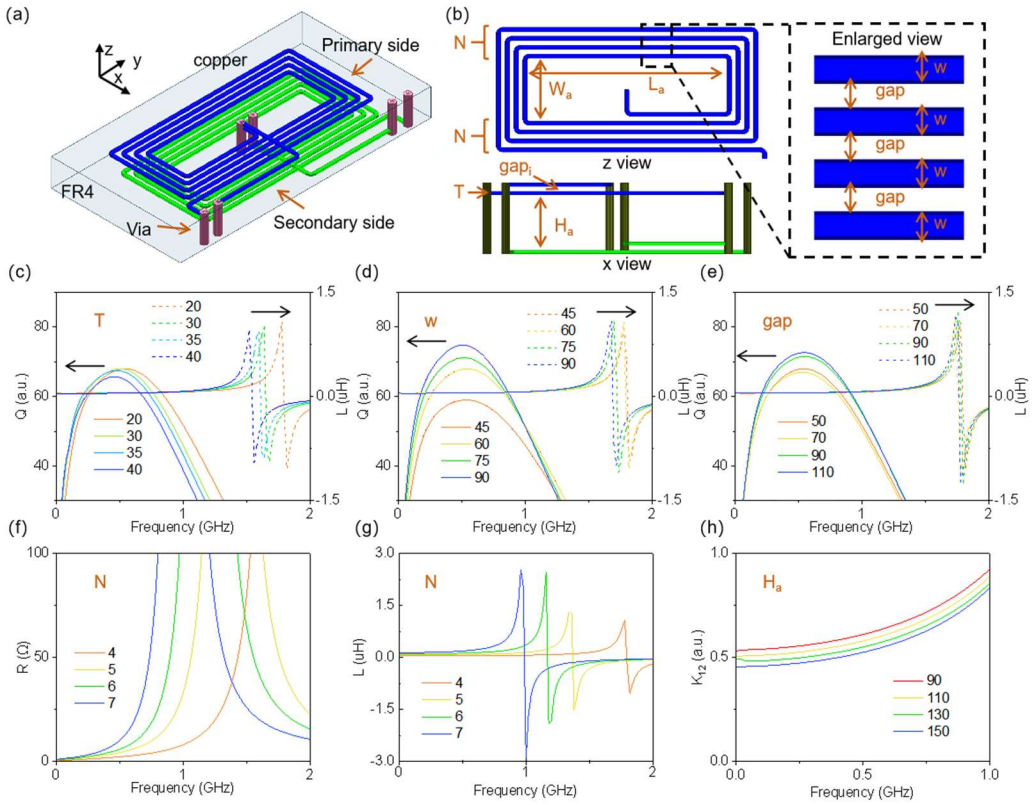

Figure 1. Structure and Simulation of On-Chip Transformer. (a) Three-dimensional view of the on-chip transformer; (b) Z-direction and X-direction views of the coil; (c) Effect of changing the copper layer thickness T of the coil on the relationship between Q value, L value, and frequency; (d) Effect of changing the coil copper wire width w on the relationship between Q value, L value, and frequency; (e) Effect of changing the coil copper wire spacing gap on the relationship between Q value, L value, and frequency; (f) Effect of changing the number of turns N of the coil on the relationship between R value and frequency; (g) Effect of changing the number of turns N on the relationship between L value and frequency; (h) Effect of changing the spacing H_a between the primary side and secondary side on the relationship between K_{12} value and frequency.

The self-inductance, coupling efficiency, and equivalent resistance of the on-chip transformer are frequency-dependent. Due to lower coupling efficiency at low frequencies, these transformers generally operate above 10 MHz. The quality factor Q indicates the energy loss of the coil in alternating signals. The gain coefficient is an important parameter for the on-chip transformer, calculated as follows [24–26]:

$$A_v = \frac{V_2}{V_1} \cong k_{12}\sqrt{\frac{L_2}{L_1}}\frac{j\omega L_1}{j\omega L_1 + R_2 + R_{LOAD}} \quad (1)$$

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Where V_2 is the peak-to-peak voltage of the secondary coil, V_1 is the peak-to-peak voltage of the primary coil, k_{12} is the coupling efficiency between the two coils, L_1 and L_2 are the self-inductance values of the primary and secondary coils respectively, R_2 and R_{LOAD} are the equivalent resistances of the secondary coil and load respectively, and ω is the angular frequency.

We obtained the frequency characteristics of the on-chip transformer using a finite element simulation method, as shown in Figures 1(c-h). We optimized multiple parameters, including copper layer thickness T, copper wire width w, copper wire spacing gap, number of turns N, and spacing Ha between the primary and secondary sides. The results indicate that increasing T and N lowers the cutoff frequency and improves the self-inductance value at specific frequencies; increasing w effectively enhances the Q value; while increasing N reduces the equivalent resistance and minimizes inductive losses. Decreasing H_a can effectively improve coupling efficiency, whereas increasing H_a helps to enhance isolation levels. Considering the transformer's size, available process adjustment space, and performance optimization, we ultimately selected a set of structural parameters to meet the needs of the isolation driver circuit. Specific parameters are withheld due to commercial confidentiality.

Improving the coupling efficiency of the on-chip transformer is crucial, as higher efficiency means lower losses [27]. Using magnetic cores with higher permeability can enhance coupling efficiency [28,29]. Figure 2a shows the structure with a magnetic core directly embedded in the center of the coil, while Figure 2b shows the structure with a magnetic material pattern added on the surface of the on-chip transformer. Figure 2c displays the finite element simulation results. While the presence of the magnetic core effectively improves coupling efficiency, the improvement is typically limited to about 15% due to the volume constraints of the magnetic core. Additionally, the ferrite 1 option presents significant challenges in planar process, whereas ferrite 2 is compatible with planar process but offers negligible improvement in coupling efficiency, making it hard to justify the additional manufacturing costs brought by the process enhancements. Hence, this paper does not adopt a magnetic core structure.

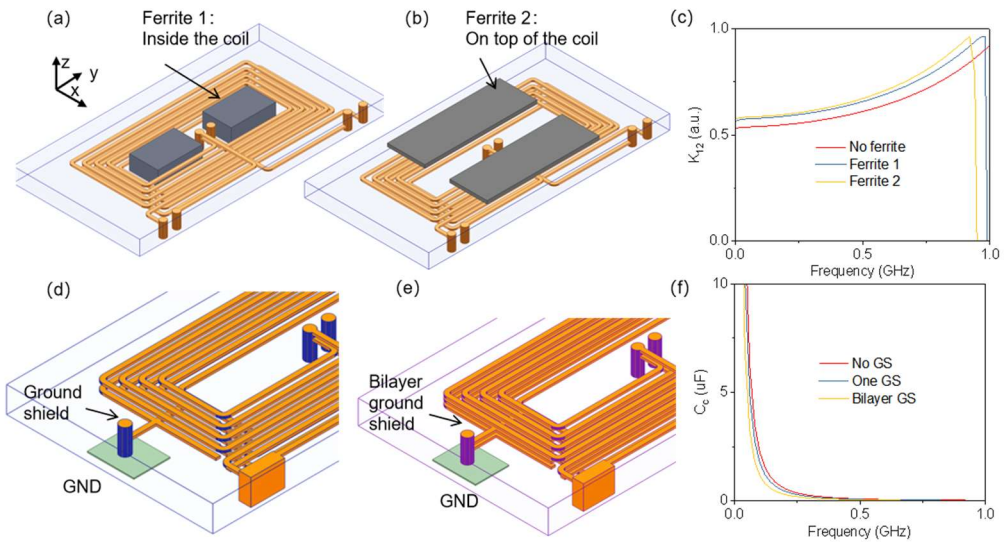

Figure 2. Influence of Magnetic Core and Ground Shielding Layer on On-Chip Transformer. (a) Three-dimensional structure with a magnetic core block added in the center of the coil; (b) Three-dimensional structure with a magnetic chip added above the coil; (c) Relationship between the presence of magnetic core and K_{12} value with frequency; (d) Three-dimensional structure of a single ground shielding layer; (e) Three-dimensional structure of a double ground shielding layer; (f) Relationship between the presence of ground shielding layer and C_C value with frequency.

To enhance the Common Mode Transient Immunity (CMTI) of the on-chip transformer, we placed a patterned metal layer above the secondary coil, forming a grounded metal structure that

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creates a Faraday shield. By employing a ground shield (GS) pattern that does not form a closed loop, the eddy currents induced by the magnetic field in the GS are suppressed, thus not affecting the normal functioning of the OCT. Meanwhile, the electric field from the primary coil is primarily intercepted by the GS. Therefore, during common mode voltage transients, the displacement current caused by capacitive coupling is directed to ground through the secondary's PGS, reducing interference in the output signal [21].

In traditional OCTs, the output voltage caused by common mode transients (dV_{CM}/dt) couples to the secondary output through an equivalent capacitance C_C, which is proportional to the CC value [30–33]. We employed finite element analysis to establish the three-dimensional models shown in Figures 2d and 2e, with the frequency characteristics of C_C presented in Figure 2f. The presence of the GS effectively reduces the equivalent capacitance C_C; for instance, at a frequency of 0.1 GHz, the C_C value of the double-layer GS is only half that of the case without GS layer. Considering the trade-off between manufacturing costs and device performance, this paper chooses to implement a double-layer GS structure

Figure 3a outlines the processing flow for the on-chip transformer, which is compatible with mature PCB manufacturing techniques. The process begins with cutting raw materials and drilling holes at designated via locations. Next, each layer undergoes copper plating and patterning. Given that the manufacturing precision is at the micrometer level, the cost of the patterning process is relatively low. Subsequently, multilayer materials are aligned, stacked, and bonded. Finally, interconnection ports are created on the surface for external electrical connectivity. Figure 3b shows a photograph of the processed on-chip transformer, indicating that the procedure is simple and reliable, making it suitable for mass production.

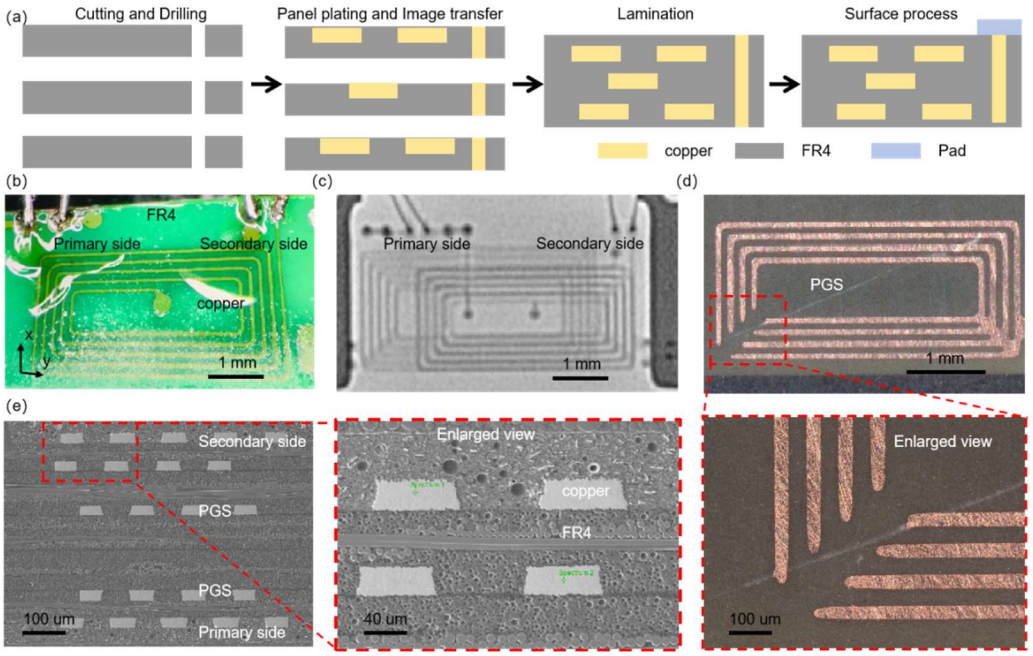

Figure 3. Fabrication and Characterization of On-Chip Transformer. (a) Fabrication process of the on-chip transformer based on PCB technology; (b) Photo of the on-chip transformer (without surface treatment); (c) X-ray tomography image of the on-chip transformer; (d) Microscopic image of the ground shielding layer and its magnified view; (e) Cross-sectional SEM images of the on-chip transformer and a magnified view.

To assess the reliability of the on-chip transformer fabricated using this PCB process, a series of characterization experiments were conducted. Figure 3c presents an X-ray tomography image of the on-chip transformer, revealing no delamination, voids, bubbles, or impurities that could negatively affect performance. Figure 3d shows the pattern of the ground shielding layer after layer removal and grinding, with uniform copper wire widths, maintaining a width consistency within 3% and a

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spacing consistency within 2.6%. Simulations were conducted to supplement the analysis of manufacturing tolerances, which were found to be within acceptable limits. Figure 3e displays cross-sectional scanning electron microscope (SEM) images of the device, indicating that the consistency of copper layer thickness is within 5%. However, due to the limitations of the pressing process, interlayer spacing has a relatively larger manufacturing tolerance, with a maximum deviation of up to 12%. These errors must be considered in circuit design adjustments, as evaluated through simulation. The insulation level of FR4 material ranges from 16 to 20 V/μm, implying that a 200 μm thick FR4 layer can withstand at least 3 kV of electrical arcing. These results demonstrate the advantages of the PCB technology-based on-chip transformer in terms of fabrication and reliability, laying a solid foundation for subsequent applications

3. Results and Discussion

We use a behavioral-level circuit model for the on-chip transformer [25], as shown in Figure 4a. This model serves as a standard unit during the chip design process, with parameters such as R, M, L, K, and Q defined based on simulation results to establish their operational ranges. Through behavioral-level simulations, we determined the range of voltage gain A_v, optimizing the goal to ensure that the fluctuations of A_v do not exceed 20%. Figure 4b displays the input and output waveforms of the primary and secondary sides at a frequency of 90 MHz, where the value of A_v is measured at 1.21.

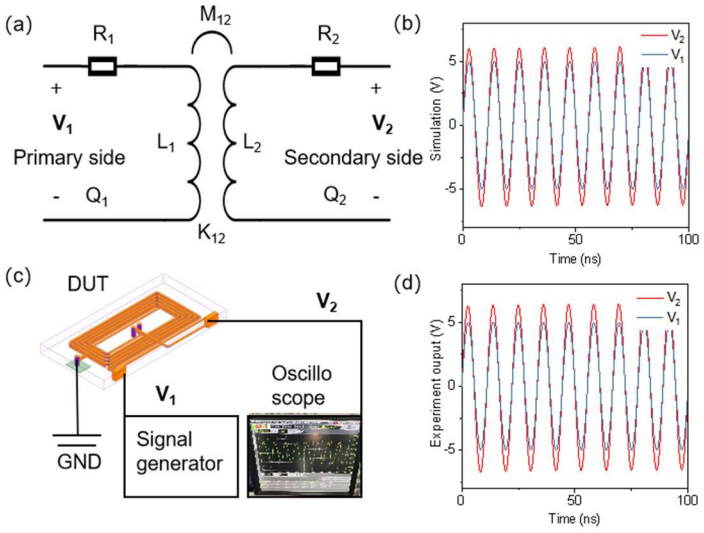

Figure 4. Simulation and Experimental Testing of On-Chip Transformer. (a) Simplified circuit model of the on-chip transformer; (b) Input and output simulation results of the primary and secondary sides of the on-chip transformer; (c) Schematic diagram of the experimental testing setup for the on-chip transformer; (d) Input and output experimental testing results of the primary and secondary sides of the on-chip transformer.

To validate our simulations experimentally, we constructed the testing platform illustrated in Figure 4c, along with a photograph of the oscilloscope used during the testing. A signal generator supplies a sine wave at a specified frequency to the primary side, while the oscilloscope measures the secondary side signal. As shown in Figure 4d, at a frequency of 90 MHz, the input and output waveforms of the primary and secondary sides yield an A_v value of 1.25. After extensive iterative experiments and optimization of simulation parameters, we successfully achieved a deviation in A_v between simulated and actual measurement results of no more than 5%. This outcome provides a stable technological platform for realizing high-consistency isolation driver products and demonstrates the reliability and effectiveness of the designed on-chip transformer in practical applications.

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Figure 5a presents a simplified circuit block diagram of the isolated driver circuit. When the input signal is fed into the circuit, the CTR module applies enable control signals to other modules based on the input signal, which is shown in Figure 5e. After introducing a 90 MHz oscillation, the signal is passed through the driver circuit to the on-chip transformer, then processed through waveform shaping and wide-threshold Schmidt trigger circuits (SMT). The output signal experiences a slight delay, enabling the signal to transition from a low voltage region in the front stage to a high voltage region in the subsequent stage.

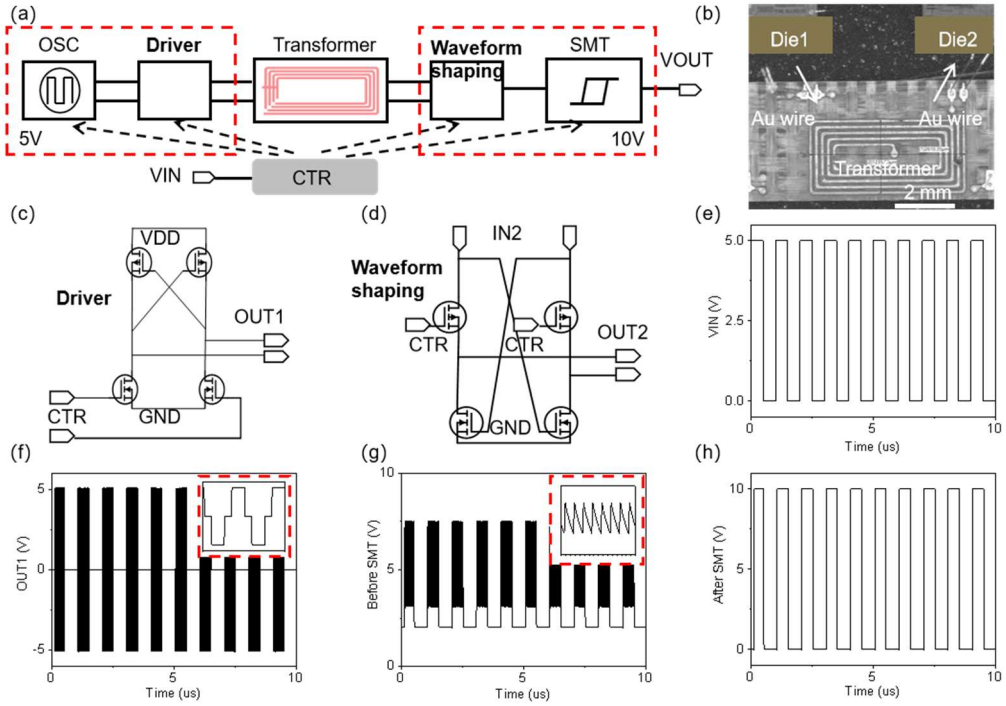

Figure 5. Simulation Results of Isolated Driver Circuit. (a) Simplified circuit block diagram of the isolated driver circuit; (b) Photo of the isolated driver packaged in SIP (System in Package) format; (c) Output circuit structure of the Driver circuit; (d) Input circuit structure of the Waveform shaping circuit; (e) Signal at the VIN terminal; (f) Differential signal output at OUT1 port, with the waveform magnified on the horizontal axis within the red dashed box; (g) Single-ended signal output from the Waveform shaping circuit, with the waveform magnified on the horizontal axis within the red dashed box; (h) Single-ended signal output at the VOUT terminal.

The isolated driver chip comprises three main parts: die1 (input section), the on-chip transformer, and die2 (output section), which are integrated on a bus via SIP, as depicted in Figure 5b. Figures 5c and 5d illustrate two circuits directly connected to the on-chip transformer. When the input signal is set at 5V, the generator (OSC) is activated, outputting an oscillating signal ranging from 0 to 5V. The output from the Driver circuit generates a driving signal between -5V and 5V, as shown in Figure 5f. The use of non-overlapping clocks prevents signal interference, creating a zero-volt level between -5V and 5V, exemplified by the waveform characteristics in the red dashed box.

After passing through the transformer, the signal becomes an AC voltage range of -5.5V to 5.5V, with a supply voltage (VDD) of 10V in the subsequent stage. The waveform shaping circuit processes the signal, moving it to a higher voltage threshold and achieving a single-ended output, as illustrated in Figure 5g. Through optimized design, the low conversion threshold of the Schmidt trigger circuit is set to 3V, allowing the oscillating signal component to rise to 10V via the level shifting module, while the non-oscillating signal portion remains at 0V, as shown in Figure 5h. This process enables efficient isolated signal transmission based on the on-chip transformer.

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4. Conclusions

In summary, we have reported an on-chip transformer compatible with PCB processes, aimed at enabling isolated driver chips. This approach not only aligns with mature CMOS processes and PCB manufacturing methods but also offers low costs and significant commercial potential, while optimizing performance. Through finite element analysis, we designed the structure and utilized processes compatible with PCB techniques to fabricate the on-chip transformer. By combining X-ray imaging, layer removal photography, as well as simulation and testing analysis, we evaluated the consistency of the device production. Ultimately, guided by a fabless model, we successfully achieved wafer production and functioned the isolated driver chip. This on-chip transformer-based isolated driver chip demonstrates vast application prospects in various fields, including gate driving, new energy vehicles, and photovoltaic energy storage. Our research provides a solid foundation for the further development and application of these technologies, with the potential to drive technological advancements and innovations in related fields.

Author Contributions: The design and simulation of the experimental device in this paper were completed by Ye Luo, while manuscript proofreading and other tasks were collectively handled by all authors.

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Conflicts of Interest: The authors declare no conflicts of interest.

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