Article

Design and Implementation Procedure of a High-Gain Three-Input Step-Up 1kW Converter

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Abstract: The use of different sources to energize a load is convenient in many applications, particularly those where two or more renewable energy sources are employed as: energy harvesting, hybrid vehicles, and off-grid systems. In these cases, a multi-input converter able to admit sources with different characteristics and, if necessary, select the output power of each source. Several topologies of multi-input converters have been proposed to this aim, however, most of them are based on multi-stage designs, which decreases efficiency and increases control complexity, particularly when more than two sources are used. In this work, a three-input step-up converter easy to control in open loop condition is analyzed. A designed procedure is described, and experimental results are presented for a 1 kW power converter. The implemented converter results in a higher voltage gain, less storage element keeping high efficiency compared to similar topologies. Using the procedure here proposed, this converter that was initially proposed for photovoltaic applications is enabled to be used in medium and high-power applications, for example when renewable energy sources are used.

Keywords: Multi-output converter; DC-DC converter; Boost converter; Renewable energy

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1. Introduction

An intense research effort has been made to increase the use of renewable energy in all human activities. Techniques to take advantage of solar [1], wind [2], and hydrogen based [3], among other clean energies, has been developed. In some applications, it is necessary to jointly use several of these sources to feed a single load. Frequently it is convenient a scheme where if a single source is not enough, a second source may be used; if both are not sufficient, a third can be used, and so on. To make such scheme possible, a multi-input converter is necessary [4]. Among the applications where this scheme is used are energy harvesting for wireless sensors [5], smart buildings [6], hybrid and electric vehicles [7], off-grid systems in rural areas [8], etc.

Multi-input step-up converters have been reported in the literature, some of them are based on the boost converter. For example, experimental results for a multi-input multi-output step-up converter for a 1 kW prototype are presented in [9]; this topology presents some disadvantages like a high number of energy storage elements and a low switching frequency operation that increase the magnetic components size. In [10] a dual-input step-up converter is presented for a 125 W prototype with a high efficiency of 97%, but the number of switching power devices are two per input. The number of semiconductor devices increases severely in the dual step-up converter presented in [11] for a 200 W output power and an efficiency of 87 %.

In [12] a model for the dual-input case of the topology proposed in [13] was derived and analysed, and a 500 W converter was evaluated. However, the real difficulty with the existing multi-input converters arises when more than two inputs are used, and a higher power is required. In this context, to make sure that the model and design procedure match the experimental results a 1 kW prototype for three input voltages is implemented in this work. Efficiency and reliability of the converter is also evaluated.

2. Principle of operation

The converter analysed in this paper is shown in Figure 1. It was firstly proposed in [13] for a low power application (100 W) for two inputs. Number of components is one mosfet to each input source added, in this case three input voltages are considered: V_{in1}, V_{in2} and V_{in3}. Since the basic construction block is the boost converter the only added component per input is a capacitor. To obtain the control switching signals, two basic conditions need to be considered; the phase shift in the control signals, φ = 360°/*inputs* = 360°/3=120°, and the minimum duty cycle which is given by d_{min} = 1-(1/*inputs*) = 0.66.

The six operating modes are shown in Figure 1. The control signals that generate these modes (M1 to M6), are presented in Figure 2. The control signals for d_{min} are indicated in red color; it can be observed that at any timeframe there are two switches in conduction at most.

To analyze the operation of each mode, the following initial conditions are considered: I_{L1}, I_{L2} and I_{L3} currents are greater than zero, C_1 and C_2 are charged to +V_{C1} and +V_{C2}. The conditions in each operating mode are as follows:

Mode 1, Δt1 (see Figure 1a): This mode starts by turning-on switches *S1*, *S2* and *S3*, at the same timeframe, diodes D_1, D_2 and D_3 are state-off. In this interval, inductors L_1, L_2 and L_3 are charged by V_{in1}, V_{in2} and V_{in3}, respectively. Currents I_{L1}, I_{L2} and I_{L3} increase linearly from its minimum value to its maximum. Considering that the average currents through capacitor C_1, C_2 and C_o are zero, then voltages V_{C1}, V_{C2} and V_{Co} are constant. This mode ends when switch *S2* is turned-off at Δt2.

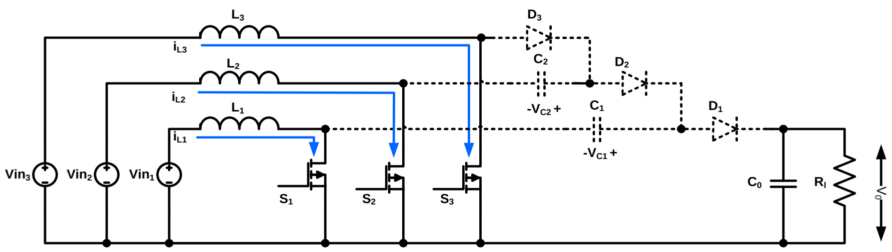
Mode 2, Δt2 (see Figure 1b). In this mode *S2* is turned-off, D_2 and D_1 are activated and allows current to flow to C_2. In this mode I_{L2} decreases linearly and begins to charge C_2 increasing its voltage linearly. This mode ends when switch *S2* is turned-on at Δt3.

Mode 3, Δt3 (see Figure 1c). This mode starts when *S2* is turned-on again, D_2 is deactivated and D_1 is activated. In this interval, inductors L_1, L_2 and L_3 are charged by V_{in1}, V_{in2} and V_{in3}, respectively and C_1 is discharged through D_1. This mode ends when switch *S3* is turned-off at Δt4.

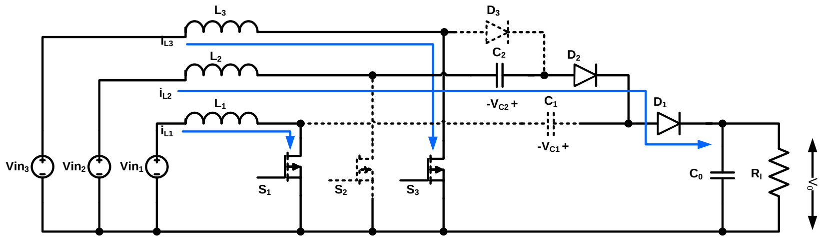
Mode 4, Δt4 (see Figure 1d). In this mode *S3* is turned-off, D_1, D_2 and D_3 are active and allows the current flow to C_2 and C_1. I_{L3} decreases linearly and holds charging the positive side of C_2 and C_1. This mode ends when switch *S3* is gated ON at Δt5.

Mode 5, *Δt5* (see Figure 1e). This mode starts when *S3* is turned-on again, D_3 is turned-off. In this interval, inductors L_1, L_2 and L_3 are charged again by V_{in1}, V_{in2} and V_{in3}, respectively. This mode ends when switch *S1* is turned-off.

Mode 6, *Δt6* (see Figure 1f). In this mode *S1* is turned-off, D_2 is turned-off, D_1 is activated and allows the current flow to C_o, I_{L1} decreases linearly and begins to charge C_o, at the same timeframe, C_1 is discharged to R_L. This mode ends when switch *S1* is gated ON.



(a)



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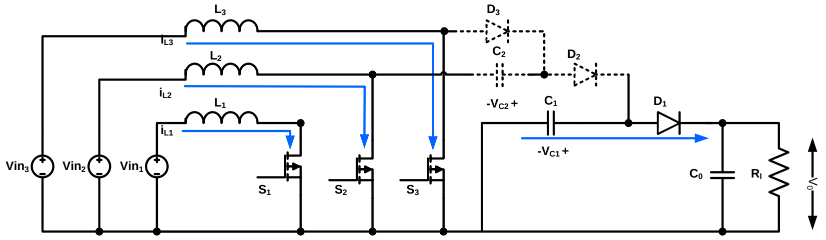

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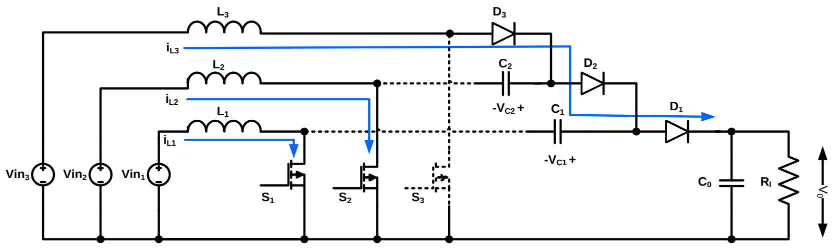

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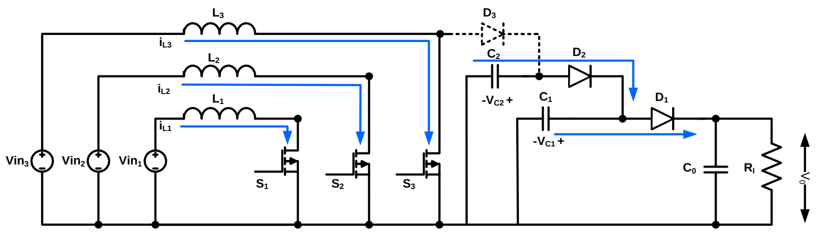
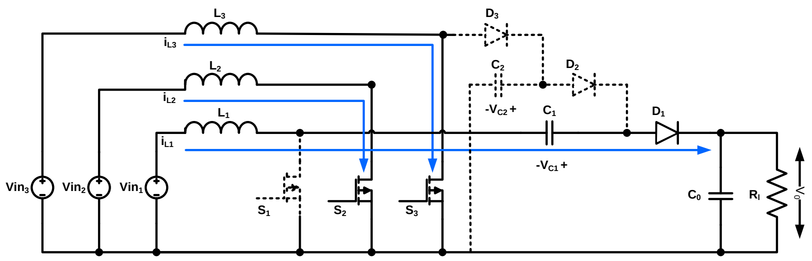


(e)



(f)

Figure 1. Operating modes of the three-input step-up converter: (a) Mode 1, *S1=S2=S3=On*, (b) Mode 2, *S1=S3=On, S2=Off*, (c) Mode 3, *S1=S2=S3=On*, (d) Mode 4, *S1=S2=On, S3=Off*, (e) Mode 5, *S1=S2=S3=On*, (f) Mode 6, *S2=S3=On, S1=On*

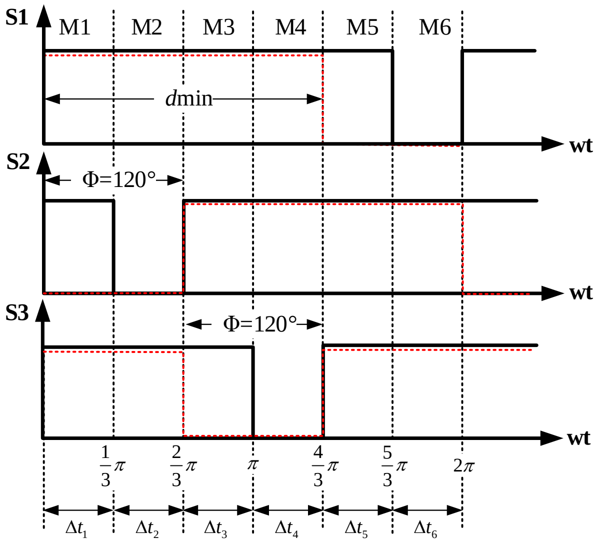


Figure 2. Control signals and operating modes in the the three-input step-up converter

Converter stationary ideal waveforms obtained from analysis of its six operation modes are shown in Figure 3.

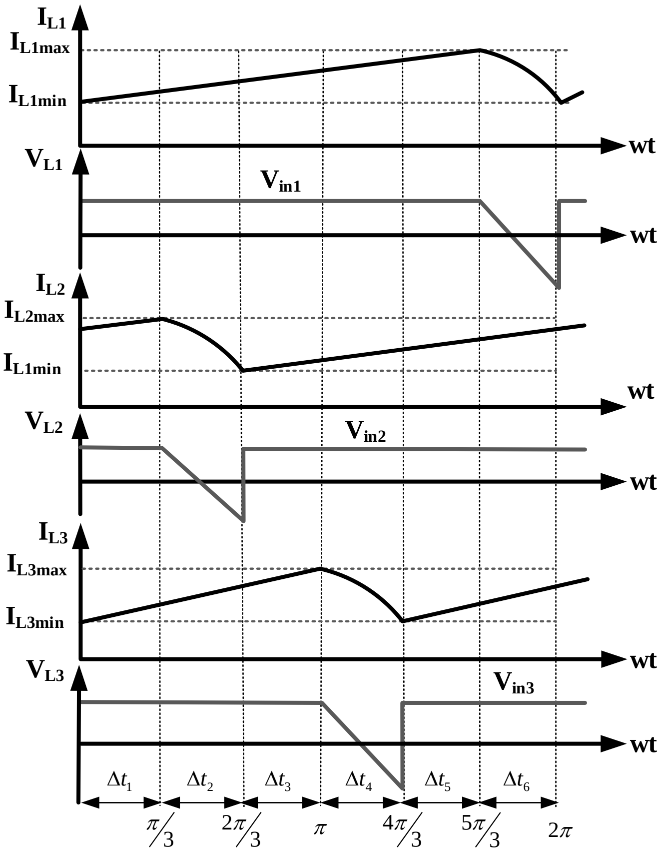


Figure 3. Ideal waveforms of three-input step-up converter

To make the state space analysis, state variables are chosen according to:

$$x_1 = I_{L_1}, \tag{1}$$

$$x_2 = I_{L_2}, \tag{2}$$

$$x_3 = I_{L_3}, \tag{3}$$

$$x_4 = V_{C_1}, \tag{4}$$

$$x_5 = V_{C_2}, \tag{5}$$

$$x_6 = V_{C_o} \tag{6}$$

State space equations for the six operating modes are shown in Table 1.

Table 1. State space equations.

Modes 1,3,5	Mode 2	Mode 4	Mode 6
$\dot{x}_1 = \frac{V_{in1}}{L_1}$	$\dot{x}_1 = \frac{V_{in1}}{L_1}$	$\dot{x}_1 = \frac{V_{in1}}{L_1}$	$\dot{x}_1 = \frac{V_{in1}}{L_1} + \frac{x_4}{L_1} - \frac{x_6}{L_1}$
$\dot{x}_2 = \frac{V_{in_2}}{L_2}$	$\dot{x}_2 = \frac{V_{in_2}}{L_2} - \frac{x_4}{L_2} + \frac{x_5}{L_2}$	$\dot{x}_2 = \frac{V_{in_2}}{L_2}$	$\dot{x}_2 = \frac{V_{in_2}}{L_2}$
$\dot{x}_3 = \frac{V_{in_3}}{L_3}$	$\dot{x}_3 = \frac{V_{in_3}}{L_3}$	$\dot{x}_3 = \frac{V_{in_3}}{L_3} - \frac{x_5}{L_3}$	$\dot{x}_3 = \frac{V_{in_3}}{L_3}$
$\dot{x}_4 = 0$	$\dot{x}_4 = \frac{x_2}{C_1}$	$\dot{x}_4 = 0$	$\dot{x}_4 = -\frac{x_1}{C_1}$
$\dot{x}_5 = 0$	$\dot{x}_5 = -\frac{x_2}{C_2}$	$\dot{x}_5 = \frac{x_3}{C_2}$	$\dot{x}_5 = 0$
$\dot{x}_6 = -\frac{x_6}{R_L C_0}$	$\dot{x}_6 = -\frac{x_6}{R_L C_0}$	$\dot{x}_6 = -\frac{x_6}{R_L C_0}$	$\dot{x}_6 = -\frac{x_1}{C_o} - \frac{x_6}{R_L C_0}$

Let introduce the notation for every switch state

$$u_n = \begin{Bmatrix} 1 & if & sw_n = off \\ 0 & if & sw_n = on \end{Bmatrix}, \tag{7}$$

n=1,2,3

Then the following general state space representation can be obtained.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \\ \dot{x}_5 \\ \dot{x}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{u_1}{L_1} & 0 & -\frac{u_1}{L_1} \\ 0 & 0 & 0 & -\frac{u_2}{L_2} & -\frac{u_2}{L_2} & 0 \\ 0 & 0 & 0 & 0 & -\frac{u_3}{L_3} & 0 \\ -\frac{u_1}{L_3} & -\frac{u_2}{L_3} & 0 & 0 & 0 & 0 \\ 0 & -\frac{u_2}{L_3} & -\frac{u_3}{L_3} & 0 & 0 & 0 \\ -\frac{u_1}{C_0} & 0 & 0 & 0 & 0 & -\frac{1}{R_L C_0} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{V_{in1}}{L_1} \\ \frac{V_{in2}}{L_2} \\ \frac{V_{in3}}{L_3} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{8}$$

3. Design procedure and simulation results

Although the converter uses three different input voltages; components are designed considering the lowest voltage, $V_{in\ min}$; due to inductors current is maximum under this condition.

The complete development of the converter design equations was derived in [12] for the two-input case. Generalization of these equations was obtained from the operating modes described in the previous section. The gain for a three-input converter, M_{VDC}, is:

$$M_{VDC} = \frac{V_o}{V_{in}} = \frac{3}{1-d} = \frac{3I_{inn}}{I_o}, \tag{9}$$

where d is the duty cycle of switching devices operation, and I_{inn} is the input current for each source. To calculate inductance values, note that the inputs of the converter are the same as the conventional boost converter, hence:

$$L_n = \frac{V_{in} d}{\Delta I_n f_s}, \tag{10}$$

where ΔI_n is the ripple current of inductor and f_s is the switching frequency.

Capacitors C_1 and C_2 were carefully designed since a small value may generate an inadequate conversion ratio and a very large value will affect the time response and create output voltage oscillations. The ripple voltage in these capacitors can have wide range since this ripple is not reflected at the converter output. As it is proved in [12], the capacitors can be calculated according to:

$$C_1 = \frac{I_o(1-d_1)}{d_2 \Delta V_{c1} f_s}, \tag{11}$$

$$C_2 = \frac{I_o(1-d_2)}{d_3 \Delta V_{c2} f_s} \tag{12}$$

$$C_o = \frac{I_o(1-d_1)}{\Delta V_o f_s} \tag{13}$$

where I_0 is the output current and ΔV_{C1}, ΔV_{C2}, ΔV_{C0} are the ripple voltage of C_1, C_2 and C_0 respectively.

The converter output voltage is given by:

$$V_o = \frac{V_{in1}}{1-d_1} + \frac{V_{in2}}{1-d_2} + \frac{V_{in3}}{1-d_3}, \tag{14}$$

Using (10) to (13) the final component values are obtained and listed in Table 2 together with the design conditions. A simulation was performed in Saber™ using ideal components to validate the design procedure and the correct operation of the three-input step-up converter.

Table 2. Test parameters and components.

Parameter	Value
Lowest input voltage, $V_{in\ min}$	12 V
First input voltage source, V_{in1}	12 V
Second input voltage source, V_{in2}	24 V
Third voltage source, V_{in3}	48 V
Output voltage, V_o	190V
Output current, I_o	5.2 A
Output power, P_o	1000 W
Switching frequency, f_s	100 kHz
Voltage gain, M_{VDC}	15.7
Duty cycle, d_n	0.66 ~ 0.8
Phase shift	120°
Voltage ripple in C_1, ΔV_{cp1}	50 V

Voltage ripple in C_2, $\Delta Vcp2$	100 V
Output voltage ripple, ΔV_o	2 V
Inductors, L_1, L_2, L_3	47 μH
Capacitor C_1	0.1 μF
Capacitor C_2	0.2 μF
Capacitor C_o	20 μF
Output load, R_o	33 Ω

Control signals *S1*, *S2* and *S3* are shown in Figure 4 with a phase shift $\varphi=120°$ and d=0.72 The voltages V_{L1}, V_{L2} and V_{L3} and currents I_{L1}, I_{L2} and I_{L3} are shown in Figures 5 to 7 respectively. They can be contrasted with the ideal waveforms of Figure 3 to verify the correct operation of the converter.

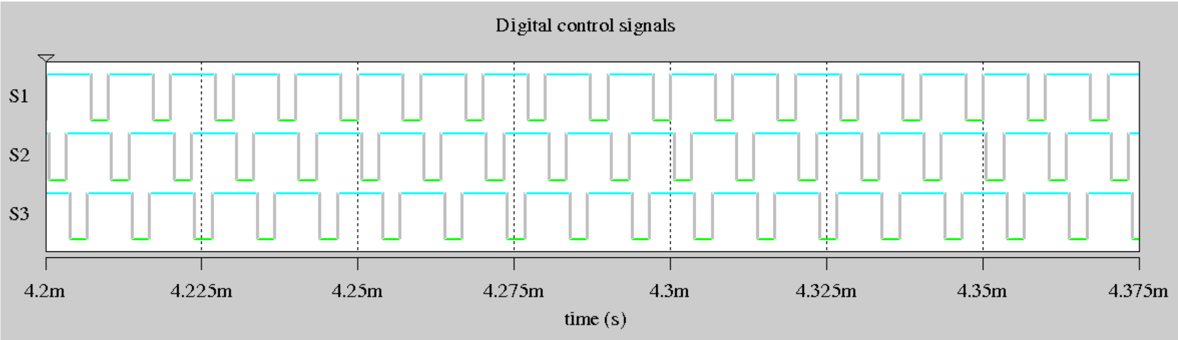


Figure 4. Simulation results for digital control signal *S1*, *S2*, *S3* with φ = 120° and *d* =0.72

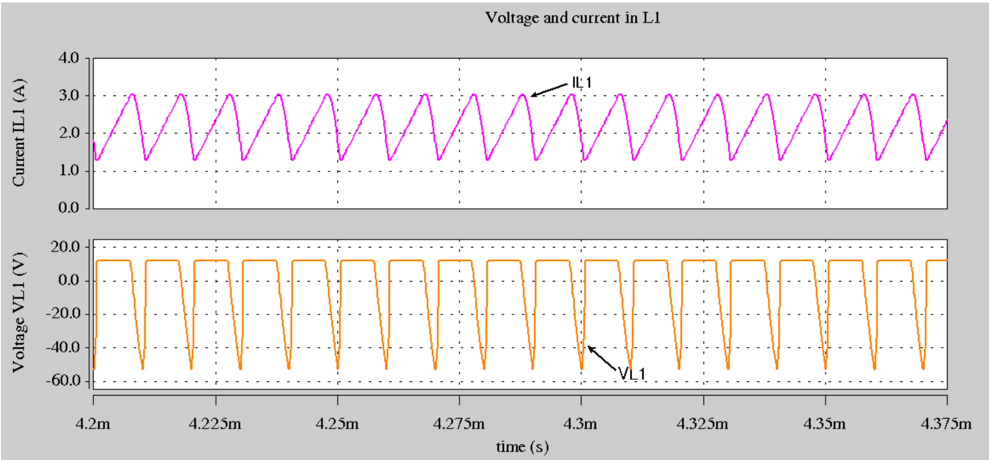


Figure 5. Simulation results for I_{L1} and V_{L1}.

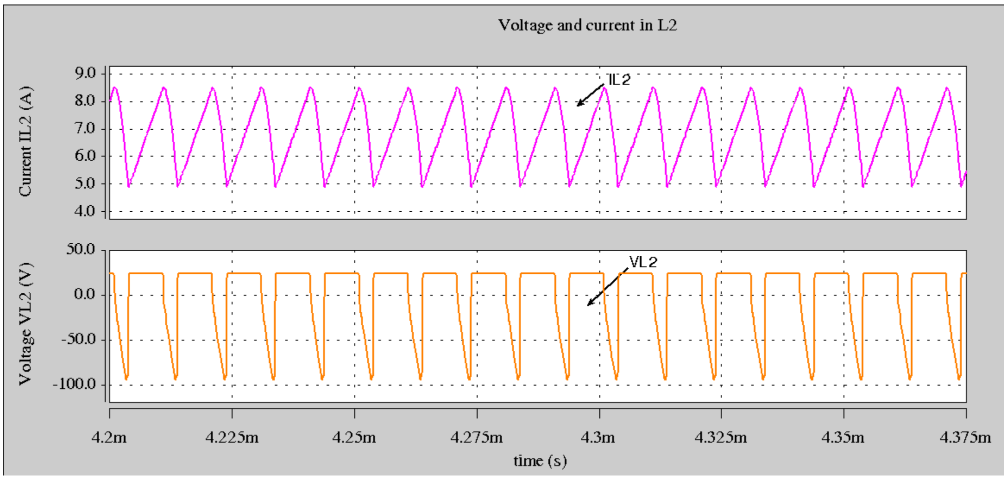


Figure 6. Simulation results for I_{L2} and V_{L2}.

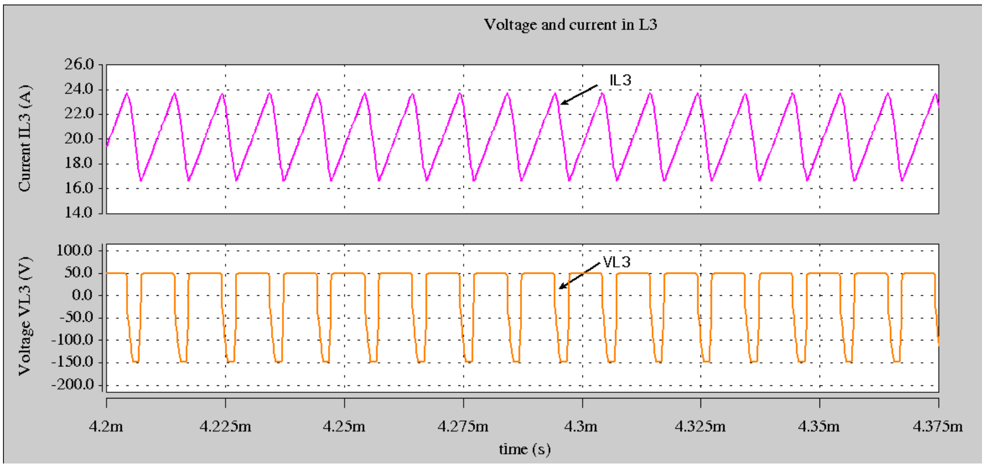


Figure 7. Simulation results for I_{L3} and V_{L3}.

Simulation results for output voltage and current, V_o and I_o are shown in Figure 8 with a DC (average) values V_{ODC} = 193.39 V and I_{ODC} = 5.52 A, getting an output power of P_o= 1.067 kW. The ripple voltage obtained ΔV_o = 951 mV.

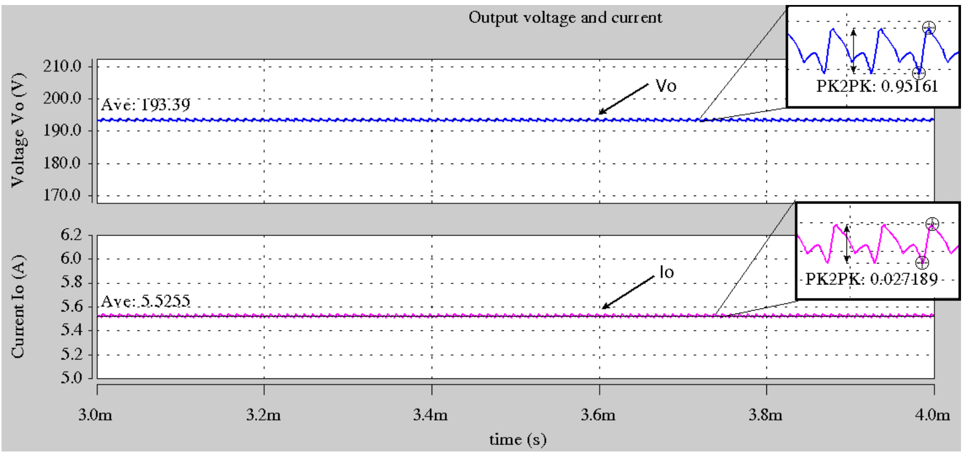


Figure 8. Simulation results for V_o and I_o.

4. Experimental Results

Considering that the maximum drain-source voltage is the output voltage, SiC transistors CMF20120, and diodes C3D06060 were employed to reduce switching losses in the implemented prototype. The NXP TWR–KV 58F220 microcontroller was used to generate the PWM pulses with a phase shifted of 120°.

The efficiency of the converter is determined by:

$$\eta = \frac{P_o}{P_{in_1} + P_{in_2} + P_{in_3}}, \tag{15}$$

The measure input current values were:

$$I_{in_1} = 18.5A,\ I_{in_2} = 12.5A,\ I_{in_3} = 11.5A$$

$$V_{in_1} = 24V,\ V_{in_2} = 12V,\ V_{in_3} = 48V$$

The implemented prototype can be seen in Figure 9, where the main components are indicated. Output voltage and current are shown in Figure 10; obtained multimeter meaurements are 190.9 V_{DC} and 5.4 A_{DC}. In Figure 11, it can be seen that the output voltage is 192.09 V_{DC} with ripple voltage of 1.005 V_{RMS} resulting in an output power of P_o= 1.037 kW.

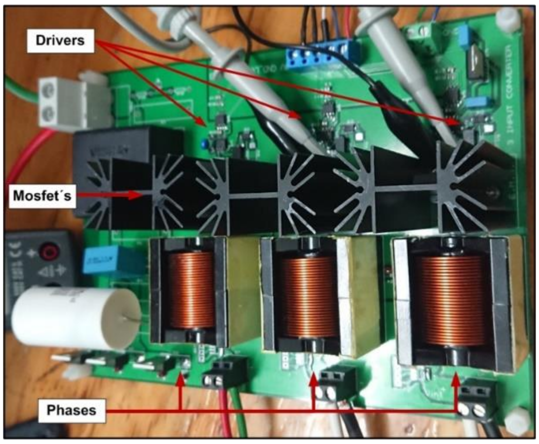


Figure 9. Implemented 1 kW prototype.

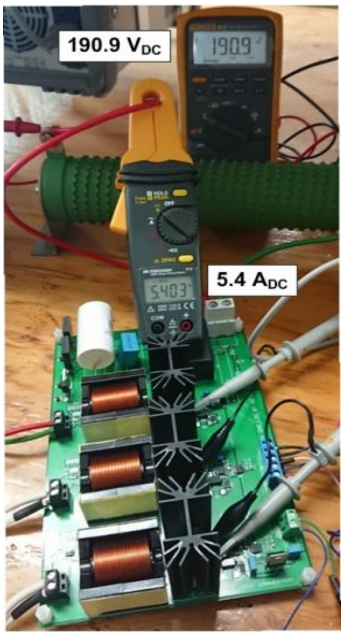


Figure 10. Implemented 1 kW prototype with voltage and current measures.

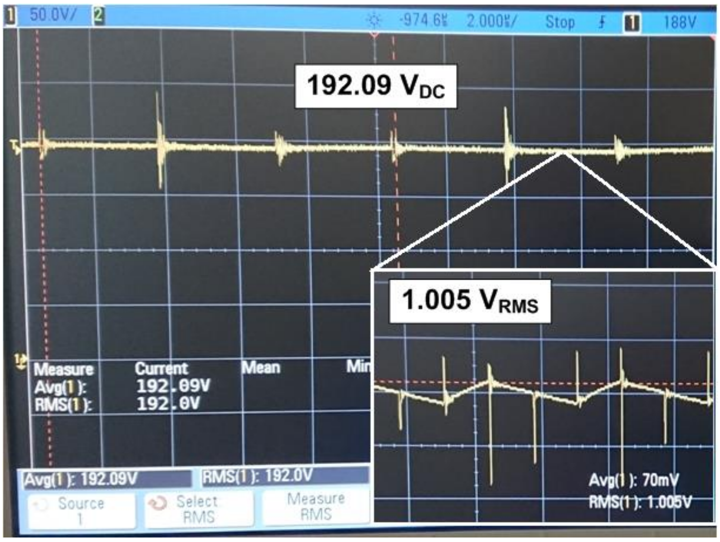
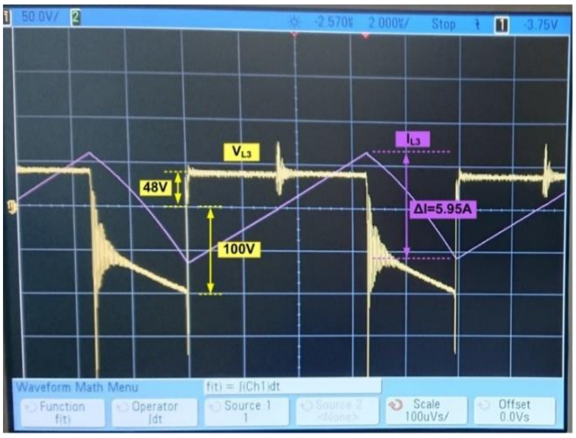


Figure 11. Experimental results $V_o = 192.09$ V_{DC}, $\Delta V_o = 1.005$ V

In Figure 12 voltage and current waveforms of inductors L_1, L_2 and L_3 are show. Positive amplitudes in voltage waveforms are approximately equal to the value of the corresponding input voltage supply. A straightforward comparison of these waveforms with the ideal waveforms of Figure 3 validates the experimental results.

(a)

(b)



(c)

Figure 12. Experimental results: (a) V_{L1} *and* I_{L1}, input voltage V_{in1} = 12 V, **(**b) V_{L2} *and* I_{L2}, input voltage V_{in2} = 24 V, (c) V_{L3} *and* I_{L3}, input voltage V_{in2} = 48 V

According to (15), and using the input voltages and currents, the efficiency obtained is η=90.51%. Figure 13 shows the experimental set up: a) three-input step-up converter, b) three input voltage sources, c) the PWM signal generator and d) the 33 Ω output load.

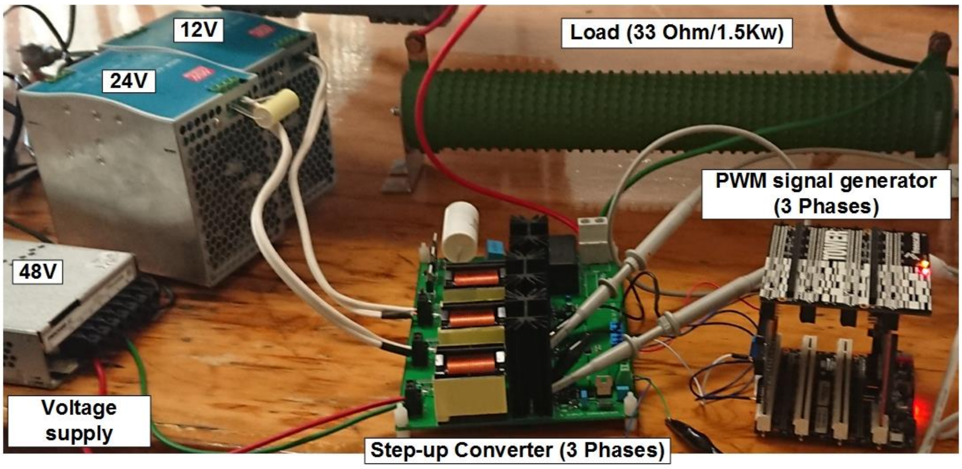


Figure 13. Experimental prototype with three input voltage sources, 33 Ω output load and the PWM signal generator

A comparison between the proposed converter and similar topologies is summarized in Table 3. The implemented converter provides the highest output power keeping a high efficiency considering three voltage sources in its design. The number of energy storage elements is less than the converters proposed in [9], [11-12] and [15]. The high switching frequency (100 kHz) is a factor to reduce its implementation size.

Table 3. A comparison between the proposed converter and similar topologies

Factor/Topologies	Proposed High-Gain Three-Input Step-Up Converter	High step-up multi-input multi-output converter [9]	Soft-switched step-up converter [10]	Modular step-up converter [11]	High-Gain Two-Input Step-Up Converter [12]	Multi-phase Buck Converter [14]	Multi-input multi-output [15]

Open-loop current unbalance	Minimum	Minimum	Minimum	Medium	Minimum	Medium	Medium
Output power	1.037 kW	1 kW (divided in 2 outputs)	125 W	200 W	500 W	152 W	100 W
Efficiency	90.51%	75% - 96.8%	97%	87%	90% - 95%	87% - 95%	86%
Number of voltage sources	3	4	2	2	2	2	2
Number of power switching devices	3	4	4	7	2	5	4
Number of diodes	3	7	4	1	2	2	6
Number of inductors	3	7	3	4	2	1	3
Number of capacitors	3	4	3	4	2	1	5
Switching frequency	100 kHz	40 kHz	100 kHz	25 kHz	100 kHz	10 kHz	100kHz

4. Conclusions

A high-gain three-input step-up converter of 1kW was analysed, designed, and implemented. The design procedure was validated through experimental results. In addition, the converter efficiency and reliability were verified, obtaining a power of 1037 W with an efficiency of 90.51%, which is superior to similar proposals. The converter topology can be used for a wide range of applications; in particular, the topology could be used as a low-cost alternative to jointly use several renewable sources that may be backed up by a non-renewable source, allowing the prioritization of power sources at any time. Based on the obtained results, it can be said that the converter topology can be used for higher powers, and more inputs

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

V_{in1}, V_{in2}, V_{in3}	Three input voltages
Φ	Control signals phase shift
d	Duty cycle in switching devices
d_{min}	Minimum duty cycle
$S1$, $S2$, $S3$	Digital control signals in each transistor
L_1, L_2, L_3	Inductors for each input voltage source

I_{L1}, I_{L2}, I_{L3}	Currents in inductor L_1, L_2 and L_3
ΔI_1, ΔI_2, ΔI_3	Ripple current in L_1, L_2 and L_3.
C_1, C_2	Capacitors in boost circuits in first and second inputs
V_{C1}, V_{C2}	Voltage in capacitors C_1 and C_2
D_1, D_2, D_3	Diodes in boost circuits for each input
C_o	Output capacitor
V_o	Output DC voltage
R_L	Output load
Δt1 to Δt6	Time interval in each operating mode
M1 to M6	Operating modes 1 to 6
x_1 to x_6	State variables in state space analysis
V_{inmin}	Minimum input voltage
M_{VDC}	Voltage gain
f_s	Switching frequency
$sw_{n,\ n=1,2,3}$	State of switches S_1, S_2 and S_3
I_o	Output current
ΔV_{c1}, ΔV_{c2}	Ripple voltage in C_1 and C_2
V_o	Output voltage
ΔV_o	Output voltage ripple
P_o	Output power
P_{in1}, P_{in2}, P_{in3}	Input power for each voltage source
η	Converter efficiency.

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