Review

Reduced Loss Tristate Converters

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Review

Reduced Loss Tristate Converters

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Abstract: In a tristate converter the basic circuit topology is extended by an additional electronic switch and an additional diode. Three modes follow each other within one switching period. During the first mode M1 both electronic switches are on and both diodes are off. In the second mode M2 only the second switch is on and the first diode is conducting, and in mode M3 only the second diode is conducting. The voltage transformation ratio is a function of the two duty cycles of the electronic switches. In a typical tristate converter current is flowing through the second switch during the first two modes. In the converters treated here the current is flowing through the second switch only during the second mode, so the losses are reduced compared to the normal tristate converter. This is shown for the Buck, the Buck-Boost, the Boost, the Zeta, the Cuk, the Super-Boost, the quadratic Buck, and a reduced duty cycle converter. The voltage transformation ratios are depicted in diagrams. As an example the reduced loss tristate Buck is used to demonstrate the derivation of the large and the small signal models. The transfer functions are also calculated and Bode plots are shown for an operating point. The voltage and the current stress of the converters are analyzed. The considerations are proved by simulations with the help of LTSpice.

Keywords: DC/DC converter; tristate; Buck; Boost; Buck-Boost; Zeta; Cuk; Super Boost; quadratic Buck; large and small signal model

1. Introduction

DC/DC converters are used to transfer a DC input voltage into a DC output voltage. Nearly all electric and electronic systems need these converters. The basic topologies are described in the textbooks of Power Electronics, e.g. [1–3]. But many other topologies can be found in the literature. A basic text about the construction of DC/DC converter topologies is [4]. A vast amount of step-up converter topologies can be found in [5]. More than hundred step-up, step-down and step-up-down topologies can be seen in [6]. Converters may have more than two pairs of connectors. A valid concept study of three terminal converters is given in [7]. Converters with reduced duty cycles are given in [8]. Here now tristate converters are investigated. A basic text is [9] where this tristate method is explained with a Boost converter. The electronic switch of a converter is replaced by a series connection of two electronic switches and an additional diode, connected to the connection point of the two active switches. In [10] this method is applied to several other converter topologies. Another extension of the tristate concept can be found in [11], where it is applied to coupled coil converters. In this case three possibilities exist to influence the voltage transformation ratio: the duty cycles of the two active switches and the winding ratio. The papers [12] and [13] show a topology change of the tristate Boost converter. The forward losses are reduced, due to this change of the position of the second switch. A combination of two tristate Buck-Boost converters is shown in [14]. The two converters are driven by control signals which are shifted by 180°, the so-called interleaved concept. The inductor of a half-bridge Boost converter is shunted by a diode and a transistor in [15]. In this case it is used to achieve ZVS (zero voltage switching). The converters with a quadratic term in the voltage transformation ratio are also interesting candidates for using the tristate conception. The basic text for these converters is [16]. The transfer function of converters with step-up behavior have a non-

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phase-minimum behavior. The design of the controller therefore leads to slower control, caused by the additional shift of minus ninety degrees, due to the zero (or n-time 90° for n positive zeros) in the right-hand side of the complex plane. A control study for the Boost converter can be found in [17–19]. The control of the Buck-Boost converter is treated in [20]. A dual output tristate converter is analyzed in [21].

The basic function of a reduced loss tristate (RLT) converter is now shown with the help of the Buck converter. The circuit diagram of the Buck converter is shown in Figure 1.

The converter consists of an electronic (active) switch S1, a diode (passive switch) D2, an inductor (coil) L1, and a capacitor C1. Parallel to the capacitor there are the output terminals to which the load R is connected. The input voltage U1 is connected to the input terminals.

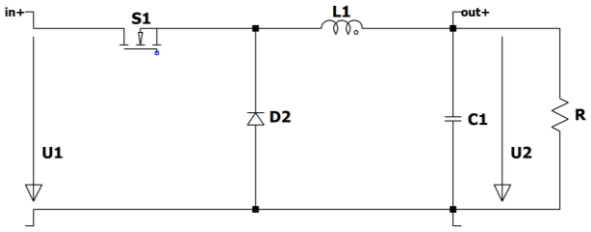

Figure 1. Circuit diagram of the Buck converter.

To transform the converter into a tristate converter, the electronic switch S1 is replaced by two electronic switches S1, S2 and a diode D1, which is connected to the connection point between the two active switches. The circuit diagram is depicted in Figure 2. The operation of this converter can be described by three modes which follow each other during one switching period. During mode M1 both active switches S1 and S2 are on. The input current which is equal to the current through the inductor is flowing through them. Both diodes are off. When the first active switch is turned off, mode M2 begins. The diode D1 turns on, and the current through the coil commutates into the diode D1. It is easy to see that the inductor is now nearly short-circuited (only the onward losses across S2 and D1 produce a small negative voltage), and the current through it therefore stays nearly constant. When the second switch S2 is turned off, too, mode M3 starts. Now the current through the coil has to commutate into the diode D2.

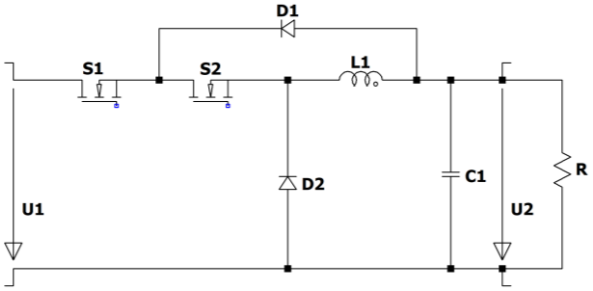

Figure 2. Circuit diagram of the tristate Buck converter.

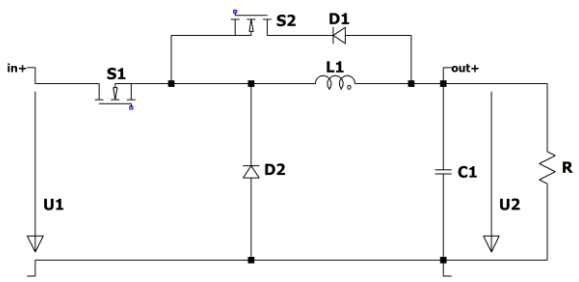

Figure 3. Circuit diagram of the RLT Buck converter.

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It is evident that in mode M1 and M2 the current is flowing through the active switches and produces forward losses. When the position of S2 is changed as shown in Figure 3, the losses are reduced because only in mode M2 current is now flowing through S2, and the over-all forward losses are reduced. This concept is now applied to several typical DC/DC converters and described in the next section.

2. Application of the Reduced Loss Tristate Concept

We start with the three basic single coil converters. These converters consist of an electronic switch S1, a diode D2, an inductor L1 and a capacitor C1. The input voltage U1 is connected to the input terminals, the load is connected to output terminals which are parallel to the capacitor. In the later part of this section the Zeta, the Cuk, the Super-Boost, the quadratic Buck, and the D1/(1-D1-D2) converter are used as examples. During mode M1 both switches are turned on at the same time and after the time interval d1·T S1 is turned off, and after the time interval d2·T the second switch turns off. Mode M1 takes d1·T and mode M2 takes (d2-d1)·T. Mode M3 takes (1-d2)·T. It should be mentioned that S2 can be turned on later within mode M1, but d2 is defined as the time interval between turn off of S2 and turn on of S1.

2.1. Reduced Loss Tristate Buck Converter

The circuit diagram of the RLT Buck is shown in Figure 3.

During mode M1 (both switches are on) the difference between the input and the output voltages is across the coil and the current through the coil increases. When the first switch S1 is turned off and the second switch S2 is still on, the current through the coil commutates into the first diode D1 and the current through the coil stays nearly constant. When the electronic switch S2 is turned off, mode M3 begins and the diode D2 turns on. The voltage across the coil is now the negative output voltage U2. If S1 and S2 are switched on contemporarily and their duty cycles are d1 and d2 respectively, the voltage-time balance can be expressed as

$$(U_1 - U_2)d_1 = |-U_2|(1-d_2) \tag{1}$$

leading to the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1}{1+d_1-d_2} \tag{2}$$

The voltage transformation ratio now has two possibilities to be influenced. Fig. 4 shows the voltage transformation ratios for the constant duty cycle d2 of the second switch and the duty cycle d1 of the first switch as variable. The straight line is the voltage transformation ratio of the classical Buck converter. Using this control method, the output voltage increases more for low duty cycles and changes less for higher duty cycles of the first electronic switch.

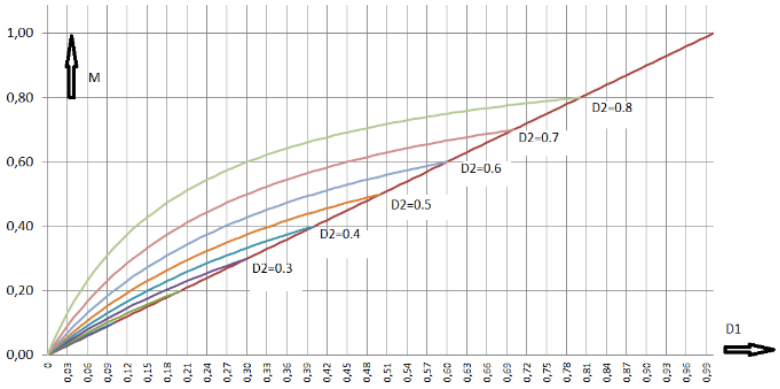

Figure 4. Voltage transformation ratio of the RLT Buck: duty cycle of switch S2 is kept constant, duty cycle of switch S1 is used as variable.

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The straight line in Fig. 4 represents the voltage transformation ratio of the normal Buck. The curves are the voltage transformation ratios of the tristate converter. If the duty cycle d2 is smaller than d1, the converter works like the normal Buck converter, and the voltage transformation ratio in dependence on d1 is linear. But when d1 is smaller than d2, the voltage transformation ratio is curved. When the curve reaches the linear line, the voltage transformation follows the line. At the point where the curve meets the straight line, the parameter for d2 is written. So it is easy to find the correct line.

One can also control the circuit by keeping the duty cycle d1 constant and using the duty cycle d2 of the second switch as variable. This is shown in Fig. 5. The straight line is the normal Buck. For low duty cycles of d2 the voltage transformation rate is hardly changing, but for higher duty cycles the derivative of the voltage transformation ratio is larger than the one of the classical Buck.

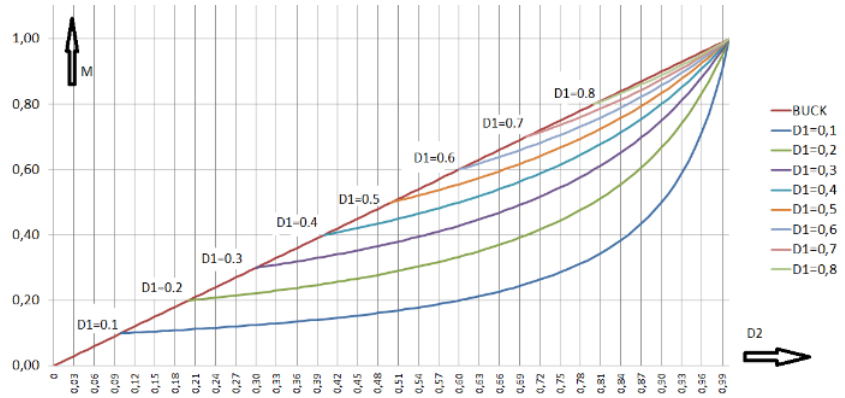

Figure 5. Voltage transformation ratio of the RLT Buck: duty cycle of switch S1 is kept constant, duty cycle of switch S2 is used as variable.

In Fig. 5 the voltage transformation ratio follows first the straight line and when the duty cycle of S2 is higher than the one of S1, the curve diverges. The parameter is always written at this point.

It should be mentioned that it is not necessary to turn on the second switch synchronous with the first switch. During M1 the switch S2 is on but no current is flowing through it. Therefore, one can turn it on later, but during the on-time of switch S1. To achieve the voltage transformation ratio according to (2) the second switch must be turned on before the first switch is turned off. In this case, variable d2 in (1) and (2) is not the duty cycle of S2, but is related to the time interval between the turn-on of switch S1 and the turn-off of switch S2.

When switch S2 is not turned on, the current commutates immediately into the diode D2 and the converter works as the basic converter without S2 and D1. When the switch S1 is longer on than the switch S2, the converter also works as a traditional converter and has the same voltage transformation ratio as the original one.

When the switch S2 is only turned on during M3, with the duty cycle d2_2 as the on-time of S2 during the off-time of S1 referred to the switching period, the voltage-time balance is

$$(U_1 - U_2)d_1 = |-U_2|(1 - d_1 - d_{2\_2}) \tag{3}$$

leading to the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - d_{2\_2}} \tag{4}$$

The duty cycle d2_2 must be smaller than (1-d1). In this paper only the first concept is treated because one switching transient is avoided and its switching loss omitted. Furthermore, this leads to linearization of the voltage transformation ratio of converters with step-up possibility and can lead to a phase-minimum system.

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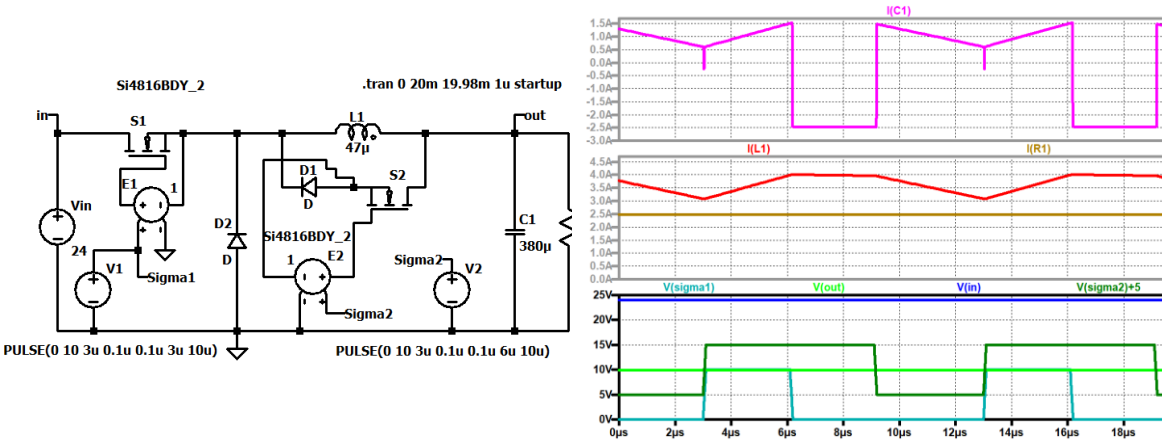
Figure 6 shows the current through the capacitor, the current through the coil, the load current, the input voltage, the control signal of the second switch, the output voltage, and the control signal of S1. The spike of the current through the capacitor is caused by charging the parasitic capacitors of the diodes, when the switches turn on again the voltage must change across the diodes.



(**a**) (**b**)

Figure 6. RLT Buck converter, **(a)** simulation circuit and **(b)** up to down: current through the capacitor (violet); current through the coil (red), load current (brown); input voltage (blue), control signal of the second switch (dark green, shifted), output voltage (green), control signal of S1 (turquoise).

2.2. Reduced Loss Tristate Buck-Boost Converter

The circuit diagram of the RLT Buck-Boost converter is shown in Figure 7. During mode M1 the input voltage is across the coil, during mode M2 nearly zero voltage, and during M3 the negative output voltage is across the inductor.

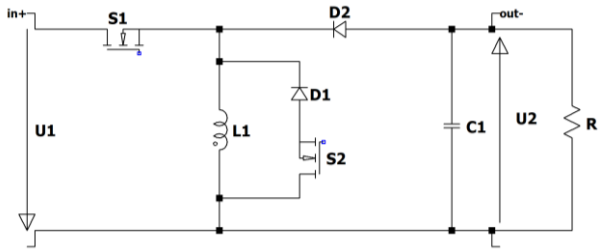


Figure 7. Circuit diagram of the RLT Buck-Boost converter.

The voltage-time balance is therefore

$$U_1 d_1 = U_2 (1 - d_2) \tag{5}$$

leading to the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - d_2}. \tag{6}$$

From (6) one can see that for a constant duty cycle d2 of S2 the voltage transformation ratio is a linear function of the duty cycle d1 of the switch S1, depicted in Fig. 8.

Figure 9 shows the voltage transformation ratio for a fixed duty cycle of S1 and a variable duty cycle of S2. When the duty cycle d2 is smaller than d1, the converter works as a normal Buck-Boost. When the duty cycle d2 is higher than d1, the converter works in the actual tristate mode. The derivative of the voltage transformation is lower and the voltage transformation ratio is still nonlinear.

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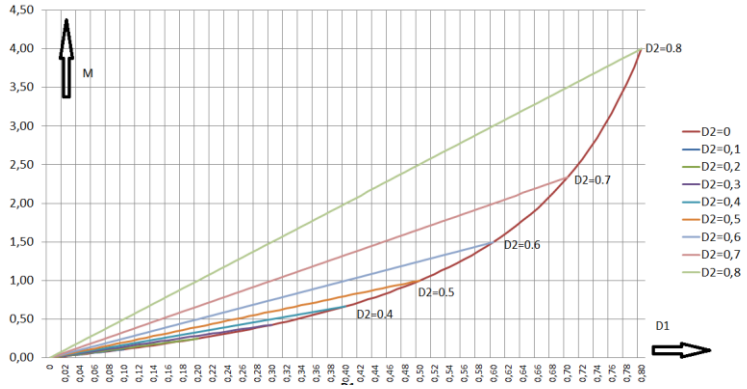


Figure 8. Voltage transformation ratio of the RLT Buck-Boost: duty cycle of switch S2 is kept constant, duty cycle of switch S1 is used as variable.

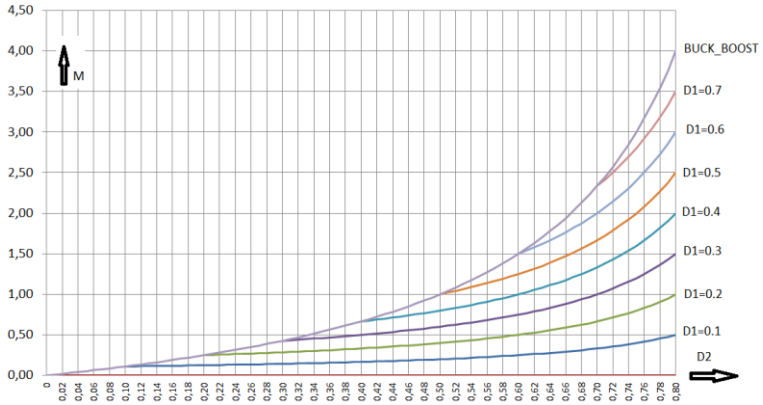
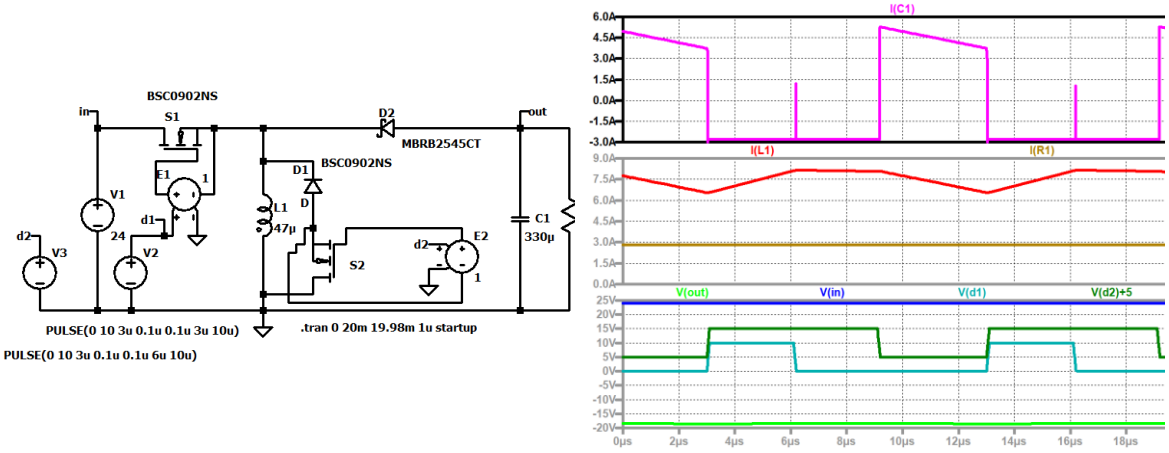


Figure 9. Voltage transformation ratio of the RLT Buck-Boost: duty cycle of switch S1 is kept constant, duty cycle of switch S2 is used as variable.

Figure 10 again shows the current through the output capacitor, the current through the coil, the current through the load, the input voltage, the control signal of the second switch S2, the control signal of the first switch S1, and the output voltage. The spike occurs when the voltages across the semiconductors change when S1 turns off.



(**a**) (**b**)

Figure 10. RLT Buck-Boost converter, **(a)** simulation circuit, and **(b)** up to down: current through the output capacitor (violet); current through the coil (red), load current through the load (brown); input voltage (blue), control signal of the second switch (dark green), control signal of the first switch S1 (turquoise), output voltage (green).

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2.3. Reduced Loss Tristate Boost Converter

The circuit diagram of the RLT Boost converter is given in Figure 11.

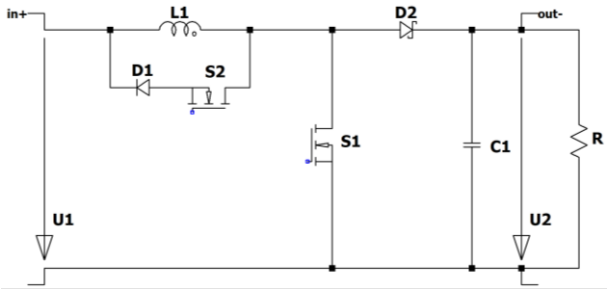

Figure 11. Circuit diagram of the RLT Boost Converter.

During mode M1 the input voltage is across L1, during M2 the coil is short-circuited, and during M3 the difference between the input and the output voltages is across the coil. For the voltage-time balance one can write

$$U_1 d_1 = |U_1 - U_2|(1 - d_2). \tag{7}$$

This leads to the voltage transformation ratio according to

$$M = \frac{U_2}{U_1} = \frac{1 + d_1 - d_2}{1 - d_2} \quad \text{with} \quad d_2 \geq d_1 \tag{8}$$

If the duty cycle d2 is smaller than d1, the converter works as a normal Boost converter. One can easily see that the voltage transformation ratio is a linear function of d1 when the duty cycle d2 is kept constant (Figure 12).

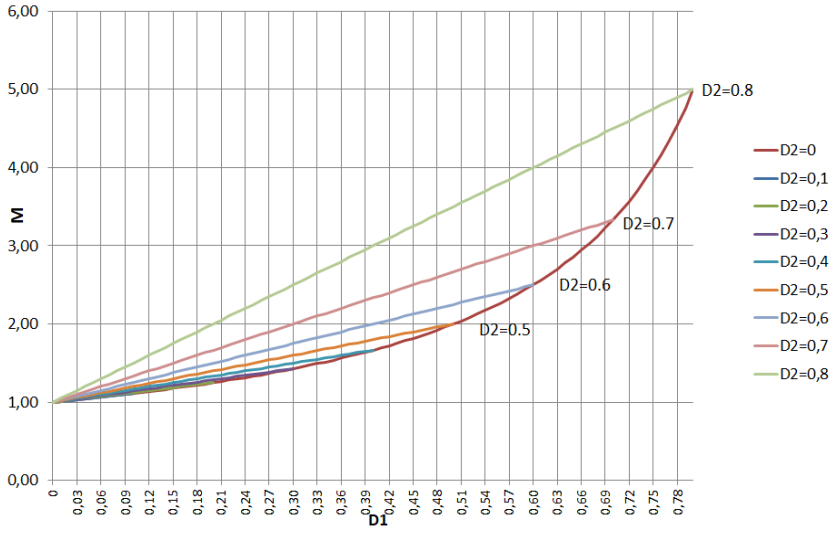

Figure 12. Voltage transformation ratio of the RLT Boost converter with fixed duty cycle d2 and the duty cycle d1 as variable.

Figure 13 shows the voltage transformation ratio with fixed duty cycle of the first switch S1 and a variable duty cycle of the second switch S2. As long as the duty cycle d2 is smaller than the duty cycle d1, the converter works as a normal Boost converter. When d2 is greater than d1, the converter operates in the tristate mode and the derivative of the voltage transformation ratio is reduced.

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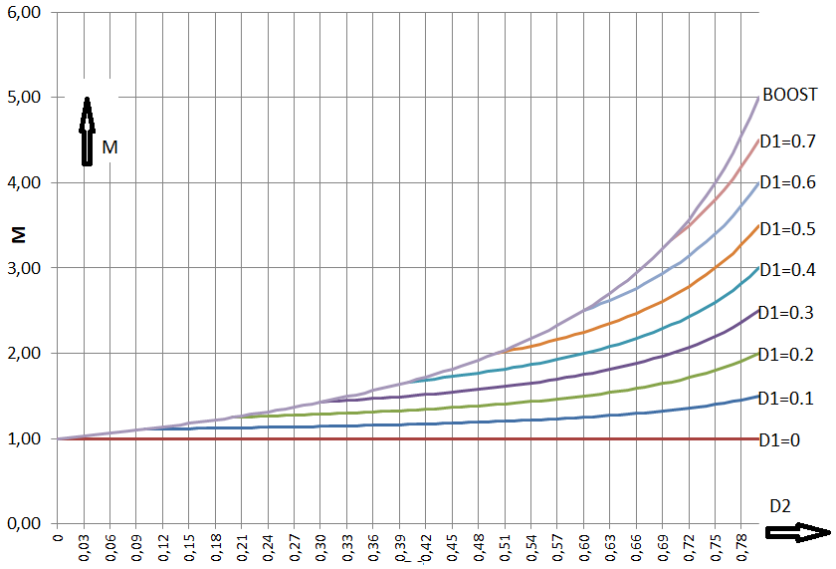
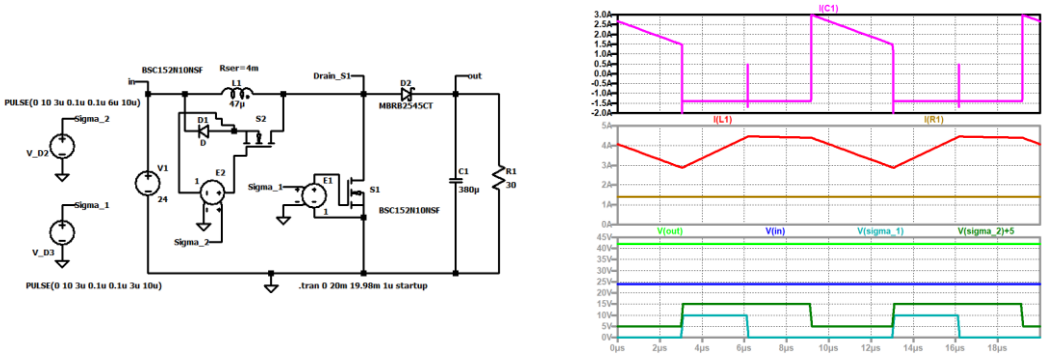


Figure 13. Voltage transformation ratio of the RLT Boost converter with fixed duty cycle d1 and the duty cycle d2 as variable.

Figure 14 shows a simulation with the current through the capacitor, the current through the coil, the load current, the input voltage, the control signal of the second switch, the output voltage, and the control signal of S1. The spike occurs when the voltages across the semiconductors change when S1 turns off.



(**a**) (**b**)

Figure 14. RLT Boost Converter, **(a)** simulation circuit, and **(b)** up to down: current through the capacitor (violet); current through the coil (red), load current (brown); output voltage (green), input voltage (blue), control signal of the second switch (dark green), control signal of S1 (turquoise).

2.4. Reduced Loss Tristate Zeta Converter

The Zeta converter is a step-up-down converter. When the circuit is applied to a stable input voltage no inrush occurs. With the switch S1 the capacitor C1 can be charged with limited input current. In the case of an error, the switch S1 can also be used as an electronic fuse. The circuit diagram of the RLT-Zeta is shown in Figure 15.

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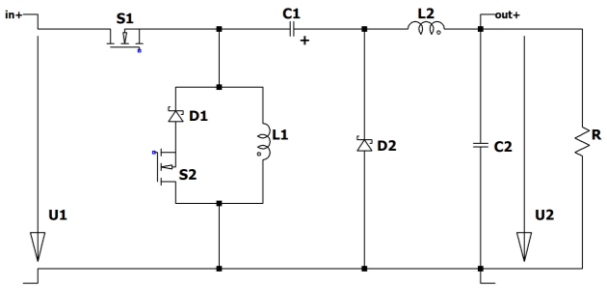


Figure 15. Circuit diagram of the RLT-Zeta converter.

During M1 the input voltage U1 is across the first inductor L1, during M2 the inductor is short-circuited, and during M3 the voltage across C1 is with negative polarity across L1. The voltage-time balance is therefore

$$U_1 d_1 = \left| -U_{C1} \right| (1 - d_2). \tag{9}$$

It can immediately be seen (the voltages across the inductors are zero in the mean) that in the steady state the voltage across C1 is equal to the output voltage U2

$$U_2 = U_{C2} = U_{C1} \tag{10}$$

The voltage transformation ratio is equal to the one of the RLT Buck-Boost converter

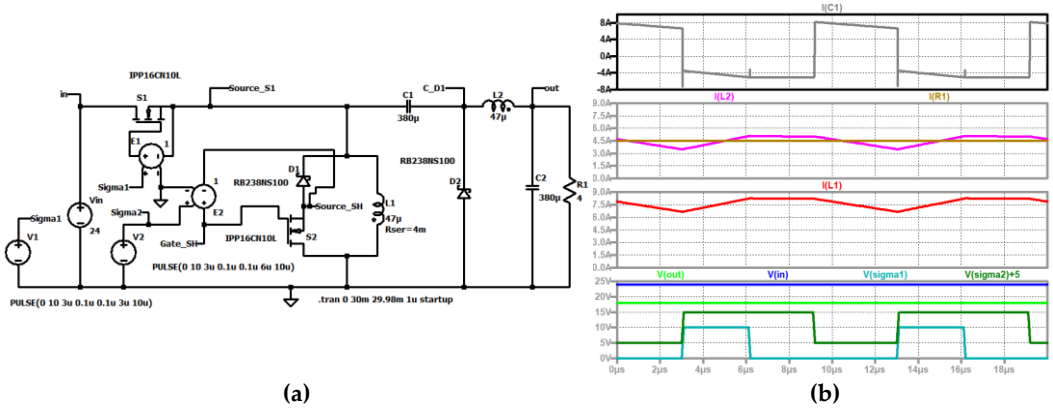
$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - d_2} \quad \text{with} \quad d_2 \geq d_1 \tag{11}$$

The diagrams of the voltage transformation ratio in dependence on one duty cycle with the other duty cycle as variable are shown in Figure 8 and Figure 9.

The voltage across the second coil has the same form as the voltage of the first coil. One could combine both windings on the same magnetic core (integrated magnetics).

When the duty cycle d2 is smaller than d1, the converter works like a normal Zeta converter with the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - d_1} \tag{12}$$



(a) **(b)**

Figure 16. RLT ZETA converter, **(a)** simulation circuit, and **(b)** up to down: current through the intermediate capacitor C1 (grey); current through the second coil L2 (violet), load current (brown); current through the first coil L1 (red); input voltage (blue), output voltage (green), control signal of the second switch (dark green), control signal of first switch (turquoise).

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A simulation of the steady state is shown in Figure 16. The signals are the current through the intermediate capacitor C1, the current through the second coil L2, the load current, the current through the first coil L1, the input voltage, the output voltage, the control signal of the second switch S2, and the control signal of S1.

A second possibility to get an RLT Zeta converter is by placing the diode D1 and the switch S2 in parallel to the output coil L2. This leads to the same voltage transformation ratio, but the circuit has now no continuous output current. Instead of L2, C2 and the load R the armature winding of a DC machine can be connected to obtain a motor driver.

2.5. Reduced Loss Tristate Cuk Converter

The Cuk converter has continuous input and output currents and operates as an inverting step-up-step-down converter. Figure 17 shows the circuit diagram of the RLT Cuk converter. Figure 18 shows the same signals as Figure 16.

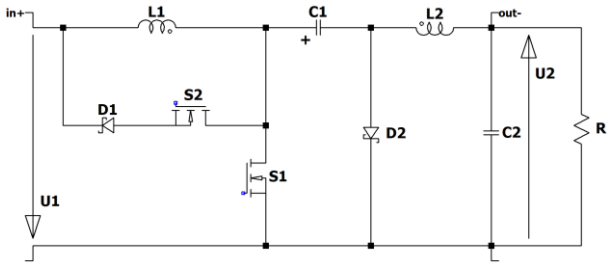
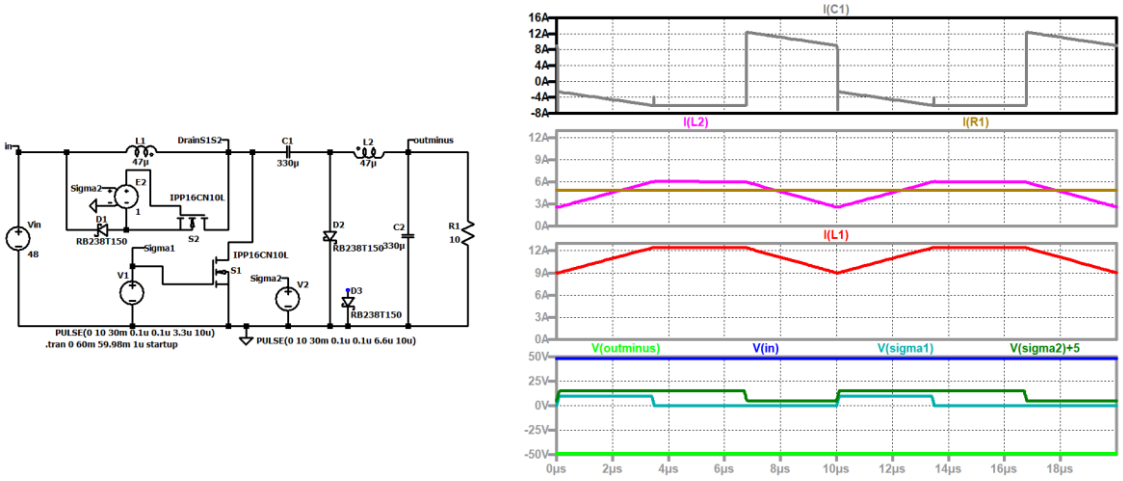


Figure 17. Circuit diagram of the RLT Cuk converter.



(**a**) (**b**)

Figure 18. RLT CUK converter, **(a)** simulation circuit, and **(b)** up to down: current through the intermediate capacitor C1 (grey); current through the second coil L2 (violet), load current (brown); current through the first coil L1 (red); input voltage (blue), control signal of the second switch (dark green), control signal of the first switch (turquoise), output voltage (green).

During mode M1 the input voltage U1 is across L1, L1 is short-circuited during M2, and during M3 the difference between the input voltage U1 and the voltage across C1 UC1 is across the coil L1 leading to the voltage-time balance

$$U_1 d_1 = \left|U_1 - U_{C1}\right|\left(1 - d_2\right). \tag{13}$$

Inspecting the circuit one can easily see that in the steady state the voltage across C1 UC1 must be equal to the input voltage U1 plus the output voltage U2

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$$U_{C1} = U_1 + U_2 . \tag{14}$$

leading to

$$M = \frac{U_2}{U_1} = \frac{d_1}{1-d_2}, \text{ with } d_2 \geq d_1 \tag{15}$$

The diagrams for the voltage transformation ratio in dependence on one duty cycle with the other duty cycle as variable are equal to the results in Fig. 8 and Fig. 9.

Figure 18 shows a simulation with the current through the intermediate capacitor C1, the current through the second coil L2, the load current, the current through the first coil L1, the input voltage, the control signal of the second switch S2, the control signal of the first switch S1, and the output voltage. During M2 the input current is zero and no more continuous.

By connecting S2 and D1 in parallel to the second inductor, a second variant of the RLT-Cuk (Figure 19) is obtained. In this case the output current is not continuous, but pulsating.

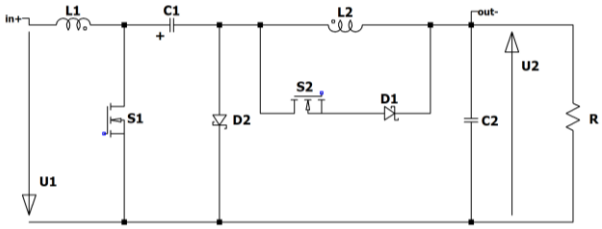

Figure 19. Circuit diagram of the RLT Cuk converter variant II.

A disadvantage of the Cuk converter is the large inrush current, when the converter is connected to a stable input source as car batteries. Fig. 20 shows a simulation with constant inductors. In reality the coils saturate and the current will be even higher. When the circuit is connected to the stable input voltage, both electronic switches are blocked. During the first half period diode D2 is on and the current through the coil L1, which is equal to the current into the circuit, is larger. When D2 turns off a damped ringing occurs between the inductors and the capacitors which form a series resonance circuit.

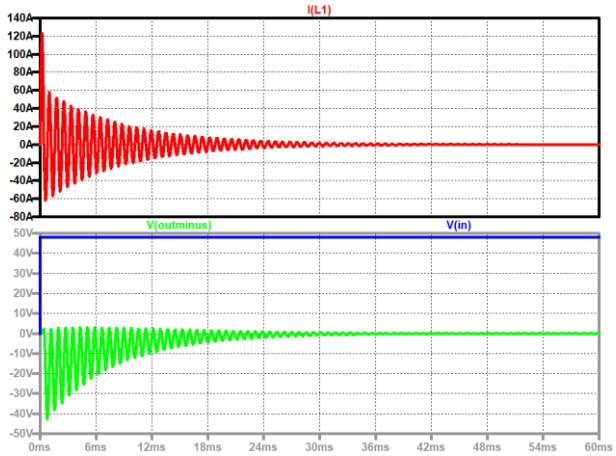

Figure 20. Inrush of a Cuk converter, up to down: current through inductor L1 (red); input voltage (blue), output voltage (green).

2.6. Reduced Loss Tristate Super-Boost Converter

The RLT Super-Boost converter (Fig. 21) has a continuous output current. During M1 the input voltage is across the first inductor L1, during M2 the coil is short-circuited, and during M3 the

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difference between the input voltage and the voltage across C1 is across the coil L1. The voltage-time balance is given by

$$U_1 d_1 = |U_1 - U_{C1}|(1-d_2). \tag{16}$$

When inspecting the loop L2, C2, L1, C1 it is obvious that the voltage across C1 must be equal to the output voltage. This leads to

$$M = \frac{U_2}{U_1} = \frac{1+d_1-d_2}{1-d_2}, \quad d_2 \geq d_1 \tag{17}$$

the same result as that of the RLT Boost converter. The diagrams Fig. 12 and Fig. 13 are also valid for the so called Super-Boost converter.

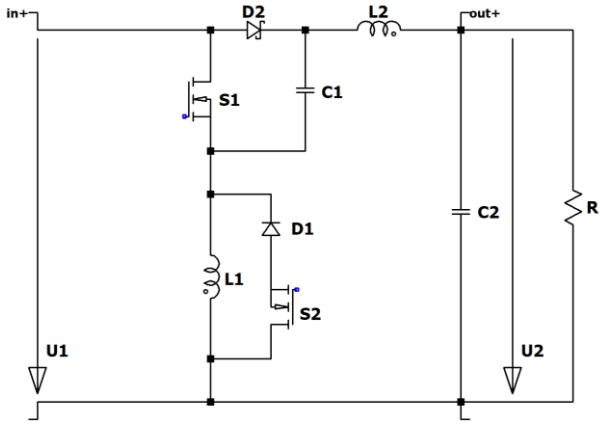
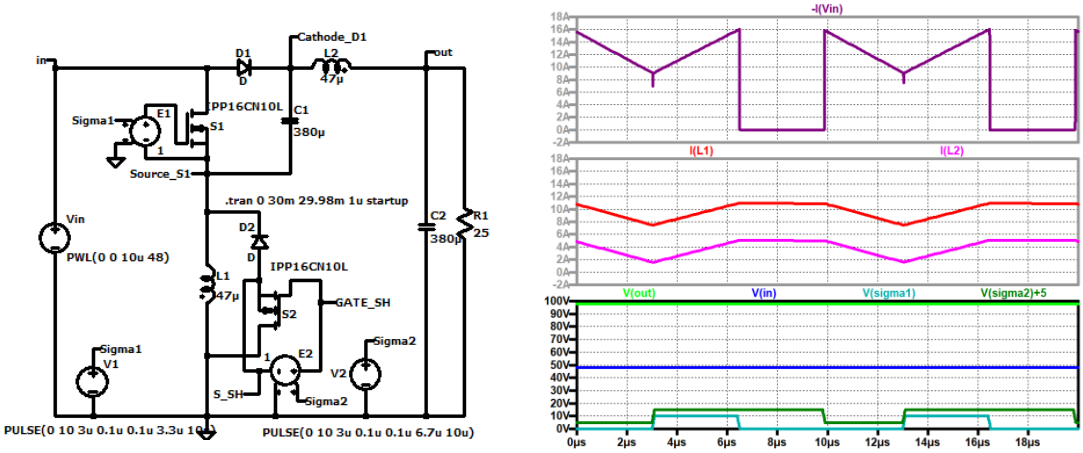


Figure 21. Circuit diagram of the Super-Boost converter.

An interesting aspect of the converter is that during the modes M1 and M3 the input current is the sum of the currents through both inductors.

Figure 22 shows a simulation with the current through the intermediate capacitor C1, the current through the second coil L2, the load current, the current through the first coil L1, the input voltage, the control signal *sigma2* of the second switch, the control signal of the first switch *sigma1*, and the output voltage U2.



(**a**) (**b**)

Figure 22. RLT Super-Boost converter, **(a)** simulation circuit, and **(b)** up to down: input current (dark violet); current through the first coil L1 (red), current through the second coil L2 (violet); output voltage (green), input voltage (blue), control signal of the second switch (dark green), control signal of the first switch (turquoise).

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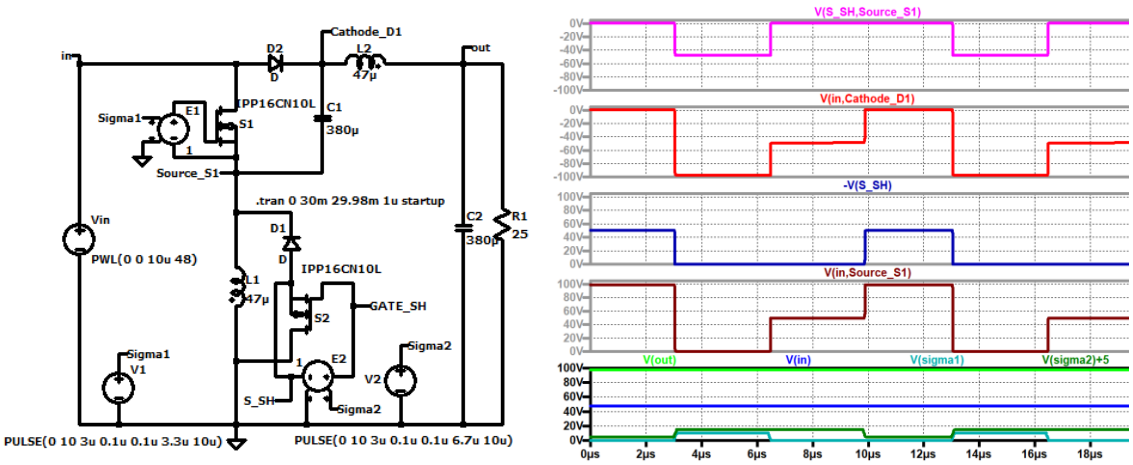
In steady state Figure 23 shows the signal diagrams of the voltages across the diodes D1 and D2, the voltages across the electronic switches S1, S2; the output voltage U2, the input voltage U1, and the control signals of the electronic switches. When S1 and S2 are on, the diode D1 has to block the input voltage, during M2 the diode is conducting and the voltage across it is equal to the forward voltage. During M3 the voltage across D1 is nearly zero. The voltage across D2 is equal to the voltage across C1 which is equal to the output voltage. During M2 the voltage is the difference between the input voltage and the voltage across C1. During M3, when the diode is conducting, only the small forward voltage can be seen. The electronic switch S1 is on during M1, has to block the input voltage during M2 and has to block the voltage across C1 during M3. Transistor S2 is on during M1 and M2, therefore the voltage across it is zero and has to block the difference between the voltage across C1 and the input voltage during M3.



(**a**) (**b**)

Figure 23. RLT Super-Boost converter, **(a)** simulation circuit, and **(b)** up to down: voltage across D1 (violet); voltage across D2 (red); voltage across S2 (dark blue); voltage across S1 (black); output voltage (green), input voltage (blue), control signal of the second switch (dark green), control signal of S1 (turquoise).

2.7. Reduced Loss Tristate D-Square Buck Converter

The quadratic Buck converter consists of a Buck stage built by the switch S1, the diode D3, the coil L2, the output capacitor C2, and a pre-stage built by the first inductor L1, two diodes D1 and D2 and the first capacitor C1. The basic text for converters with a quadratic term in the voltage transformation ratio is the paper [16]. When the switch S1 is turned on also the diode D1 is on, and when switch S1 is turned off also the diode D1 turns off and diode D2 turns on. The branch for the tristate operation is built by the second switch S2 and the fourth diode D4. The circuit diagram is depicted in Fig. 24.

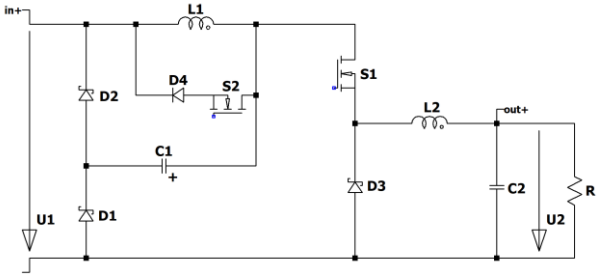


Figure 24. Circuit diagram of RLT d-square converter.

For the tristate operation the three modes follow each other again. During M1 the input voltage minus the voltage across C1 is across L1, and the difference between the voltage across C1 and the output voltage is across the second coil. When S1 turns off mode M2 begins. The current through L1

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commutates into the series connection of S2 and D4, D1 turns off, D2 is still off and D3 must turn on, and the current through L2 commutates into D3. When S2 is turned off, too, the current through L1 commutates into the branch C1 and D2. The capacitor C1 is now being charged. The voltage-time balance is therefore

$$\text{L1:}\quad (U_1 - U_{C1})d_1 = |-U_{C1}|(1-d_2), \tag{18}$$

$$\text{L2:}\quad (U_{C1} - U_2)d_1 = |-U_2|(1-d_1) \tag{19}$$

which leads to the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1^2}{1+d_1-d_2}, \quad d_2 \geq d_1 \tag{20}$$

Figure 25 shows the voltage transformation ratio of the RLT d-Square converter with the duty cycle of switch S2 as parameter and the duty cycle of switch S1 as variable. The black line shows the voltage transformation ratio of a quadratic Buck. For duty cycles of switch S2 lower than 0.5 nearly no difference exists referred to the simple quadratic converter. For duty cycles d2 higher the voltage transformation ratio is higher than that of the simple quadratic converter.

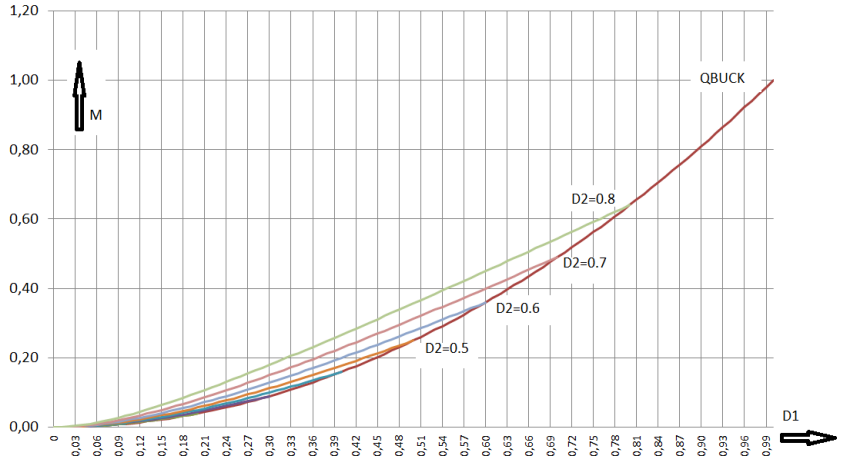

Figure 25. Voltage transformation ratio of the RLT d-square converter, duty cycle of switch S2 as parameter and duty cycle of switch S1 as variable.

Figure 26 shows the voltage transformation ratio of the RLT d-square converter with the duty cycle of switch S1 as parameter and the duty cycle of switch S2 as variable. The black line shows the voltage transformation ratio of a quadratic Buck. The lines are all under the line of the voltage transformation ratio of the quadratic Buck converter and their derivative is smaller.

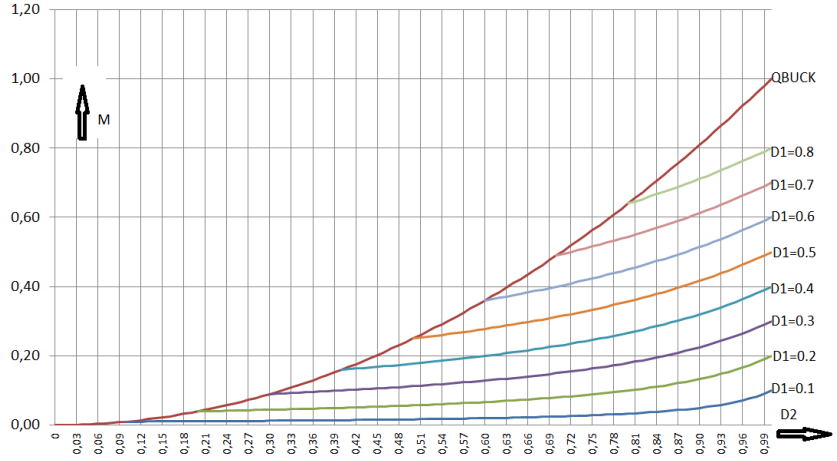

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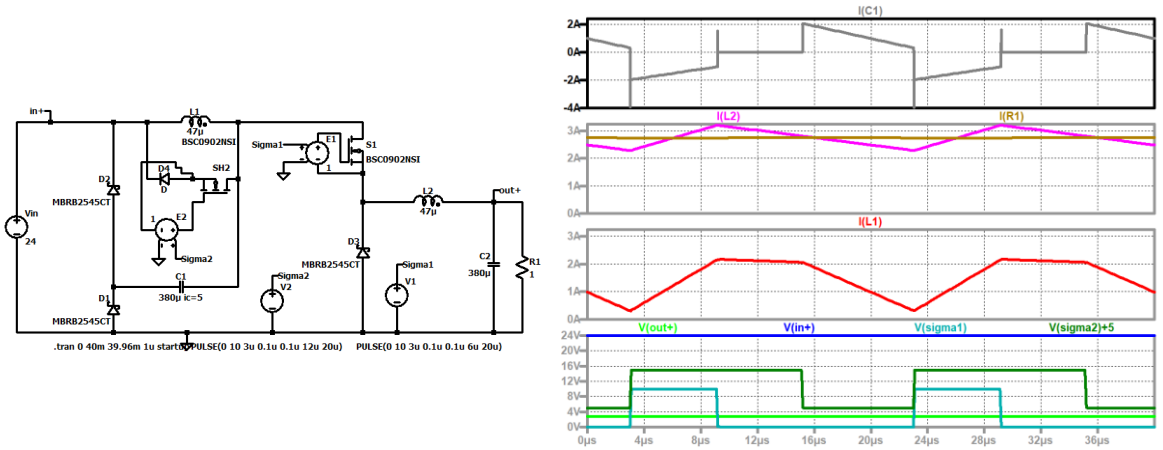
Figure 26. Voltage transformation ratio of the RLT d-square converter, duty cycle of switch S1 as parameter and duty cycle of switch S2 as variable.

Figure 27 shows the current through the intermediate capacitor C1, the current through the second coil L2, the load current, the current through the first coil L1, the input voltage, the control signal of the second switch S2, the output voltage, and the control signal of the first switch S1.



(a) **(b)**

Figure 27. RLT d-square Buck converter, **(a)** simulation circuit, and **(b)** up to down: current through the intermediate capacitor C1 (grey); current through the second coil L2 (violet), load current (brown); current through the first coil L1 (red); input voltage (blue), control signal of the second switch (dark green), output voltage (green), control signal of S1 (turquoise).

2.8. Reduced Loss Tristate D1/(1-D1-D2) Converter

This converter topology, shown in Figure 28, has an electronic switch in series to the input source. Therefore, no inrush current occurs when the converter is connected to a stiff input source. Another interesting feature is that the converter has a limited duty cycle range. An early study of these converters can be found in [8].

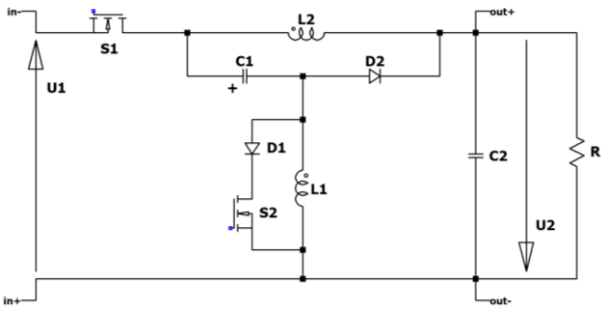


Figure 28. RLT D1/(1-D1-D2) converter.

During mode M1 the sum of the input voltage and the voltage across C1 is across L1. During M2 the L1 is short-circuited. During M3 the negative output voltage is across the first coil. It can be directly seen that the voltage across C1 must be equal to the output voltage in the mean. With

$$U_2 = U_{C2} = U_{C1} \tag{21}$$

and with the voltage-time balance

$$(U_1 + U_{C1})d_1 = |-U_2|(1-d_2) \tag{22}$$

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one gets for the voltage transformation ratio

$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - d_1 - d_2} \quad \text{with} \quad d_1 + d_2 < 1 \quad \text{and} \quad d_2 \geq d_1 . \tag{23}$$

For lower duty cycles d2 than that of d1 the converter does not work in the tristate modus. Without the additional branch D1, S2 the voltage-time balance across L1 can be calculated according to

$$(U_1 + U_{C1})d_1 = |-U_2|(1 - d_1) \tag{24}$$

and again with

$$U_{C1} = U_2 \tag{25}$$

one gets the voltage transformation ratio according to

$$M = \frac{U_2}{U_1} = \frac{d_1}{1 - 2d_1}, \quad d_1 < 0.5 \tag{26}$$

Figure 29 shows the voltage transformation ratio of the RLT D1/(1-D1-D2) converter with the duty cycle of the second switch as parameter and the duty cycle of the first switch as variable. The voltage transformation rate is flatter and higher than that of the D/(1-2D)-converter.

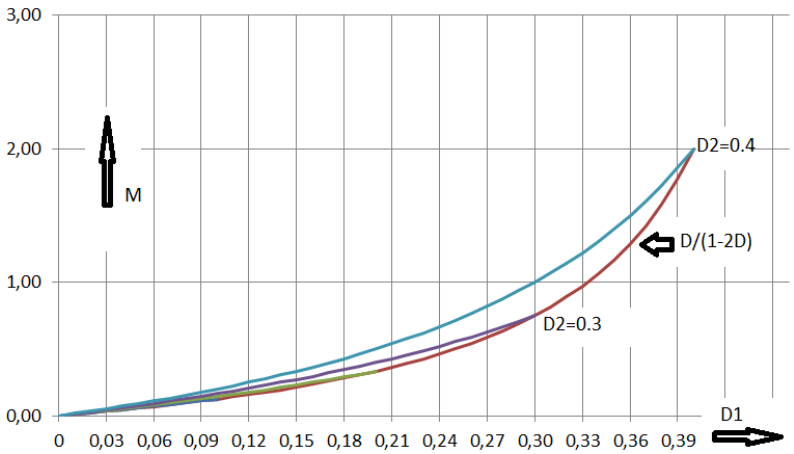

Figure 29. Voltage transformation ratio of the RLT D1/(1-D1-D2) converter, duty cycle of switch S2 as parameter and duty cycle of switch S1 as variable.

Figure 30 shows the voltage transformation ratio of the RLT D1/(1-D1-D2) converter with the duty cycle of the first switch as parameter and the duty cycle of the second switch as variable. The voltage transformation rate is flatter than that of the original converter.

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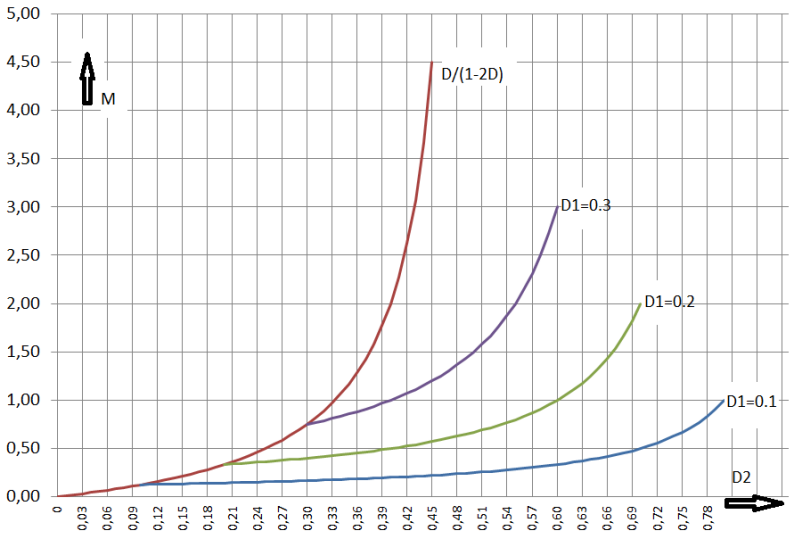
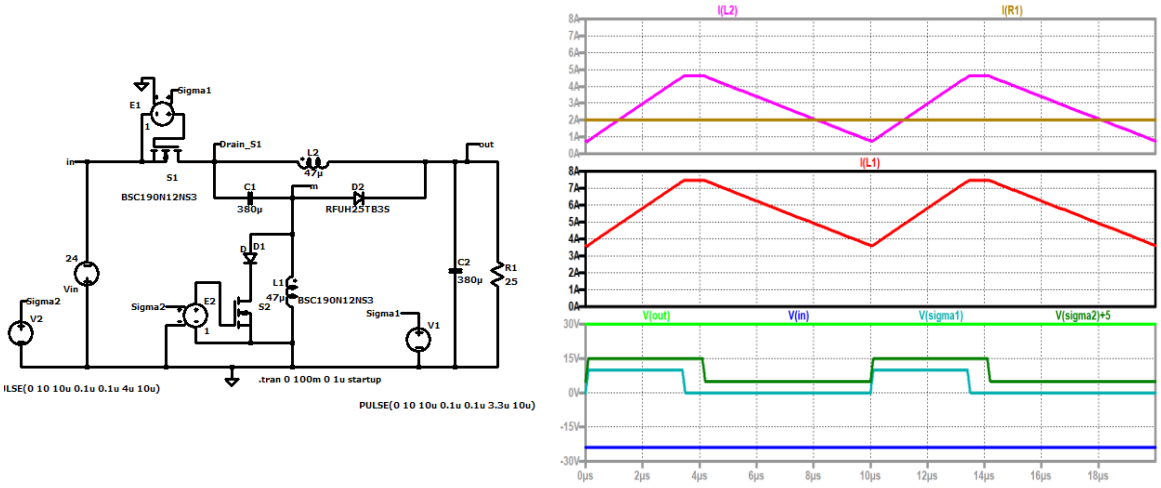


Figure 30. Voltage transformation ratio of the RLT D1/(1-D1-D2) converter, duty cycle of switch S1 as parameter and duty cycle of switch S2 as variable.

For the steady state one gets the exemplary simulation results shown in Fig. 31. One sees the current through the second coil L2, the load current, the current through the first coil L1, the output voltage, the control signal of the second switch S2, the control signal of the first switch S1, and the input voltage.



(**a**) (**b**)

Figure 31. RLT D1/(1-D1-D2) converter, **(a)** simulation circuit, and **(b)** up to down: current through the second coil L2 (violet), load current (brown); current through the first coil L1 (red); output voltage (green), control signal of the second switch (dark green), control signal of S1 (turquoise), input voltage (blue).

For another duty cycle of S2 Figure 32 shows the input current into the converter, the current through the second coil L2, the load current, the current through the first coil L1, the output voltage, the control signal of the second switch, the control signal of the first switch, and the input voltage.

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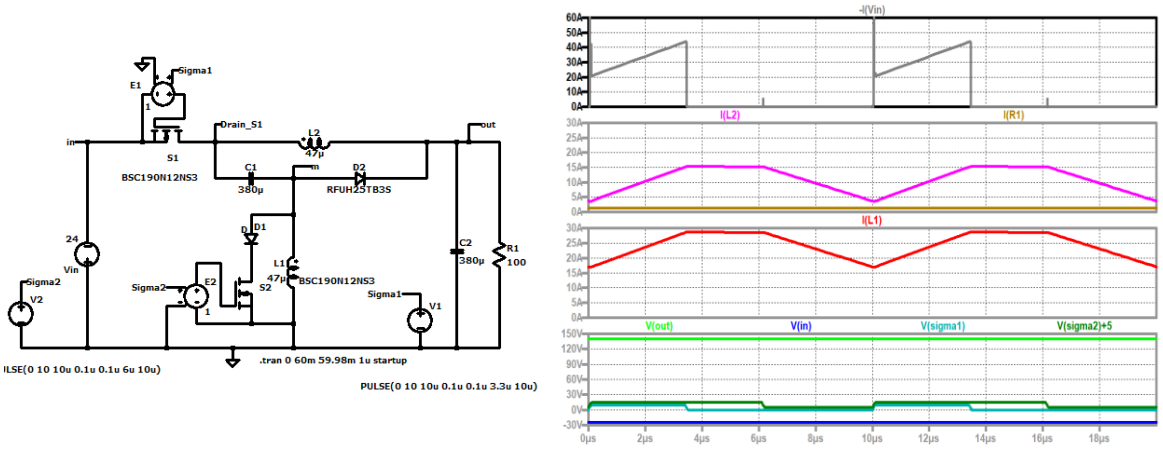

(**a**) (**b**)

Figure 32. RLT D1/(1-D1-D2) converter, **(a)** simulation circuit, **(b)** and up to down: input current (grey); current through the second coil L2 (violet), load current (brown); current through the first coil L1 (red); output voltage (green), control signal of the second switch (dark green), control signal of S1 (turquoise), input voltage (blue).

3. RLT Buck Transfer Functions and Bode Diagrams

In the continuous mode and with ideal components (no losses, infinite fast switching) the three modes can be described by the three matrix equations

$$\text{M1}\quad \frac{d}{dt}\begin{pmatrix} i_L \\ u_C \end{pmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{pmatrix} i_L \\ u_C \end{pmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}(u_1), \tag{27}$$

$$\text{M2}\quad \frac{d}{dt}\begin{pmatrix} i_L \\ u_C \end{pmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}\begin{pmatrix} i_L \\ u_C \end{pmatrix}, \tag{28}$$

$$\text{M3}\quad \frac{d}{dt}\begin{pmatrix} i_L \\ u_C \end{pmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{pmatrix} i_L \\ u_C \end{pmatrix}. \tag{1}$$

When the time constants of the converter are large (e.g. a factor from about 10 t0 100) compared to the time period of the switching frequency, the three equations can be combined by multiplying (27) by d1, (28) by (d2-d1), and (29) by (1-d2) and adding them. This leads to the large signal model

$$\frac{d}{dt}\begin{pmatrix} i_L \\ u_C \end{pmatrix} = \begin{bmatrix} 0 & -\frac{1+d_1-d_2}{L} \\ \frac{1+d_1-d_2}{C} & -\frac{1}{RC} \end{bmatrix}\begin{pmatrix} i_L \\ u_C \end{pmatrix} + \begin{bmatrix} \frac{d_1}{L} \\ 0 \end{bmatrix}(u_1). \tag{30}$$

To linearize this equation around the operating point, the variables are replaced by the operating point value (written with a capital letter with the index 0) plus a disturbance variable around the operating point (written with a small letter with a roof on top). This leads to the linear small signal model around the operating point according to

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_L \\ \hat{u}_C \end{pmatrix} = \begin{bmatrix} 0 & -\frac{1+D_{10}-D_{20}}{L} \\ \frac{1+D_{10}-D_{20}}{C} & -\frac{1}{RC} \end{bmatrix}\begin{pmatrix} \hat{i}_L \\ \hat{u}_C \end{pmatrix} + \begin{bmatrix} \frac{D_{10}}{L} & \frac{U_{C0}}{L} & -\frac{U_{C0}}{L} \\ 0 & \frac{I_{L0}}{C} & -\frac{I_{L0}}{C} \end{bmatrix}\begin{pmatrix} \hat{u}_1 \\ \hat{d}_1 \\ \hat{d}_2 \end{pmatrix}. \tag{31}$$

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This model has three input variables: the disturbances of the input voltage and of the duty cycles around the operating point. Using the Laplace transformation

$$\begin{bmatrix} s & \frac{1+D_{10}-D_{20}}{L} \\ -\frac{1+D_{10}-D_{20}}{C} & s+\frac{1}{RC} \end{bmatrix} \begin{pmatrix} I_L(s) \\ U_C(s) \end{pmatrix} = \begin{bmatrix} \frac{D_{10}}{L} & \frac{U_{C0}}{L} & -\frac{U_{C0}}{L} \\ 0 & \frac{I_{L0}}{C} & -\frac{I_{L0}}{C} \end{bmatrix} \begin{pmatrix} U_1(s) \\ D_1(s) \\ D_2(s) \end{pmatrix} \tag{32}$$

one can now calculate six transfer functions. The most important ones are the output voltage (which in the ideal case is equal to the voltage across the capacitor) referred to the duty cycles and to the input voltage. With the help of Crammer's law one gets

$$\frac{U_2(s)}{D_1(s)} = \frac{s\frac{I_{L0}}{C} - \frac{U_{20}(1+D_{10}-D_{20})}{CL}}{s^2 + s\frac{1}{CR} + \frac{(1+D_{10}-D_{20})^2}{CL}}, \tag{33}$$

$$\frac{U_2(s)}{D_2(s)} = \frac{-s\frac{I_{L0}}{C} + \frac{U_{20}(1+D_{10}-D_{20})}{CL}}{s^2 + s\frac{1}{CR} + \frac{(1+D_{10}-D_{20})^2}{CL}} \tag{34}$$

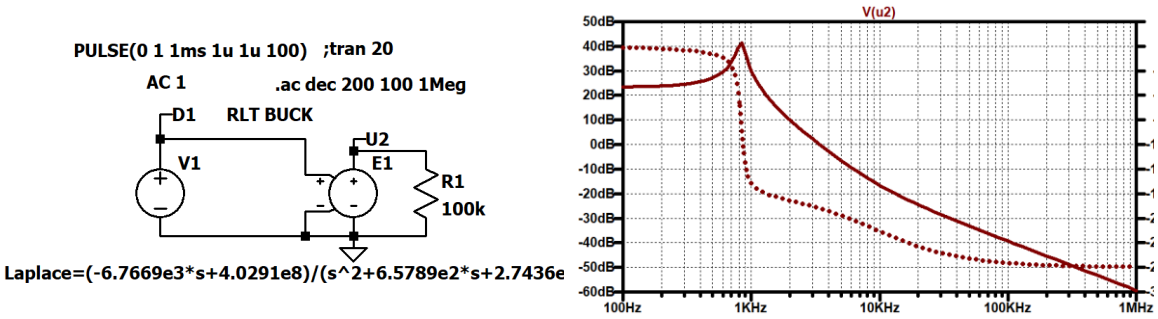
$$\frac{U_2(s)}{U_1(s)} = \frac{\frac{D_{10}(1+D_{10}-D_{20})}{CL}}{s^2 + s\frac{1}{CR} + \frac{(1+D_{10}-D_{20})^2}{CL}}, \tag{35}$$

The transfer functions of the influence of the duty cycles have a zero

$$s_Z = +\frac{U_{20}(1+D_{10}-D_{20})}{I_{L0}L} \tag{36}$$

on the right side of the complex plane. This means that they are non-phase-minimum systems and therefore have an additional phase shift of minus 90° for high frequencies. The original Buck, however, is a phase-minimum system.

Figure 33 shows the Bode plot of the output voltage in dependence on the duty cycle. The resonance is caused by the inductor and the capacitor, which leads to a sharp change of the phase. The position of the pole has an imaginary part of about 830 Hz. The parameters used for the Bode plot are the same ones used for the simulation (Figure 6) (D01=0.3, D02=0.6, U10=24 V, C=380 µF, L=47 µH). The break caused by the zero is at 10 kHz (at the phase shift of -225°).



(**a**) (**b**)

Figure 33. RLT Buck converter, output voltage U2 referred to the duty cycle D1, transfer function: **(a)** simulation circuit, **(b)** Bode plot (solid line: gain response, dotted line: phase response).

For the influence of the input voltage U1 on the output voltage U2one gets the Bode plot Figure 34. The transfer function describes a phase-minimum system.

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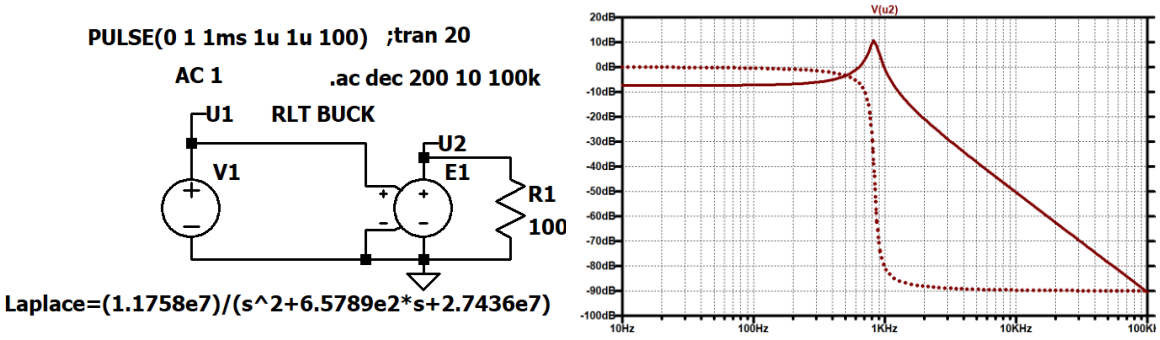

(**a**) (**b**)

Figure 34. RLT Buck converter, output voltage U2 referred to the input voltage U1 transfer function: simulation circuit, Bode plot (solid line: gain response, dotted line: phase response).

Looking at the other converters treated in section 2 one can see that the converters according Figure 7 (the RLT Buck-Boost), Fig. 12 (the RLT Boost), Fig. 15 (the RLT Zeta), Fig. 17 (the RLT Cuk), Fig. 20 (the RLT Super Boost) have a linearized voltage transformation ratio, when the duty cycle of the second switch is held constant. This leads to a phase-minimum behavior of the transfer function between the output voltage and the duty cycle of the first switch.

4. Voltage Stress Across the Semiconductors of RLT Converters

4.1. RLT Buck (Figure 3)

The first switch is on during the first mode, has to block the difference between the input and the output voltages in the second mode and during the third mode the input voltage. The second switch is turned on during the first two modes and has to block the output voltage during the third mode. The first diode must block the output minus the input voltages during the first mode, is conducting during the second mode and stays nearly at zero during mode three. The second diode has to block the input voltage during mode one, the output voltage during mode 2 and is conducting during the third mode.

4.2. RLT Buck-Boost (Figure 7)

The active switch S1 is on during M1, must block the input voltage during M2 and the sum of the input and the output voltages during M3. The second switch S2 is on during M1 and M2 and has to block the output voltage during M3. The diode is D1 is stressed only during M1, during which it must hold the input voltage. Diode D2 is stressed during M1 with the sum of the input and the output voltages, stressed with the output voltage during M2 and is conducting during M3.

4.3. RLT Boost (Figure 11)

During M1 S1 is on, during M2 it has to block the input voltage and during M3 the output voltage. The second switch S2 is on during M1 and M2 and must block during M3 the difference between the output and the input voltages. Diode D1 must hold the input voltage during M1, conducts during M2 and stays near zero during M3. The output diode D2 has to block the output voltage during M1, during M2 only the difference between output and input voltages and conducts during M3.

4.4. RLT Zeta (Figure 15)

The first switch has to block during M2 the input voltage and during M3 the sum of the input and output voltages. The second switch is on during M1 and M2 and blocks the voltage across the intermediate capacitor C1 which is equal to the output voltage. Diode D1 blocks the input voltage during M1, is conducting during M2 and stays near zero in M3, because the second transistor takes

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the voltage. The diode D2 must block the voltage across the intermediate capacitor C1 which is equal to the output voltage during M1, blocks only the difference between the voltage across C1 and the input voltage during M2 and conducts during M3.

4.5. RLT Cuk (Figure 17)

The voltage across the intermediate capacitor C1 is the sum of the input and the output voltages. When switch S1 turns off and mode M2 begins, the transistor S1 has to block the input voltage, and in mode M3 the voltage of the intermediate capacitor C1. Switch S2 is on during M1 and M2 and has to block the input voltage during M3. The diode D1 blocks the input voltage during M1 and is nearly zero during M2 and M3. The free-wheeling diode D2 must hold the voltage across C1 during M1 and during M2 the difference between the input and the intermediate capacitor voltages which is equal to the output voltage.

4.6. RLT Super Boost (Figure 21)

The voltage across C1 is equal to the output voltage. So one gets for the voltage stress across S1 the input voltage during M2 and the capacitor voltage during M3. S2 is turned off at the end of M2 and has to block the difference between U2 and U1. The maximum voltage across D1 is during M1 and is equal to the input voltage. The diode D2 is stressed during M1 with the voltage across C1 and during M2 by the input voltage.

4.7. RLT D-Square Buck (Figure 24)

The voltage stresses across the diodes D1 and D2 are equal to the input voltage. The main transistor S1 has to block the input voltage during M2 and the sum of the voltage across C1 and the input voltage during M3. The maximum stress across S2 is during M3 and is equal to the voltage across C1. The additional diode D4 must block the difference between the input voltage and the voltage across C1 during the first mode. The free-wheeling diode D3 is conducting during the second and the third modes and has to block the voltage across C1 during mode M1. D4 has to block the input voltage minus the voltage across C1.

4.8. RLT D1/(1-D1-D2) converter (Figure 28)

The voltage across the intermediate capacitor C1 is equal to the output voltage. When the main transistor S1 turns off, the voltage across it goes up the sum of the voltage across C1 and the input voltage and reaches two times the output voltage plus the input voltage in M3. The additional switch S2 has to block the output voltage during M3. The sum of the input and the voltage across C1 stresses the diode D1 during M1. The diode D2 is stressed by two times the output voltage plus the input voltage during M1, and during M2 the output voltage.

4.9. Summery voltage stress

The voltage stress of the semiconductors is now summarized. Table 1 summarizes the results for the second order converters, Table 2 for the fourth order converters, and Table 3 for the D-square converter. The D-square converter has four diodes and the numbers for the diodes are different, therefore an own table is used.

Table 1. Voltage stress across the semiconductors of the second order converters.

	S1	**S2**	**D1**	**D2**
Buck	U1	U2	U1	U1
Boost	U2	U2-U1	U1	U2
Buck-Boost	U1+U2	U2	U1	U1+U2

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Table 2. Voltage stress across the semiconductors of the fourth order converters.

	S1	S2	D1	D2
RLT Zeta	U1+U2	U2	U1	U2
RLT Cuk	U1+U2	U1	U1	U1+U2
RLT Super Boost	U2	U2-U1	U1	U2
RLT D1/(1-D1-D2)	2U2+U1	U2	U1+U2	2U2+U1

Table 3. Voltage stress across the semiconductors of the d-square Buck converter.

	S1	S2	D1	D2	D3	D4
D-SquareBuck	U1*(1+D1)	U1*D1	U1	U1	D1*U1	U1*(1-D1)

5. Connections Between the Currents

5.1. Simple Approximation of the Currents

Considering large inductors means that the current ripple is low. To get the connections between the mean values of the current through the coils one has to observe the currents through the capacitors. In the steady state they must be zero in the mean.

5.1.1. Currents Through the Second Order Converters

In the RLT Buck converter the current which flows through the output capacitor is the current through the coil reduced by the load current during M1, the negative load current during M2 and again the same current as in M1 during M3. Therefore, the charge balance leads to

$$\bar{I}_L(1+d_1-d_2)=I_{LOAD}. \tag{37}$$

For the Buck-Boost converter the negative load current flows through the capacitor during the first and the second mode, and during M3 the difference between the current through the coil and the load current leads to the balance

$$\bar{I}_L(1-d_2)=I_{LOAD}. \tag{38}$$

The current balance through the capacitor in the Boost converter is the same as that for the Buck-Boost converter. For a small current ripple through the coils the rms value is near to the mean value. The rms values are calculated with large inductors (small current ripple). This is now shown for the primary switch S1. The square of the rms value is given by

$$I_{S1rms}^2=\frac{1}{T}\int_0^{d1T}\bar{I}_L^{\,2}dt=\bar{I}_L^{\,2}\,d_1. \tag{39}$$

The results are summarized in Table 4.

Table 4. Currents through the components of the second order converters.

	$\frac{\bar{I}_L}{I_{LOAD}}$	$\frac{I_{S1rms}}{I_{LOAD}}$	$\frac{I_{S2rms}}{I_{LOAD}}$	$\frac{I_{D1rms}}{I_{LOAD}}$	$\frac{I_{D2rms}}{I_{LOAD}}$
Buck	$\frac{1}{1+d_1-d_2}$	$\frac{\sqrt{d_1}}{1+d_1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1+d_1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1+d_1-d_2}$	$\frac{\sqrt{1-d_2}}{1+d_1-d_2}$

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Buck-Boost	$\frac{1}{1-d_2}$	$\frac{\sqrt{d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{\sqrt{1-d_2}}{1-d_2}$
Boost	$\frac{1}{1-d_2}$	$\frac{\sqrt{d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{\sqrt{1-d_2}}{1-d_2}$

5.1.2. Currents Through the Fourth Order Converters

A glance at the circuit diagrams of the Zeta (Figure 15), the Cuk (Figure 17), the Super Boost (Figure 21), and the d-square Buck (Figure 24) converters shows that the mean current through the second inductor must be equal to the load current.

For the first three topologies the negative current through the second coil flows through the intermediate capacitor C1 during M1 and M2. During the third mode M3 only the current through the first coil flows through C1. So one gets

$$I_{LOAD} d_2 = \bar{I}_{L1}(1-d_2). \tag{40}$$

The results are summarized in Table 5.

Table 5. Currents through the components of the fourth order converters.

	$\frac{\bar{I}_{L1}}{I_{LOAD}}$	$\frac{\bar{I}_{L2}}{I_{LOAD}}$	$\frac{I_{S1rms}}{I_{LOAD}}$	$\frac{I_{S2rms}}{I_{LOAD}}$	$\frac{I_{D1rms}}{I_{LOAD}}$	$\frac{I_{D2rms}}{I_{LOAD}}$
Zeta, Cuk, Super-Boost	$\frac{d_2}{1-d_2}$	1	$\frac{\sqrt{d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_2}$	$\frac{1}{\sqrt{1-d_2}}$

5.1.3. Currents Through the d-Square Converter

The current-time balance at the capacitor C1 can be found according to

$$\left|\bar{I}_{L1}-\bar{I}_{L2}\right| d_1 = \bar{I}_{L1}(1-d_2) \quad \text{and with} \quad \bar{I}_{L2} = I_{LOAD}. \tag{41}$$

one can calculate the mean value of the current through L1. Table 6 shows the mean value of the currents and the rms values of the currents through the semiconductors.

Table 6. Currents through the components of the d-square Buck converter.

	$\frac{\bar{I}_{L1}}{I_{LOAD}}$	$\frac{\bar{I}_{L2}}{I_{LOAD}}$	$\frac{I_{S1rms}}{I_{LOAD}}$	$\frac{I_{S2rms}}{I_{LOAD}} = \frac{I_{D4rms}}{I_{LOAD}}$	$\frac{I_{D1rms}}{I_{LOAD}}$	$\frac{I_{D2rms}}{I_{LOAD}}$	$\frac{I_{D3rms}}{I_{LOAD}}$
D-Square Buck	$\frac{d_1}{1+d_1-d_2}$	1	$\frac{d_1\sqrt{d_1}}{1+d_1-d_2}$	$\frac{d_1\sqrt{d_2-d_1}}{1+d_1-d_2}$	$\frac{(1-d_2)\sqrt{d_1}}{1-d_2}$	$\frac{d_1\sqrt{1-d_2}}{1+d_1-d_2}$	$\sqrt{1-d_1}$

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5.1.4. Currents Through the d1/(1-d1-d2) Converter

The charge balance of the capacitors

$$\left|-\bar{I}_{L2}-I_{LOAD}\right|d_2=\left(\bar{I}_{L1}-I_{LOAD}\right)(1-d_2),\quad \bar{I}_{L1}d_1+\bar{I}_{L2}(d_2-d_1)+\bar{I}_{L2}(1-d_2)=0 \tag{42}$$

leads to the results shown in Table 7.

Table 7. Currents through the components of the d1/(1-d1-d2) converter.

	$\frac{\bar{I}_{L1}}{I_{LOAD}}$	$\frac{\bar{I}_{L2}}{I_{LOAD}}$	$\frac{I_{S1rms}}{I_{LOAD}}$	$\frac{I_{S2rms}}{I_{LOAD}}$	$\frac{I_{D1rms}}{I_{LOAD}}$	$\frac{I_{D2rms}}{I_{LOAD}}$
d1/(1-d1-d2)	$\frac{1-d_1}{1-d_1-d_2}$	$\frac{d_1}{1-d_1-d_2}$	$\frac{\sqrt{d_1}}{1-d_1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_1-d_2}$	$\frac{\sqrt{d_2-d_1}}{1-d_1-d_2}$	$\frac{\sqrt{1-d_2}}{1-d_1-d_2}$

5.2. Onward Losses

With the help of these tables (Tables 4–7) one can approximately calculate the onward losses of the components of the converters. With the parasitic resistors of the inductors RL1, RL2 one obtains for the coils

$$P_{LL1}=R_{L1}\left(\bar{I}_{LL1}\right)^2,\quad P_{LL2}=R_{L2}\left(\bar{I}_{LL2}\right)^2 \tag{43}$$

With on-resistors of the electronic switches RS1 and RS2 one gets for the losses

$$P_{LS1}=R_{S1}\left(\bar{I}_{S1rms}\right)^2,\quad P_{LS2}=R_{S2}\left(\bar{I}_{LS2rms}\right)^2 \tag{44}$$

The diodes are modelled by a fix knee-voltage VD and the differential resistor RD to obtain the losses across the diodes according to

$$P_{LDi}=R_{Di}\left(\bar{I}_{Dirms}\right)^2+V_{Di}\bar{I}_{Dirms} \tag{45}$$

with *i* as the number of the diode. The losses of the diodes dominate the losses of the complete converter. It should be mentioned that the rms value for the bypass of the coil (the anti-serial connection of S2 and D1) has a larger error (in the next section a more precise calculation for the rms through the switches is given). For higher power it can be useful to connect an active electronic switch antiparallelly to the diodes, but additional driver units are necessary which immediately increase the cost, but can sometimes also reduce the weight and the volume and even the cost, because the cooling effort is reduced, too. As an example this is shown for the Super-Boost converter. Figure 35a shows an improvement of the bypass by connecting the auxiliary switch SH1 antiparallelly to the first diode, and Figure 35b shows both diodes shunted by an additional auxiliary switch.

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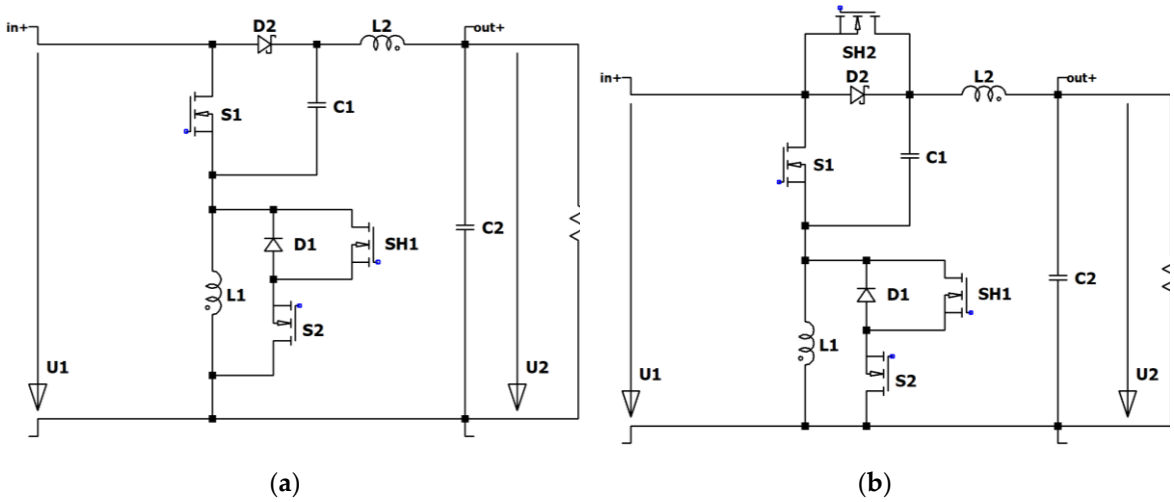

Figure 35. RLT Super-Boost with efficiency improvement, **(a)** with improved bypass, and **(b)** with two auxiliary switches.

Summarizing all losses of the components to PL one gets the efficiency

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_L} \tag{46}$$

To reduce the switching losses fast semiconductors based on SiC technology can be used, and/or snubbers or zero voltage switching ZVS concepts can be applied.

5.3. Reduction of the loss compared to the traditional tristate converter

In the here treated tristate converters the current flows through the switch S2 only during mode M2. In the traditional one, however, the current through the coils are also flowing through the second switch S2. The losses at all other components do not change. For the traditional tristate Buck converter, one can write for the square of the rms value of the current through S2

$$I_{S2rms}^2 = \frac{1}{T}\int_0^{d_2 T} \bar{I}_L^{\,2}\, dt = \left(\frac{I_{LOAD}}{1 + d_1 - d_2}\right)^2 d_2 . \tag{47}$$

The approximate loss reduction factor of S2 is defined by

$$\frac{I_{S2rmsRLT}}{I_{S2rms}} = \frac{\sqrt{d_2 - d_1}}{\sqrt{d_2}} . \tag{48}$$

The same result can also be found for the Buck-Boost and Boost converters. For the linear fourth order converters the sum of both currents through the coils is always flowing through S2 during the first two modes. The reduction factor is the same as given in (48).

For the quadratic converter the reduction factor is more complicate and can be found according to

$$\frac{I_{S2rmsRLT}}{I_{S2rms}} = \frac{\dfrac{d_1\sqrt{d_2 - d_1}}{1 + d_1 - d_2}}{\sqrt{d_1 + \dfrac{d_1^2 (d_2 - d_1)}{(1 + d_2 - d_1)^2}}} = \frac{d_1\sqrt{d_2 - d_1}}{\sqrt{d_1 + 2d_1^2 - 2d_1 d_2 - d_1^2 d_2 + d_1 d_2^2}} . \tag{49}$$

5.4. Input and Output Currents

The form of the input and the output currents is another interesting question. Are the currents continuous (abbreviation C) or discontinuous (abbreviation D)? Table 8 summarizes the results.

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Table 8. Continuous or discontinuous input and output currents.

	Buck	Buck-Boost	Boost	Zeta	Cuk I	Cuk II	Super-Boost	Quadratic Buck	D1/(1-D1-D2)
IN	D	D	D	D	D	C	D	D	D
OUT	D	D	D	C	C	D	C	C	D

When the input current is discontinuous, an input capacitor must be placed at the input of the converter to avoid overvoltage at the switching devices caused by the parasitic inductance between the supplying source and the converter. When the output current is discontinuous, a larger output capacitor is necessary than that which must be used in the continuous case.

5.5. Precise Calculation of the Currents

For the Super-Boost the more precise calculation of the currents is demonstrated. We start with the load current. It is nearly constant, because the output capacitor C2 is so large that the voltage across it is nearly constant. During M1 the current rises starting from IL20 according to the voltage across the coil of UC1+U1-U2. The voltage across the capacitor C1 is equal to the output voltage U2. The current rises by ΔI_{L2}. During M2 the voltage across the coil is nearly zero and the current stays nearly constant. The current decreases by ΔI_{L2} in the third mode. To better understand the following calculation Figure 36 is included.

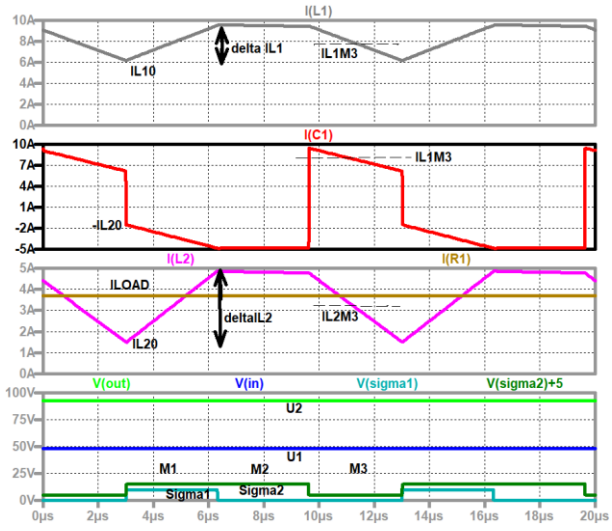

Figure 36. Super-boost converter, up to down: Current through L1 (grey); current through the capacitor C1 (red); current through L2 (violet), load current (brown); output voltage (green), input voltage (blue), control signal of S2 (dark green), control signal of S1 (turquoise).

One obtains the mean value of the current through the coil ideally be integration of

$$\bar{I}_{L2} = I_{LOAD} = \frac{1}{T}\int_0^{d1T}\left(I_{L20} + \frac{\Delta I_{L2}}{d_1 T}t\right)dt + \frac{1}{T}\int_{d1T}^{d2T}\left(I_{L20} + \Delta I_{L2}\right)dt + \frac{1}{T}\int_{d2T}^{T}\left(I_{L20} + \Delta I_{L2} - \frac{\Delta I_{L2}}{(1-d_2)T}t\right)dt \quad (50)$$

.

This results in

$$\bar{I}_{L2} = I_{LOAD} = I_{L20} + \frac{\Delta I_{L2}}{2}\left(1 + d_2 - d_1\right). \quad (51)$$

From (51) one can obtain the starting point of the current in the steady state to

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$$I_{L20} = I_{Load} - \frac{\Delta I_{L2}}{2}(1 + d_2 - d_1). \tag{52}$$

The current ripple can be found by

$$\Delta I_2 = \frac{U_1 d_1 T}{L_2} \tag{53}$$

The maximum value is given by

$$I_{L2\max} = I_{L20} + \Delta I_{L2} = I_{L20} + \frac{U_1 d_1 T}{L_2}. \tag{54}$$

In the next step we look at the current through the capacitor C1. During M1 and M2 the negative current through L2 discharges the capacitor a little, and during M3 the capacitor is charged again by the current through L1. The mean value of the current through L1 only referred to the duration of M3 must be so large that it leads to the same charge as that which was taken from the capacitor during the modes M1 and M2. Therefore, one can write

$$\bar{I}_{L1M3}(1 - d_2)T = \left[\int_0^{d1T} \left(I_{L20} + \frac{\Delta I_{L2}}{d_1 T} t \right) + \int_{d1T}^{d2T} (I_{L20} + \Delta I_{L2}) dt \right]. \tag{55}$$

The mean value of the current through L1 referred to the off-time of switch S2 is now obtained to

$$\bar{I}_{L1,M3} = \left[I_{20} d_2 + \Delta I_{L2} \left(d_2 - \frac{d_1}{2} \right) \right] \Big/ (1 - d_2). \tag{56}$$

The maximum value of the current through L1 can now be calculated according to

$$I_{L1,\max} = \bar{I}_{L1,M3} + \frac{\Delta I_{L1}}{2}. \tag{57}$$

One can now calculate the current ripple according to

$$\Delta I_{L1} = \frac{U_1 d_1 T}{L_1}. \tag{58}$$

and obtain the starting point of the current through L1 according to

$$I_{L10} = \bar{I}_{L1,M3} - \frac{\Delta I_{L1}}{2}. \tag{59}$$

The mean value of the current through L1 can be found by the same method as for the mean value of L2 leading to

$$\bar{I}_{L1} = I_{L10} + \frac{\Delta I_{L1}}{2}(1 + d_2 - d_1). \tag{60}$$

5.6. Inrush currents

When the converter is connected to a constant input voltage with low output resistor, a very high inrush current can occur (cf. 2.5). Converters with a switch directly at the input avoid this and the start-up of the converter is done by increasing the duty cycle starting from zero. Table 9 shows for the here discussed converters whether an inrush (Y) or no one occurs (N).

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Table 9. Continuous or discontinuous input and output currents.

	Buck	Buck-Boost	Boost	Zeta	Cuk I	Cuk II	Super-Boost	Quadratic Buck	D1/(1-D1-D2)
IN	N	N	Y	N	Y	Y	Y	N	N

5. Conclusion

To reduce the forward losses in a tristate converter, a series connection of a second electronic switch and an additional diode is connected in parallel to the coil of a basic DC/DC converter. In higher order converters with two coils there are two possibilities to make this variation. During the first mode M1 both electronic switches are on and both diodes are off. In the second mode M2 only the second switch is on and the first diode is conducting, and in mode M3 only the second diode is conducting. Compared to the traditional tristate converter, where current is flowing through both electronic switches during the modes M1 and M2, current flows through the second switch only during M2. This reduces the forward losses of the converter. The voltage transformation ratio is now a function of the duty cycles of the two switches. The duty cycle of the first switch is defined as the on-time of the switch S1 referred to the switching period. If the two switches are not switched on contemporarily, the definition of the duty cycle d2 of the second switch S2 is different from the usual definition: d2 must be defined as the time interval between the turn-on of switch S1 and the turn-off of switch S2 referred to the switching period. To achieve the tristate operation, the duty cycle of switch S2 must be larger than that of switch S1. In the simulations both switches are turned on at the same time. Using the duty cycle of switch S2 as the parameter, and the duty cycle of switch S1 as independent variable, the voltage transformation ratio of step-up converters (e.g. the Boost, the Buck-Boost, the Zeta, the Cuk, the Super-Boost) is linearized, and the small signal model has phase-minimum behavior. In the figures depicting the voltage transformation ratio of the converters one can see that the steepness can be adapted to fit the application used. Compared to other tristate concepts the losses across the second switch are reduced leading to a small improvement of the efficiency, depending on the operating point and the used components of about 0.5 up to 2 %. Other features of the original converter are maintained.

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