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Article

A Three-Phase Space Vector PWM Inverter for Induction Motor Drive with Leakage Current Reduction

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Abstract

Several industrial applications rely on induction motors to carry out processes essential for product manufacturing. Speed control of an induction motor commonly requires a pulse width modulated inverter capable of driving a system with long cables, suppression of common mode voltage, reduction of common mode current, and suppression of electromagnetic interference. This paper proposes a three-phase motor drive aimed to make constant the common mode voltage. The proposed system consists of two three-phase conventional full bridge inverters connected in parallel and having as an input two separate direct current sources. The proposed system is controlled by using the space vector pulse width modulation technique. By designing the adequate signal sequences of the switches for both converters, it is possible to keep constant the common model voltage and therefore reduce the associated common mode current making the system more reliable. The proposed system is validated through numerical simulations and by the implementation of an experimental prototype. Low common mode current values as low as 83mA are obtained in both simulations and experiments.

Keywords: common mode voltage; induction machine; leakage ground current; space vector PWM; three-phase PWM inverter

1. Introduction

Power electronic drives are widely used for controlling AC induction machines, particularly in industrial processes where variable speed control and high energy efficiency are essential. In recent years, the electric vehicle industry has grown significantly, reaching sales of around 14 million in 2023, contributing to sustainability by helping to mitigate global warming [1,2]. Power electronic motor drives are used to move and control the speed of electric vehicles, improving both speed regulation and motor efficiency by adjusting the frequency and magnitude of the output voltage [3,4]. Typically, conventional three-phase inverters are used as motor drives, due to their inherent simplicity and power flow in either direction. However, this topology has been less used due to its common mode voltage (CMV) and common mode current (CMC) issues [5,6].

In a star-connected three-phase electric induction machine, the CMV is defined as the voltage of the neutral point of the load concerning a common node in the circuit which can be the midpoint of the inverter DC bus. This, in turn, produces CMC that flows to the ground through parasitic capacitances between the stator windings and the motor case [7–9]. This phenomenon may cause several issues, such as damage to motor bearings, increased electromagnetic interference, and unwanted ground-fault

shutdowns. For these reasons, low dv/dt transitions and magnitude of CMV and thereby CMC are key to guarantee a good performance of motor drive systems [10–12]. To address these issues, there are different proposals in the literature including passive solutions, topology structure, sinusoidal pulse width modulation (PWM) strategies, Space Vector PWM techniques (SVPWM), active circuits and control methods [13–16]. Concerning topology-based solutions dealing with the CMV issue, in [17] a double-bridge three-phase inverter fed by a single DC source is proposed. In this configuration a SVPWM technique is used to control both bridges simultaneously, where the null vectors are constructed by using a combination of opposite active vectors. Then, a full match must be ensured between the vectors generated by both inverters to guarantee a proper operation. Therefore, the design of the control system and control algorithms is complex limiting the applications of the presented system. In [18] the H10 inverter is presented which consists in a full-bridge two-level three-phase inverter plus an active circuit at the DC input formed by two half-bridge circuits. The DC source requires three different DC sources connected in series where the active circuit clamps the full-bridge structure achieving constant CMV. However, the DC source must be designed to meet specific voltage levels, which make its implementation challenging. Moreover, in reference [19] two SVPWM strategies are proposed for a modified H10 topology. The main difference regarding [18] is that the DC bus power supply can be now implemented using two symmetric DC sources which expands the possible applications of this topology. The new H10 topology requires specific SVPWM strategies which are designed to provide a reduced magnitude of the CMV. In addition, the two proposed SVPWM deals with the CMV jumps issue due to the dead-time by clamping the CMV when entering and leaving the null vectors.

An asymmetric three-phase inverter topology is presented in [20] consisting of a full-bridge inverter with one leg modified. The modified leg is divided into two parts, the first, introduce a switched capacitor unit which consists of two switches, two diodes and two capacitors and the second includes two switches operating at the line frequency. The switched capacitor unit enables the boosting capability and a three-voltage level leg which contributes to improve the phase current total harmonic distortion (THD), however, the analysis of the CMV is not included for this topology. Finally, [21] proposes a four-leg, two-level three-phase inverter. The proposed structure significantly reduces the CMV component, however due to the required additional leg, an additional LC or LCL filter is also required, namely, increasing the cost, size and weight of the total system.

This paper proposes a motor drive system that consists of two main modules connected in parallel, each module has a two-level three-phase full-bridge inverter having as an input two separated DC sources. Each module includes a DC decoupling circuit that allows the disconnection of the DC source during the application of null vectors. By designing a specific sequence of the space vectors the total CMV of the system can be kept constant and the CMC achieves magnitudes close to zero. The rest of this paper is organized as follows; Section II presents the analysis and model of an induction machine in high frequency to clearly identify its parasitic elements. Section III explains and describes the proposed two-level three-phase topology, its advantages and drawbacks, and the different operation modes. In Section IV, the proposed specific space vector based modulation strategy is explained and the corresponding switching signals are derived. Section V and VI provide the numerical simulation and experimental results respectively. Finally, Section VII presents the concluding remarks of this research work.

2. High-Frequency Induction Machine Modeling

In a three-phase inverter, the sum of the three-phase voltages is always different from zero at the neutral point. Consequently, a voltage with the same switching frequency as that of the switches and with a magnitude equal to the input bus voltage appears between the motor's neutral point and ground [23]. This voltage is called CMV and it is given by,

$$V_{CMV1} = \frac{V_{aZ1} + V_{bZ1} + V_{cZ1}}{3}, \quad (1)$$

where v_A, v_B, v_C are the per-phase stator voltages of motor. The CMV variations generate CMC that flow to the ground through the parasitic capacitances. Such capacitances are always present between the stator windings and the stator iron [22,23]. The IEEE Standard 112 was established to obtain test methods and parameters for a low-frequency per-phase T-equivalent induction motor model in Figure 1 [24].

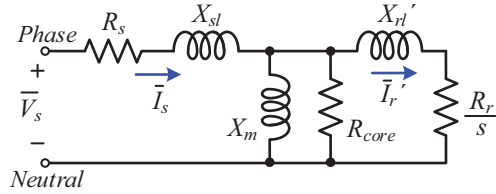


Figure 1. IEEE 112 recommended per-phase low-frequency equivalent circuit.

The electrical behavior of the per-phase equivalent circuit of the induction motor shown in Figure 1 is given by the following equations (where R_{core} is neglected):

$$\bar{V}_s = (R_s + jX_{sl})\bar{I}_s + jX_m(\bar{I}_r' - \bar{I}_s), \quad (2)$$

$$0 = (\frac{R_r'}{s} + jX_{rl}')\bar{I}_r' + jX_m(\bar{I}_r' - \bar{I}_s), \quad (3)$$

where $\bar{V}_s$ is the phasor of the per-phase stator voltage, R_s and R_r' are the per-phase stator and rotor resistances, respectively, $X_{sl} = \omega_s(L_s - M)$ and $X_{rl}' = \omega_s(L_r' - M)$ are the per-phase stator and rotor leakage reactance, respectively (with ω_s being the electrical pulsation, L_s and L_r' the stator and rotor inductances, and M the mutual inductance between the stator and the rotor windings), $X_m = \omega_s M$ is the per-phase mutual reactance, $s = (\omega_s - p\omega_m)/\omega_s$ is the mechanical slip of the induction motor (with p being the pole pairs and ω_m the mechanical speed), and the super index ' stands for the rotor magnitudes reduced to the stator winding.

High-frequency motor models can be mainly divided into two classes, i.e., distributed and lumped parameter models. Based on the analysis of the electrical characteristics inside the motor, the equivalent lumped parameter model can be used to express the distributed parameters model. According to [25], the rotor circuit of electric machines does not contribute at high frequencies, as no flux penetrates the rotor's magnetic circuit. Hence, a high-frequency model of the motor is shown in Figure 2, where C_{sf} denotes the capacitance between the stator windings and the motor frame and C_{sw} is the stator inter-turn capacitance per phase [22]. Two methods are commonly used to determine the high-frequency parameters of the induction motor [26]; the first is the finite-element method, which requires knowledge of the physical and geometrical characteristics of the conductor and insulation [27], and the second is the experimental method [28].

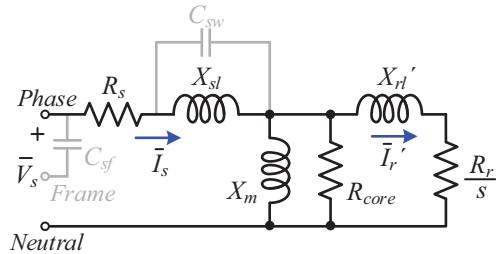


Figure 2. High-frequency common mode model.

In addition to the model shown in Figure 2, it is important to consider the motor-bearing model, which is where the CMV is present. Here, the capacitances that represent the model of the motor bearings are: C_{sf} which is the stator to frame capacitance, C_{sr} which is the stator to rotor capacitance, C_{rf} represents the rotor to frame capacitance, C_b models the lubricating grease films existing between

each bearing ball and sw represents the non-linear behavior of dielectric-breakdown voltage [22,29]. Figure 3 shows the motor-bearing model, then based on latter model the CMV in that follows is modeled using an equivalent parasitic capacitance connected between the neutral point of the load and the negative terminal of the DC source [30].

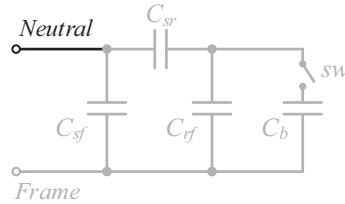


Figure 3. Motor-bearing model.

3. Proposed Induction Motor Drive

The proposed inverter consists of two conventional full-bridge two-level three-phase inverters connected in parallel sharing the AC side of the system as shown in Figure 4. On the DC side, two separated and isolated power sources are proposed with two switches to perform a decoupling action, this concept can be extended to multiple DC sources at the input of each three-phase inverter allowing, for instance, the balancing capability of a bank of batteries or several arrays of photovoltaic modules. Note that C_{p1} and C_{p2} model the parasitic capacitors of the DC buses, C_{pb} represents the equivalent capacitor of the bearing model and Z_g is the ground path impedance. The switches S_7 and S_8 (A and B) in each DC source are used to perform a decoupling action of the DC input power sources from the AC side of the inverter. On the right side of the DC decoupling circuit, the circuits denoted as *InverterA* and *InverterB* are used to set the appropriate space vector to feed the three-phase induction motor. According to the proposed power circuit, the operation modes of the proposed system can be described as follows. First, the null state can be adopted by configuring the simplified circuit depicted in Figure 5 and taking into account the next three considerations:

- The reference vector is located at the first sector as it is shown in Figure 6,
- The load is predominantly inductive as is the case of an induction motor,
- The space vector sequence is the one that is used for the conventional two-level three-phase inverter.

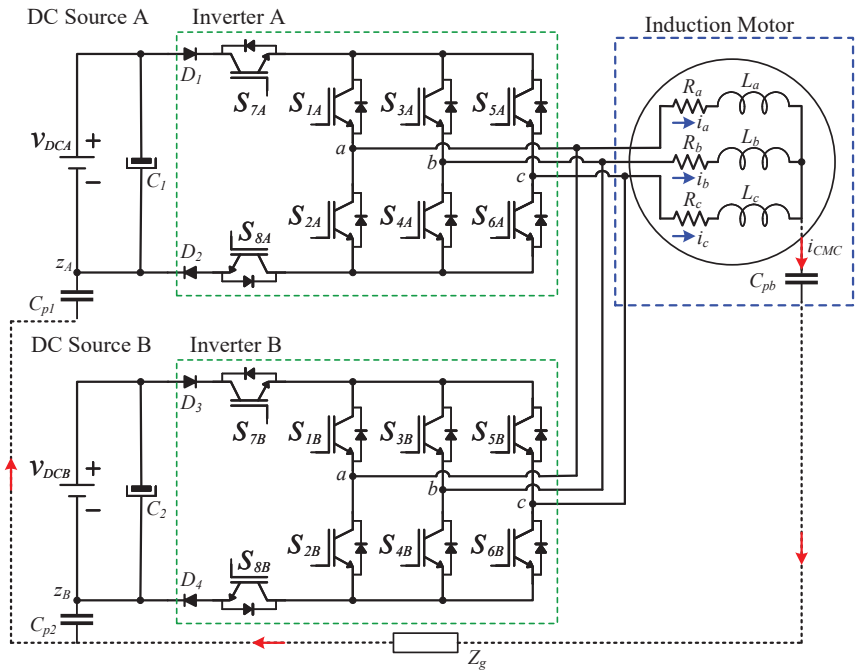


Figure 4. Inverter topology to reduce leakage ground current in three-phase induction machines.

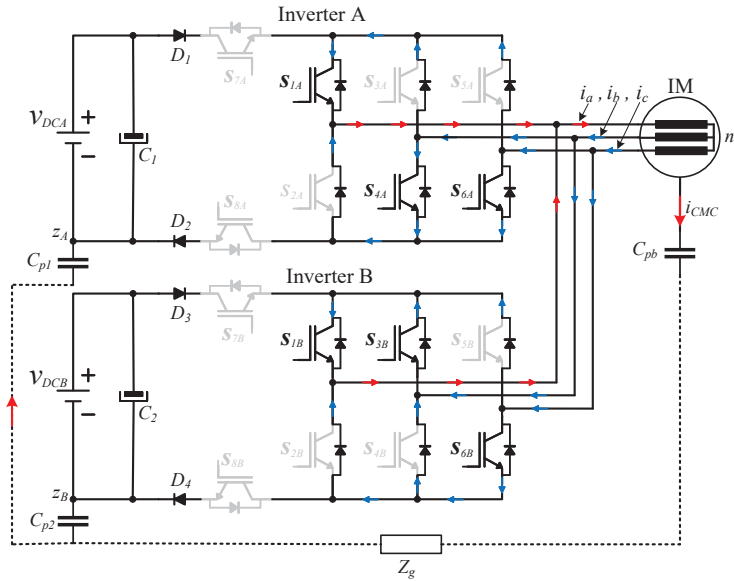


Figure 5. Null state for the proposed inverter when V_{ref} is located at Sector I.

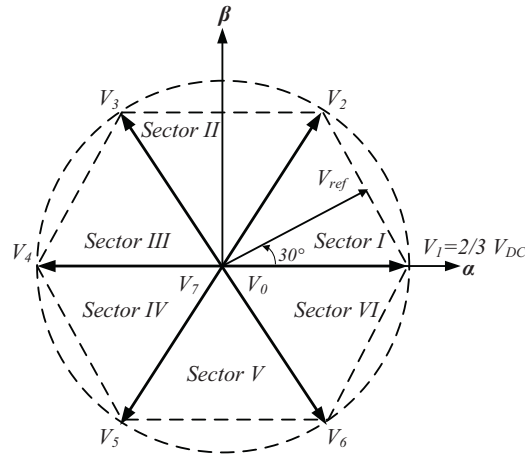


Figure 6. Space vectors along a grid period in a complex plain with V_{ref} located at Sector I.

Note that in this case all the output voltages are equal to zero which corresponds with the freewheeling operation. It can also be observed that *Inverter A* is set with an odd active vector which in this case is V_1 . At the same time *Inverter B* is configured with the next even vector to be applied in the sequence which is V_2 with the switches $S_{7A,B}$ and $S_{8A,B}$ in the off state. Therefore, the load current is distributed equally between the switches of the two inverters, allowing a well balanced distribution of the power losses.

The second system state is devoted to the application of an active vector, according to the conventional space vector modulation (SVM), the next vector to be applied is V_1 , then S_{7A} and S_{8A} are turned on, allowing the output current to flow towards the load as is depicted in Figure 7. As it can be observed the load current flows through the switches S_{1A} , S_{4A} and S_{6A} as in a conventional three-phase full-bridge inverter, while the *Inverter B* remains in the same configuration as in the previous state. Moreover, the third state of the proposed drive system, is devoted to the application of the second active vector which is V_2 , as is depicted in Figure 8. Then, S_{7A} and S_{8A} are turned off while S_{7B} and S_{8B} are turned on with vector V_2 already configured in the previous state, allowing the load current to flow through the switches S_{1B} , S_{3B} and S_{6B} . Finally and according with the conventional SVM sequence, a null vector is applied using the configuration depicted in Figure 9, where the load current can be equally distributed among the semiconductors in both inverters.

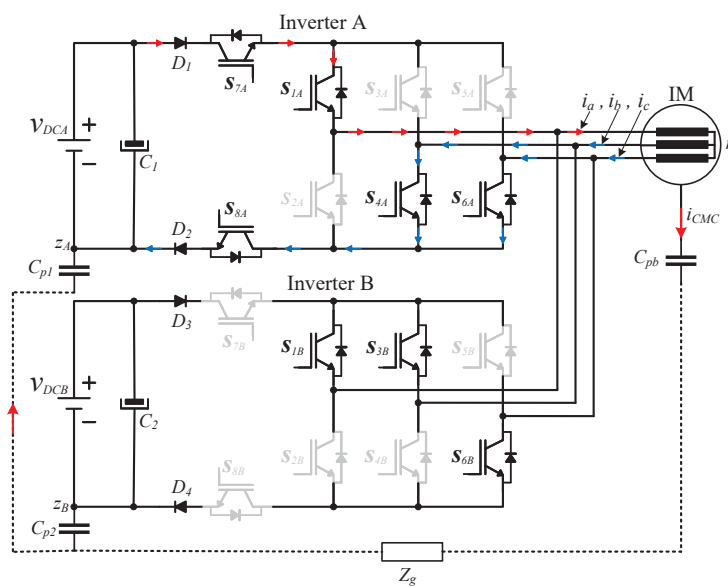


Figure 7. Active state V_1 for the proposed inverter when V_{ref} is located at Sector I.

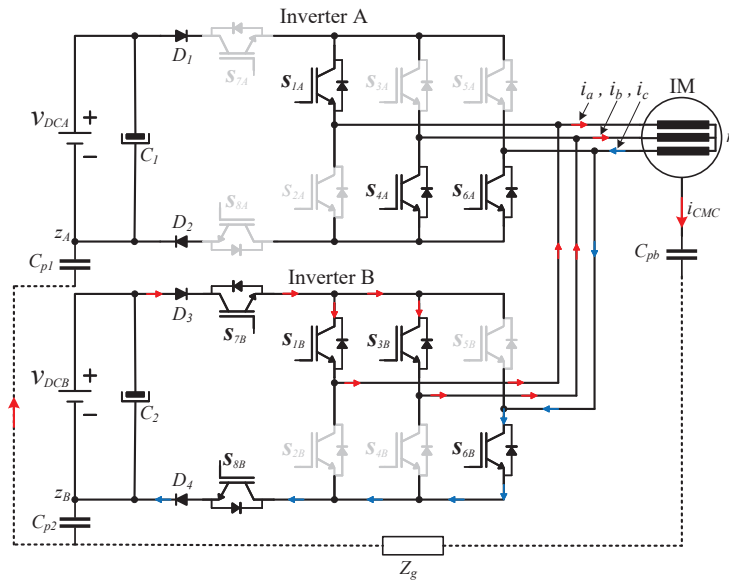


Figure 8. Active state V_2 for the proposed inverter when V_{ref} is located at Sector I.

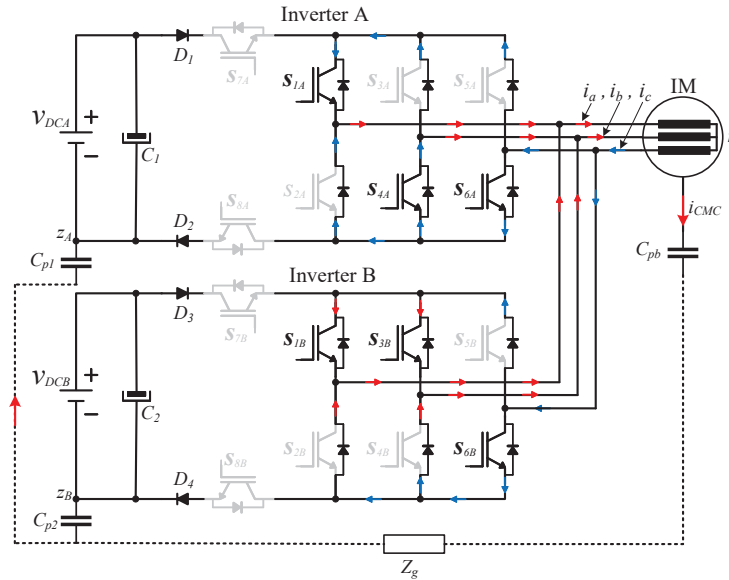


Figure 9. Null state for the proposed inverter when V_{ref} is located at Sector I.

The operating states described above are applied each switching period along sector one. This means that, by using only the decoupling switches, the reference vector can be synthesized; therefore, no commutations are required in the remaining switches. Table 1 summarizes the different operation states described above for the proposed system. Moreover, the same vector sequence strategy can be extended to the complete grid period by using the corresponding active vectors to configure each inverter, as it will be explained in the next section.

Table 1. Inverter modulation states along Sector 1.

State	S_{1A}	S_{3A}	S_{5A}	S_{1B}	S_{3B}	S_{5B}	$S_{7A,8A}$	$S_{7B,8B}$
1	1	0	0	1	1	0	0	0
2	1	0	0	1	1	0	1	0
3	1	0	0	1	1	0	0	1
4	1	0	0	1	1	0	0	0

Summarizing, *Inverter A* supplies the odd active vectors along the grid period which according to [31] produce a CMV equal to $1/3V_{DCA}$ concerning the node Z_A . Moreover, *Inverter B* supplies the even active vectors along the grid period which produce a CMV equal to $2/3V_{DCB}$ concerning the node Z_B . Therefore the magnitude of the CMV is kept constant in each inverter module along the total grid period. Constant CMV does not generate CMC; thus the magnitude of i_{CMC} in the proposed system of Figure 4 is close to zero making the proposed system a strong solution for induction motor drive applications.

4. Proposed Modulation Strategy

The modulation strategy is designed based on SVPWM theory. The inverter states described in the previous section are considered to define the modulation sequences shown in Figure 10. As shown, the vector sequences follow the conventional space vector modulation technique. For example, in Sector I, the conventional sequence is $V_0-V_1-V_2-V_7-V_7-V_2-V_1-V_0$. However, the proposed SVPWM sequence incorporates the states required by the decoupling switches in each three-phase bridge. Therefore, the vector names have been modified to form a sequence such as $SV_{10}-SV_{11}-SV_{10}-SV_{20}-SV_{21}-SV_{21}-SV_{20}-SV_{10}-SV_{11}-SV_{10}$. In this case, the odd active vectors, for instance SV_{11} , are supplied by Inverter A, while the even vectors, such as SV_{21} , are supplied to the load by Inverter B. The freewheeling state is achieved by disconnecting both DC sources while maintaining the inverters configured with their respective active vectors. In this way, it is possible to reduce the switching losses improving the inverter efficiency.

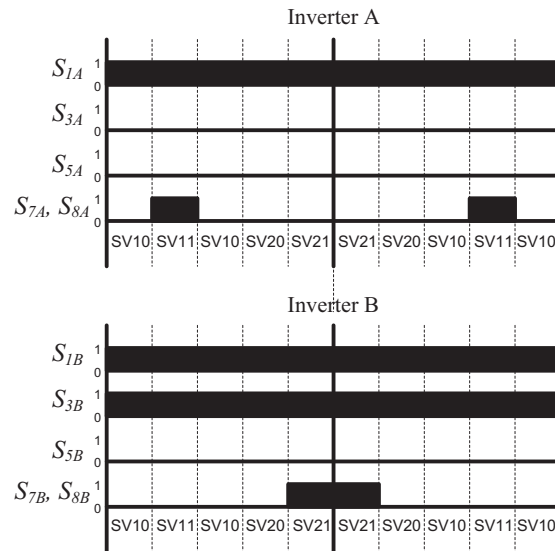


Figure 10. Proposed space vector modulation sequence for Sector I in one switching period.

For a balanced three-phase system V_{ref} in Figure 6 can be expressed as follows:

$$V_{ref} = V e^{j\omega t} \quad (4)$$

The reference vector V_{ref} can be approximated by using a sequence of three vectors in a switching period ($T_s = 1/f_s$). Such vectors can be the adjacent active vectors V_1 and V_2 depicted in Figure 6 for Sector I. V_1 and V_2 are the vectors SV_{11} and SV_{21} defined for the specific modulation sequence of the proposed inverter which are depicted in Figure 10. Note that the third vector can be selected from the null vectors V_0 and V_7 , as shown in Figure 6. These correspond to SV_{10} and SV_{20} in Figure 10. The sum of the applied vectors over a switching period T_s is equal to the reference vector V_{ref} , thus,

$$V_a t_a + V_b t_b + V_N t_0 = V_{ref} T_s, \quad (5)$$

where V_a and V_b are the active vectors and V_N can be any of the null vectors and the addition of the application times (t_a , t_b and t_0) must be equal to T_s ,

$$t_a + t_b + t_0 = T_s. \quad (6)$$

The duty cycles for each active and null vector can be calculated by analyzing the real and imaginary components of V_{ref} . However, since this theory is extensively covered in the literature [32], it is omitted in this paper.

$$t_a = \frac{\sqrt{3}|V_{ref}|T_s \sin(60^\circ - \theta)}{V_{DC}}, \quad (7)$$

$$t_b = \frac{\sqrt{3}|V_{ref}|T_s \sin(\theta)}{V_{DC}}, \quad (8)$$

$$t_0 = T_s - t_a - t_b. \quad (9)$$

Equations (7)-(9) are a general solution for t_a , t_b and t_0 and these are used to calculate the times for vectors SV11, SV21, SV10 and SV20. Note that, t_0 is divided into six equal parts to cover the complete switching period according to the sequence proposed in Figure 10.

5. Numerical Results

Simulations using a predominantly inductive load are performed using PSIM software. The numerical results are obtained in an open loop configuration under the parameters listed in Table 2. The developed simulations allow validation of the common mode behavior of the proposed topology. Figure 11 shows the switching pattern along more than two 60 Hz grid periods for the odd switches and the decoupling switches of both inverter modules. The sectors along each period are also included for reference. Note that, if sector 1 is observed, the switching pattern corresponds to that shown in Figure 10, after that, Sector 2 changes to the new active vectors V_2 and V_3 , and so forth, until the total period is completed. In Figure 12 from top to bottom the output three-phase currents and the common mode current are depicted. Note that, the output currents correspond with a sinusoidal waveform plus the switching ripple expected due to the commutations of the semiconductors. The $THD_{ia,ib,ic}$ measured is around 13.76 % which is mainly due to the switching ripple. Moreover, the common mode current presents a small RMS value which is 4.4 mA which fulfills the main objective of the proposed system. The line-to-line voltages are depicted in Figure 13 where it can be observed that the waveforms correspond to those typical in a two-level three-phase full-bridge inverter. Additionally, Figure 14 shows, from top to bottom, the parasitic capacitor voltages v_{cp1} and v_{cp2} and the CMC, i_{CMC} . As observed, the voltages across the parasitic capacitors remain constant at values of $-1/3V_{DCA}$ for C_{p1} and $-2/3V_{DCB}$ for C_{p2} . These constant voltages are produced by the space vector algorithm used to control the proposed inverter. A dynamic measurement has also been performed, as shown in Figure 15, where a step load change from 50Ω to 25Ω is applied. Notably, this power step does not cause transients in the common-mode current, indicating that the proposed system is robust against variations of inverter power.

Table 2. Simulation and experimental parameters.

Parameter	Value	Parameter	Value/Part number
V_{DCA}	250 V _{DC}	Z_g	10 Ω
V_{DCB}	250 V _{DC}	R_a, R_b, R_c	25 Ω
C_1 and C_2	2200 μF	f_{sw}	7.7 kHz
L_a, L_b, L_c	2 mH	f_g	60 Hz
C_{p1}, C_{p2}, C_{pb}	160 nF	DIODES/IGBTs	STTH200R04TV / SKM50GB12T4

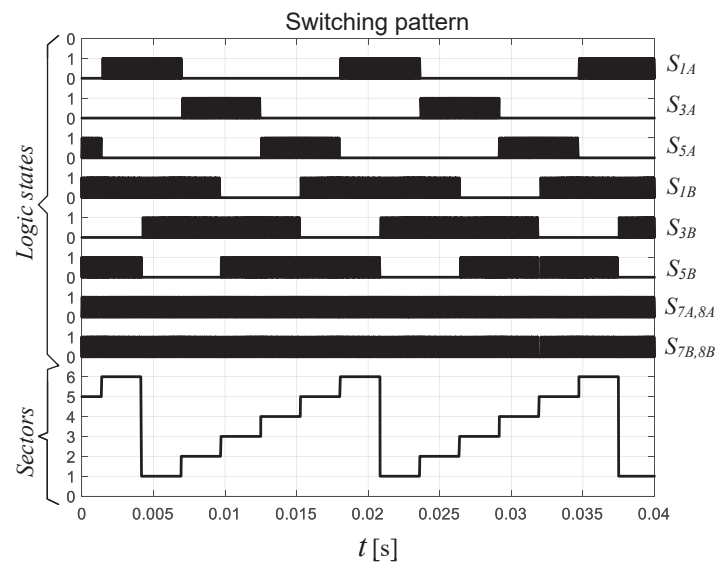


Figure 11. Proposed switching pattern and evolution of Sectors along a grid period.

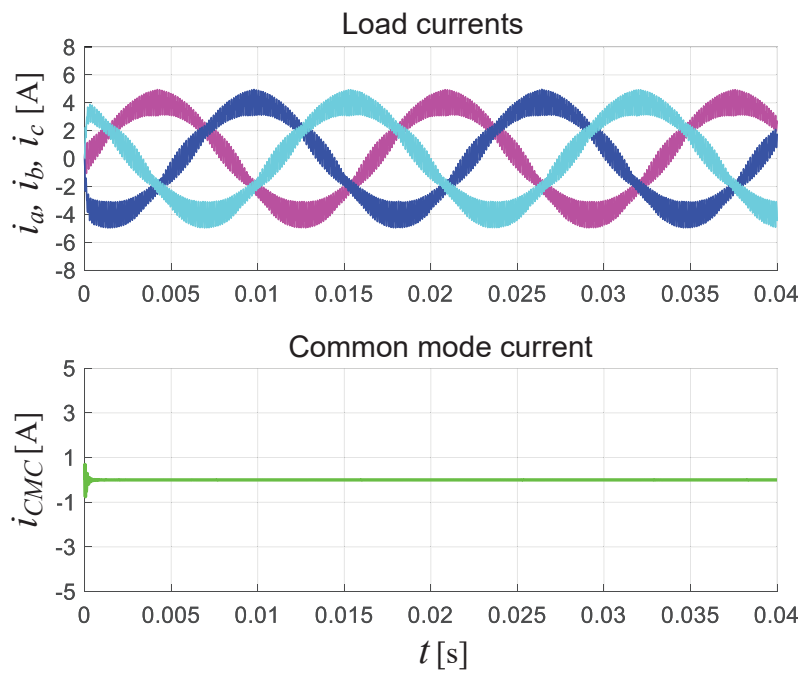


Figure 12. (From top to bottom) Steady-state response of output currents (i_a, i_b, i_c), and leakage ground current (i_{CMC}).

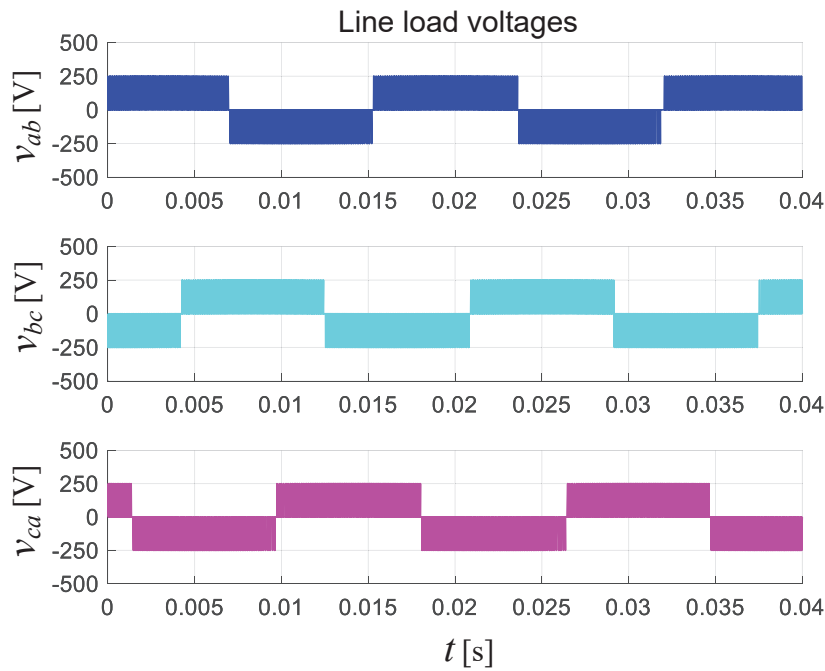


Figure 13. (From top to bottom) Steady-state response of output line voltages (v_{ab} , v_{bc} , v_{ca}).

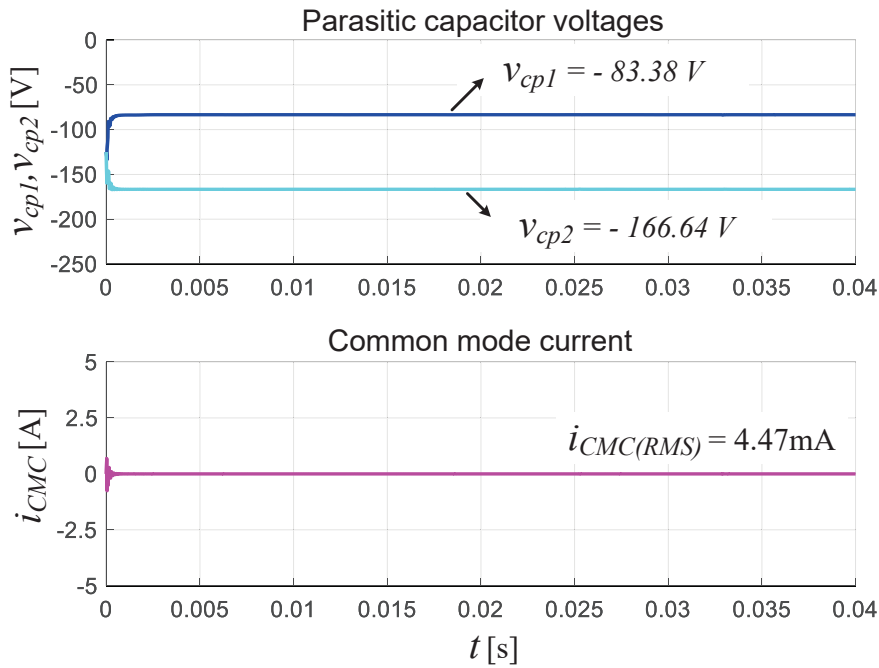


Figure 14. (From top to bottom) Steady-state response of parasitic capacitor voltages, v_{cp1} , v_{cp2} , and common ground current, i_{CMC}

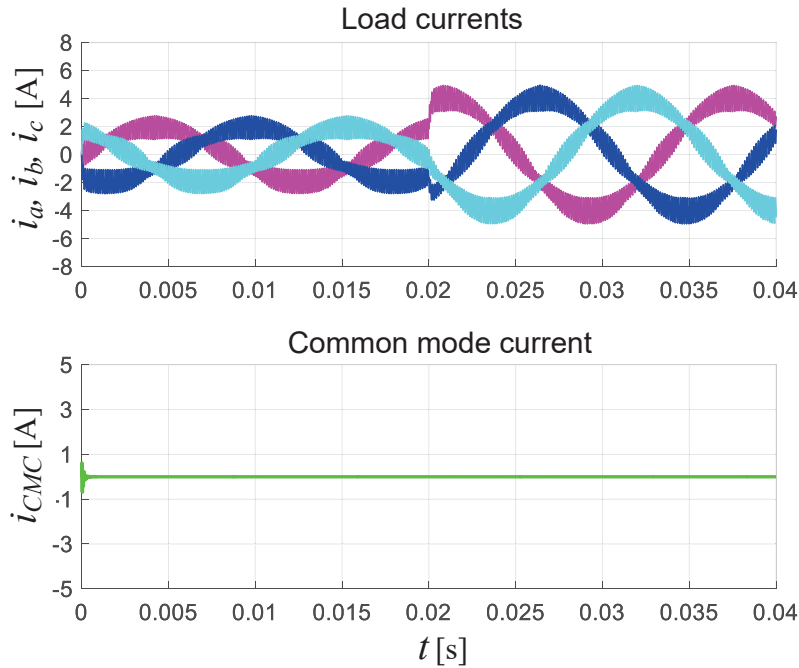


Figure 15. (From top to bottom) transient response of output currents, i_a , i_b , i_c , and common ground current, i_{CMC} .

6. Experimental Results

The experimental validation has been performed by implementing a laboratory prototype. The experimental prototype parameters are the same as those declared in Table 2. The semiconductors of the system are implemented using diode modules STTH200R04TV from STMicroelectronics and IGBT modules SKM50GB12T4 from Semikron. The modulation algorithm is programmed in a Digital Signal Processor (DSP) model TMS320F28335 mounted in a development board designed in the lab and using PSIM. The SVPWM signals are measured at the output of the DSP to validate the algorithm which are shown in Figure 16. As it can be noted, these signals contain the same sequence as in the simulation results, note also that only one grid period is considered. Moreover, Figure 17 shows the experimental three-phase output currents whose waveforms are almost sinusoidal plus the switching ripple as in the simulation results. The CMC is also measured, with an *RMS* value of 92.3 *mA*, higher than in simulation, due to the presence of passive parasitic components in the circuit. Moreover, experimental results are also obtained for line-to-line voltages. The results are depicted in Figure 18 where the common mode current is also included. The voltage waveforms show the corresponding three-level and the maximum voltage corresponds with 250V as is defined in Table 2.

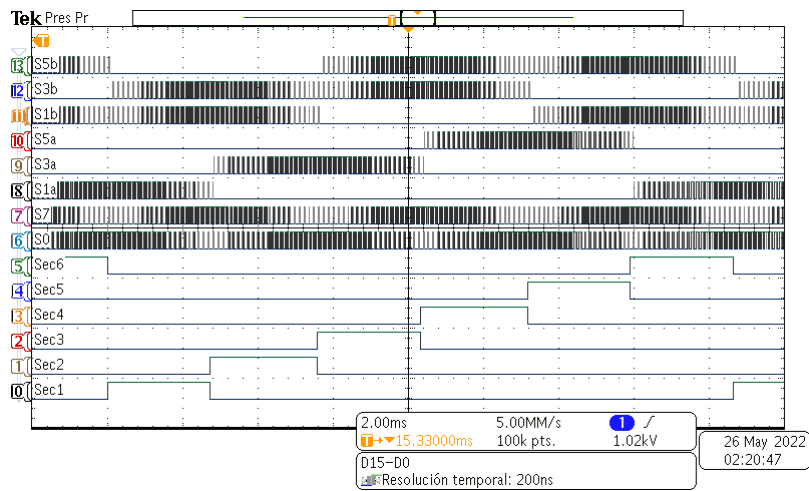


Figure 16. (From top to bottom) Space vector modulation sequence.

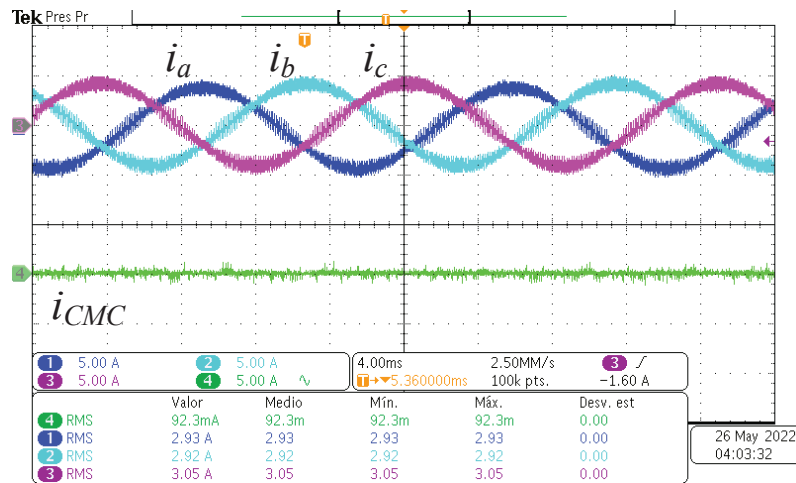


Figure 17. (From top to bottom) Steady-state response of outputs currents (i_a , i_b , i_c), and leakage ground current (i_{CMC}).

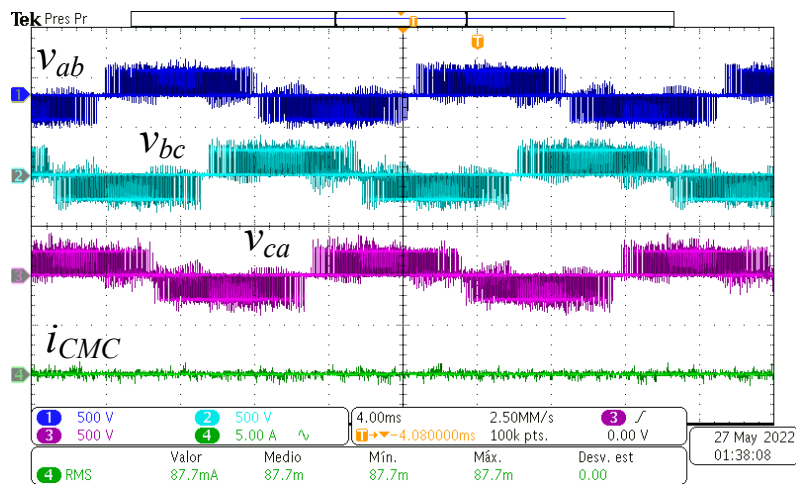


Figure 18. (From top to bottom) Steady-state response of line-to-line voltages (v_{ab} , v_{bc} , v_{ca}), and leakage ground current (i_{CMC}).

Voltages across the parasitic capacitors v_{Cp1} and v_{Cp2} are depicted in Figure 19. Note that, these voltages are constant as expected according to the proposed SVPWM algorithm. The voltage magnitudes are around 83V and 170V for v_{Cp1} and v_{Cp2} respectively, consistent with the simulation results. Finally, to validate the robustness under power changes the experimental results in Figure 20 are also obtained. A step-up power load varying the load resistance from 50Ω to 25Ω is applied to demonstrate that the i_{CMC} magnitude remains with the same waveform and value.

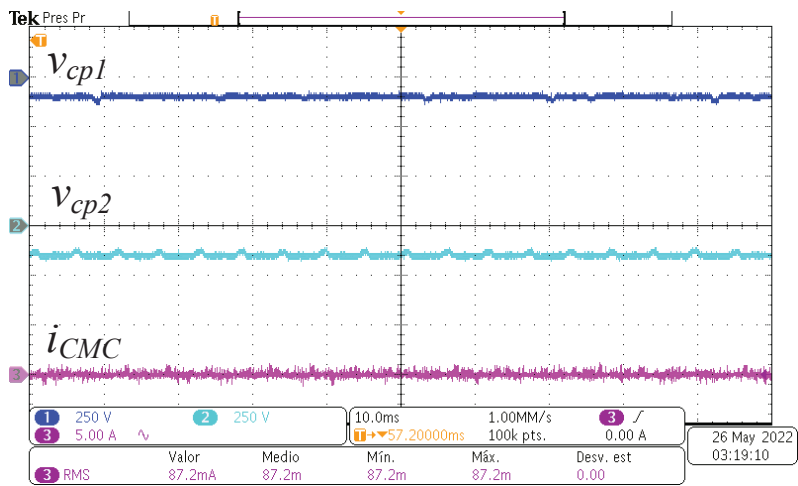


Figure 19. (From top to bottom) Steady-state response of capacitor voltages (C_{p1} , C_{p2}), and leakage ground current (i_{CMC}).

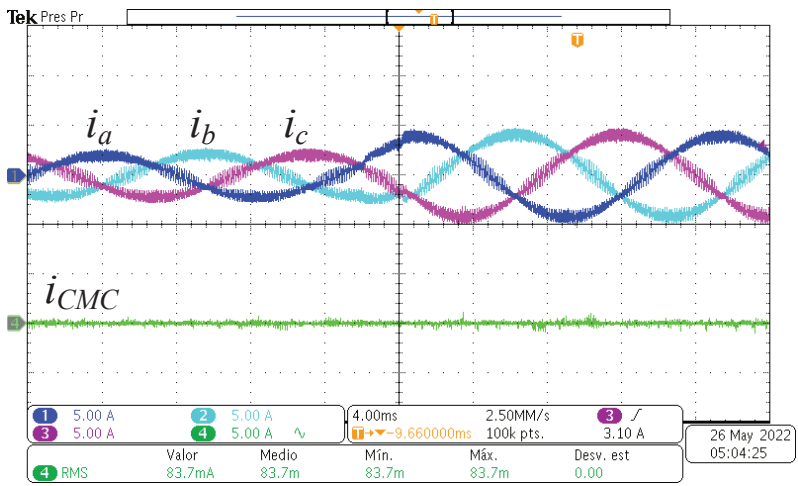


Figure 20. (From top to bottom) Transient response of output currents (i_a , i_b , i_c) and ground leakage current (i_{CMC}), under step load changes from 100% to 50%.

7. Conclusions

In this paper, a three-phase inverter topology and its space vector modulation strategy were proposed to deal with the common mode current problem in induction motor drives. The proposed system made use of two three-phase two-level full-bridge inverter modules with a DC decoupling circuit. Each module was intended to set the odd active vectors or the even active vectors achieving in this way constant common mode voltage and as a result very low common mode current. An key advantage of the proposed method was that the active vectors can be configured once along a complete sector, then the DC decoupling circuit allows allows the application of both active and zero vectors, thereby reducing power losses. Experimental and simulation results demonstrate that the common mode current was effectively reduced and the independence of the proposed method regarding system power. These results support the conclusion that the proposed inverter topology is well-suited for motor drive systems and transformerless photovoltaic applications.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Altern Current
DC	Direct Current
PWM	Pulse Width Modulation
CMV	Common Mode Voltage
CMC	Common Mode Current
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
IGBT	Isolated Gate Bipolar Transistor
DSP	Digital Signal Processor

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