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Probe Card Technologies in Advanced Semiconductor Testing for Wide Band Gap Devices

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Abstract

The rapid adoption of Wide Band Gap (WBG) and Ultra-Wide Band Gap (UWBG) semiconductor technologies, most notably Silicon Carbide (SiC) and Gallium Nitride (GaN), is reshaping wafer-level electrical testing beyond conventional silicon-based probing infrastructures [1,2]. Modern SiC devices require blocking voltage verification in the 650 V–3.3 kV range, extending beyond 6.5 kV, while GaN HEMTs operate with voltage slew rates exceeding 50–150 V/ns and current slew rates above 1–5 kA/µs. Under these conditions, probe cards evolve from passive interconnects into multi-physics systems coupling electrical, thermal, and mechanical domains [3,4]. Vertical MEMS probe card architectures enable high contact density, per-contact currents of 2–10 A (aggregated >1–3 kA), and loop inductance in the single-digit nanohenry range. This work analyzes probe-to-wafer contact physics, including constriction resistance (10–50mΩ) and wear under high current (>10^5 A/cm²) and high-frequency conditions [4]. Electro-thermal limitations are discussed with focus on insulation integrity, partial discharge, di/dt-induced overshoot, and localized heating (>100–200 °C) [5–7]. Emerging high-voltage solutions include ceramic insulation, controlled atmospheres, and on-board sensing. Wafer-level testing combines full-wafer screening with burn-in-like stress methodologies, where body diode characterization enables early defect detection in SiC devices. These results highlight the critical role of probe cards in WBG manufacturability and test reliability.

Keywords: Wide Band Gap semiconductors; wafer-level testing; PROBE card architectures; vertical MEMS probes; high-voltage semiconductor testing

1. Introduction

Wafer-level electrical testing is a dominant contributor to both manufacturing yield loss and overall cost of test, accounting for up to 20–30 % of total test cost for power semiconductor devices with full parametric and reliability screening[2]. The probe card, acting as a space-transforming contact interface, represents the most stressed element of the test cell, serving as the electrical, thermal, and mechanical interface between the Automated Test Equipment (ATE)-typically limited to ≤ 3 kV per channel-and the Device Under Test (DUT).

In silicon technologies, probing environments were historically limited to DC voltages below 800 V, maximum currents below 2 A per pin, and pad pitches ≥ 60 µm. These conditions allowed the use of cantilever-based or hybrid probe technologies with modest electrical optimization. In contrast, Wide Band Gap power devices fundamentally alter this landscape. State-of-the-art SiC MOSFETs exhibit critical electric fields of 2.5–3 MV/cm (compared to approximately 0.3 MV/cm for silicon)[1], on-state current densities exceeding 500–1000 A/cm², and junction temperature ratings up to 175–200 °C. GaN HEMTs, conversely, are characterized by very low intrinsic device capacitances, switching frequencies corresponding to effective bandwidths in the hundreds of megahertz, and dv/dt values routinely exceeding 100 V/ns. These figures push wafer-level probing well beyond traditional design envelopes, exposing hard limits in contact resistance stability, parasitic inductance and loop area, dielectric spacing and surface discharge behavior, and local thermal dissipation at the probe tip [1,3,6]. As a result, probe card development has shifted toward a system-level co-design

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paradigm, integrating Vertical MEMS probe architectures, multilayer space transformers, Kelvin sensing, and controlled electromagnetic routing as standard practice in WBG test environments [4].

2. Vertical Probe Card Architectures

The transition from silicon to Wide Band Gap power devices fundamentally alters the physical and electrical requirements imposed on wafer-level probing. Conventional cantilever-based probe cards, historically optimized for moderate voltage, current, and switching speed, encounter intrinsic limitations when applied to SiC and GaN technologies. These limitations arise primarily from extended current loop geometries, insufficient control of parasitic inductance, and inadequate dielectric spacing under multi-kilovolt stress [4].Vertical probe card architectures were introduced to overcome these constraints by re-engineering the probe-to-tester interconnect as a compact, symmetric, and scalable three-dimensional system. Unlike cantilever solutions, vertical probe cards orient probe elements orthogonally to the wafer surface and integrate them into multilayer redistribution structures, commonly referred to as space transformers. Figure 1 illustrates the conceptual architectural differences between cantilever-based and Vertical MEMS probe card solutions.

By minimizing electrical path length and loop area, vertical architectures significantly reduce parasitic inductance, typically achieving 1–3 nH per probe channel, compared to 5–15 nH commonly observed in cantilever solutions. This reduction is critical for dynamic WBG measurements, where high di/dt values can otherwise produce substantial voltage overshoot and waveform distortion. Furthermore, the vertical geometry naturally improves symmetry between force application, current conduction, and electric-field distribution, reducing localized stress concentrations at the probe-to-pad interface [3,6,7].

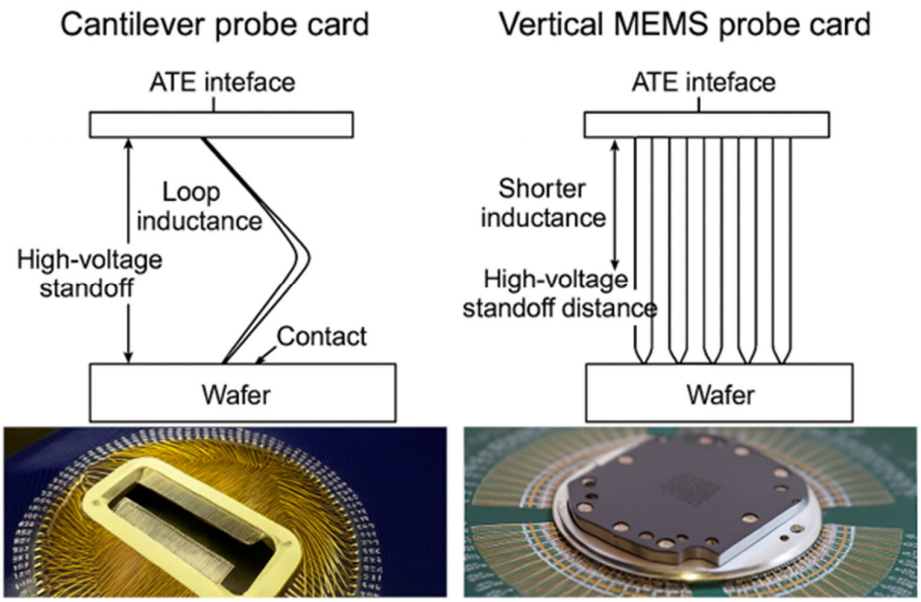

Figure 1. Conceptual and practical comparison between conventional cantilever probe cards and Vertical MEMS probe card architectures. The upper diagrams highlight differences in current loop length, parasitic inductance, and high-voltage standoff. The lower photographs show representative cantilever and Vertical MEMS probe cards.

The intrinsic complexity of vertical probe cards is best understood by examining their internal mechanical and electrical composition. Figure 2 shows an exploded view of a representative Vertical

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MEMS probe card assembly, highlighting the probe head, multilayer space transformer, printed circuit board, intermediate mechanical rings, and stiffening structures. This architecture illustrates the tight coupling between mechanical stability, electrical routing density, insulation integrity, and thermal management required for advanced WBG wafer-level testing.

The architectural features of vertical probe cards directly address the core challenges of WBG probing. Reduced parasitic inductance enables accurate dynamic characterization of fast-switching GaN devices, while improved dielectric spacing and field control support reliable high-voltage SiC testing without premature partial discharge inception. The mechanical robustness and scalability of vertical architectures further enable compatibility with increasing wafer diameters and higher test parallelism.

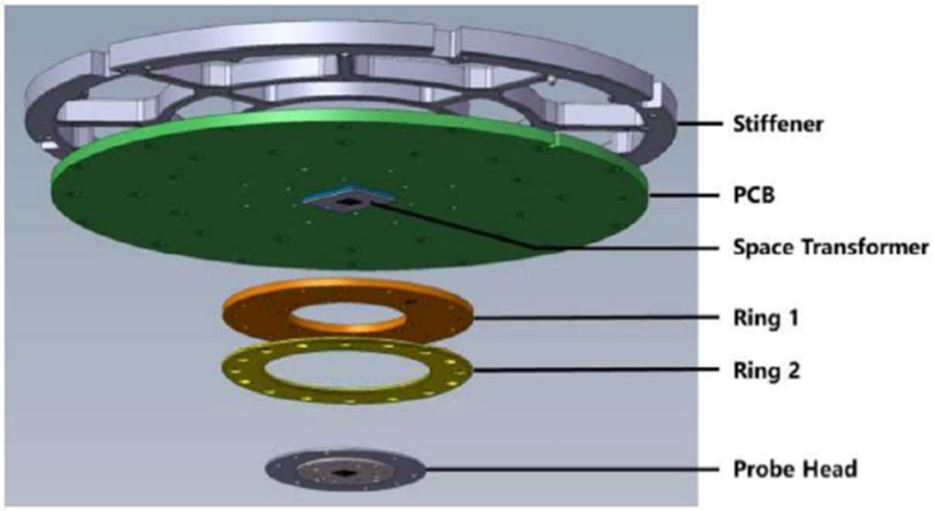

Figure 2. Exploded view of a Vertical MEMS probe card assembly highlighting the probe head, multilayer space transformer, PCB, mechanical rings, and stiffening structures.

2.1. Probe Card as a Multi-Physics System

A modern probe card must be treated as a strongly coupled electro-thermal-mechanical system, where second-order effects become first-order error sources under WBG operating conditions [4].

2.1.1. Electrical Domain

Each probe channel constitutes a distributed interconnect characterized by DC resistance in the range of 20–80mΩ per probe, depending on geometry and metallurgy, self-inductance of approximately 5–15nH in cantilever architectures and 1–3nH in Vertical MEMS architectures, and parasitic capacitance in the order of 50–200fF per channel [4].

For GaN devices switching with di/dt ≈ 2 kA/μs, even 2nH of loop inductance generates a voltage overshoot of approximately 4 V per switching event, which is sufficient to corrupt dynamic RDS(on) or switching-loss measurements and, in extreme cases, to overstress sensitive gate structures [3,5].

2.1.2. Contact Physics and Resistance Evolution

At the probe-to-pad interface, the true electrical contact area is typically less than 1 % of the apparent contact footprint and is governed by asperity-level deformation mechanisms. For gold- or rhodium-based probe tips contacting aluminum or copper pads, typical contact forces range from 1 to 5 gf, resulting in an initial contact resistance of approximately 10–30mΩ. Over the probe lifetime, contact resistance generally increases, reaching values two to five times higher after 10^5–10^6 touchdowns. Under high-current stress, localized Joule heating occurs at the micro-contact spots

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where current constriction is maximum. Even when the wafer chuck temperature is controlled between 25 °C and 125 °C, local temperatures at the probe-to-pad interface can exceed 150–250 °C. These conditions promote oxide growth, material transfer, micro-welding phenomena, and pad damage, making contact resistance a time- and history-dependent parameter. This behavior directly impacts test repeatability, measurement margins, and long-term probe card reliability [4,8].

2.1.3. Mechanical and Thermal Coupling

Vertical MEMS probes typically operate with spring constants between 0.3 and 1.5 N/mm, elastic stroke values of 40–80 μm, and planarity tolerance across the probe card of ± 5–10 μm. In large arrays exceeding 30,000–50,000 probes, even a 10 % force variation can translate into measurable electrical dispersion due to non-uniform contact formation. From a thermal standpoint, power dissipation per probe can reach 50–200 mW during high-current testing. Heat extraction depends on the entire mechanical stack, including probe metallurgy, space transformer materials, mechanical stiffeners, and PCB structure. Coefficients of thermal expansion mismatch between these elements introduce additional mechanical stress during temperature cycling and contribute to long-term fatigue of MEMS structures. These coupled electro-thermal-mechanical effects reinforce the need for electro-thermal-mechanical co-simulation during probe card design [4,8].

2.2. Signal and Power Integrity Limitations

In advanced WBG device testing, signal integrity (SI) and power distribution network (PDN) behavior of the probe card become first-order design constraints rather than post-layout verification concerns [5]. Unlike silicon logic devices, WBG power semiconductors impose the simultaneous presence of high current, high voltage, and fast edge-rate excitation, forcing the probing system to behave as a distributed power delivery network rather than a simple measurement interconnect.

GaN HEMTs operating with dv/dt values of 50–150 V/ns and edge rates corresponding to > 100–300 MHz spectral content makes probe-level impedance discontinuities directly observable at the device terminals. Even short probe paths introduce reflection coefficients exceeding 10–15 % for modest impedance deviations, resulting in voltage ringing of 5–15 V on 650 V-rated devices and timing uncertainty exceeding 2–5 ns in dynamic waveforms. These effects directly compromise dynamic RDS(on) and switching-loss characterization unless probe impedance is tightly controlled and properly de-embedded [3,5,7]. In WBG testing, PDN analysis is no longer limited to voltage droop estimation but becomes a predictive tool for thermal management. A typical vertical probe card PDN exhibits DC path resistance of 5–20mΩ per power pin, including probe, redistribution, and connector contributions, and supports aggregate switching currents of 0.5–3 kA in multi-site wafer-level testing. Transient simulations show that current crowding at probe micro-contacts can generate local power densities exceeding 200–400 W/cm², leading to transient junction-to-probe temperature rises of 40–80 °C within milliseconds and peak contact temperatures surpassing 200–250 °C, even with chunk temperature set at 125 °C. Integrating PDN impedance extraction with transient thermal solvers allows prediction of thermal runaway conditions and definition of safe test duty cycles, making PDN analysis a preventive thermal management tool rather than a simple SI verification step [4].

3. Wide Band Gap Device Testing Challenges

SiC wafer probing routinely requires blocking voltage verification at 1.2 kV, 1.7 kV, and 3.3 kV, with emerging technologies extending toward 6.5 kV [1,6]. Electric-field management below 0.2–0.3 MV/cm along probe card surfaces is essential to prevent partial discharge inception, particularly in air or nitrogen environments. Improper spacing and geometric field enhancement can lead to partial discharge well below the intrinsic breakdown voltage of the device under test, especially at wafer edges and scribe streets [4].

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At the probe-to-pad interface, effective current densities can exceed 10^5–10^6 A/cm², resulting in contact hot-spot formation, accelerated wear, and probe metal recrystallization. GaN devices operating with dv/dt > 100 V/ns amplify the impact of every parasitic element in the test path. In this regime, loop inductance reduction below 2nH is no longer optional but mandatory for accurate dynamic characterization.

Traditional ATE platforms were historically optimized for silicon devices operating below 300–600 V, with limited current density, moderate dv/dt, and relatively low electromagnetic stress. Wide Band Gap devices fundamentally invalidate these assumptions. Standard tester load boards and pogo-based interfaces are not designed for continuous operation above 1.5–3 kV, leading to partial discharge inception and long-term insulation degradation.

Furthermore, WBG testing often requires tens to hundreds of amperes per site, with transient current slew rates exceeding kA/μs, far beyond the PDN capability of conventional ATE channels [2,6,7]. GaN devices impose effective bandwidth requirements above 200–300 MHz, making traditional tester interconnects dominant sources of measurement error in dynamic testing [3,5]. Thermal instability adds an additional constraint: the ATE–prober–probe card stack is not thermally symmetric, and without coordinated redesign, localized temperature drift leads to parametric instability and reduced test repeatability.

As a consequence, testing WBG devices without upgrading the entire ATE ecosystem results in systematic measurement errors, yield loss, and accelerated hardware degradation.

Effective WBG testing requires co-optimization of tester power architecture, load board materials and spacing, prober mechanics and insulation, and probe card electrical and thermal design. This shifts WBG testing from a component-level problem to a system-level engineering challenge, fundamentally altering cost-of-test models [2,4].

3.1. Technology Trends

The technology trends reported in industrial forums such as SWTEST clearly indicate that high-voltage wafer-level testing of Wide Band Gap devices is driving a transition from conventional probe card solutions toward highly engineered, application-specific architectures. Beyond Vertical MEMS probe card architectures, which remain the primary enabler for low-inductance and high-parallelism probing, several additional technologies have been introduced to address the specific challenges of kilovolt-level operation. A key development concerns the use of advanced insulating materials within the probe card stack. In particular, ceramic-based structures are increasingly adopted in high-voltage probe card design due to their high dielectric strength, low permittivity, and thermal stability. These materials enable improved electric field control, reduced risk of surface discharge, and enhanced mechanical robustness under thermal cycling conditions, as reported in recent industrial contributions. In parallel, high-voltage probing is increasingly performed in controlled environments to suppress partial discharge and arc formation. Pressurized chambers or controlled atmosphere solutions (e.g., nitrogen environments) are employed to increase the breakdown voltage of the surrounding medium and stabilize high-field regions. Such approaches, widely discussed in SWTEST contributions on high-voltage probing, allow reliable operation above 2–3 kV by mitigating air ionization effects and reducing sensitivity to humidity and contamination. Another emerging trend is the integration of on-board sensing and monitoring capabilities within the probe card. Embedded sensors, including current and temperature monitoring elements, are used to detect abnormal operating conditions such as localized overheating or current runaway during high-power testing. These sensing capabilities enable real-time protection strategies, preventing damage to both the device under test and the probe card itself, and improving overall test reliability. From an electrical standpoint, electric field engineering remains the dominant design constraint above approximately 1–2 kV. Techniques such as guard-ring implementation, field grading, and optimization of creepage distance are required to prevent premature partial discharge and ensure insulation integrity across the probe card structure. In addition to voltage constraints, current density represents a critical limitation. Advanced probe technologies and materials are being introduced to support tens of

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amperes per contact, while minimizing Joule heating and contact degradation. This is particularly relevant for SiC devices, where high current and high voltage are simultaneously present. Thermal management has consequently become an integral part of probe card design. Heat dissipation must be addressed at the probe, interconnect, and system level, requiring co-design of mechanical structures, materials, and test methodologies, including duty-cycle-controlled stress conditions. These trends demonstrate that probe cards for WBG applications are evolving into integrated electro-thermal-mechanical and insulation-engineered systems, where material selection, environmental control, and real-time monitoring play a fundamental role in enabling reliable high-voltage wafer-level testing [7,9–12].

4. Industrial Implementation and Advanced Probe Card Technologies

Probe card design for WBG devices diverges significantly depending on the test insertion point within the manufacturing flow.

4.1. Wafer-Level Test (Parametric and Screening)

Wafer-level testing of SiC and GaN devices is performed across the entire wafer, enabling full electrical screening prior to singulation. Unlike selective or limited-parallelism approaches, wafer-level test is inherently designed to maximize coverage, allowing early identification of defective dies and improving overall manufacturing yield. In the context of *W*ide *B*and *G*ap devices, wafer-level test is not limited to basic parametric characterization but increasingly includes stress-oriented screening methodologies, analogous to burn-in concepts traditionally applied at package level. These tests are performed under controlled electrical and thermal conditions to accelerate failure mechanisms and identify weak devices at an early stage. A key screening technique at wafer level is the evaluation of the intrinsic body diode in SiC MOSFETs. Body diode conduction and leakage characteristics provide a fast and effective indicator of crystal defects, dislocations, and process-induced anomalies. As a result, body diode testing is widely used as a first-level screening method across the entire wafer before proceeding to more complex measurements. From an architectural standpoint, wafer-level probe cards must support simultaneous high-voltage and moderate-to-high current operation across a large number of contact points.

This requires:

- Vertical MEMS probe architectures for dense and uniform contact distribution;
- *H*igh-voltage insulation design;
- Optimized creepage distance;
- Field control ,Kelvin configurations for accurate low-current;
- Leakage measurements *and* Integration with controlled atmosphere or insulation strategies to suppress partial discharge

Thermal management is also critical, as wafer-level stress conditions can lead to cumulative heating effects across the wafer surface. Test methodologies therefore rely on controlled duty cycles and coordinated thermal control between chuck and probe card. Overall, wafer-level testing for WBG devices represents a combination of parametric characterization and early-stage reliability screening, where full-wafer coverage and defect-oriented measurements, such as body diode evaluation, play a central role in ensuring device quality and process stability [2,4].

4.2. Medium Parallelism Test (Selective Parallel Test)

In mid-volume power device test flows, such as automotive applications, parallelism typically ranges from 4 to 16 sites, with stress-oriented testing including avalanche and short-circuit conditions [4]. Higher per-device current pulses in the 50–200 A range require reinforced power buses, reduced site-to-site coupling, enhanced PDN decoupling near probe tips, and increased mechanical robustness, often prioritized over extreme contact density. For WBG devices, medium parallelism test is primarily used for advanced electrical characterization under realistic operating conditions.

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Typical test activities include:

- Blocking voltage verification up to the rated device limits (1.2 kV–3.3 kV and beyond)
- Leakage current measurement under high electric field conditions
- Dynamic switching characterization, including double-pulse-like tests for extraction of switching losses
- On-state resistance (RDS(on)) evaluation under controlled current levels
- Body diode characterization, including forward conduction and reverse recovery behavior
- Compared to wafer-level screening, these tests require tighter control of electrical parasitics and improved measurement fidelity, particularly for fast switching devices such as GaN HEMTs and SiC MOSFETs.

4.3. Known-Good-Die (KGD) Testing

Known Good Die (KGD) testing represents the final screening stage before device assembly, ensuring that only fully functional and reliable dies are used in advanced packaging solutions such as multi-chip modules (MCM) and system-in-package (SiP). In contrast to wafer-level testing, KGD testing is performed after wafer dicing on individual dies, enabling more accurate electrical characterization under application-relevant conditions. Wafer-level parametric screening alone is often insufficient for WBG devices, as it cannot fully reproduce the electrical stress conditions required to validate high-voltage and high-current operation. In particular, limitations in voltage, current capability, and die-to-die interaction effects reduce the effectiveness of wafer-level measurements for final device qualification. For this reason, KGD testing is essential to guarantee device performance and reliability prior to assembly [4].

Typical KGD test flows include both static and dynamic electrical characterization:

- Static tests: blocking voltage verification, leakage current, and threshold voltage
- On-state characterization: RDS(on) measurement under high current conditions
- Dynamic tests: switching behavior and double-pulse-like measurements
- UIS (Unclamped Inductive Switching) tests for ruggedness evaluation
- Burn-in or test-during-burn-in to screen early-life failures.

Dedicated KGD test cells and die handlers are used to perform these measurements. These systems support high-voltage and high-current operation (e.g., up to ~2 kV and hundreds of amperes) and enable multi-site testing with controlled thermal environments. Advanced handlers allow testing under different temperature conditions, including room and elevated temperature, and integrate anti-arcing protection features to ensure safe high-voltage operation [10–13]. A critical aspect of KGD testing is the handling and contacting of singulated dies. Dies are typically mounted on carriers or trays and aligned individually before probing. Electrical contact is achieved using probe pins or contactors, while vacuum or mechanical clamping is used to ensure positioning stability. Automated alignment systems compensate for die placement variability, enabling repeatable measurements across large volumes [3].Thermal and environmental control is also essential. KGD systems integrate temperature-controlled chucks and may include controlled atmosphere environments to improve measurement stability and reduce the risk of electrical discharge during high-voltage testing. Finally, KGD testing enables binning and sorting of dies based on performance, ensuring that only devices meeting the required specifications are selected for assembly. This step is particularly critical in high-reliability applications, where defective dies would significantly impact system yield and long-term reliability. Overall, KGD testing extends wafer-level screening by enabling full electrical validation under realistic operating conditions, playing a key role in the manufacturability of advanced WBG-based systems [4,5,10].

5. Integrated Outlook and Conclusions

Advanced probe cards for WBG applications exhibit intrinsic mechanical and electrical complexity, reflecting the tight coupling between stiffness, alignment, routing density, insulation

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integrity, and thermal management. This complexity naturally motivates joint development approaches across the test ecosystem, involving probe card manufacturers, ATE suppliers, prober vendors, and end customers. Such collaborations also provide opportunities for industry–academia research in micro-contact physics, insulation materials, partial discharge mitigation, and electro-thermal-mechanical co-simulation [4,7].

Wide Band Gap semiconductor technologies are not only redefining power device performance but are also transforming the fundamental requirements of wafer-level electrical testing. High voltage, high current density, and fast switching dynamics push traditional probing infrastructures beyond their safe operating limits, forcing a transition toward system-level test engineering.

Vertical MEMS probe card architectures emerge as the most scalable solution to these challenges, combining low parasitic inductance, high current capability, and robust insulation integrity within compact form factors. However, their effectiveness depends on coordinated redesign of the entire test ecosystem. In this context, probe cards evolve from passive interfaces into strategic enablers of WBG manufacturability, reliability, and cost control, positioning wafer-level test as a key discipline in the successful industrialization of next-generation power electronics.

Conflicts of Interest: The author declares no conflict of interest.

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