Article

On Nonlinear Dynamic Characteristics of Peak-Current-Mode Controlled DC–DC Boost Converters with Fractional-Order Output Filtering Capacitor

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Abstract: The concepts of fractional calculus and the related techniques have been gaining momentum in circuit system fields, and an increasing body of evidence suggests that fractional-order characteristics are widely distributed in electronic components. In this paper, we consider the fractional characteristics of non-solid aluminum electrolytic capacitors and focus on the nonlinear dynamic characteristics of peak-current-mode controlled (PCMC) dc-dc boost converters with such components. In the work, we establish a piecewise smooth non-commensurate fractional-order model to describe the converter, in which the fractional-order equivalent impedance model of capacitors is adopted and the detailed control loop is considered. In order to analyze the converter, we use the fractional Adams-Bashforth-Moulton typed method (F-ABM) and stroboscopic map technique to obtain the time-domain solutions and the bifurcation diagram. The results of bifurcation diagrams indicate that, with the change of different parameters, the converter enters chaotic state through period doubling bifurcation. In order to provide empirical evidence for the nonlinear dynamic analysis, we consider both circuit-level simulation and experiments in the work, the results of which further confirm the results of theoretical analysis.

Keywords: fractional-order characteristics; capacitors; dc-dc boost converter; piecewise smooth; nonlinear dynamic characteristics

1. Introduction

Power electronic converters, such as dc-dc converters, are typical piecewise smooth circuit systems due to the turn-on and turn-off effects of power switches, and their performance is closely related to operation conditions. It is generally believed that, when the load or power source fluctuates, or the parameters of passive components are not properly configured, one may be able to observe nonlinear dynamic phenomena such as bifurcations and chaos in power electronic converters, which are undesired in practical applications [1]. For instance, the active duty ratio of a PCMC dc-dc boost converter is generally limited to less than 0.5 in continuous conduction mode (CCM), because when the ratio exceeds this range, the converter will be in period-2 sub-harmonic oscillation state, so the voltage boost capability is limited in applications [2].

In order to better predict the nonlinear phenomena of power electronic converters and provide design-oriented guidance in practice, lumped parameter models and integer-oder piecewise linear differential equations are widely adopted to describe the the electrical relationship of the state variables of power electronics converters [3]. To analyze the nonlinear behaviours of the converters, one can solve the initial value problem (IVP) of integer-oder ordinary differential equations (ODEs) by both numerical and analytical calculation methods, and use the stroboscopic map technique to sew up the solutions

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of piecewise linear differential equations [4]. Based on these methods, a large number of researches have been conducted to explore nonlinear dynamic phenomena in power electronic converters, such as those surveyed in literature [5–7].

By reviewing the key publications in the related field, one can find that, the parameters of traditional lumped parameter models usually appear in the form of parameter variables (or parameter vector), while in the solving process of IVP, these parameter variables are usually substituted with constant nominal values or the measured constant values under a fixed condition. However, not only the load and power supply may change, but also some other electronic components may experience parameter drift in practice [8,9,11**?**]. For instance, non-solid electrolytic aluminum capacitors are widely adopted in power electronic converters, but their capacitance and equivalent series resistance (ESR) can be easily affected by operating frequency, working temperature, and so on. In order to reflect the impacts of parameter variations on the nonlinear characteristic of converters, one can draw bifurcation diagrams by changing the parameters of traditional lumped parameter models, but the model itself cannot reflect the parameter drift of the components. That is to say, traditional models cannot reflect the correlation between the microscopic characteristics of electronic components and the macroscopic electrical characteristics of converter systems. The results obtained by using traditional integer-order models may be biased in practice. Therefore, it is worthwhile to develop more precise and reliable methods to address the aforementioned concerns.

In recent decades, exploring the characteristics of electronic components arouses ever-increasing attention in circuit theory and application fields [12], and a rich source of evidence suggests that the characteristics of electronic components can be more effectively captured by using the concepts of fractional calculus compared to classical calculus-based models [13–15], and factional-order impedance (or constant phase elements, CPEs) based models have been widely adopted to describe the characteristics of electronic components, such as inductors [16], ultracapacitors (UCs) [17,18], lithium batteries [19], power MOSFETs [20], and non-solid electrolytic capacitors [21]. Therefore, using this model to bridge the gap between the microscopic characteristics of electronic components and the macroscopic characteristics of circuit systems has become a hot issue in recent years.

In this paper, taking a PCMC dc-dc boost converter as an example, we study the nonlinear characteristics of the converter with a fractional-order output filtering capacitor, and we carried out the following works:

- A piecewise smooth non-commensurate fractional-order model is developed for a PCMC dc-dc boost converter, which contains a fractional-order output filtering capacitor and a detailed control loop design based on a type UC3842 PCMC power management chip.
- A large-signal stability analysis is performed for the converter, in which the fractional Adams-Bashforth-Moulton typed method (F-ABM) and stroboscopic map technique are applied for tiem-domain calculation, while bifurcation diagrams are obtained for dynamic states justification.
- Both circuit-level simulations and experiments are provided to verify the correctness of the theoretical analysis.

To present the above features in detail, the rest of this paper begins with the derivation of the piecewise smooth model of the converter in section II. After that, a detailed nonlinear dynamic characteristic analysis of the converter is provided in section III. Then, in section IV, both the circuit-level simulation platform and experiment prototype are established, and the results are provided for validation and comparison. Finally, conclusion is outlined in Section V.

2. Piecewise Smooth Fractional-Order Model of PCMC DC-DC Boost Converters

2.1. Circuit configuration

It is a fast and cost effective option to use power management chip to control dc-dc converters in application. In this work, we use a type-UC3842 power management chip,

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which is a fixed frequency current-mode controllers [21], its internal structure is as depicted in Figure 1.

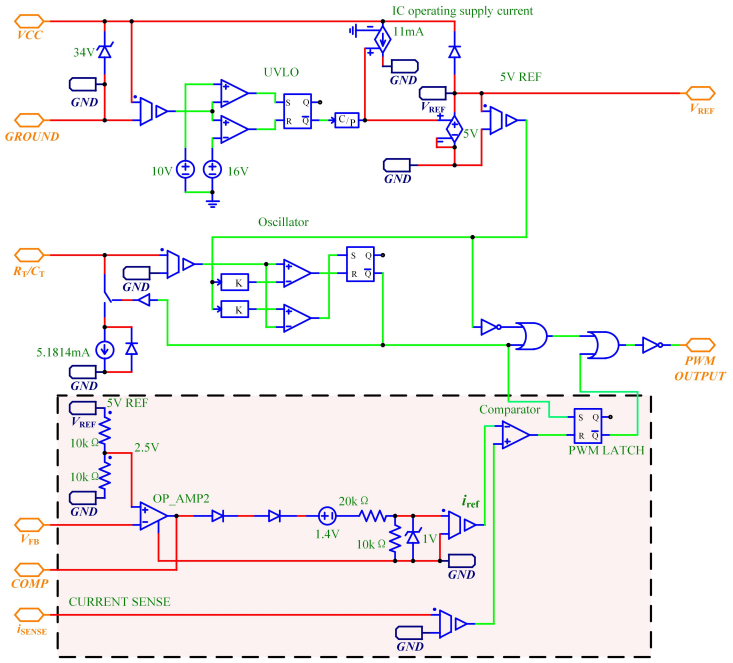

Figure 1. Internal structure of UC3842 type current-mode controller chip.

By adopting this chip to a dc-dc boost converter, one can achieve a PCMC design, the schematic diagram of which is depicted in Figure 2.

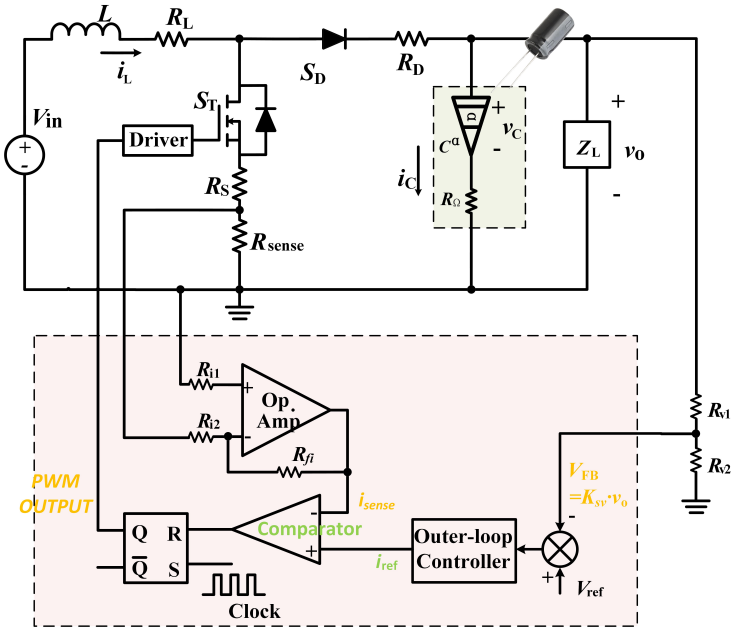

Figure 2. PCMC DC-DC boost Converter.

Note that the output filtering capacitor in Figure 2 is a non-solid electrolytic capacitor. According to a previous work [23], the capacitance and the equivalent series resistance of the capacitor have frequency-related fractional-order characteristics in a wide frequency band. Therefore, we use a fractional-order equivalent impedance model to represent it, where an ideal fractional-order capacitor C^{α} (or constant phase element, CPE) is in series

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with an estimated equivalent series resistance R_Ω. The symbol C is the nominal capacitance of the capacitor and the symbol α is the estimated fractional order of the capacitor.

In addition, note that in both Figure 1 and Figure 2, the two boxes with red background correspond to the same function module. Specifically, there are the same output voltage current sensing unit, inductor current sensing unit, the inner curent loop controller, and the outer voltage loop controller. The inner current loop usually includes an inductor current sensing resistor R_{sense}, and a proportional sampling unit is used to sample the inductor current i_L. The V_{FB} pin of the UC3842 chip is connected to a voltage divider composed by two resistors R_{v1} and R_{v2}, which is used to sample the output voltage v_o. The outer-loop controller can be achieved by configuring the circuit between the V_{FB} pin and the $COMP$ pin of the chip. For example, if one wants to used a typical PI controller in the outer loop, then one can configure the above two pins of the operational amplifier OP_{AMP2} as follows.

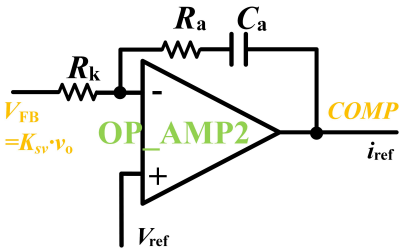

Figure 3. Implementation of an outer-loop PI controller.

According to the above Figure 3, one can deduce the the output of the outer voltage loop, or the reference signal i_{ref} of the inner current loop, as follows.

$$\begin{aligned} i_{ref}(t) &= V_{ref} - R_a C_a \frac{dv_a(t)}{dt} - v_a(t) \\ &= (1 + \frac{R_a}{R_k})V_{ref} - \frac{R_a}{R_k} K_{sv} v_o(t) + \frac{1}{R_k C_a} \int [V_{ref} - K_{sv} v_o(t)] dt, \end{aligned} \tag{1}$$

If one uses a typical proportional controller for the outer voltage loop, then the the output of the outer voltage loop, or the reference signal i_{ref} of the inner current loop, will be as follows.

$$i_{ref}(t) = (1 + \frac{R_a}{R_k})V_{ref} - \frac{R_a}{R_k} K_{sv} v_o(t). \tag{2}$$

in which the symbol K_{sv} is the sampling ratio for the output voltage v_o, the value of which is determined by $R_{v2}/(R_{v1} + R_{v2})$. In addition, one can obtain the values of the proportional and integral coefficients K_{vp} and K_{vi} are R_a/R_k and $1/(R_k C_a)$, respectively.

Meanwhile, the sampling current i_{sense} is:

$$i_{sense}(t) = K_{si} i_L(t), \tag{3}$$

in which the symbol K_{si} is the sampling ratio for the inductor current iL, the value of which is determined by R_{sense}, R_f, R_{i1}, and R_{i2}.

According to the schematic and the working principle, the output of the outer voltage loop is employed as the reference signal i_{ref} of the inner current loop. The comparison result of two signals i_{sense} and i_{ref} is sent to an R-S trigger, the output of which is fed to two driving circuits to control the turn-on and off state of two power MOSFETs S_T and S_D.

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2.2. Fractional-order piecewise smooth model

Because of the turn-on and turn-off operations of power MOSFETs S_T and S_D, the converter is a typical piecewise smooth dynamic system. If one uses a proportional controller for the outer loop, and takes the inductor current i_L and the voltage v_C of the CPE as state variables, the converter will have a state vector of $\mathbf{x}(\mathbf{t}) = [i_L(t), v_C(t)]^{Tr}$, and the switching modes of the converter can be governed by:

- Switching mode 1: When the power MOSFETs S_T is on and S_D is off, the state of the converter can be governed by:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{V_{in}}{L} - \dfrac{R_{sense} + R_L + R_S}{L} i_L(t) \\ \dfrac{d^\alpha v_C(t)}{dt^\alpha} = -\dfrac{1}{(R_o + R_\Omega)C} v_C(t). \end{cases} \tag{4}$$

- Switching mode 2: When the power MOSFETs S_T is off, S_D is on, and the inductor current is not 0, the state of the converter can be governed by:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{V_{in}}{L} - \dfrac{R_L + R_D}{L} i_L(t) - \dfrac{R_o R_\Omega}{(R_o + R_\Omega)L} i_L(t) - \dfrac{R_o}{(R_o + R_\Omega)L} v_C(t) \\ \dfrac{d^\alpha v_C(t)}{dt^\alpha} = \dfrac{R_o}{(R_o + R_\Omega)C} i_L(t) - \dfrac{1}{(R_o + R_\Omega)C} v_C(t). \end{cases} \tag{5}$$

- Switching mode 3: When the power MOSFETs S_T is off, S_D is on, and the inductor current is 0, the state of the converter can be governed by:

$$\begin{cases} \dfrac{di_L(t)}{dt} = 0 \\ \dfrac{d^\alpha v_C(t)}{dt^\alpha} = -\dfrac{1}{(R_o + R_\Omega)C} v_C(t). \end{cases} \tag{6}$$

According to the internal structure of Figure 1 and the schematic of Figure 2, when the output of the outer voltage loop is less than $1V$, the switching condition of switching modes 1 and 2 is:

$$\begin{aligned} s(t) &= i_{ref}(t) - i_{sense}(t) \\ &= \frac{1}{3}\left[(1 + \frac{R_a}{R_k})V_{ref} - \frac{R_a}{R_k} K_{sv} v_o(t) - 1.4\right] - K_{si} i_L(t), \end{aligned} \tag{7}$$

in which the term 1.4 corresponds to the forward voltage of two series diodes, which are in series with the output of the voltage controller. In addition, the coefficient $1/3$ comes from the voltage divider of two resistors $20k\Omega$ and $10k\Omega$, which are in series with the two diodes. These details can be found in Figure 1.

When the output of the outer voltage loop is not less than $1V$, the reference signal $i_{ref}(t)$ will be clamped at $1V$, and the switching condition of switching modes 1 and 2 will be:

$$s(t) = 1 - K_{si} i_L(t). \tag{8}$$

At the switching-mode transition time t_s, the condition of $i_{ref}(t_s) = i_{sense}(t_s)$ is satisfied, thus one can obtain the duty cycle $d(t)$. In steady state, if the converter works in the current continuous mode (CCM), that is, the current does not drop to 0 at the end of switching mode 2, the converter switches between switching modes 1 and 2 periodically.

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3. Time-Domain Analysis

To reveal the time-domain performances and nonlinear dynamic characteristics of the PCMC DC-DC boost converter, the state equations 4 to equations 6 should be calculated, which are all fractional-order ordinary differential equations (FO-ODEs). Basically, these FO-ODEs can be generalized by the following following initial value problem (IVP)

$$D_*^q \mathbf{x} = f(\mathbf{x}),$$
$$\mathbf{x}(\mathbf{0}) = \mathbf{x_0}, \tag{9}$$

in which the term $q = [\frac{1}{q}, \alpha]^{Tr}$ is the non-commensurate order vector, the function $f : \mathbb{R}^n \rightarrow \mathbb{R}^n$, and the operator D^* is the differential operator of order q.

3.1. Preliminaries: Principles of Some Related Techniques

To solve the above IVP, this section introduces the principle of fractional Adams-Bashforth-Moulton typed method (F-ABM), and applies the stroboscopic map technique to cope with piecewise smooth situations.

3.1.1. F-ABM calculation method

In case of $-1 \leq \alpha \leq 1$, according to the definition of F-ABM method [23], the IVP of the fractional-order system of Equation 9 can be determined by:

$$x(n+1) = x(0) + \frac{h^\alpha}{\Gamma(2+\alpha)} f\left[t_{n+1}, x^P(n+1)\right] + \frac{h^\alpha}{\Gamma(2+\alpha)} \sum_{j=0}^{n} A_{j,n+1} f\left[t_j, x(j)\right], \tag{10}$$

where the term n is any integer and $A_{j,n+1}$ is

$$A_{j,n+1} = \begin{cases} = n^{\alpha+1} - (n-\alpha)(n+1)^\alpha, j = 0 \\ = (n-j+2)^{\alpha+1} + (n-j)^{\alpha+1} \\ -2(n-j+1)^{\alpha+1}, 1 \leq j \leq n \\ = 1, j = n+1 \end{cases} \tag{11}$$

The predictor $x^P(n+1)$ in Equation 9 is

$$x^P(n+1) = x_0 + \frac{1}{\Gamma(\alpha)} \sum_{j=0}^{n} B_{j,n+1} f\left[t_j, x(j)\right], \tag{12}$$

in which the term $B_{j,n+1}$ is

$$B_{j,n+1} = \frac{h^\alpha}{\alpha}\left[(n+1-j)^\alpha - (n-j)^\alpha\right]. \tag{13}$$

Note that, the term h in equation 10 and equation 13 is a predetermined step size, the value of which is defined according to the switching period T_s of the converter. In this work, we will set the step size to $1/100$ of the switching period T_s, which satisfies the Nyquist sampling theorem.

3.1.2. Stroboscopic map technique

As introduced in section 1.2, the state of the converter cycles between switching mode 1 and switching mode 2 in each switching period in CCM. Along with the on- and off operations of power MOSFETs S_T and S_D, there are a set of discontinuous points.

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Accordingly, a technique called stroboscopic map should be employed in calculations. This technique has been widely adopted in the dynamic analysis of piecewise-smooth systems and switching power converters. The principle of stroboscopic map technique is depicted in Figure 4.

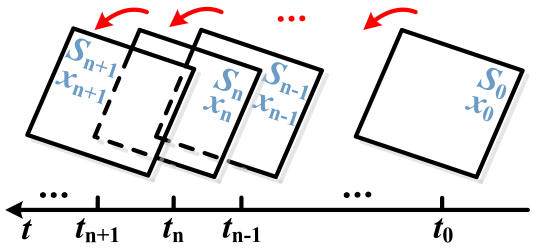

Figure 4. Principle of stroboscopic map technique.

By this technique, the dynamic behavior of the converter at each switching mode S_n will be collected in one switching cycle, that is, the solution $\mathbf{x_n}$ of the previous switching mode at time t_n will be employed as the initial value of the next switching mode, thus a cycle-by-cycle calculation can be carried out.

3.2. Bifurcation analysis

According to the discrete form of the obtained fractional-order piecewise smooth model, one can carry out the cycle-by-cycle numerical simulation for the converter in Figure 1. In simulation, the parameters are as Table 1.

Table 1. Parameters of the PCMC DC-DC Boost converter.

Parameter	Symbol	Value
Power supply	V_{in}	$5V \sim 20V$
Reference voltage	V_{ref}	2.5V
Switching frequency	f_s	$25k$Hz
On resistance of power MOSFETs	R_S	$\approx 10m\Omega$
Inductor	L	492μH
Equivalent series resistance of inductor	R_L	$\approx 4m\Omega$
Load resistance	$Z_L = R_o$	$10\Omega \sim 100\Omega$
Output filtering capacitor	C	10μF
Fractional order of capacitor	α	≈ 0.9615
Equivalent series resistance of capacitor	R_Ω	$\approx 0.9630\Omega$
Sampling resistor for inductor current	R_{sense}	$100m\Omega \sim 680m\Omega$
Input resistors of current conditioning circuit	R_{i1},R_{i2}	$10k\Omega$
Feedback resistors of current conditioning circuit	R_{fi}	$10k\Omega$
Output voltage divider resistors	R_{v1},R_{v2}	$0.5k\Omega \sim 33k\Omega$
Reference voltage	V_{ref}	2.5V
Compensation resistors of voltage loop controller	R_k,R_a	$1k\Omega \sim 100k\Omega$

Note that in the above table, the fractional order α and the ESR R_Ω of the output filtering capacitor are obtained by using a LCR meter and the parameter estimation method developed in [21]. According to Table 1, the sampling ratio K_{si} of inductor current equals to $R_{sense} = 0.1 \sim 0.68$, the sampling ratio K_{sv} of the output voltage equals to $R_{v2}/(R_{v1} + R_{v2}) = 0.015 \sim 0.5$, and the proportional coefficient K_{vp} of the outer voltage loop controller equals to $R_a/R_k = 1 \sim 100$.

Then by using the F-ABM method to calculate equation 4 to equation 6, and by sewing up the solutions of these equations end to end by the stroboscopic map technique, one can obtain the bifurcation diagrams of state variables versus different parameters, such as i_L versus power supply V_{in}, i_L versus load resistance R_o, and i_L versus output voltage divider resistance R_{v1}, as depicted in Figure 5.

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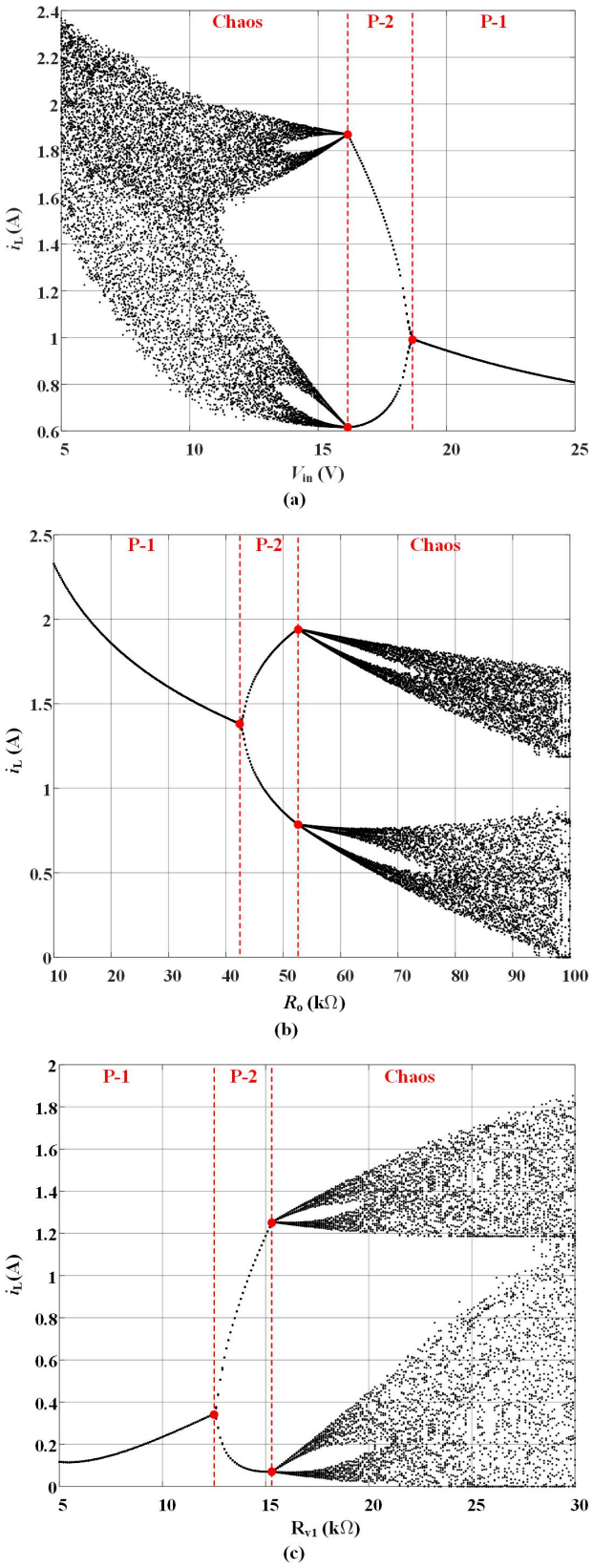

Figure 5. Bifurcation diagrams of inductor current i_L versus different parameters: (**a**) i_L versus power supply V_{in}, (**b**) i_L versus load resistance R_o, (**c**) i_L versus output voltage divider resistance R_{v1}.

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In Figure 5, one can find that, the PCMC dc-dc boost converter enters chaotic state through period-doubling bifurcation in three cases. Specifically, when one set the load resistance R_o to be 60Ω, the compensation resistors of voltage loop controller $R_k = 7k\Omega$, $R_a = 10k\Omega$, the voltage divider resistor $R_{v2} = 1k\Omega$, $R_{v1} = 25k\Omega$, and other parameters to be as those listed in Table 1, the converter keeps in chaotic state when the power supply is lower than $16V$. Increasing the power supply above this value will lead to the converter enters period-2 (P-2) sub-harmonic oscillation state. After around $V_{in} = 18.8V$, the converter will be in period-1 (P-1) stable state. As to the load variation situation, when one set the power supply V_{in} to be $15V$ and other parameters as in the previous case, the converter will be in P-1 stable state when the load resistance R_o is less than 42.6Ω. After around $R_o = 53\Omega$, the converter enters chaos. In addition in the output-voltage sampling ratio variation situation, when one set the power supply V_{in} to be $15V$, the load resistance R_o to be 100Ω, and other parameters as in the previous case, the converter will be in P-1 stable state when the resistance R_{v1} is less than $12.6k\Omega$, and the converter will fall into chaos when the resistance R_{v1} is greater than $15.3k\Omega$.

4. Validation and Comparison

4.1. Circuit-level simulation

In order to validate the results of theoretical analysis, circuit-level simulation is conducted in PSIM software in this section, the schematic of the simulation paltform is as follows:

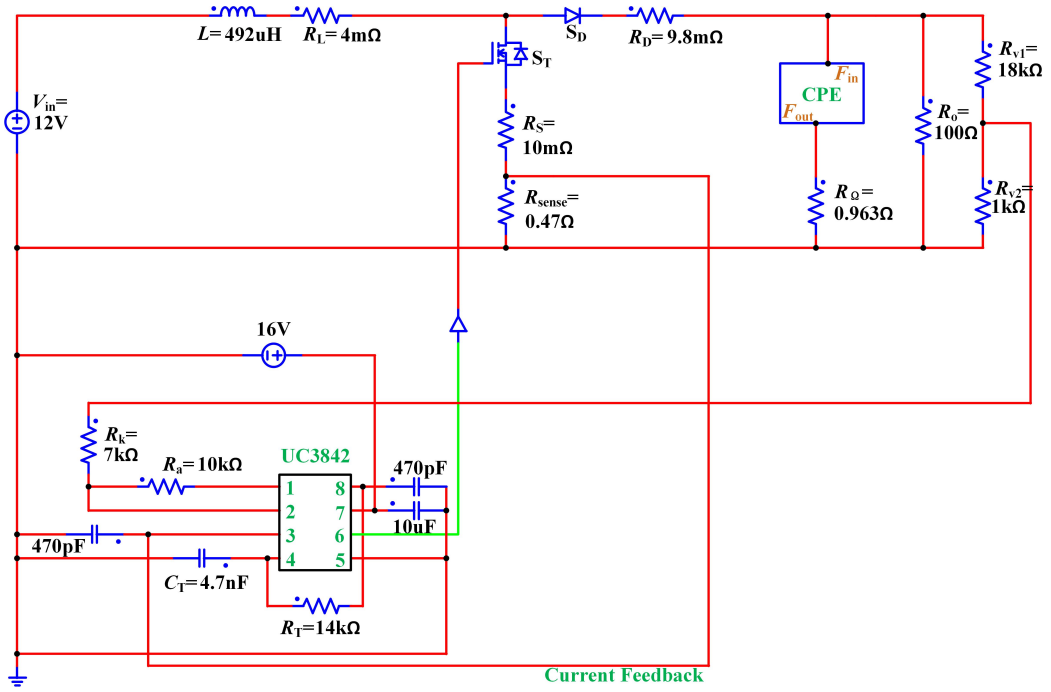

Figure 6. Circuit-level simulation in PSIM software.

In the above schematic, the PCMC module UC3842 is actually Figure 1, the CPE module, or an ideal order-0.9615 CPE, is constructed based on the rational approximation method, which has been used in a previous work [25]. The details of the rational approximation circuit is as Figure 7, in which the rational approximation circuit of $10/(second)^{1-0.9615}$ CPE contains eight groups of R-C parallel unit. These groups are in series one by one, their vaules are obtained by a frequency-domain approximation method proposed in literature [26–28] and the circuit network synthesis method adopted in previous work [25,29], in which we set the approximate phase error is within $1dB$. The detailed values of the CPE is listed in Table 2.

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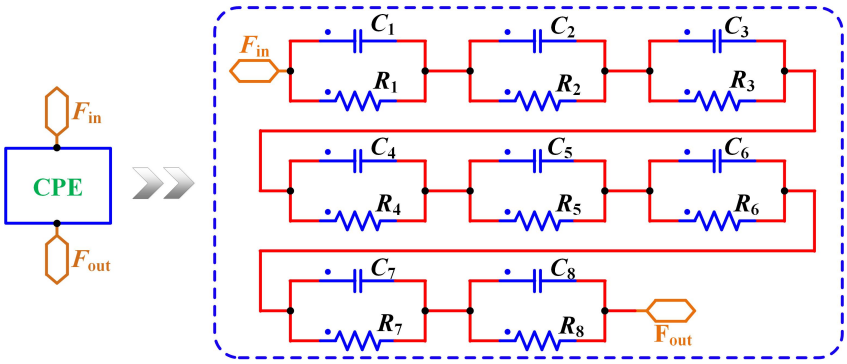

Figure 7. Rational approximation circuit of $10/(second)^{1-0.9615}$ CPE.

Table 2. R_i and C_i values of an order-0.9615 rational approximation circuit.

i	$R_i(\Omega)$	$C_i(\mu F)$
0	0	0
1	$0.7961m$	41.5040
2	$15.7435m$	47.0628
3	0.3131	53.0628
4	6.2286	59.8130
5	123.9148	67.4164
6	$2.4692k$	75.8646
7	$51.0412k$	82.2952
8	$8.5964M$	10.9568

By using the values of R_i and C_i listed in the above table, one can plot the Bode diagrams of the constructed CPE, as dipicted in Figure 8, in which the black solid lines represent the ideal order-0.9615 CPE and the blue dash curves belong to the devices obtained by rational approximation method and synthesis method.

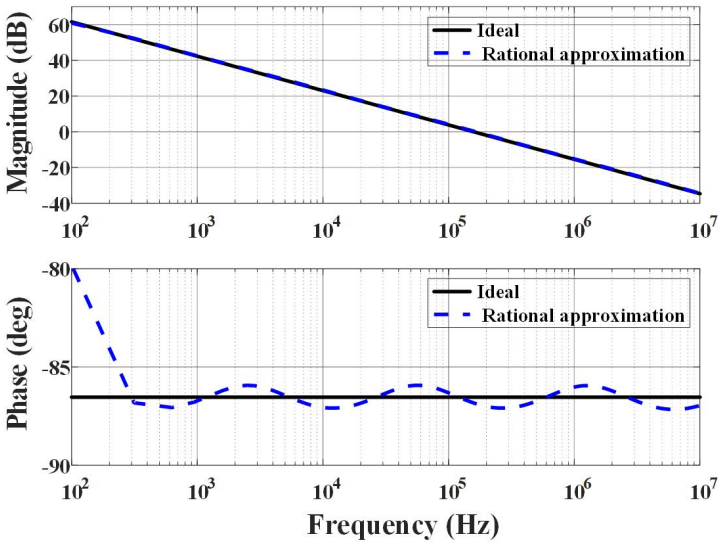

Figure 8. Bode diagrams of fractional-order devices with different orders: (a) C^{β} with $\beta = 0.9$.

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Additionally, one can obtain the theoretical impedance Z_i and the synthesis impedance Z_s of the $10\mu F/(second)^{1-0.9615}$ capacitor as follows.

$$\begin{cases} Z_i \approx 0.0610 - 1.0072i \\ Z_s \approx 0.0583 - 1.0496i, \end{cases} \tag{14}$$

respectively. And one can find that the errors of the real part and the imaginary part of the two impedance are 4.39% and 4.20%, respectively. These error can be reduced by using a lower approximate phase error, but it will lead to an increase in the numbers of R_iC_i units in the chain structure, as those discussed in literature [25] and [29]. It can be seen from Figure 8 and Equation 14 that, both the frequency characteristic curves and two impedance values meet well with each other. It means that the constructed CPE can be used in simulation for validation.

Then one can use the constructed order-0.9615 CPE in PSIM software to obtain the time-domain results of the PCMC dc-dc boost converter. In the first place, we set the voltage dividing resistor $R_{v1} = 10k\Omega$, the time-domain results of circuit-level simulation in PSIM software is as the following Figure 9.

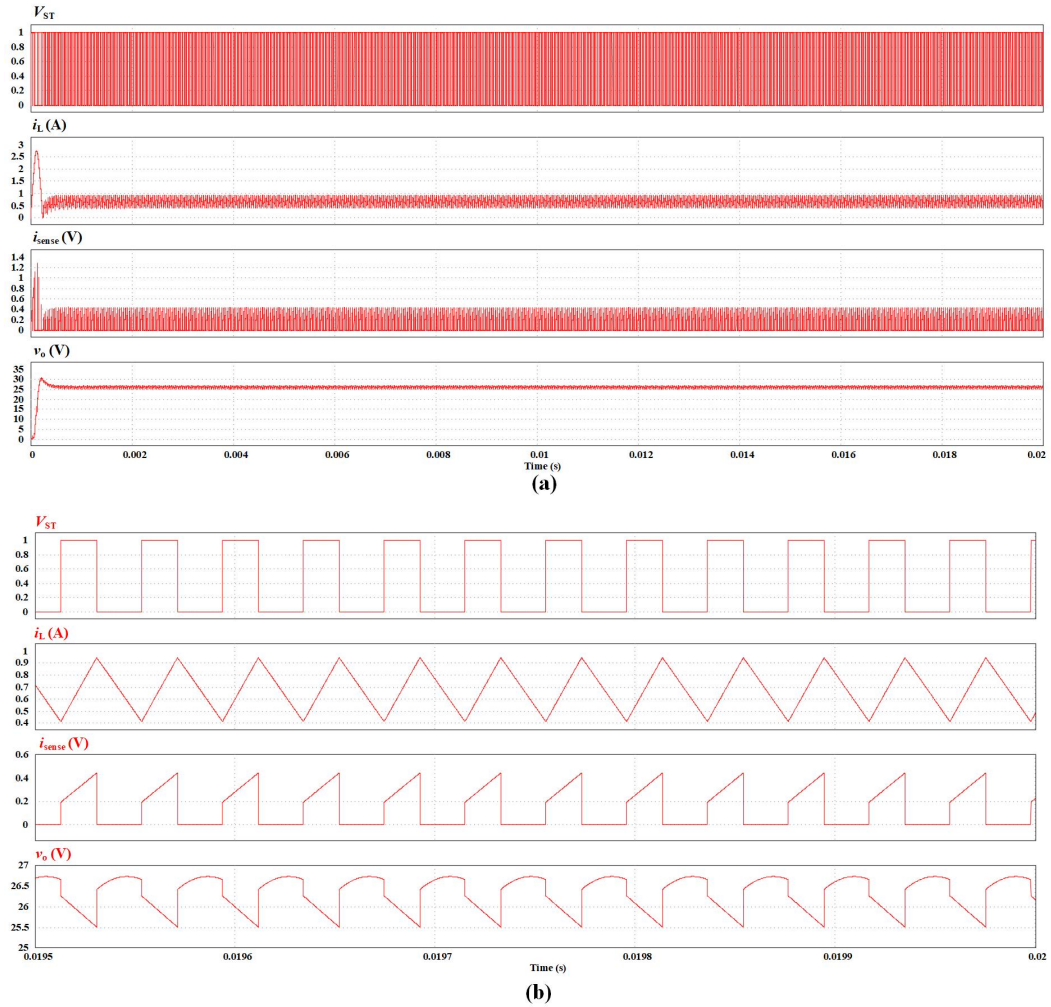

Figure 9. Time-domain simulation results by setting $R_{v1} = 10k\Omega$: (**a**) the whole operation process from initial state to 0.02s, (**b**) enlarged plot from 0.0195s to 0.02s.

In the figure above, from top to bottom, sub-figures correspond to the G-S voltage of power switch S_T, the inductor current i_L, the sampling value of the inductor current i_{sense} (which is actually the voltage of R_{sense}), and the output voltage v_o. One can find that, the

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PCMC dc-dc boost is in P-1 stable state under the configuration of parameters. The result is consistent with the results of bifurcation diagrams.

Then, we set the voltage dividing resistor $R_{v1} = 12k\Omega$, the time-domain results of circuit-level simulation in PSIM software is as Figure 10.

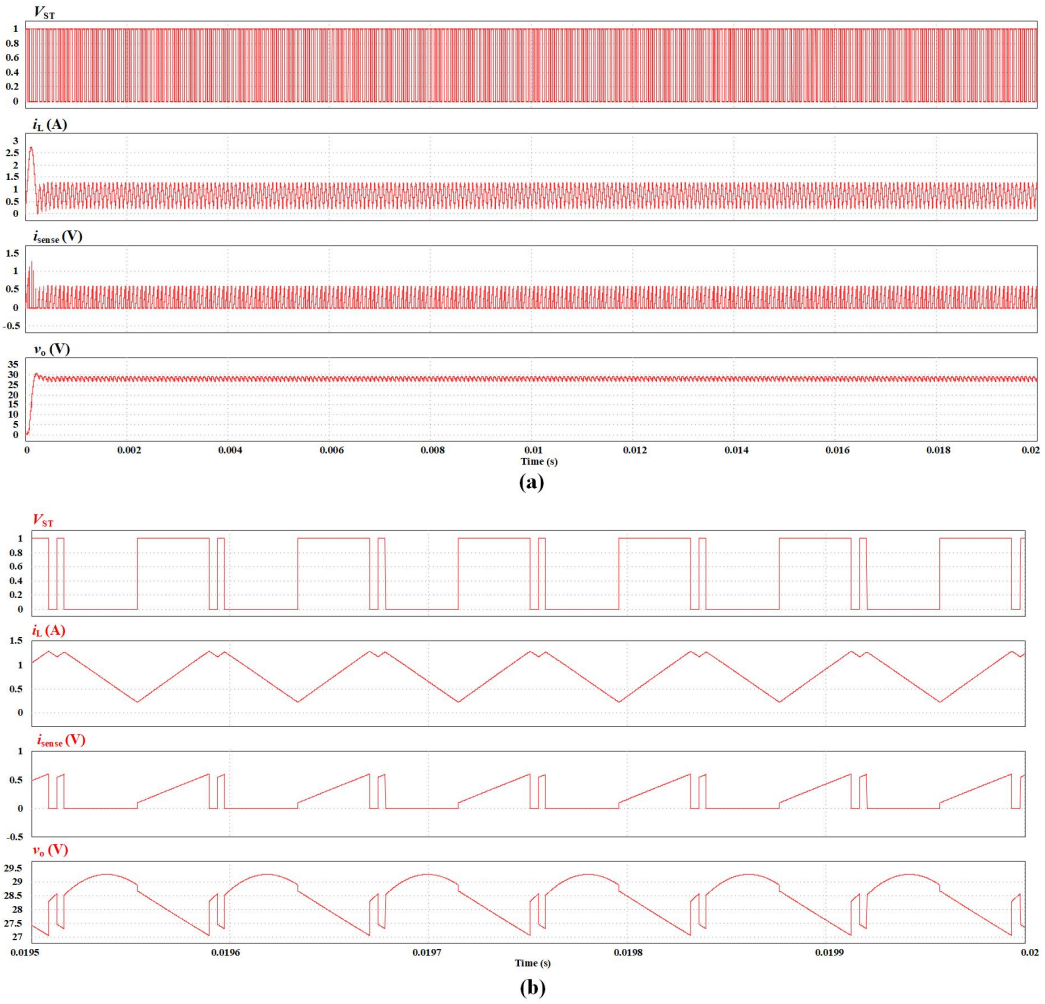

Figure 10. Time-domain simulation results by setting $R_{v1} = 12k\Omega$: (**a**) the whole operation process from initial state to 0.02s, (**b**) enlarged plot from 0.0195s to 0.02s.

In Figure 10, from top to bottom, sub-figures correspond to the G-S voltage of power switch S_T, the inductor current i_L, the sampling value of the inductor current i_{sense} (which is actually the voltage of R_{sense}), and the output voltage v_o. One can find that, the PCMC dc-dc boost is in P-2 sub-harmonic oscillation state under the configuration of parameters. The result is also consistent with the results of bifurcation diagrams.

At last, we set the voltage dividing resistor $R_{v1} = 25k\Omega$, the time-domain results of circuit-level simulation in PSIM software is as Figure 11, in which sub-figures correspond to the G-S voltage of power switch S_T, the inductor current i_L, the sampling value of the inductor current i_{sense} (which is actually the voltage of R_{sense}), and the output voltage v_o from top to bottom. One can find that, the PCMC dc-dc boost is in chaotic state under the configuration of parameters. The result is also consistent with the results of bifurcation diagrams.

4.2. Experiments

In order to further validate the results of both theoretical analysis and circuit-level simulation, a simple prototype is established in this work, in which a $10\mu F$ aluminum

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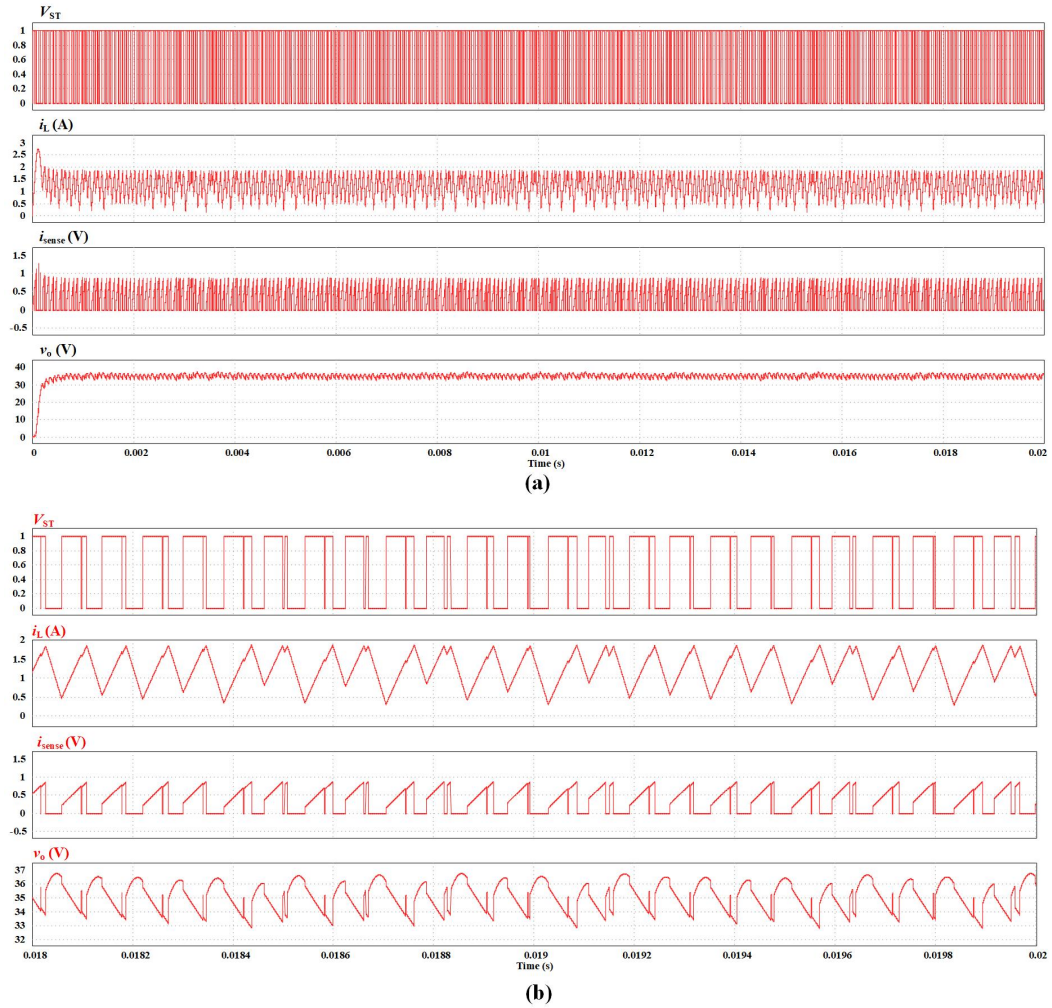

Figure 11. Time-domain simulation results by setting $R_{v1} = 25k\Omega$: (**a**) the whole operation process from initial state to 0.02s, (**b**) enlarged plot from 0.018s to 0.02s.

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electrolytic capacitor is adopted as the output filtering capacitor, a type-IRF640B power MOSFET and a type-1N5008 rectifier diode are exploited as S_T and S_D of the converter, and a UC3842 IC is employed to control the dc-dc boost converter. The experiment scene is as follows:

(a) (b)

Figure 12. A glimpse of experiment scenes: (**a**) capacitance measurement scene, (**b**) experimental prototype.

By rotating the bar of the type-3296 potentiometer on the circuit board to adjust the voltage dividing ratio, one can observe that the PCMC dc-dc boost converter experiences different nonlinear dynamic states.

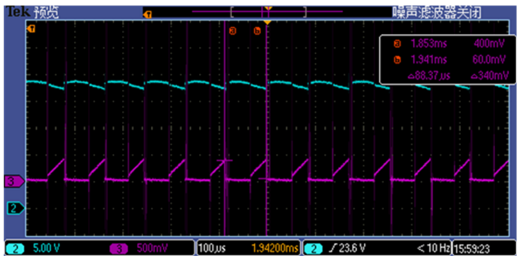
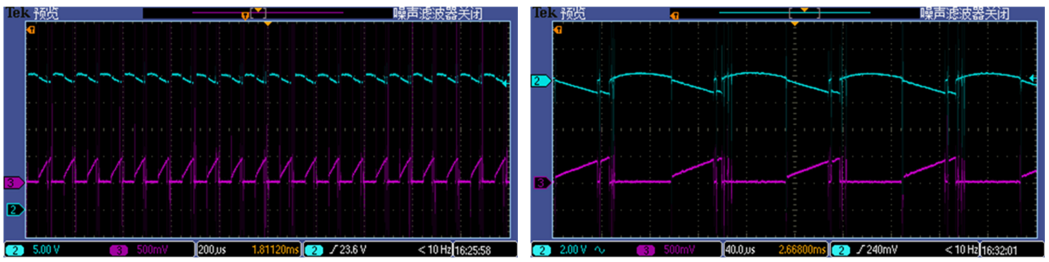


Figure 13. Experiment waveforms of P-1 stable state when the resistance of type-3296 potentiometer is around $1k\Omega$.



(a) (b)

Figure 14. Experiment waveforms of P-2 sub-harmonic oscillation state when the resistance of type-3296 potentiometer is around $1k\Omega$: (**a**) time-domain waveforms, (**b**) enlarged peak-to-peak waveforms.

It can be found that experimental waveforms are very similar to the results of circuit-level simulation, and the variation trend is consistent with the results of bifurcation diagrams, which confirm the correctness of theoretical analysis.

5. Conclusions

The concept of fractional-order components and circuit systems has received widespread attention recently. This study appears to be the very few empirical studies on the nonlinear dynamic of real-world fractional-order circuit systems, in which the nonlinear dynamic characteristics of a real-world fractional-order system are objectively measured and evaluated, that is, a PCMC dc-dc boost converter using an aluminum electrolytic capacitor

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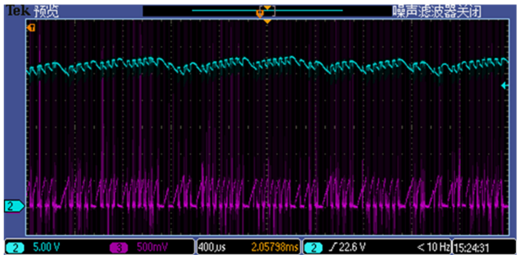

Figure 15. Experiment waveforms of chaotic state when the resistance of type-3296 potentiometer is around $1k\Omega$.

as the output filtering capacitor. Returning to the question posed at the beginning of this paper, it is now possible to state that, the fractional-order piecewise smooth model built in this work can be used for the large-signal stability analysis of the converter, by which one can draw bifurcation diagrams of the converter. The results of bifurcation diagrams emerged as reliable predictors of nonlinear dynamic analysis for the converter, when different parameters change, they can be used to predict the dynamics of the converter. Both circuit-level simulations and experiments have confirmed the correctness of the theoretical analysis. Notwithstanding the relatively limited example, this work offers a reference for the parameter selection and optimal design for power electronic converters which have fractional-order characteristics.

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