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Article

Optimization of Non-Alloyed Backside Ohmic Contacts to N-Face GaN for Fully Vertical GaN-on-Silicon Based Power Devices

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Abstract: In the framework of fully vertical GaN-on-Silicon device technology development, we report on the optimization of non-alloyed ohmic contacts on the N-polar n⁺ doped GaN face backside layer. This evaluation is made possible by using patterned TLMs (Transmission Line Model) through direct laser writing lithography after locally removing the substrate and buffer layers in order to access the n⁺ doped backside layer. As deposited non-alloyed metal stack on top of N-polar orientation GaN layer after buffer layers removal results in poor ohmic contact quality. To significantly reduce the related contact resistances, an HCl treatment is applied prior to metallization under various time and temperature conditions. A 3-minutes HCl treatment at 70°C is found to be the optimum condition to achieve thermally stable high ohmic contact quality. To further understand the impact of the wet treatment, SEM (Scanning Electron Microscopy) and XPS (X-ray Photoelectron Spectroscopy) analysis were performed. XPS revealed a decrease in Ga-O concentration after applying the treatment, reflecting the higher oxidation susceptibility of the N-polar face compared to the Ga-polar face, which was used as a reference. SEM images of the treated samples show the formation of pyramids on the N-face after HCl treatment, suggesting specific wet etching planes of the GaN crystal from the N-face. The size of the pyramids is time-dependent; thus, increasing the treatment duration results in larger pyramids, explaining the degradation of ohmic contact quality after prolonged high temperature HCl treatment.

Keywords: GaN-on-Si; N-face N-GaN ohmic contact; backside contact; fully vertical; power devices

1. Introduction

Gallium nitride (GaN) based material has shown an outstanding potential as a candidate for future power devices overcoming silicon (Si) and silicon carbide (SiC) limitations such as physical properties or cost of fabrication. Indeed, high GaN epi-layer quality can be grown on silicon substrate, enabling to benefit from a high electron mobility, a high electric field and a large band gap at silicon cost. However, reliability issues still plague well established lateral GaN high electron mobility transistors (HEMTs) for high voltage (HV) applications (beyond 600 V voltage operation)[1,2]. Vertical GaN technology grown on low-cost foreign substrates is a promising solution for medium and high voltage applications[3–8].

GaN P-N junction based vertical structures offer robust performance including avalanche breakdown capability and high current spreading while maintaining small device dimensions[3,9,10]. Most of the reported vertical GaN on silicon devices have a pseudo vertical structure, where the backside layer is reached from the front side by dry etching. This structure is widely used since the process is relatively straightforward as no backside processing is required to fabricate the discrete devices. On the other hand, unlike fully vertical structures, pseudo-vertical

devices suffer from the so-called current crowding effect directly affecting the on-state behavior due to thermal dissipation issues[11]. It can be pointed out that this undesired effect scales with the device dimensions, which makes the fully vertical structure mandatory. The development of a fully vertical structure based on GaN grown on silicon substrate is achieved by means of a local substrate and buffer layer removal[12,13]. In this case, one of the key challenges is the development of the backside ohmic contact due the inherent N-face polarity of the n⁺ doped GaN layer[14]. This problem is also faced with the vertical GaN-on-GaN structure in the field of power electronics and optoelectronics [14–19]. Unlike Ga-face, the formation of low resistive ohmic contacts on the nitrogen face of n⁺ layer is more complex due to the inversed polarity from the backside, the atom position in Wurtzite crystal of GaN is prone to high oxidation (Figure 1a)[20]. In this work, we propose a simple approach to overcome this issue. A high temperature HCl based wet treatment of the GaN surface was developed which significantly enhanced the ohmic contact quality under specific treatment conditions. TLM lift-off inside GaN on Silicon membranes using laser direct lithography has been developed allowing proper characterization of the contact resistances on top of the N-face n⁺ doped GaN backside layer. The electrical results are supported by X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM) analysis to reveal the impact of the wet treatment.

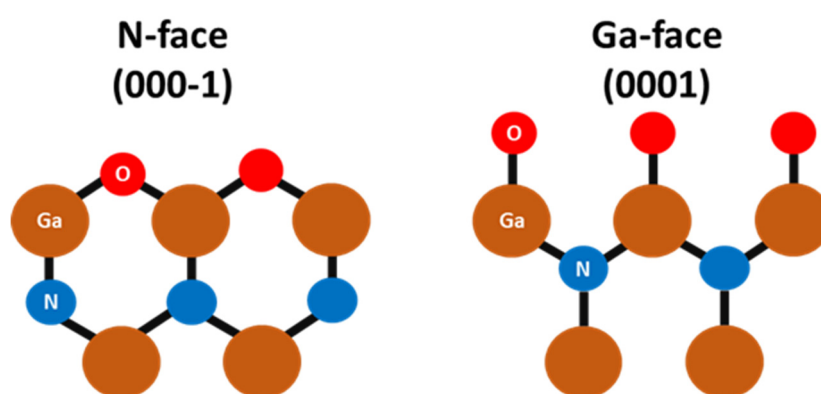


Figure 1. Side view diagram of the N-face (a) and Ga-face (b) GaN in the presence of oxygen atoms.

2. Materials and Methods

A GaN-based PIN diode heterostructure was grown on a 6-inch silicon substrate using metal-organic chemical vapor deposition (MOCVD). The GaN epitaxy started with the growth of a thick buffer layer, followed by an 800 nm n⁺ doped GaN layer with a Si-doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$. Subsequently, a 3.5 μm n- doped GaN drift layer was grown with a Si-doping concentration of $3 \times 10^{16} \text{ cm}^{-3}$ corresponding to a net doping of $9 \times 10^{15} \text{ cm}^{-3}$ considering the residual carbon concentration. The growth was completed with a p-type GaN layer on top, doped with $2 \times 10^{19} \text{ cm}^{-3}$ of Magnesium (Mg), resulting in a hole concentration of $3 \times 10^{17} \text{ cm}^{-3}$ as assessed by Hall effect measurements.

To avoid robustness issues of the membranes, the vertical GaN fabrication process started with the bonding of the front side on a silicon substrate by thermal compression of gold at 300°C (Figure 2a). The metal used for bonding was Ti (100 nm)/Au (200 nm), deposited by evaporation on both the silicon substrate and the PIN diode frontside. The backside process began with thinning the Si substrate from 1 mm down to 150 μm , followed by the deposition and patterning of a thick resist layer using standard lithography. This resist layer served as a mask during the local removal of Si using deep reactive-ion etching. The buffer layer was subsequently removed using a Cl₂ ICP (inductively coupled plasma)-based recipe. Due to the membrane's critical etching depth, etching control is not trivial. Therefore, etching time was calibrated by monitoring the electrical conductivity. Direct I(V) measurements on the surface (without metals) at 30V resulted in the following current level for each layer: nA range for the buffer layers, mA range for the n⁺ layer, and μA range for the n- layer (Figure 3).

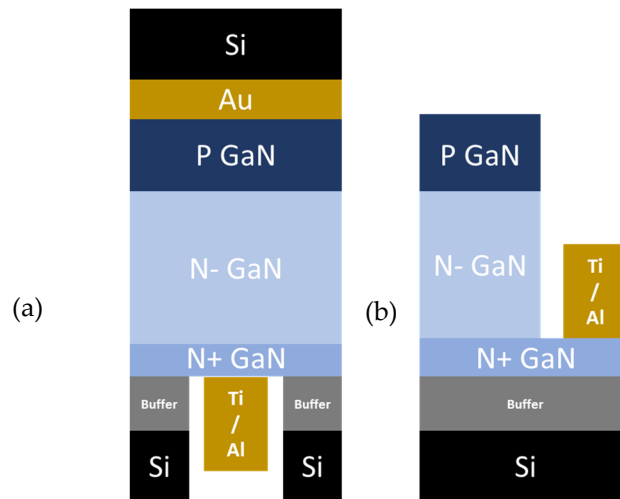


Figure 1. Schematic overview of the studied samples to characterized the ohmic contacts on N-face GaN layer, samples B-D (a) and Ga-face GaN layer, sample A.

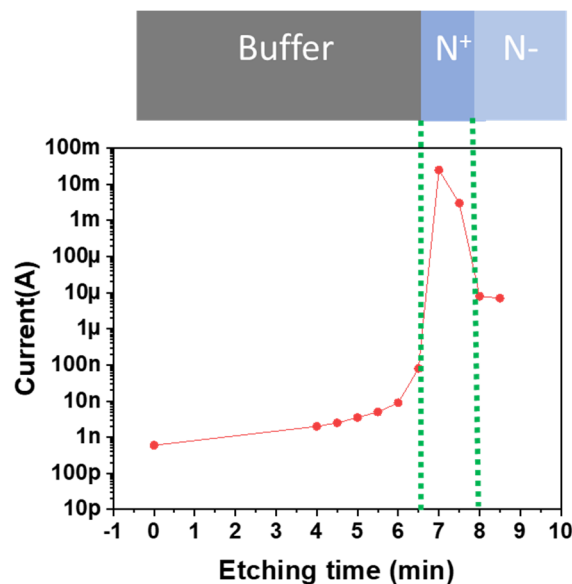


Figure 3. current versus etching time curves to control the etch depth.

Standard photolithography based on hard mask to pattern the TLM through the resist was not feasible due to the large gap between the GaN membrane surface and the optical exposure level. Therefore, direct laser writing was applied to achieve the TLM patterns. The vertical device processing concluded with the deposition of a Ti (25 nm)/Al (100 nm) contact layer using evaporation and subsequent lift-off on the backside (Figure 4). The aforementioned recipe was used to generate several samples from the same wafer avoiding any epi-variation. The various samples were used to define a design of experiment prior to the deposition of the contact layer as follows:

- Control samples B1 and B2 were metallized without any treatment, with a delay of 10 minutes and 24 hours after buffer etching, respectively.
- To investigate the time dependence, samples C1, C2, C3, and C4 were treated with HCl (37%) at 70°C for 1 min, 2 min, 3 min, and 5 min prior to metallization, respectively.
- To investigate the temperature dependence, samples D1, D2, and D3 were treated with HCl (37%) for 1 minute at room temperature, 55°C, and 70°C prior to metallization, respectively.
- An additional sample, referred to as sample A, was prepared with a pseudo-vertical structure. This configuration involved contacting the n+ layer from the front side on the Ga-face after ICP mesa etching (Figure 2b) to compare the Ti/Al ohmic contact quality with the N-face from the same GaN layer.

Transmission line measurements (TLMs) were performed to assess the electrical quality of the ohmic contacts in all cases. In addition to electrical characterization, the samples were also structurally characterized using XPS and SEM. XPS analysis have been performed right after the HCl treatment using a Sigma Probe instrument of Thermo Fisher Scientific Inc. with a base pressure of approximately 10^{-9} mbar. A monochromatic Al K α X-ray source is used as the excitation source. The spectra are calibrated by setting the N-Ga component in the N1s spectra to 397.7 eV [21–24]. Next, the O-Ga to Ga ratio in the Ga3d spectra is determined by fitting the spectra using CasaXPS (Casa Software Ltd.). The error on the atomic concentrations obtained via CasaXPS is typically estimated to be roughly 10% of the reported value. After XPS, SEM images are obtained from the samples using an FEI Quanta 200F instrument. Cross-sectional images are obtained after cleaving the samples.

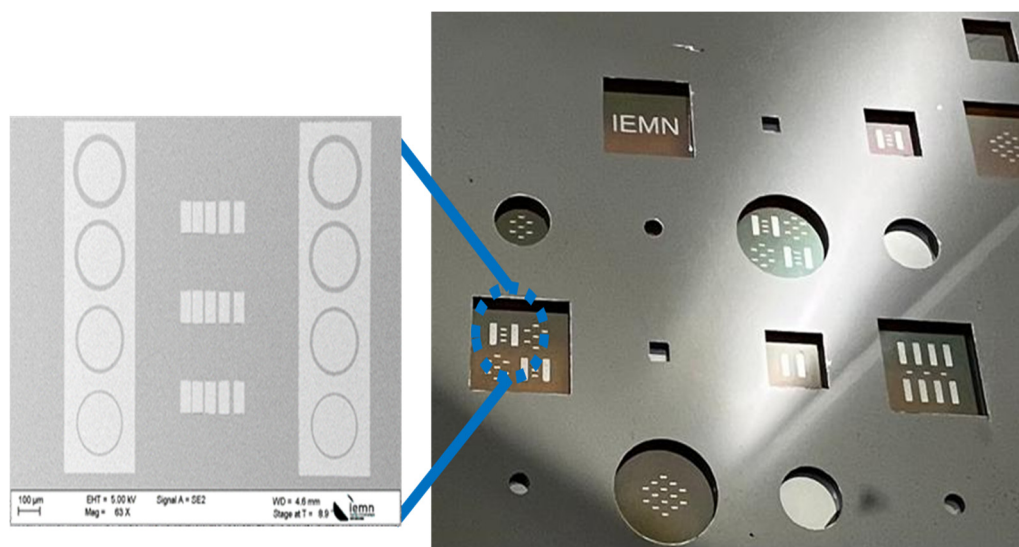


Figure 4. SEM and optical images of vertical GaN membranes with TLM patterns after metallization and lift-off.

3. Results

Figure 5a shows TLM measurements on the N-face for a 10-minute delay between the buffer etching and the deposition of metal (sample B1). The IV characteristics reveal a poor linear behaviour although a rather high current of 100 mA at 4.5 V is observed resulting in $2.4 \times 10^{-4} \Omega \cdot \text{cm}^2$ contact resistances. When increasing the delay to 24 hours (sample B2), the measured current drops to 40 mA at 5 V due to much higher contact resistances $> 10^{-3} \Omega \cdot \text{cm}^2$. These results suggest that an oxidation phenomenon occurs during the delay time. An HCl (37%)-based wet treatment was developed with a temperature initially fixed at 70°C in agreement with reported results in [25] demonstrating the need of high temperature to efficiently remove the native oxide.

Figure 5b shows the time dependence of the HCl wet treatment at 70°C on the ohmic contact resistance. Up to 3 min time duration (samples C1, C2, and C3), the HCl treatment reduces significantly the contact resistance down to $9 \times 10^{-6} \Omega \cdot \text{cm}^2$ without additional annealing (see Figure 6), making this approach fully compatible with any frontside post-process. On the other hand, when further increasing the treatment time up to 5 min and above (sample C4), the quality of the ohmic contacts severely deteriorates, and the extracted current drops dramatically, indicating a surface degradation due to prolonged treatment.

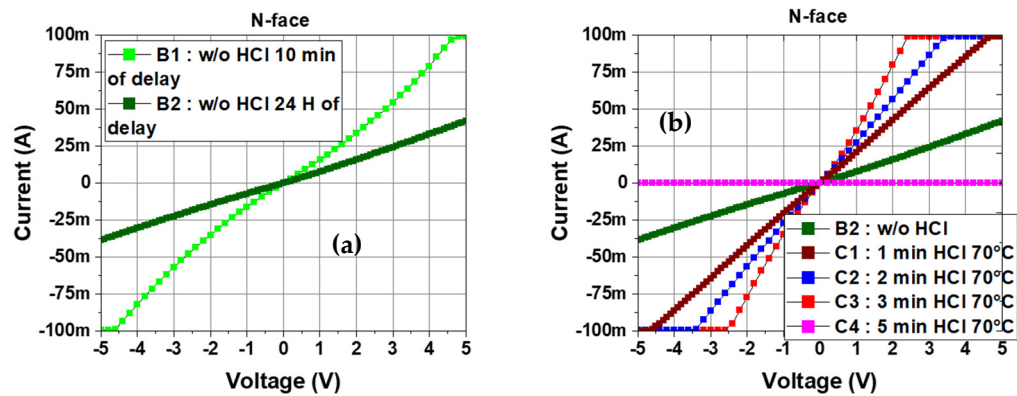


Figure 5. (a) TLM measurements of the N-face ohmic contact without treatment after various time duration between buffer etching and metal deposition. (b) N-face TLM measurements comparison of different HCl treatment time (0-5 min) at 70°C.

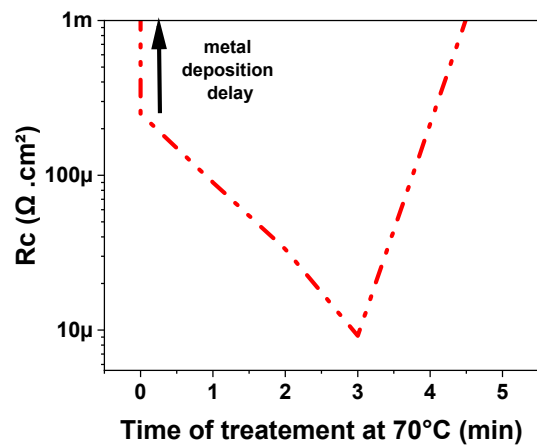


Figure 6. R_c versus time of treatment at 70°C.

An additional test was performed in order to get some initial insights about the thermal stability of the ohmic contacts. Sample C3 (using the optimum conditions of 3 min HCl treatment at 70 °C) has been introduced in an oven in rich N₂ environment at 300 °C for 1 h. Figure 7 shows the electrical current-voltage TLM measurements before and after 1 h thermal stress at 300 °C. The identical IV curves clearly indicate that the ohmic contacts are stable with no short-term impact of the temperature on the applied wet pretreatment.

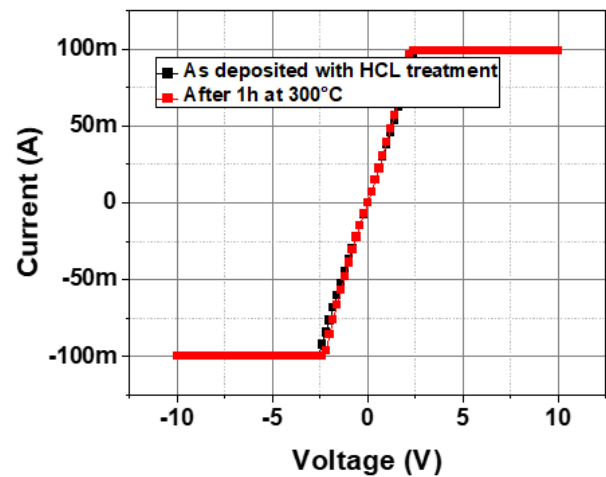


Figure 7. TLM measurements of the N-face ohmic contact with HCl pretreatment before and after thermal stress during 1 h at 300°C.

To observe the chemical modification of the GaN surface with the HCl treatment, various N-face and Ga-face samples have been treated with HCl at 70 °C for time duration ranging between 1-20min and immediately measured by XPS. The oxidation state of the surface can be determined by deconvoluting the Ga3d spectra into three peaks: Ga-N, Ga-O and Ga-Ga at a binding energy of 20.0-20.1eV, 20.5-21.0eV and 18.5-19.1eV, respectively.[21,22,24] As an example, the deconvolution of the Ga3d spectrum of the 5 min HCl treated N-face sample can be found in Figure 8a. Using these fits, the O-Ga to Ga ratio is then calculated and plotted as a function of HCl treatment time at 70 °C in Figure 8b. The data shows that the untreated N-face is oxidized to a greater extent than the untreated Ga-face. In addition, the HCl treatment is observed to reduce the N-face upon treatment time, while even after a treatment time of 20 min, the Ga-face remains roughly unaffected. These findings correspond well to the electrical results, showing no impact of the HCl treatment for the Ga-face, while an initial increase in contact quality is found upon removal of the Ga-O surface species for the N-face. The latter is also in agreement with literature, reporting that the removal of native oxide from the GaN surface is crucial to obtain low resistance ohmic contacts [18,26].

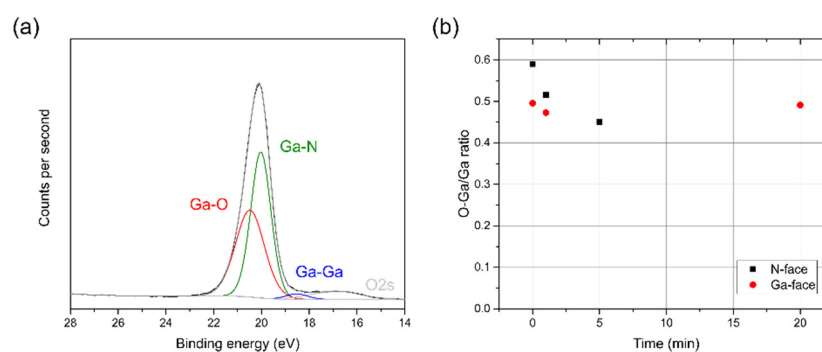


Figure 8. (a) Ga3d spectra of the 5min HCl-treated N-face sample demonstrating how the spectra is fitted. (b) O-Ga/Ga ratio in the Ga3d spectra as measured by XPS as a function of HCl treatment time at 70 °C for N-face (squares) and Ga-face (circles).

SEM images display that the HCl treatment not only reduces the N-face, but can also be associated with the formation of hexagonal pyramid-shaped features at the surface, as displayed in Figure 9. While the Ga-face again remains unaffected even after 20 min HCl treatment at 70 °C (Figure 9d), the features are observed to enlarge upon treatment time for the N-face (Figure 9a-c). After 5 min HCl treatment, the height and width of the features is estimated to be approximately 128 nm and 166 nm, respectively (Figure 9e). Similarly, [27] report the formation of sixfold nanopyramids on N-face GaN after etching for 45 min in 2 M KOH at 90 °C whereas the Ga-face is observed to remain smooth. Their observations demonstrate that the hexagonal pyramid shape is originating from preferential etching of crystal-line planes. Also in [28,29] report the formation of pyramid shapes which are observed to increase upon time after etching in heated KOH or H3PO4 solutions.

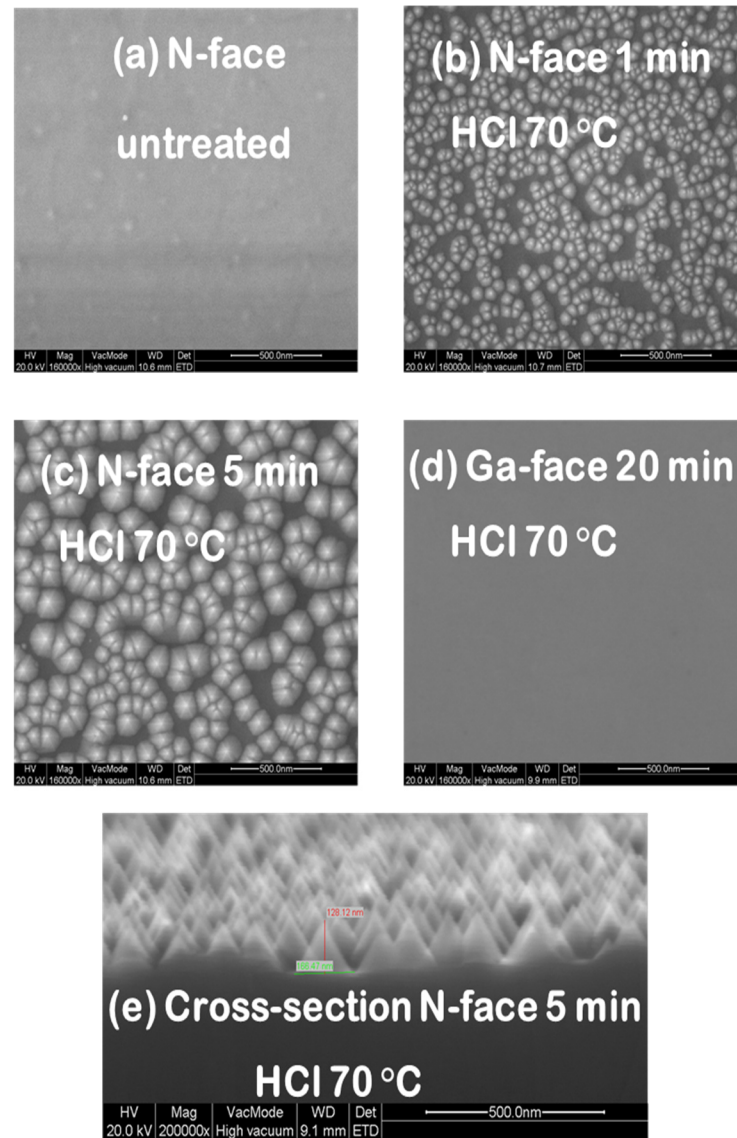


Figure 9. SEM images of the HCl treated GaN surfaces.

The formation of these features is accompanied by an increase in roughness of the surface. Hypothetically, this increase in roughness might explain why the 5 min HCl treated sample behaves poor in comparison to the 3 min HCl treated sample as observed by TLM. This would suggest that an optimal HCl treatment time exists on N-face GaN, showing the perfect trade-off between native oxide removal and surface roughness increase to obtain the lowest contact resistances.

Figure 10a compares TLM measurements of different samples treated with HCl for 1 minute at various temperatures to study the impact of treatment temperature on the ohmic contact quality. Sample B2 is the control sample without any treatment. It can be observed that room temperature (RT) treatment (sample D1) improves the TLM characteristics with a higher current. This is also the case for the 55°C treatment (sample D2) delivers still high contact resistances $>10^{-3} \Omega \cdot \text{cm}^2$. The most effective treatment temperature was found to be at 70°C (sample C1), resulting in a significantly improved current level with an associated contact resistance of $7-8 \cdot 10^{-5} \Omega \cdot \text{cm}^2$. It is important to note that additional samples were treated with longer treatment times at RT and 55°C, but the ohmic contact resistances never reached the ones achieved at 70°C.

For a fair benchmark, contact resistances on Ga-face n+ GaN layer were measured with (sample A1) and without HCl treatment at 70°C (sample A2) (Figure 10b). Despite the absence of pretreatment, Ga-face contact resistances are comparable to the N-face in sample B1 without delay between buffer etching and metallization. Furthermore, no impact of HCl wet treatment at 70°C was observed on Ga-face ohmic contacts that generally require extra annealing to further reduce the

contact resistances. These results confirm that the properties of N-face are significantly different from those of Ga-face GaN layer, suggesting that the native oxide of N-face GaN layer is the major factor influencing the ohmic contact quality but can be mitigated using a proper wet pretreatment without any annealing.

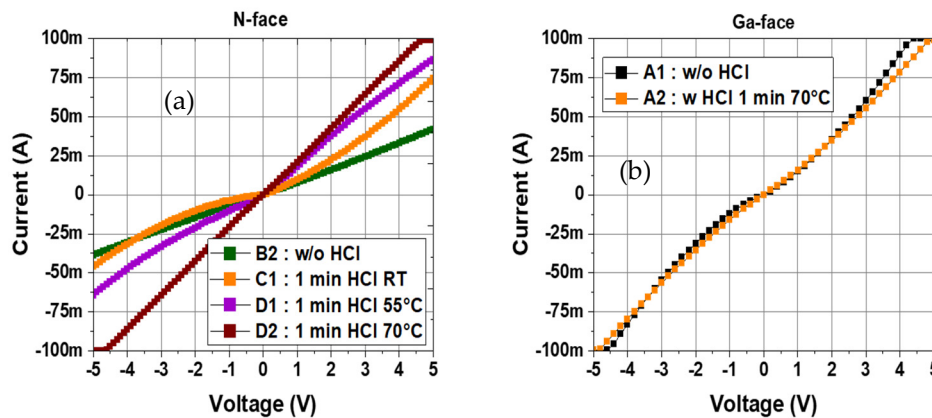


Figure 8. (a) N-face TLM measurements for samples treated with HCl treatment at different temperature (RT, 55°C, and 70°C) (b) Ga-face TLM measurements comparison with and without HCL treatment.

5. Conclusions

In this work, N-face backside ohmic contacts in fully vertical GaN-on-Silicon PIN diodes are assessed. Direct laser writing lithography enabled to pattern TLMs inside the membrane, as standard photolithography could not be used in this frame. TLM measurements from as deposited metal stack showed high contact resistances, which degrades over time between membrane opening and metal deposition. This suggests a gradual oxidation of the N-face GaN. Therefore, an HCl treatment was developed and found to be effective in reducing contact resistances and improving the maximum current. The optimum HCl treatment was found to be 3 minutes at 70°C while the contacts were severely degraded for longer time. It can be pointed out that short-term thermal stability up to 300°C shows no degradation of the optimized ohmic contacts. XPS analysis revealed a clear reduction in Ga-oxide with the HCl treatment. Moreover, SEM images showed the formation of pyramids, especially for prolonged HCl treatment explaining the ohmic contact drastic degradation for longer time. Finally, it has also been shown that the treatment temperature of 70°C is critical as much lower improvement occurs when reducing the temperature. This simple approach can be used for fabricating any types of fully vertical GaN-on-silicon devices as no extra annealing is required to achieve negligible backside contact resistances and thus fully compatible with frontside processing.

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