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Article

An 8–15-GHz Doherty Power Amplifier with a Compact Quadrature-Hybrid-based Output Combiner in 22nm FD-SOI

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Abstract

A compact 8–15 GHz Doherty power amplifier (DPA) is proposed and fabricated in 22-nm FD-SOI CMOS. The proposed DPA relies on quadrature-hybrid splitter and combiner to replace the bulky $\lambda/4$ impedance inverters at the input and the output of the conventional DPA enabling load modulation over a large fractional bandwidth (FBW=61%) with efficient and compact integration. The proposed DPA achieves a peak gain of 19.6 dB; ≥ 17 dB across 8–15 GHz, 18 dBm P_{1dB}, 19.5 dBm P_{sat}, and a peak PAE of 21% at 10 GHz, while sustaining 17% PAE at 6 dB back-off. The proposed DPA enables a modulation BW up to 200 MHz for a 256-QAM single carrier (SC) signal with a peak to average power ratio (PAPR) of 6 dB. Under this setting, the average output power (P_{avg}) is measured at 12.5 dBm with an RMS error vector magnitude (EVM) of -24.3 dB and an average PAE of 15%. Within the scope of CMOS power amplifiers in 22-nm FD-SOI, we found no published example that jointly demonstrates 8–15 GHz coverage and sustained PAE at 6 dB back-off using a quadrature hybrid.

Keywords: Doherty power amplifier (DPA); X-band; Ku-band; CMOS; 22-nm FD-SOI; quadrature hybrid coupler; impedance inverter; millimeter-wave integrated circuits

1. Introduction

Next-generation microwave transmitters—including satellite payloads, phased arrays, and high-capacity backhaul—demand power amplifiers (PAs) that are both compact and efficient across wide frequency spans to enable low-cost, large-scale integration. Achieving these targets in nanoscale CMOS is challenging due to reduced supply voltages, device breakdown limits, and RF substrate losses that depress output power and power-added efficiency (PAE) [1].

In silicon technologies, substrate-induced loss and parasitics in passives and interconnects are first-order constraints on achievable efficiency and bandwidth. Silicon-on-insulator (SOI) platforms alleviate loss compared with bulk CMOS; however, aggressive scaling of the buried oxide and metal stack can reintroduce attenuation and phase error in on-chip lines and networks. For example, in 22-nm FD-SOI, on-chip transmission lines may incur on the order of 0.5 dB/mm loss around 10–12 GHz, with commensurate phase dispersion that penalizes Doherty load modulation if not co-optimized [2].

The Doherty power amplifier (DPA) is a leading architecture for high efficiency at output back-off, but classical quarter-wave ($\lambda/4$) impedance inverters are area- and loss-prohibitive at X/Ku bands: even with slow-wave structures, $\lambda/4$ sections are millimeters long and introduce multi-dB loss, eroding PAE and narrowing bandwidth [3,4].

To mitigate these limits, prior works explored alternative load-modulation networks and multi-input DPAs, trading off complexity, area, or broadband performance [5,6].

This work leverages a compact quadrature hybrid as a unifying element for both the input splitter and the output combiner, thereby realizing the load modulation for Doherty operation while

simultaneously improving bandwidth and reducing footprint. The fabricated DPA in GlobalFoundries 22-nm FD-SOI shows a continuous operating band from 8 to 15 GHz (Ku-band coverage in addition to X-band), aligning closely with electromagnetic and circuit co-simulations. Across this 8–15 GHz span, the proposed DPA maintains relatively high gain and back-off efficiency while benefiting from the hybrid's inherent 90° phase balance and low insertion loss, enabling wideband load modulation without bulky $\lambda/4$ sections [7].

Main contributions. (i) A compact quadrature-hybrid-based Doherty topology that replaces lossy on-chip $\lambda/4$ inverters while preserving the Doherty load-line trajectory; (ii) wideband 8–15 GHz *measured* operation in 22-nm FD-SOI with maintained back-off efficiency; and (iii) a passive co-design methodology that accounts for on-chip attenuation and phase dispersion to sustain hybrid balance and DPA linearity over a large fractional bandwidth.

This paper has been organized as follows. Section 2 briefly discusses the quadrature hybrids operating as impedance inverters for the DPA, while Section 3 provides an insight on the proposed DPA relying on the hybrid splitter / combiner. Measurements of the fabricated DPA have been presented in Section 4, which also provides a comparison with the state-of-the-art. Finally, conclusions have been drawn in Section 5.

2. Quadrature Hybrids as Impedance Inverters: Robust DPA Operation Alongside Broader Bandwidth

A miniaturized quadrature hybrid coupler is proposed as an alternative for the lossy $\lambda/4$ transmission lines in the conventional DPA, shown in Figure 1, to perform impedance inversion and coherent power combining/splitting.

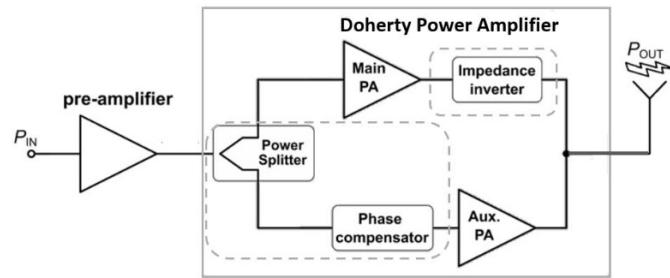


Figure 1. Block Diagram of the Conventional DPA.

The targets of this section are:

- (i) validation for the quadrature hybrid combiner as an impedance inverter ensuring stable and robust operation for the DPA.
- (ii) Proving the broader bandwidth operation due to using a quadrature hybrid as a splitter / combiner instead of $\lambda/4$ transmission lines. In the end of this section, the layout of the proposed hybrid combiner is introduced associated with a brief characterization for that output combiner.

2.1. Validation of DPA Load Modulation Using a Quadrature Hybrid Combiner

Assuming an ideal quadrature hybrid is used as an output combiner for a DPA. For this implementation, Port-1 to Port-4 are connected to the output of the main amplifier, the output of the auxiliary amplifier, the load, and $50\ \Omega$ termination, respectively.

With ports 3 and 4 terminated in Z_0 , the four-port reduces to the driving-point two-port seen at ports 1–2 [8]:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \mathbf{Z}_{\text{hyb}} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \quad \mathbf{Z}_{\text{hyb}} = \frac{Z_0}{3} \begin{bmatrix} 1 & 2\sqrt{2}j \\ 2\sqrt{2}j & 1 \end{bmatrix}. \quad (1)$$

Treat the PA outputs as Norton sources with main current I_M and auxiliary current in quadrature $I_A = j\rho I_M$ with $\rho \geq 0$:

$$I_A = j\rho I_M. \quad (2)$$

Using (1)–(2) yields purely real driving-point loads at the drains:

$$Z_M^{(0)}(\rho) = \frac{Z_0}{3}(1 - 2\sqrt{2}\rho), \quad Z_A^{(0)}(\rho) = \frac{Z_0}{3}\left(1 + \frac{2\sqrt{2}}{\rho}\right). \quad (3)$$

As depicted, by using a quadrature hybrid as an output combiner, the impedance seen at the drain of the main amplifier is inversely proportional to the auxiliary amplifier current. This is similar to the load modulation when the $\lambda/4$ transmission lines are used as impedance inverters in the conventional DPAs [9] as shown in Figure 2.

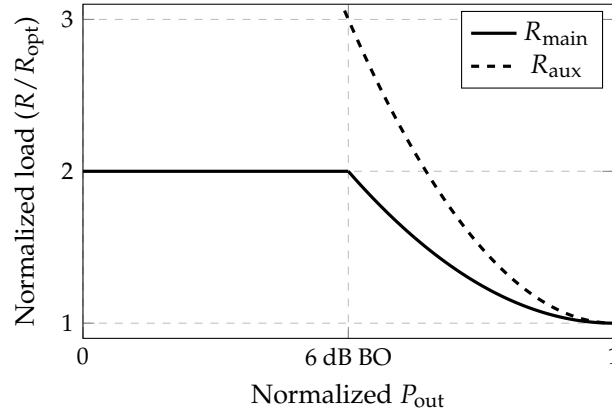


Figure 2. Conceptual active load modulation in a two-way Doherty PA.

However, Equation (3) shows that $Z_A^{(0)}(\rho) > 0$ for all $\rho > 0$, while $Z_M^{(0)}$ crosses zero at $\rho_0 = 1/(2\sqrt{2})$. An indication for unstable operation if an ideal quadrature hybrid is used as an output combiner. In fact, silicon non-idealities and finite output conductance of the main and the auxiliary amplifiers eliminate that instability condition.

Silicon non-idealities are captured by (i) a common insertion-loss factor $a \leq 1$ (voltage) in the hybrid/passives, a small dissipative offset $r \geq 0$ referred to the ports, and (ii) a net auxiliary-path deficit factor $\kappa \in [0, 1]$ (extra loss and/or gain imbalance). These map the physical ratio ρ to an effective ratio at the drains:

$$\rho_{\text{eff}} = \kappa \rho, \quad 0 \leq \rho \leq n, \quad 0 \leq \rho_{\text{eff}} \leq \kappa n, \quad (4)$$

where $n \triangleq I_{\text{max},A}/I_{\text{max},M}$ is the physical sizing (aux:main). With loss only (no quadrature error), the baseline loads remain real:

$$Z_M^{(0)}(\rho_{\text{eff}}) = \frac{Z_0}{3}(1 + r - 2\sqrt{2}a\rho_{\text{eff}}), \quad Z_A^{(0)}(\rho_{\text{eff}}) = \frac{Z_0}{3}\left(1 + r + \frac{2\sqrt{2}a}{\rho_{\text{eff}}}\right). \quad (5)$$

Let $G_M > 0$ and $G_A > 0$ be the devices' shunt output conductance at the main and auxiliary drains. The actual driving-point impedances are the parallel combinations

$$Z_M(\rho_{\text{eff}}) = \frac{Z_M^{(0)}(\rho_{\text{eff}})}{1 + G_M Z_M^{(0)}(\rho_{\text{eff}})}, \quad Z_A(\rho_{\text{eff}}) = \frac{Z_A^{(0)}(\rho_{\text{eff}})}{1 + G_A Z_A^{(0)}(\rho_{\text{eff}})}. \quad (6)$$

Since (5) are real, the exact real part reduces to

$$\Re\{Z_k\} = \frac{X_k + G_k X_k^2}{(1 + G_k X_k)^2}, \quad X_k \triangleq Z_k^{(0)} \in \mathbb{R}, \quad k \in \{M, A\}, \quad (7)$$

so $\Re\{Z_k\} > 0$ if $X_k + G_k X_k^2 > 0$.

In the 6 dB back-off peak PAE design, the reachable effective ratio is bounded as

$$0 \leq \rho_{\text{eff}} \leq \rho_{\text{max}} \approx \kappa n \approx 1. \quad (8)$$

The worst-case (most negative) baseline for the main occurs at $\rho_{\text{eff}} = \rho_{\text{max}}$:

$$X_{M,\min} \equiv Z_M^{(0)}(\rho_{\text{max}}) = \frac{Z_0}{3} (1 + r - 2\sqrt{2} a \rho_{\text{max}}). \quad (9)$$

From (7), a single design-time bound on G_M guarantees $\Re\{Z_M\} > 0$ for all $\rho_{\text{eff}} \in [0, \rho_{\text{max}}]$:

$$G_M > \frac{1}{|X_{M,\min}|} = \frac{3}{Z_0(2\sqrt{2} a \rho_{\text{max}} - (1 + r))}. \quad (10)$$

Because $a \lesssim 1$, $r \ll 1$, and $\rho_{\text{max}} \approx 1$, the threshold (10) is modest and the instability condition is eliminated; the auxiliary path is unconditionally positive since $Z_A^{(0)}(\rho_{\text{eff}}) > 0$ for all $\rho_{\text{eff}} > 0$.

2.2. Why a Quadrature Hybrid Yields Wider Doherty Bandwidth than a $\lambda/4$ Inverter

1) $\lambda/4$ inverter off the design frequency.

Consider a transmission line of characteristic impedance Z_0 and electrical length θ , terminated in a real Z_L [10]:

$$Z_{\text{in}}(\theta) = Z_0 \frac{Z_L + jZ_0 \tan \theta}{Z_0 + jZ_L \tan \theta}. \quad (11)$$

At the design frequency f_0 , the line is a quarter-wave ($\theta_0 = \pi/2$) and (11) reduces to the ideal *real* inversion $Z_{\text{in}} = Z_0^2/Z_L$. For a small fractional detuning, write $\theta = \frac{\pi}{2} + \Delta$ with

$$\Delta \triangleq \frac{\pi}{2} \left(\frac{f}{f_0} - 1 \right), \quad |\Delta| \ll 1. \quad (12)$$

Using $\tan(\frac{\pi}{2} + \Delta) = -\cot \Delta$ and the series $\cot \Delta = \frac{1}{\Delta} - \frac{\Delta}{3} + O(\Delta^3)$, the input impedance expands to first order as

$$Z_{\text{in}}(\theta) \approx \frac{Z_0^2}{Z_L} + j\Delta Z_0 \left(1 - \frac{Z_0^2}{Z_L^2} \right) + O(\Delta^2). \quad (13)$$

Implication. The $\lambda/4$ inverter accumulates a reactive error that is *linear in frequency detuning* ($\propto \Delta \propto f/f_0 - 1$). In a Doherty, this dispersive reactance corrupts the intended real load-modulation and 90° phasing as we move off f_0 , rapidly collapsing back-off efficiency over wide fractional bandwidth.

2) Quadrature hybrid (3 dB, 90°) across frequency.

The driving-point matrix seen at the PA drains (ports 1–2) is

$$\mathbf{Z}_{\text{hyb}}(f) = \frac{Z_0}{3} \begin{bmatrix} 1 & j2\sqrt{2}a(f)[1 + \varepsilon(f)]e^{j\Delta\phi(f)} \\ j2\sqrt{2}a(f)[1 + \varepsilon(f)]e^{j\Delta\phi(f)} & 1 \end{bmatrix}, \quad (14)$$

where $a(f) \leq 1$ is the common (voltage) insertion factor, $\varepsilon(f)$ a small coupling-magnitude ripple, and $\Delta\phi(f)$ the quadrature phase error. With Doherty phasing $I_A = j\rho I_M$ ($\rho \geq 0$), the active-seen main impedance is

$$Z_M(f, \rho) = \frac{Z_0}{3} [1 - 2\sqrt{2}a(f)[1 + \varepsilon(f)]\rho e^{j\Delta\phi(f)}]. \quad (15)$$

For small errors ($|\varepsilon| \ll 1$, $|\Delta\phi| \ll 1$),

$$\Re\{Z_M\} \approx \frac{Z_0}{3} [1 - 2\sqrt{2}a(f)\rho \cos \Delta\phi(f)], \quad (16)$$

$$\Im\{Z_M\} \approx -\frac{Z_0}{3} 2\sqrt{2}a(f)\rho \sin \Delta\phi(f). \quad (17)$$

Implication. The hybrid's frequency dependence enters only through the *small* variations $a(f)$ and $\Delta\phi(f)$. The reactive error is *first order in a small angle* $\sin \Delta\phi(f)$ (typically a few degrees), not first order in the detuning Δ as in (13). Thus the hybrid preserves the Doherty load-modulation trajectories and near-90° phase balance across substantially larger fractional bandwidth.

3) Quantitative comparison at 8–15 GHz.

Let $f_0 = \frac{8+15}{2} = 11.5$ GHz. At the band edges

$$|\Delta| = \frac{\pi}{2} \left| \frac{f}{f_0} - 1 \right| = \frac{\pi}{2} \cdot \frac{15 - 11.5}{11.5} \approx 0.477 \text{ rad } (\approx 27.3^\circ). \quad (18)$$

(a) **$\lambda/4$ inverter:** using (13) with, e.g., $Z_L = Z_0/2$ (a typical inversion ratio in Doherty), the reactive error magnitude at the edge is

$$|\Im\{Z_{in}\}| \approx |\Delta| Z_0 \left| 1 - \frac{Z_0^2}{Z_L^2} \right| = 0.477 \cdot 50 \cdot |1 - 4| \approx 71.6 \Omega. \quad (19)$$

(b) **Hybrid:** with $a(f) \approx 0.9$, $\Delta\phi(f) \approx 5^\circ = 0.087$ rad, and $\rho \approx 1$ near the mid-high-power region, (17) gives

$$|\Im\{Z_M\}| \approx \frac{Z_0}{3} \cdot 2\sqrt{2} a \rho \sin \Delta\phi \approx \frac{50}{3} \cdot 2.828 \cdot 0.9 \cdot 0.087 \approx 3.7 \Omega. \quad (20)$$

Result. For the same wide 8–15 GHz span, the $\lambda/4$ inverter accumulates a reactive error on the order of $\sim 70 \Omega$ (case-dependent via Z_L), whereas the hybrid's reactive error stays at only a few ohms— more than an order of magnitude smaller. This directly translates to a far less distorted load-line and a wider back-off efficiency plateau with the hybrid.

4) Takeaways for Doherty bandwidth.

(i) The $\lambda/4$ inverter embeds the $\tan \theta$ dispersion, yielding a reactive error $\propto \Delta \propto (f/f_0 - 1)$; Doherty load modulation and the 90° condition degrade rapidly away from f_0 . (ii) The quadrature hybrid's driving-point law (15) is almost frequency-invariant to first order; only small $a(f)$ and $\Delta\phi(f)$ ripples appear, so the Doherty trajectories and phase quadrature are preserved across large FBW. Consequently, quadrature-hybrid combining is intrinsically wider-band for Doherty operation than $\lambda/4$ -based inversion.

2.3. The Proposed Quadrature Hybrid Combiner: Layout and Characterization

The proposed hybrid, shown in Figure 3, is designed using a branch-line topology with stacked microstrip lines. For this implementation, Port-1 to Port-4 are connected to the output of the main amplifier, the output of the auxiliary amplifier, the load, and 50 Ω termination, respectively.

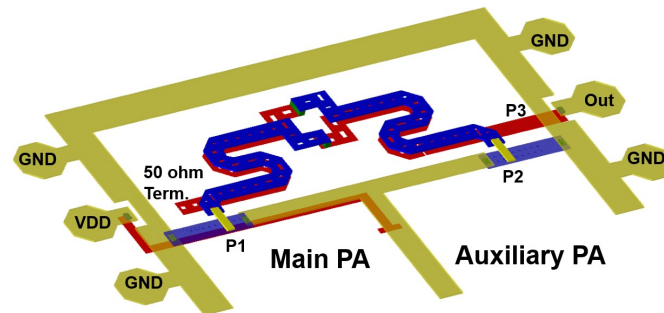


Figure 3. Layout of the Quadrature Hybrid Combiner.

Load modulation is realized by designing the hybrid combiner to transform the load impedance from R_L to $R_L/2$ from the start of operation of the auxiliary amplifier at 6 dB back-off to P_{sat} , an

impedance transformation ratio of 0.5, when the outputs of the main and auxiliary amplifiers maintain a 90° phase difference. Figure ??(a) shows the simulated impedance transformation ratio at the drain of the main amplifier versus the phase difference of the signals at the output of the main and auxiliary amplifiers at 10 GHz. As indicated, a transformation ratio of 0.5 is obtained at 90° phase difference. Simulation results in Figure ??(b) show that the hybrid achieves an insertion loss below 1.2 dB and a phase imbalance within $\pm 3^\circ$ across the frequency range from 8 to 15 GHz.

3. The Proposed DPA: Design Details

The Doherty power amplifier employing the proposed hybrid is depicted in Figure 4.

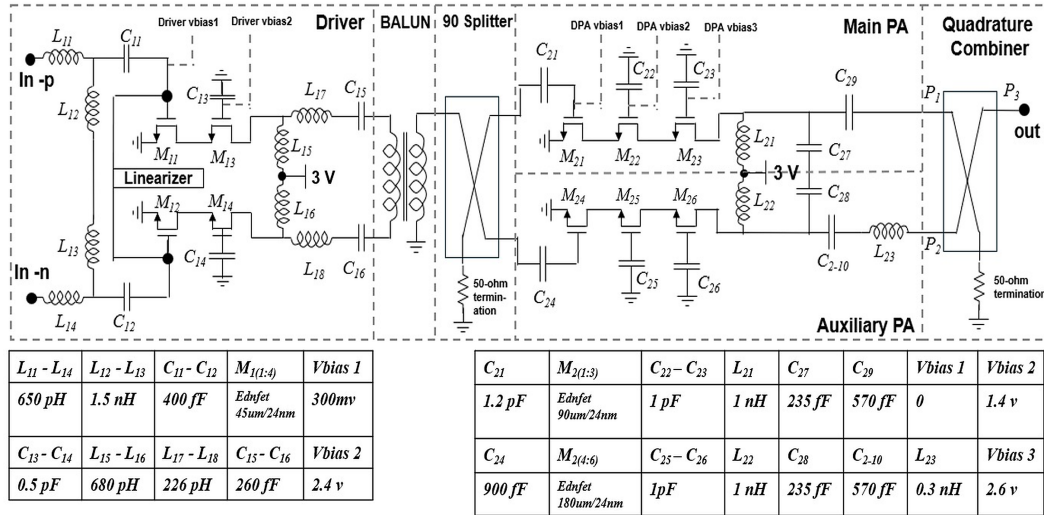


Figure 4. Schematic diagram of the proposed DPA.

3.1. The Driver Stage

The driver stage employs a two-stacked FET differential amplifier for effective AM–AM linearization, operating from a 3 V supply. The width (M_{11} – M_{14}) is half that of the main-stage FETs, ensuring a 3 dB drive margin and improved PAE. A linearization loop senses the RF input and adjusts the gate bias, compensating AM–AM distortion in both the driver and the DPA [11].

The driver output is converted to single-ended I/Q signals by a BALUN and quadrature hybrid, identical to the output stage, thereby ensuring the required 90° phase difference between the main and auxiliary inputs/outputs. The passive input network introduces ≈ 4 dB insertion loss. The driver output matching (C_{21} , C_{24}) is co-optimized with the BALUN and quadrature hybrid for conjugate matching at the DPA input.

3.2. The DPA Stage

The proposed Doherty PA employs a Class-AB biased main amplifier and a Class-C biased auxiliary amplifier, which is activated only at high output power levels.

We begin the design of the main amplifier core with choosing a current density of $100 \mu\text{A}/\mu\text{m}$, which is slightly below the peak Ft current density of $120 \mu\text{A}/\mu\text{m}$. This margin is maintained to safely operate within the electro-migration limits, especially after current ramping. By applying this current density across various sizes of the ednFET (the optimal FET for power amplifiers in the GF22nm CMOS node [12]), it was determined that a total current of 3 mA through a unit FET of $30 \mu\text{m}/24 \text{ nm}$ results in a self-heating of 20 degrees Celsius above ambient temperature. The main amplifier core transistors (M_{21} – M_{23}) consist of three units of these with a total gate width of $90 \mu\text{m}/24 \text{ nm}$ to set the maximum power that can be delivered to the load to 20 dBm. The drain-source breakdown voltage (V_{ds}) of the ednFET is 2.2 volts. Consequently, a configuration of three stacked FETs is chosen, with a 3 volts supply to allow a maximum voltage swing of 2 volts per device, corresponding to a theoretical maximum P_{sat} level of 18 dBm. This level goes up to ≈ 19.5 dBm after being combined with the

auxiliary amplifier in addition to the losses of the matching network and the combiner. Capacitor values (C_{22} - C_{26}) and bias points ($V_{bias\ 1}$ - $V_{bias\ 3}$) were chosen carefully to adjust the voltage swings equally over the three stacked FETs.

For a two-way Doherty, the back-off efficiency knee is set by

$$B_{OBO,peak} = 20 \log_{10}(1 + \kappa n). \quad (21)$$

In the ideal conventional DPA, the sizing of the main and the auxiliary PAs should be equal to get $B_{OBO,peak} = 6$ dB but realistic non-idealities enforce the FET size of the auxiliary amplifier to be larger than that of the main amplifier to achieve peak PAE at 6 dB back-off yielding the theoretical asymmetric DPA to achieve the theoretical PAE of the symmetric DPA. Figure 5 shows the simulated DPA PAE at 10 GHz versus the ratio between the FET size of the auxiliary amplifier and the FET size of the main amplifier (n). Also, Figure 5 compares the simulated PAE of the proposed DPA to the PAE of the class B PA. Choosing $n=2$ yields the DPA to have superior PAE compared to the DPA of $n=1$ and class B PA.

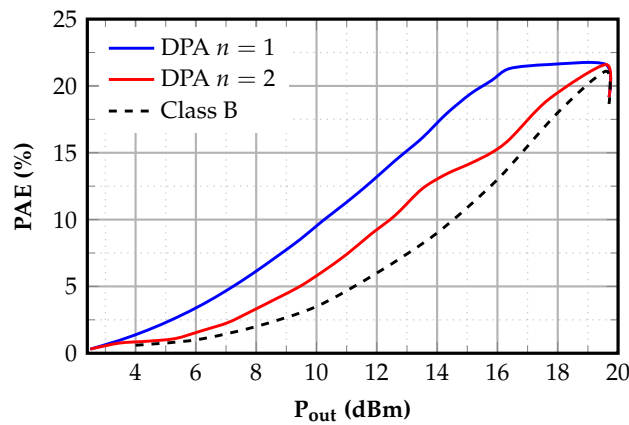


Figure 5. Simulated Power-added efficiency at 10GHz versus output power. for a DPA with $n = 2$, DPA with $n = 1$, and Class B PA.

The drain impedance of the two cores are primarily determined by the quadrature hybrid and the ratio between the main and the auxiliary amplifiers as shown in equation 3. In practice, unavoidable parasitics and layout effects shift these ideal values. Load-pull simulations with directly combined cores show the main PA optimum impedance is about $(50+j10) \Omega$ when the auxiliary is active and $(75+j25) \Omega$ when inactive. With the hybrid combiner, the main port instead sees $\approx 25 \Omega$ and $\approx 50 \Omega$. So, the main output network steps these impedances to the required R_{opt} , while the auxiliary matching presents $R_{opt}/2$ to its drain, ensuring effective load modulation.

4. Measurements

The micrograph of the PA implemented in GF 22-nm FD-SOI is shown in Figure 6. The two-stage PA occupies 0.5 mm^2 . RF and dc biasing signals are applied and monitored using on-wafer probing to reduce losses and mismatches introduced by measurements. Differential GSGSG pads are employed for the input, while single-ended GSG pads are utilized for the output. Figure 7 shows measured and simulated S-parameters where a peak gain of 19.6 dB is achieved with 3-dB small signal gain bandwidth from 8 to 15 GHz.

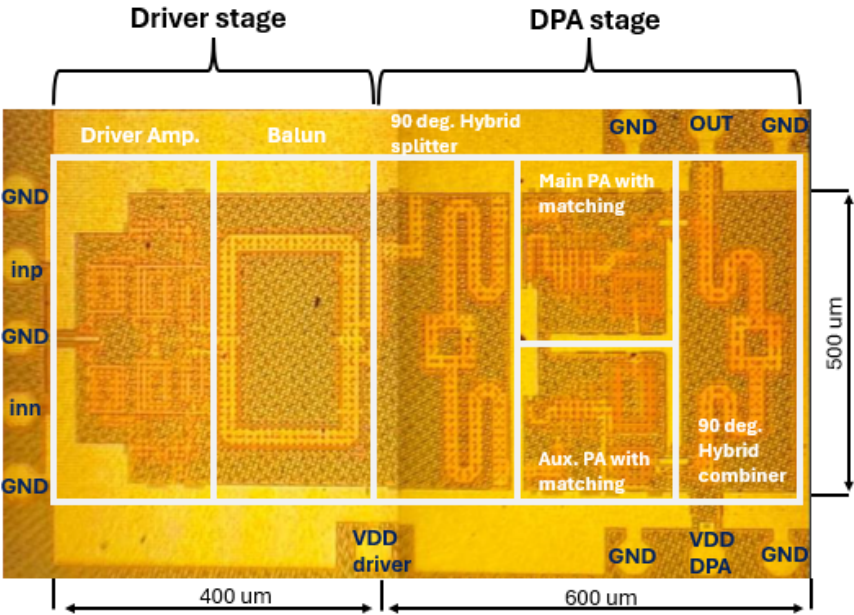


Figure 6. DPA micrograph

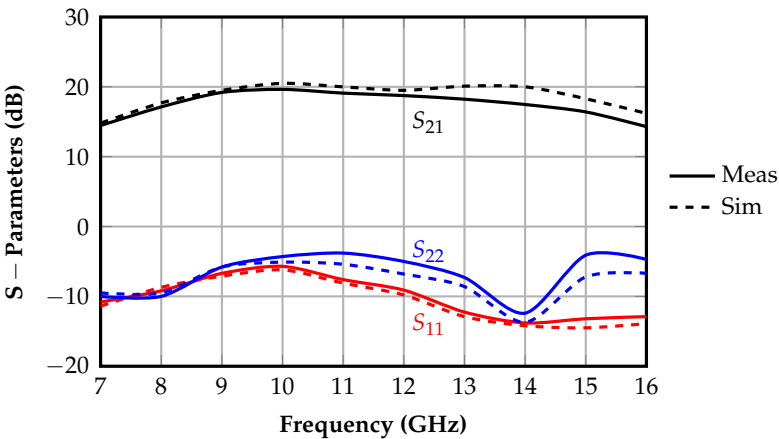


Figure 7. Measured versus simulated S_{21} , S_{11} , and S_{22} for the proposed DPA

Figure 8 shows that the saturated output power, P_{sat} , of the proposed PA is 19.5 dBm at 10GHz while the P1dB is 18 dBm. A peak PAE of 21% is achieved at 10 GHz, and it is 17% at 6 dB back-off.

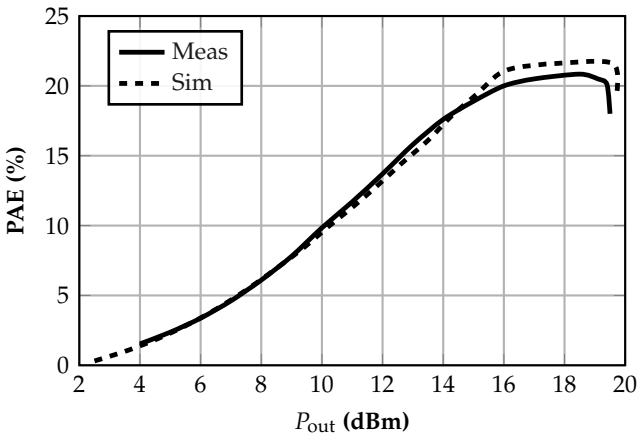


Figure 8. Measured versus simulated PAE versus P_{out} at 10GHz.

Figure 9 compares measured and simulated P_{sat} across the target frequency range from 8 to 15 GHz while Figure 10 shows a similar comparison for the PAE.

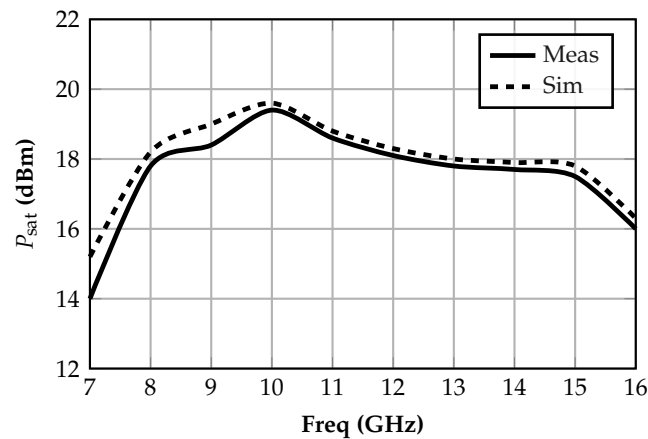


Figure 9. Measured versus simulated P_{sat} across frequency.

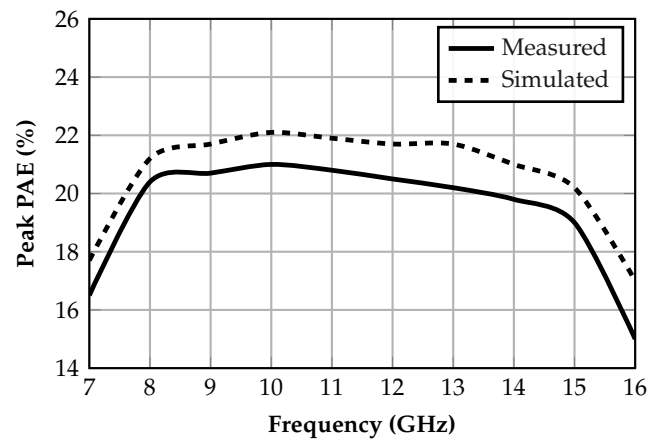


Figure 10. Peak PAE versus frequency.

Figure 11 compares measured and simulated AM-AM where the P1dB is set to be at $P_{out} = 18dBm$ while Figure 12 shows that The measured AM-PM of the PA exhibits less than 9 degrees at the P1dB of the PA.

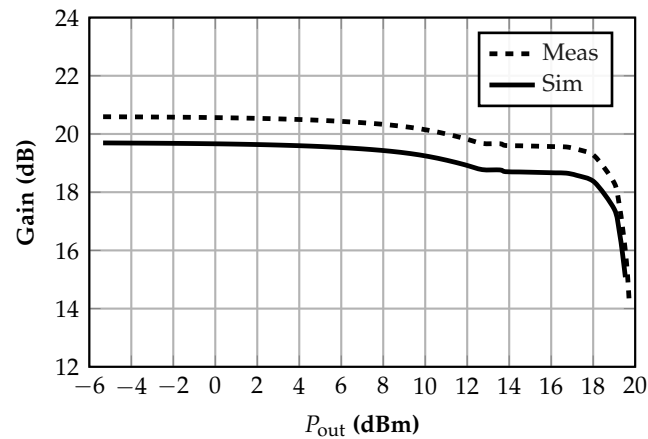


Figure 11. Measured vs. simulated AM-AM at 10 GHz.

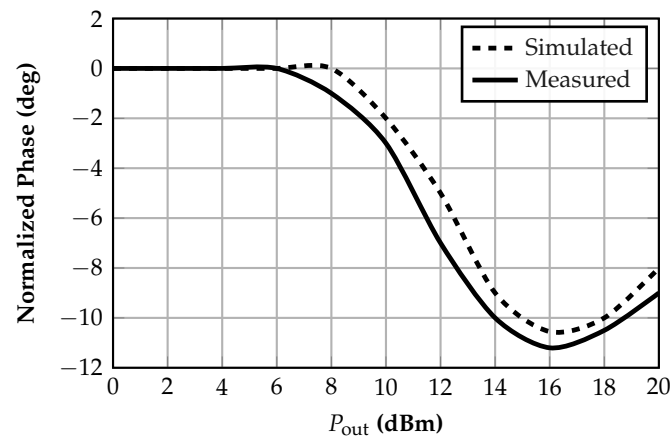


Figure 12. AM-PM: normalized phase (degrees) versus output power (dBm).

From 8 to 15 GHz, the DPA achieves at least a 17 dB gain with more than 17.9- dBm Psat, over 19% peak PAE proving robustness over a large FBW. The measurement results are well correlated to simulations with slight variance due to the measurement setup.

For modulated signal measurements shown in Figure 13, the PA exhibits an EVM of −24.3 dB for a 100-MHz single carrier (SC) 256- QAM signal at an average Pout of 12.5 dBm with 15% average PAE as shown in Figure 14. EVM is -24.1 dB for a 200-MHz signal.

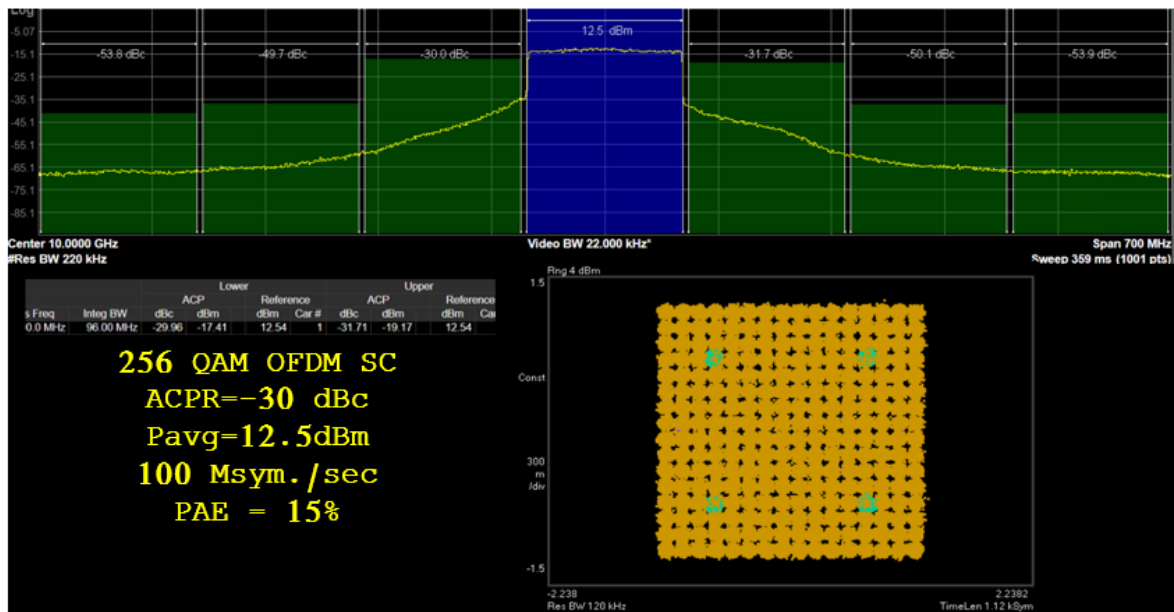


Figure 13. Measured ACPR for 256 QAM SC

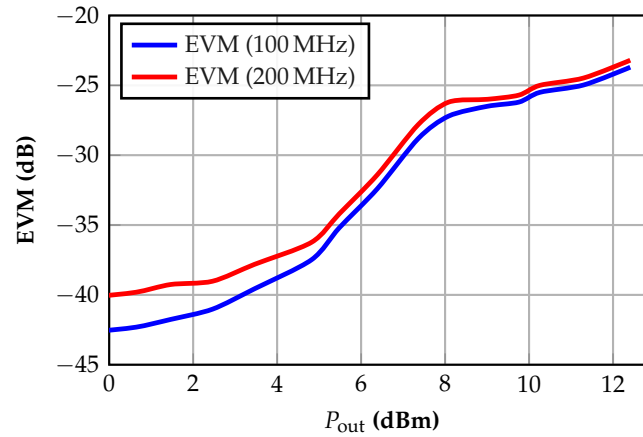


Figure 14. Measured EVM (dB) versus P_{out} for 100 MHz and 200 MHz modulation bandwidths.

Table 1 summarizes performance against state-of-the-art CMOS DPAs. These measurement results indicate that the hybrid can be used as an impedance transformer of the DPA offering a compact and efficient replacement of the $\lambda/4$ transmission lines, also enabling load modulation for a broader Bandwidth.

Table 1. Comparison with state-of-the-art CMOS PAs

Spec/Ref.	This work	[13] [†]	[14]	[15]	[16] [†]	[17] [†]
Technology	22nm FD-SOI	45 nm CMOS SOI	65nm Bulk CMOS	65nm Bulk CMOS	22-nm FD-SOI	28nm Bulk CMOS
Frequency (GHz)	8–15	12-18	8.5-9.5	8–11.4	27–29	24.5-29.5
FBW (%)	61	40	11.1	35	7.1	18.5
Gain (dB)	19.6 : 17	16	23.2	24.4	26.1	16.5
Psat (dBm)	19.5	25.5	20.9	20.5	22.5	18.8
P1dB (dBm)	18	25	16.5	15.2	21.1	17.5
Peak PAE (%)	21	31.9	24	24.5	28.5	30
PAE (%) at 6 dB PBO	17	23	N/A	9	22.1	20
Supply (V)	3	2 / 4.8	3.3	1.2	2.4	1.8
Modulation	256 QAM SC	64 QAM SC	256 QAM SC	N/A	256 QAM SC	64 QAM SC
Data rate (MSym/sec)	100	200	600	N/A	800	100
EVM (dB)	-24.3	-25	-35.9	N/A	-30	-25
Pavg (dBm)	12.5	16.4	12.7	N/A	10.2	12.4
PAE at Pavg (%)	15	15	4.58	N/A	9	20
Die size (mm ²)	0.5	1	0.22	0.48	0.2	0.16

Entries annotated by [†] are DPAs, $FBW = \frac{f_{max} - f_{min}}{f_0}$ with $f_0 = \frac{f_{max} + f_{min}}{2}$.

5. Conclusions

A compact 8–15 GHz Doherty PA was proposed in 22-nm FD-SOI CMOS using a quadrature-hybrid-based output combiner in place of $\lambda/4$ inverters. A detailed analysis was presented to demonstrate the validity of quadrature hybrids in DPAs and their impact on the operating bandwidth. The DPA achieved 19.6 dB gain, 18 dBm P1dB, 19.5 dBm Psat, 21% peak PAE, 17% PAE at 6-dB back-off and an EVM of -24.3 dB for a 100 MSym./sec 256 QAM single carrier signal. Compared with prior CMOS DPAs, the proposed design offered robust performance in a larger FBW, highlighting the effectiveness of quadrature-hybrid combiners in mitigating loss and enhancing load modulation for

broadband applications. These results demonstrate scalability, broadband compatibility, and suitability for practical, compact, efficient 5G/6G X-band and Ku-band transceivers. In addition, the presented architecture offered scalability to millimeter-wave bands.

Author Contributions: Mohamed El-Nozahi was responsible for identifying the concepts and deriving mathematical proofs. Mohamed K. Hussein was responsible for the design and layout of the proposed DPA. Mostafa G. Ahmed was responsible for verification of the amplifier. Hani Fikri Ragaai was responsible for the paper manuscript. Adham Nafee was responsible for the measurements of the DUT.

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