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Article

Precision Operational Amplifier Using Complementary BJT and n-JFET Input Transistors

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Abstract

A novel precision operational amplifier scheme has been developed and investigated, implemented using complementary bipolar transistors and input field-effect transistors controlled by a p-n junction. Computer simulation of the developed circuit was performed in LTSpice environment, which demonstrates that the proposed schematic solution provides a high voltage gain (over 80 dB) with low static current consumption and relatively low load resistances ($R_L = 2\text{ k}\Omega$). The systematic component of the zero voltage offset does not exceed 100 μV .

Keywords: operational amplifier; complementary bipolar transistors; input field-effect transistor controlled by a p-n junction; systematic component of zero voltage offset; voltage gain coefficient

1. Introduction

An operational amplifier (op amp) with input junction-gate field effect transistors (JFETs) is a fundamental functional block in many radio-electronic systems. Currently, leading microelectronics companies are mass-producing op amps with input JFETs such as AD8244, AD8625, AD8220 (Analog Devices), and WSH223 (Tesla). In many cases, there is a need for precision operational amplifiers with small input zero voltage offset (V_0). [1].

The input zero voltage offset (V_0) of classical direct-coupled operational amplifiers consists of two main components.

$$V_0 = V_{OS,1} + V_{OS,2}, \tag{1}$$

where $V_{OS,1}$ – the schematic contribution to V_0 , whose numerical values depend on the quality of implementation of op amps functional blocks and relate to the influence of the following factors on $V_{OS,1}$:

- voltage asymmetry in the collector–base bias conditions of the dominant transistor pair;
- internal feedback factors in transistors caused by the Early effect;
- base current gain coefficients (β) of bipolar transistors, which in many cases have relatively low values ($\beta=50\text{-}200$).

In equation (1), $V_{OS,2}$ represents the process-related component, which depends on transistor fabrication tolerances, their design features and layout rules, the presence of temperature gradients across the elements of the input differential pair, etc. Various methods are effectively employed to reduce the process-related offset voltage component $V_{OS,2}$ [2–4]. Achieving low $V_{OS,2}$ value falls within the responsibility of process engineers and specialists in semiconductor device physics.

A significant disadvantage of the classic differential operational amplifier (Figure 1), which was selected for comparison with the proposed operational amplifier, is that it exhibits elevated values of the systematic component of the input offset voltage. This is caused by the implementation of

inefficient circuit design solutions. At the same time, as simulation shows, the circuit-induced component $V_{OS,1}$ in the conventional circuit amounts to several millivolts.

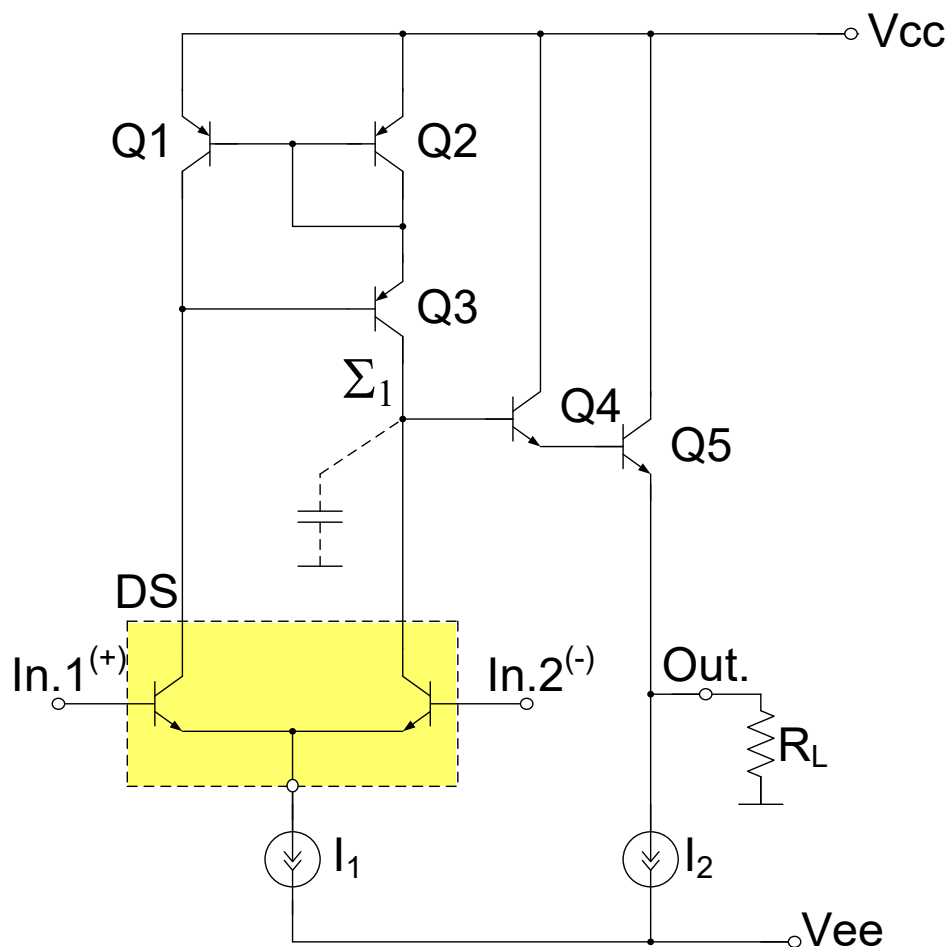


Figure 1. Circuit diagram of a classic differential operational amplifier (Motorola (USA) patent US 4,042,886, 1975).

In practical op amp circuits, the numerical values of the circuit-induced offset voltage component $V_{OS,1}$ in equation (1) dominate, necessitating specialized design of their fundamental functional blocks. Minimization of $V_{OS,1}$ falls within the responsibility of circuit designers developing operational amplifiers. The proposed op amp addresses this class of problems and enhances the performance parameters of differential stages implemented with field-effect transistors (FETs) [5–13].

2. Analysis of the Basic Scheme of the Proposed Op Amp

Figure 2 shows the circuit diagram of the proposed precision operational amplifier [14], which is implemented using complementary n-p-n and p-n-p bipolar transistors, as well as input junction field-effect transistors (JFETs). This integrated fabrication process has been adopted by several microelectronics companies, including the Novosibirsk Semiconductor Devices Factory “Vostok.”. At the same time, the systematic component of the zero offset voltage is significantly reduced in the developed circuit, and the effect of the current gain coefficients of the base of bipolar transistors on $V_{OS,1}$ is minimized. In addition, the circuit of the proposed op amp is characterized by the effect of reducing the effect of the low-resistance load resistance of the op-amp on its open voltage gain.

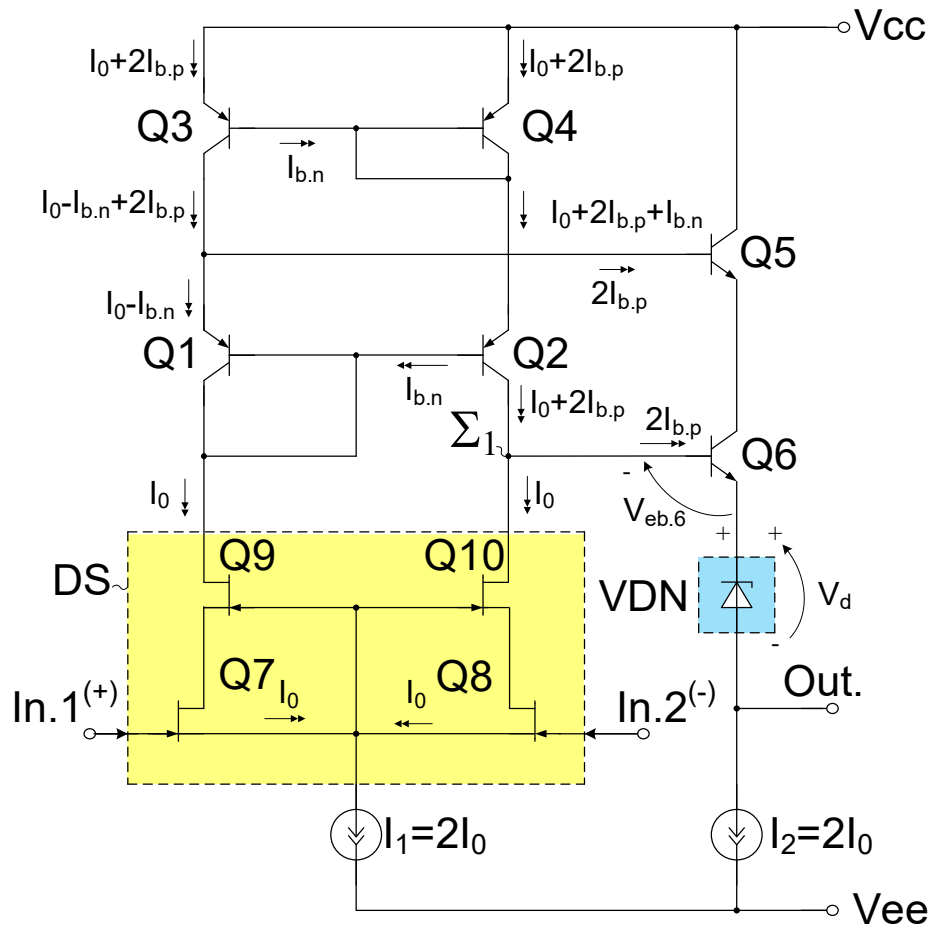


Figure 2. Circuit diagram of the proposed complementary BJT and n-JFET op amp with a single high-impedance node (Σ_1).

The DC operating point of the transistors in the circuit of Figure 2 is set by reference current sources ($I_1 = I_2 = 2I_0$), which in practical implementations are realized using n-JFET transistors.

According to Kirchhoff's current law, with bias currents $I_1 = I_2 = 2I_0$, the base, emitter, and collector currents of bipolar transistors Q1–Q6 shown in Figure 2 are established as indicated.

It also follows from Figure 2 that at the high-impedance node Σ_1 , the sum of the currents flowing into this node is equal to the sum of the currents flowing out, i.e., the current error at the high-impedance node is zero. This is a necessary condition for minimizing the circuit component of the zero bias voltage $V_{OS,1}$ in formula (1). This conclusion is confirmed by computer simulation of the circuit shown in Figure 3, where $V_{OS,1} = 65.7\mu V$. The open-loop gain of the op amp with a high-impedance load is close to 90 dB (Figure 4).

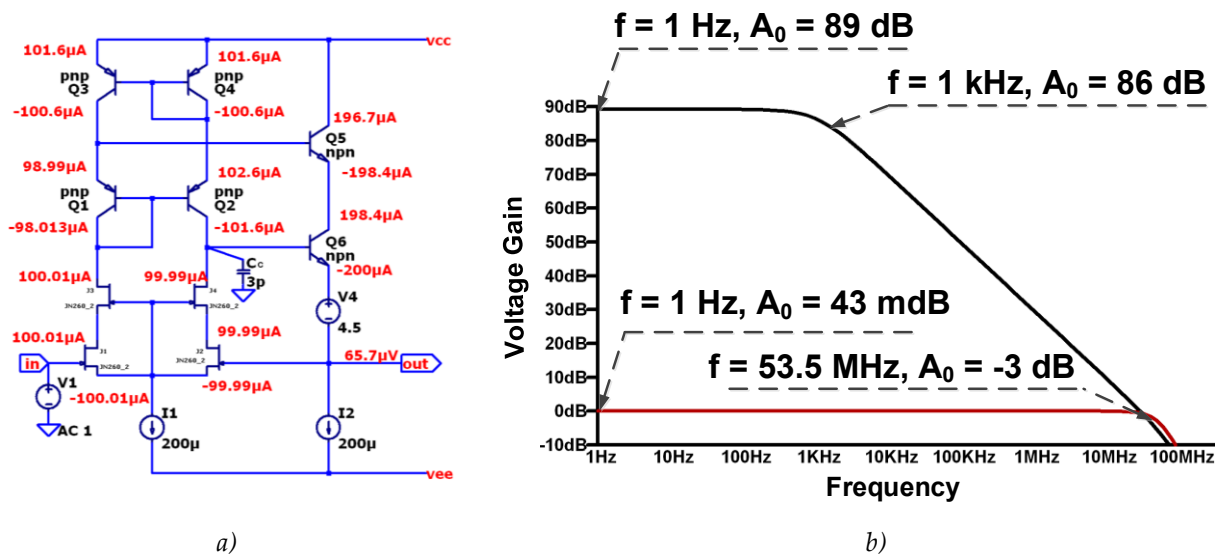


Figure 3. DC operating point of the transistors in the op amp (a); logarithmic amplitude-frequency characteristic of the voltage gain coefficient of the op amp(b).

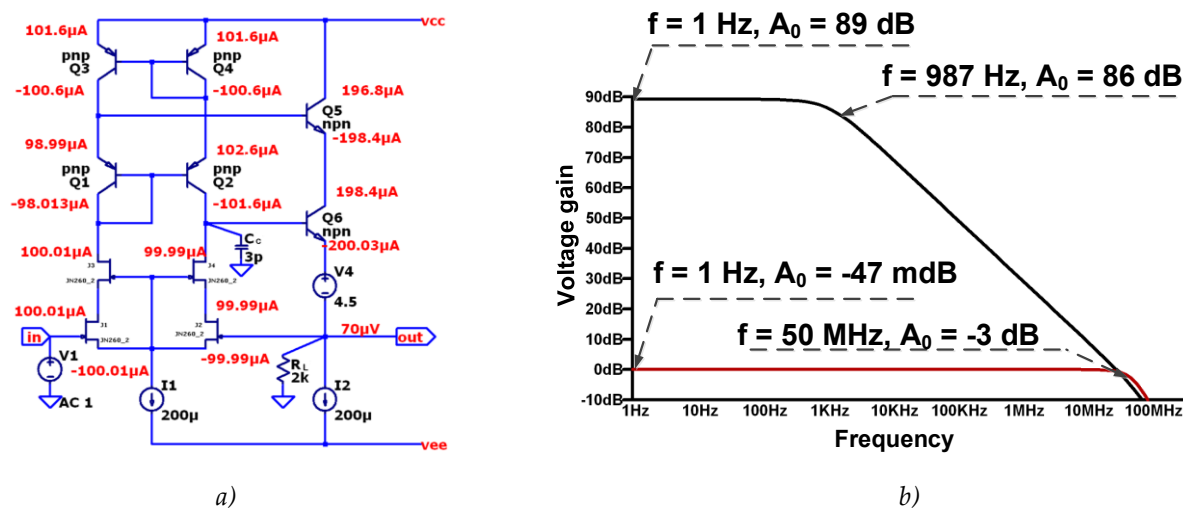


Figure 4. DC operating point of transistors (a); The logarithmic amplitude-frequency characteristic plot of the voltage gain (b).

3. Results of Computer Simulation

Figure 3 presents the DC operating point of the operational amplifier transistors (a) as well as the logarithmic amplitude-frequency plot of the voltage gain (b) of the operational amplifier, which is illustrated in Figure 2, within the LTSpice environment. The analysis is conducted under the following conditions: $I_1=I_2=200\mu\text{A}$, V_4 (VDN)=4.5V, temperature ($t^\circ=27^\circ\text{C}$), and supply voltages $V_{cc}=V_{ee}=\pm 10\text{V}$.

In the proposed op amp topology, the influence of the load resistance R_L the voltage gain is minimized. As demonstrated by the simulations in Figure 4.a and Figure 4.b for $R_L=2\text{k}\Omega$, the voltage gain coefficient of the op amp (Figure 2) remains virtually unchanged - close to 90 dB - compared to the case of an infinite load resistance ($R_L=\infty$).

Figure 4 illustrates the DC operating point for the transistors (a) and the logarithmic amplitude-frequency characteristic of the voltage gain (b) for the developed operational amplifier (Figure 2). The analysis is conducted under the following conditions: I_1 and I_2 are set at 200 μA , V_4 (VDN) is 4.5 V, compensation capacitor C_c is 3 pF, the ambient temperature is 27 $^\circ\text{C}$, the supply voltages V_{cc} and V_{ee} are $\pm 10\text{ V}$, and the load impedance is relatively low at 2 k Ω .

Figure 5 shows the DC operating point of transistors (a) and the logarithmic amplitude-frequency response (b) of the classic op amp circuit (Figure 1) at $I_1=I_2=200\text{ }\mu\text{A}$, $V_4(\text{VDN})=4.5\text{V}$, $C_c=3\text{pF}$, $t^\circ=27^\circ\text{C}$, $V_{cc}=V_{ee}=\pm 10\text{V}$ and high-impedance load ($R_L=\infty$).

Figure 5 presents a comprehensive DC operating point analysis of the transistors, as well as the logarithmic amplitude-frequency response, for the classic operational amplifier circuit depicted in Figure 1. This analysis is conducted under a set of conditions, including $I_1=I_2=200\text{ }\mu\text{A}$ for equal current sources, $V_4(\text{VDN})=4.5\text{V}$ for the input voltage, $C_c=3\text{pF}$, $t^\circ=27^\circ\text{C}$ for operating temperature, $V_{cc}=V_{ee}=\pm 10\text{V}$ for the supply voltages, and a high-impedance load ($R_L=\infty$).

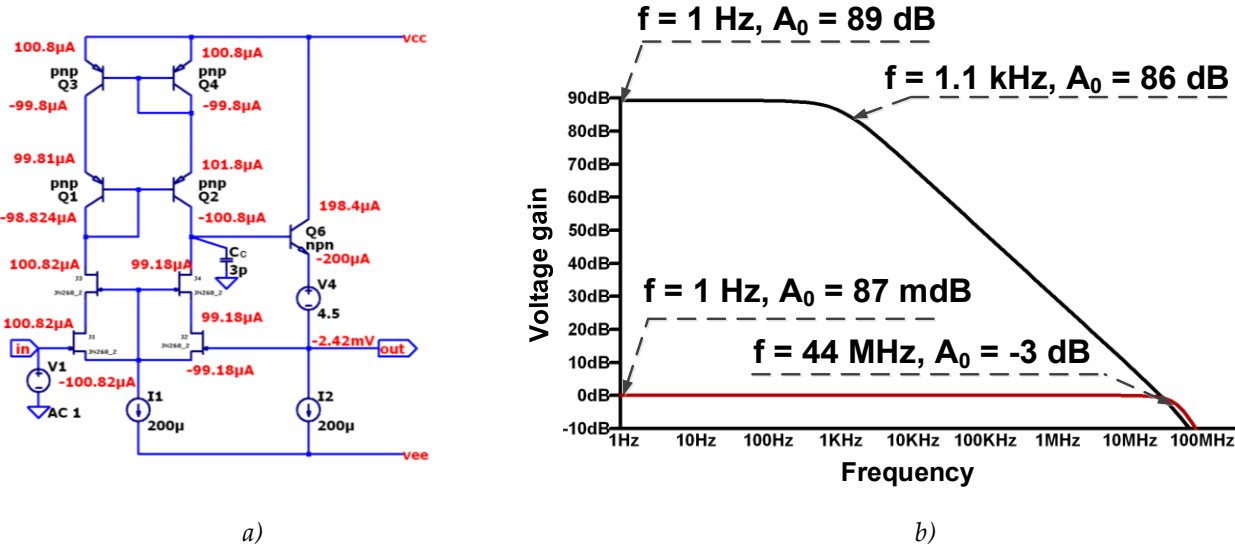


Figure 5. DC operating point of transistors (a); Logarithmic amplitude-frequency characteristic of the voltage gain (b).

Figure 6 demonstrates the DC operating points (a) and the logarithmic amplitude-frequency characteristic of the voltage gain (b) for the transistors within the standard operational amplifier circuit shown in Figure 1. The conditions are established with a current $I_1=I_2$ set at 200 μA , a voltage $V_4(\text{VDN})$ of 4.5V, a capacitor C_c with a capacitance of 3pF, at a temperature of 27°C, and utilizing a supply voltage of $\pm 10\text{V}$. The load impedance is configured at $R_L=2\text{ k}\Omega$, which is relatively low.

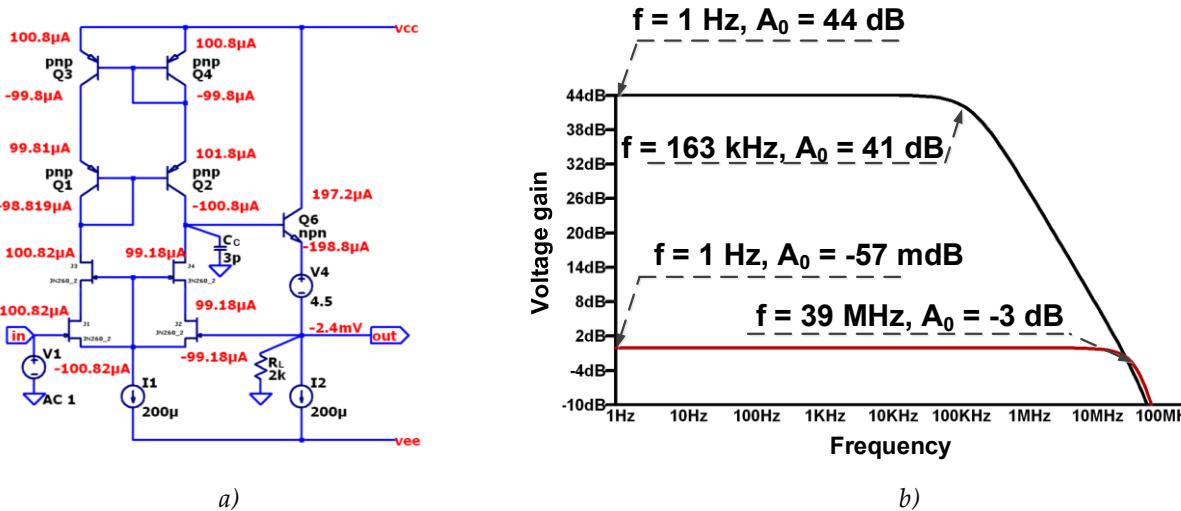


Figure 6. DC operating point of transistors (a); Logarithmic amplitude-frequency characteristic of the voltage gain (b).

Thus, comparative modeling of two op-amps shown in Figures 7 and 8, as well as Figures 9 and 10 shows that in the absence of the bipolar transistor Q5 in the circuit (as is done in Figure 9), the voltage gain of the op amp at $R_L = 2 \text{ k}\Omega$ decreases by 45 dB, i.e. by more than two orders of magnitude. In addition, the proposed op-amp circuit creates conditions under which the current error in the high-impedance node Σ_1 is minimized, since here:

$$I_{c,2} = I_{d,10} + I_{b,6}I, \quad (2)$$

where $I_{c,2} = 2I_0 + 2I_{b,b}$ – DC current of the bipolar transistor Q2 collector;

$I_{b,6} = 2I_{b,b}$ – DC current of the bipolar transistor Q6 base;

$I_{d,10} = I_0$ – DC drain current of the Q10 output field-effect transistor with a control p-n junction.

This allows us to obtain small values of $V_{OS,1}$ in formula (1), which is confirmed by the results of computer modeling in Figure 3, Figure 5, where

$$V_{OS,1} = 65\text{--}70 \text{ }\mu\text{V}.$$

The proposed op amp circuit is shown in Figure 2 and is also characterized by an increased level of voltage gain A_0 (about 90 dB) at a load resistance of $2 \text{ k}\Omega$, which is more than two orders of magnitude higher than A_0 in the op amp circuit (Figure 9, Figure 10).

Thus, the proposed op amp has significant advantages in comparison with the known circuit design (Figure 1).

4. Conclusion

A precision operational amplifier circuit has been developed and investigated, which can be implemented based on technological processes implementing n-JFET transistors, as well as p-n-p and n-p-n bipolar transistors. Comparative modeling of the proposed circuit and op-amp with a typical circuit design shows that the new circuit provides a higher gain (by 40 dB), can operate at relatively low load resistances, and provides a low level of the systematic component of the zero offset voltage (less than $100 \text{ }\mu\text{V}$).

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