Enhanced Extremum Seeking Control (EESC) Structure for Dual Bridge DC-DC Converters

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Posted Date: 6 March 2026

doi: 10.20944/preprints202603.0464.v1

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 doi:10.20944/preprints202603.0464.v1

Article

Enhanced Extremum Seeking Control (EESC) Structure for Dual Bridge DC-DC Converters

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Abstract

This paper analyzes the phenomenon of output voltage collapse under step load perturbations in dual bridge converters where an extremum seeking control (ESC) optimization algorithm is employed. Although ESC is an effective online duty-cycle optimization method under steady-state power transfer conditions, it can result in severe output voltage degradation during large-signal transients. This degradation is primarily caused by two factors: the reduced power transfer capability associated with the optimized duty-cycles, and the limited dynamic capability of the ESC structure to rapidly adjust the duty-cycles. To overcome this limitation, an enhanced extremum seeking control (EESC) structure is proposed, which enables fast output voltage reference tracking under dynamic operating conditions, while preserving ESC's capability for online duty-cycle optimization to minimize losses and improve efficiency. The proposed method extends the applicability of ESC from steady-state optimization to large-signal dynamic scenarios. Comparative experimental results on a dual active half-bridge (DAHB) converter reveal the output voltage collapse associated with conventional ESC structure and verify the high efficiency and absence of dynamic voltage collapse achieved by the proposed EESC structure.

Keywords: dual active half-bridge (DAHB) converters; extremum seeking control (ESC); output voltage collapse; online duty-cycle optimization

1. Introduction

Low level control of dual bridge converters, both half-bridge (DAHB) and full bridge (DAB) type, often exploits the available degrees of freedom, mostly bridge duty-cycles, to optimize converter efficiency. The DAHB converter is a low-component-count and low-cost topology. It inherently avoids transformer dc bias current, thereby eliminating the need for dc-blocking capacitors, typically required in DAB converters. On the other hand, for a given rated power, in the DAHB converter, each semiconductor device must withstand higher current stress than in the DAB. Overall, the DAHB converter has become increasingly attractive for low-medium power applications and has been validated as a promising topology [1] for many applications. Regarding modulation methods, the DAB converter is typically controlled by phase-shift modulation [2], but efficiency is often improved by jointly modulating both bridge duty-cycles (inner phase shifts) to generate symmetrical three-level transformer-port voltages with equal positive and negative amplitudes. In contrast, the DAHB converter achieves efficiency optimization solely through asymmetric positive and negative voltage amplitudes in a two-level transformer-port voltage modulation scheme [3,4]. Regardless of whether symmetric modulation is employed in DAB converters or asymmetric modulation is used in DAHB converters, properly optimized duty-cycles can reduce the transformer RMS current and expand the zero-voltage-switching (ZVS) operating range, thereby improving the overall converter efficiency. It should be noted, however, that duty-cycle optimization is unnecessary when the input and output dc-port voltages are perfectly matched. Duty-cycle optimization becomes particularly important under conditions of port voltage mismatch and operation below the rated power.

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Especially in those conditions, a key challenge lies in determining how to calculate the optimal duty-cycles in an effective and reliable manner. The most direct and fundamental approach for calculating the optimal duty-cycles is to describe the transferred power, transformer-port voltages, and transformer current using analytical expressions, corresponding to the different converter operating regions, that result from the different possible sequences of switching events within the modulation period. The analytical expressions, that vary with the power level and the input and output dc-port voltages [5–7], can then be used in classical constrained optimization techniques, such as the Lagrange multiplier method (LMM) to find the optimal modulation parameters. This approach is not only highly complex, requiring the evaluation of a large number of expressions, but also depends on the consistency between ideal circuit models and practical implementations, which may be difficult to achieve in some cases.

Alternatively, other offline methods, like particle swarm optimization (PSO), can be employed to obtain optimal duty-cycles. However, they also require explicit expressions, involving multiple switching variables. The optimal duty-cycles can then be stored in look-up-tables (LUT) leading to implementations [8] that require storing a large number of pre-calculated values, possibly exceeding the memory capacity of practical digital controllers.

To address these limitations, extremum seeking control (ESC) has been proposed as an online, memory-efficient, and model-free alternative for computing optimized duty-cycles without the need to derive explicit conduction and switching loss models. ESC has been applied in DAB converters to reduce the high-frequency transformer RMS current, thereby mitigating conduction losses [9]; to reduce the input current, leading to reductions in both conduction and switching losses [10]; and to suppress electromagnetic interference (EMI), which is particularly difficult to model accurately [11].

It should also be noted that ESC can be formulated in a multi-dimensional manner, while the underlying operating principle remains the same. For example, conventional single-dimensional ESC algorithms optimize only one degree of freedom and are commonly used for maximum power point tracking (MPPT) [12,13]. In contrast, multi-dimensional ESC variants [9–11] are designed to optimize multiple duty-cycles in DAB converters. Meanwhile, the phase-shift angle, which directly determines the transferable power under the optimized duty-cycles, is regulated by the output-voltage control loop. Notably, the duty-cycles generated by ESC evolve on a much slower time scale than the voltage control loop [9–11]. This control structure, in which ESC optimizes part of the circuit degrees of freedom (more than one) while another degree of freedom is determined by a PI controller, is generally applicable to both DAB and DAHB converters. Although optimized duty-cycles improve steady-state efficiency, especially under light-load conditions, they simultaneously reduce the power transfer capability, which poses a potential risk in dynamic operating conditions.

Specifically, in a DAHB converter, ESC achieves efficiency optimization by slowly moving the duty-cycles away from their nominal values, typically set by design at 0.5. The duty-cycles fundamentally determine the power transfer capability of the DAHB converter, and any deviation from 0.5 leads to a reduced power transfer capability compared with the nominal value. As a consequence, if the load steps from light to heavy, exceeding the reduced power transfer capability, the reference power will not be achieved, resulting in output voltage collapse, even if the phase shift angle will be rapidly increased up to its saturation limit.

To preserve the favorable steady-state efficiency optimization capability of ESC, while overcoming its output voltage dynamic collapse issue, this paper proposes an enhanced ESC (EESC), and applies it, as an example, to a DAHB converter with optimized asymmetric duty-cycles with phase shift angle still controlled by PI regulator. The EESC is indeed applicable, with simple modifications, to any dual bridge topology.

Based on the duty-cycle-transferred-power characteristics, the proposed EESC incorporates a load-responsive duty-cycle regulation loop, which promptly restores compatible duty-cycles when the power transfer capability is lower than the reference power. This mechanism enables rapid duty-cycle transitions when the output-voltage controller operates in a saturated condition. As a result, the

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proposed approach maintains tight output-voltage tracking during large-signal load transients, while preserving the steady-state efficiency benefits of ESC and achieving higher efficiency than fixed 50% duty-cycle operation. Beyond applications in dual-bridge converters represented by DAHB and DAB, the proposed EESC strategy can also be extended to other classes of power electronic converters that require duty-cycle optimization [14,15].

2. Analysis of ESC Limitations in Dual Bridge Converters

Figure 1 illustrates the application of ESC to generate optimal symmetrical duty-cycles D_1 and D_2 for the DAB converter. Operating online and without requiring analytical or Fourier-domain models, the ESC adjusts the duty-cycles [9–11] to convert the transformer-port voltages v_p and v_s from two-level to symmetrical three-level waveforms (the duty-cycles refer to the positive and negative pulses of v_p and v_s, which have identical widths and can be optimized from 0.5 down to 0), and finally reshape the transformer current i_p. This results in a reduction of the input current (input power), when this is set as the objective function. The reason is that duty-cycle adjustments tend to extend the ZVS region and reduce the transformer RMS current, which correspond to lower switching and conduction losses, thereby improving the converter efficiency [9–11].

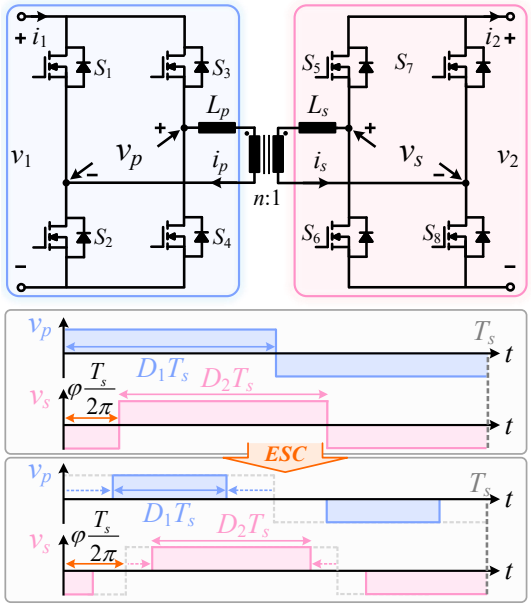

Figure 1. DAB converter with symmetrical duty-cycle modulation.

Since DAB and DAHB share very similar operating characteristics and the same number of degrees of freedom, ESC can also be applied to the DAHB converter to determine the optimized duty-cycles D_1 and D_2. These duty-cycles are associated with the positive voltage level durations of the transformer-side voltages v_p and v_s, respectively. In this case, the positive and negative amplitudes of v_p and v_s are asymmetric, as illustrated in Figure 2. Both the transformer current and the transformer-port voltages of the DAHB converter exhibit shape symmetry with respect to duty-cycles of 0.5 [16], so that, for example, the operating point $(D_1, D_2) = (0.2, 0.3)$ is symmetric to $(D_1, D_2) = (0.8, 0.7)$. Therefore, this paper focuses only on the case where both D_1 and D_2 are less than or equal to 0.5.

Essentially, ESC is an optimization algorithm that requires a power constraint for both DAB and DAHB converters. Effective duty-cycle optimization with the objective of minimizing the input current can only be achieved when the output voltage control loop successfully regulates the output voltage to track its reference. Without output voltage control, the input-current-minimization-based duty-cycle optimization becomes invalid, because the minimum input current occurs at zero transferred power, where the input current is zero. Obviously, such an operating point is meaningless from a power conversion perspective.

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Under dynamic conditions, when the reference transferred power suddenly increases beyond the current power transfer capability, the output voltage control loop becomes saturated and fails to maintain voltage regulation, indicating that the power constraint is violated. In this situation, conventional ESC cannot properly increase D_1 and D_2 to first restore the required power transfer capability and then re-enter the efficiency optimization mode. Under the given duty-cycles, the maximum transferred power $P_{\mathrm{o,max}}$, also known as the power transfer capability P_c (achieved by applying the appropriate phase shift angle under the given duty-cycles), for arbitrary values of D_1 and D_2 is given by [16]:

$$P_{\mathrm{o,max}} = P_c = \frac{D_1 D_2 (1-D_1)(1-D_2) n V_1 V_2}{2 f_s L_T} \leq \frac{n V_1 V_2}{32 f_s L_T} = P_{\max} \tag{1}$$

where the total leakage inductance is given by $L_T = L_p + n^2 L_s$, f_s is switching frequency (constant), V_1 and V_2 denote the given DC-port voltages, and $P_{\max}$ represents the upper limit of transferable power of DAHB, which is attained when $D_1 = D_2 = D_{\max} = 0.5$ and can alternatively be interpreted as the power transfer capability of the DAHB converter. It should also be noted that [16] also indicates that when $\phi_{\max} = D_1(1-D_2)$, the DAHB reaches its power transfer limit under given D_1 and D_2. From (2), when D_1 and D_2 are reduced by the ESC optimization process, the power transfer capability is correspondingly reduced, and the achievable maximum output power $P_{\mathrm{o,max}}$ may no longer be sufficient to meet the load requirement. As a consequence, the output voltage regulator may enter saturation, ultimately leading to output voltage collapse. To address the dynamic collapse caused by the conventional ESC, shown in Figure 3, a mechanism is required to rapidly adjust D_1 and D_2 from their original steady-state optimized values when ϕ saturates at its predefined threshold value ϕ_{th}.

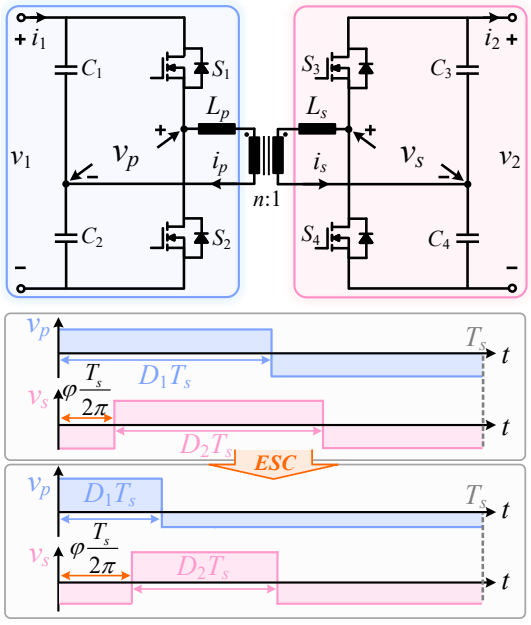

Figure 2. DAHB converter with asymmetrical duty-cycle modulation.

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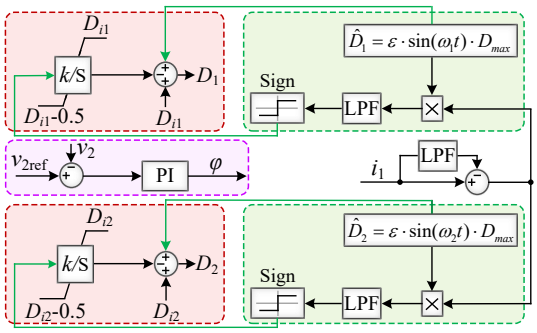

Figure 3. Traditional extremum seeking control (ESC) structure.

For the output voltage PI regulator, if its output ϕ reaches the phase shift angle required to achieve the maximum power under the ESC-optimized steady-state duty-cycles, it indicates that the power transfer capability corresponding to the optimized duty-cycles is insufficient to meet the reference power. Accordingly, the structure of the conventional ESC must be modified, leading to the proposed enhanced ESC (EESC), as shown in Figure 4.

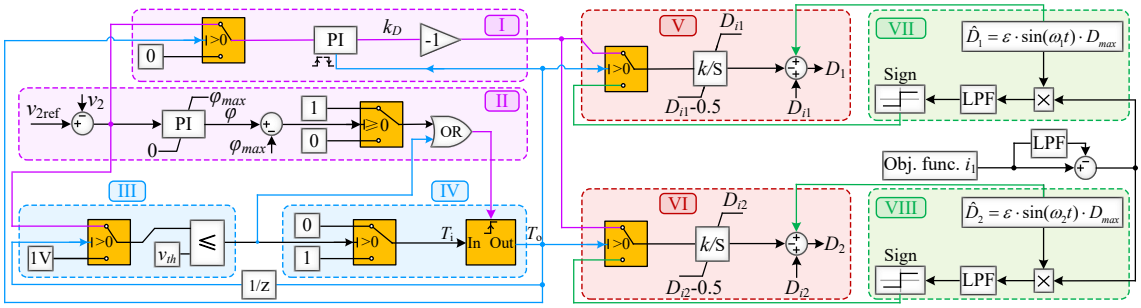

Figure 4. Proposed enhanced extremum seeking control (EESC) structure.

3. Mechanism of the Proposed EESC Structure

The proposed EESC structure not only incorporates a conventional ESC-based duty-cycle optimization loop with small-amplitude sinusoidal perturbations, enabling a slow optimization of the duty-cycles to minimize the objective function (e.g., the input current i_1) and thus maximize converter operating efficiency, but also allows rapid adjustment in the duty-cycles to promptly increase the power transfer capability. These two components, responsible for the slow variation and rapid increase of the duty-cycles, are coordinated through multiple switching conditions and logical selectors, resulting in eight functional blocks labeled from I to VIII. Among them, only the sinusoidal duty-cycle injection blocks (VII and VIII) are retained from the conventional ESC as Figure 3.

- **Block I:** This block contains a PI regulator that generates the coefficient k_D, which is multiplied by the integrator gain k in Blocks V and VI. The PI regulator in Block I is not continuously active; it is enabled only when a valid trigger signal is issued by Block IV. When the regulator is disabled, it is reset and its input is forced to zero. Only when the regulator is enabled does its input correspond to the error between the output voltage and its reference.
- **Block II:** A PI-based phase-shift angle regulator continuously processes the output voltage error and determines the phase shift angle ϕ. The regulator output is limited and clamped by a predefined threshold $\phi_{\text{th}} = D_1(1 - D_2)$. The difference between the regulator output ϕ and ϕ_{th} is then compared with zero and used as the decision condition of a threshold-controlled switch. The output of this threshold-controlled switch, together with the output of Block III, forms a trigger signal for Block IV through a logical OR operation.
- **Block III:** This block consists of a threshold-controlled switch cascaded with a comparator. The signal from the trigger system in block IV determines whether the output is the voltage error or a specific value exceeding v_{th} (e.g., 1 V), with $v_{\text{th}} = 0$ V. Once the threshold is reached, the output

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of the switch is compared with v_{th}, and the comparison result—either 0 or 1—is sent to block II and block IV.

- **Block IV:** This part contains a threshold-controlled switch, which essentially inverts the signal sent from block III. When block III sends a high-level signal (1), the threshold-controlled switch outputs a low-level signal (0). This output serves as the input to trigger the trigger system, and together with the driving signal from block II, it determines the resulting high- or low-level output.
- **Blocks V and VI:** These two blocks are responsible for selecting the operation mode, choosing either the perturbation-based, slowly optimized duty-cycles from block VII with block VIII, or the fast-rising non-optimized duty-cycles from block I.
- **Blocks VII and VIII:** In these blocks, small-amplitude perturbations with identical magnitudes but different frequencies are injected into the duty-cycles. Based on the resulting objective function (input current i_1) response, the duty-cycle adjustments required to achieve the objective function minimization objective are generated and superimposed onto the initial duty-cycles D_{i1} and D_{i2}. Accordingly, the optimization procedures implemented in these blocks, define the primary- and secondary-side duty-cycles, D_1 and D_2, as per

$$\begin{aligned} D_1(t) &= D_{i1} + \hat{D}_1(t) - k \int \text{sign}\Big(\Big[i_1(t) - i_{1,\text{LPF}}(t) \Big] \hat{D}_1(t) \Big) \text{d}t, \\ D_2(t) &= D_{i2} + \hat{D}_2(t) - k \int \text{sign}\Big(\Big[i_1(t) - i_{1,\text{LPF}}(t) \Big] \hat{D}_2(t) \Big) \text{d}t, \end{aligned} \tag{2}$$

where D_{i1} represents the initial conditions, k denotes the integral gain of the duty-cycles, and ω_c is the cutoff frequency of the low-pass filters (LPFs) employed to compute the averaged values of objective function (input current i_1) and the ESC correlation terms [9]. In addition, (3) accounts for the duty-cycle perturbations $\hat{D}_1$ and $\hat{D}_2$, defined as follows:

$$\hat{D}_1(t) = \varepsilon \cdot D_{\text{max}} \sin(\omega_1 t), \qquad \hat{D}_2(t) = \varepsilon \cdot D_{\text{max}} \sin(\omega_2 t) \tag{3}$$

where $\varepsilon \cdot D_{\text{max}}$ denotes the magnitude of the injected duty-cycle perturbation, while ω_1 and ω_2 represent the angular frequencies of the injected perturbations. The former is typically kept small to prevent the transformer current and transferred power from exhibiting relatively large fluctuations, undesirable from the load perspective. Therefore, in this study, this value is chosen as 0.2% of D_{max}. The latter, to ensure proper operation, are set higher than the cutoff frequency of the low-pass filters. Also, all low-pass filters are set with the same cutoff frequency; otherwise, the EESC may fail to converge to the correct high-efficiency operating point [10].

The detailed operating sequence of the proposed EESC is illustrated in Figure 5. Overall, it can be divided into two main states, ① and ②, where the second main state further consists of two sub-states.

In the main state ①, the blue lines represent the signal transmission paths. It can be observed that the perturbation duty-cycles are injected to activate the objective function-optimization (efficiency-optimization) mode through block V, block VI, block VII, and block VIII. Meanwhile, the voltage PI controller in block II operates in the normal (unsaturated) region. Since $\phi - \phi_{\text{max}}$ is smaller than zero, its output remains at a low logic level (0). In addition, the output of block III is also a low logic level (0), such that the trigger system in block IV is not activated. Consequently, the values generated by the sign function in block VII and block VIII, multiplied by the gain k, are applied as the duty-cycle variation slopes for block V and block VI.

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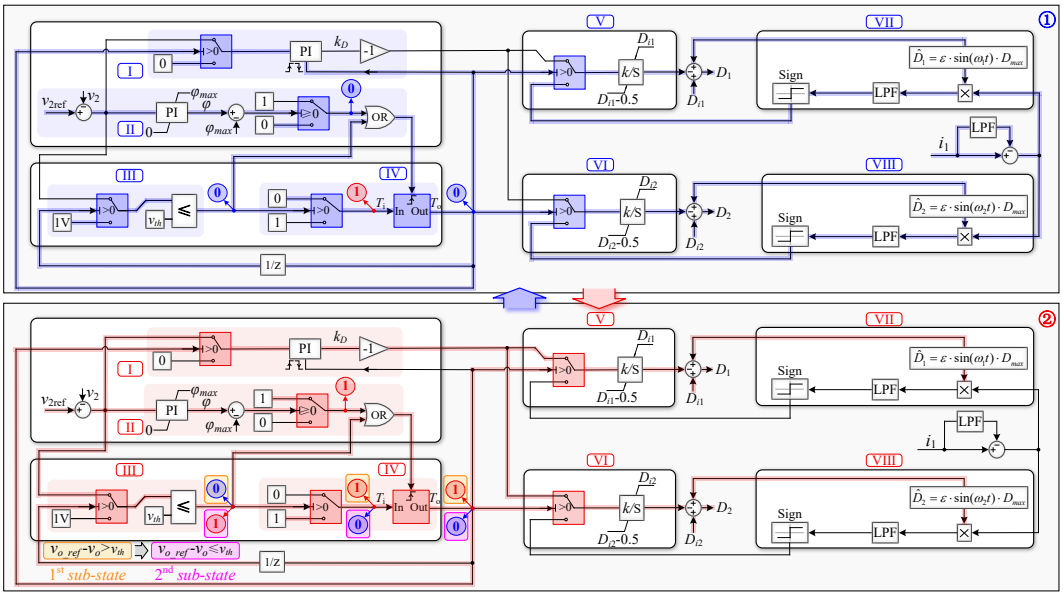

Figure 5. Operating sequence of the proposed enhanced extremum seeking control (EESC) structure.

Regarding the second sub-state of the main state ②, illustrated by the red lines in Figure 5, when the load demand (i.e., the reference output voltage in the case of resistive loads) increases so much that the phase shift angle reaches its saturation limit ϕ_{th} (trigger condition I), the trigger system in block IV is activated upon receiving a high-level signal from block II. The trigger system activation results in the outputs of the switches in block V and block VI being determined by the product of the PI controller output k_D from block I and the gain k in block V and block VI. As a consequence, the duty-cycles D_1 and D_2 can be increased from D_{l1} and D_{l2} to D_{h1} and D_{h2} such that the difference between v_2 and v_{2ref} remains less than or equal to v_{th}, i.e.,

$$\begin{aligned} D_{h1} &= D_{l1} - \int k \cdot k_D \, \mathrm{d}t, \\ D_{h2} &= D_{l2} - \int k \cdot k_D \, \mathrm{d}t. \end{aligned} \tag{4}$$

where the applied duty-cycles rapidly increase from the lower values D_{l1} and D_{l2} to the higher values D_{h1} and D_{h2} to increase the power transfer capability for both DAB and DAHB converters, ensuring that $v_{2\text{ref}} - v_2 \leq v_{\text{th}}$ (in this structure, v_{th} can be set to 0). When $v_{2\text{ref}} - v_2 \leq v_{\text{th}}$, the output of block III changes from low (0) to high (1), while the input of the trigger system in block IV switches from high (1) to low (0). Since the trigger system remains active throughout state ②, its output transitions from 1 to 0. Overall, the input–output behavior of the trigger system, together with its trigger signal, denoted by T_{i} and T_{o}, is summarized as

$$\begin{aligned} &① \quad T_{\text{i}} = 1, \quad T_{\text{o}} = 0, \\ &② \quad \begin{cases} v_{2\text{ref}} - v_2 > v_{\text{th}} & T_{\text{i}} = 1, \quad T_{\text{o}} = 1, \\ v_{2\text{ref}} - v_2 \leq v_{\text{th}} & T_{\text{i}} = 0, \quad T_{\text{o}} = 0. \end{cases} \end{aligned} \tag{5}$$

Notably, the output of the trigger system in block IV must first pass through a one-step delay before reaching the threshold input of the switch in block III; omitting this delay would cause the control loop to lock up. Therefore, after this one-step delay, main state ② is completed and the system transitions to main state ①.

4. Experimental Results

Figure 6 shows the experimental platform using an Imperix Boombox 3.0 controller to implement both the conventional ESC and the proposed EESC. The converter is built from an Imperix power rack

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together with an external transformer, inductor and split capacitors, forming a DAHB converter as an experimental case, with the specific parameters listed in Table 1. The duty-cycle perturbations $\hat{D}_1$ and $\hat{D}_2$ are injected at frequencies of 12 Hz and 18 Hz, respectively, with equal amplitudes of 0.001.

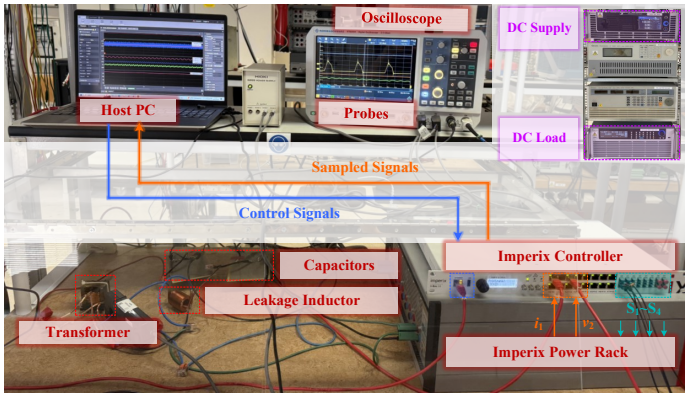

Figure 6. Experimental platform for verifying DAHB operation under ESC and proposed EESC.

Table 1. DAHB experimental parameters.

Parameters	Symbol	Value
Input voltage	v_1	70 V
Reference output voltage	$v_{2\text{ref}}$	40 V
Switching frequency	f_s	50 kHz
Transf. turns ratio	n	1
Transf. leakage inductance	L_T	11.3 μH
Split capacitors	C_1–C_4	44 μF
Dead time	t_d	0.1 μs
Rated power	P_{rated}	105 W

Figure 7 shows the input and output voltages, v_1 and v_2, together with the transformer current and the output current i_2, corresponding to the non-optimized and optimized duty-cycles D_1 and D_2, respectively. In the non-optimized case, both duty-cycles are set to 0.5, resulting in transformer RMS currents (which are closely related to conduction losses) of 3.49 A and 3.88 A at 25% P_{rated} and 50% P_{rated}, respectively. Under the same operating conditions, the optimized duty-cycles are $(D_1, D_2) = (0.163, 0.250)$ at 25% P_{rated} and $(D_1, D_2) = (0.235, 0.335)$ at 50% P_{rated}, leading to reduced transformer RMS currents of 1.86 A and 3.34 A, respectively. As a result, the optimized duty-cycles improve the conversion efficiency by 14.67% and 2.06% at 25% P_{rated} and 50% P_{rated}, respectively. This demonstrates that the proposed EESC can effectively optimize the efficiency of the converter.

Figure 8 shows the dynamic comparison of the DAHB converter during a load step from 25% P_{rated} to 50% P_{rated} under ESC and EESC. For a fair comparison, the ESC is conducted with a fixed phase shift angle saturation as Figure 8(a) and a time-varying phase shift angle saturation according to $\phi_{\max} = D_1(1 - D_2)$ as Figure 8(b). It can be clearly observed that, when using the traditional ESC, whether the phase shift angle saturation is fixed or varies with duty-cycles, the output voltage v_2 drops suddenly by more than 20 V and 5 V immediately after the load step and then remains far below $v_{2\text{ref}}$, collapsing gradually.

In contrast, when using the proposed EESC, as Figure 8(c), the output voltage experiences a maximum deviation of only 2 V at the instant of the load step and reaches steady state within approximately 30 ms. No voltage collapse occurs, demonstrating that the traditional ESC suffers from power transfer limitations and voltage collapse issues, whereas the EESC effectively avoids such problems.

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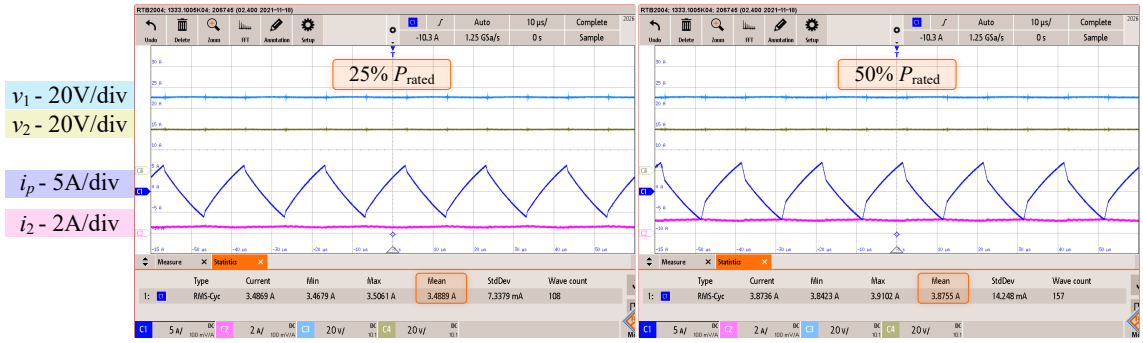
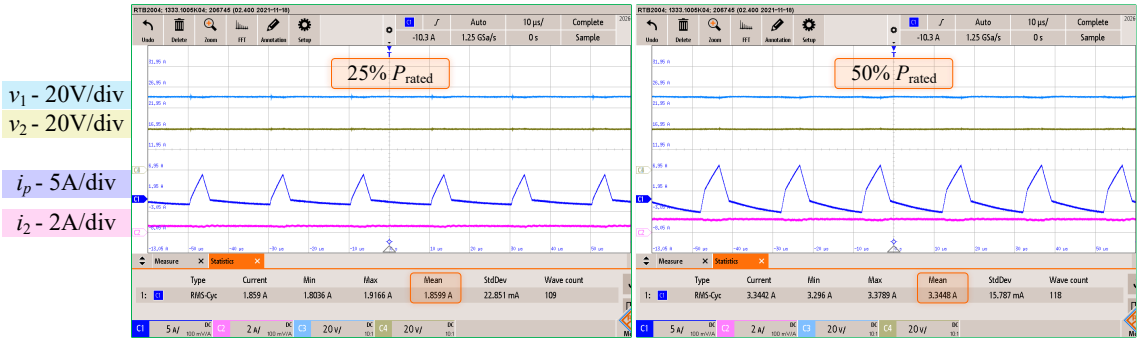


(**a**)



(**b**)

Figure 7. Comparison of waveforms at 25% and 50% of P_{rated}: (**a**) with non-optimized duty-cycles; (**b**) with duty-cycles optimized by the EESC.

Figure 9 shows the evolution of the control parameters D_1, D_2, and ϕ, as recorded by the control monitoring system, during a load step, corresponding to the experimental plots in Figure 8 (same order). Before the load step, both the traditional ESC and the proposed EESC maintain D_1, D_2, and ϕ at the appropriate steady-state values. However, when the load step occurs, the duty-cycles prior to the step result in a power transfer capability that is insufficient to meet the load requirement. In this case, under the traditional ESC with both fixed and time-varying phase-shift angle saturation limits as Figure 9(a), ϕ immediately saturates at its limit, D_2 remains nearly constant under fixed phase-shift angle saturation, whereas D_2 decreases initially and then remains constant under time-varying phase-shift angle saturation as Figure 9(b), and D_1 all decreases continuously. This behavior is due to the lack of power constraint: the ESC still attempts to adjust D_1 and D_2 to minimize the input current i_1. As D_1 decreases (further limiting the power transfer), i_1 naturally decreases as well, rendering the adjustment meaningless.

In contrast, Figure 9(c) shows the performance under EESC, where the proposed strategy suspends the slow optimization of i_1 during the load step, and both D_1 and D_2 are rapidly increased to enhance the converter's power transfer capability. Once D_1 and D_2 reach values that bring the output voltage v_2 close to $v_{2\text{ref}}$, the slow optimization targeting input current minimization resumes. Meanwhile, ϕ does not remain saturated as in the traditional ESC.

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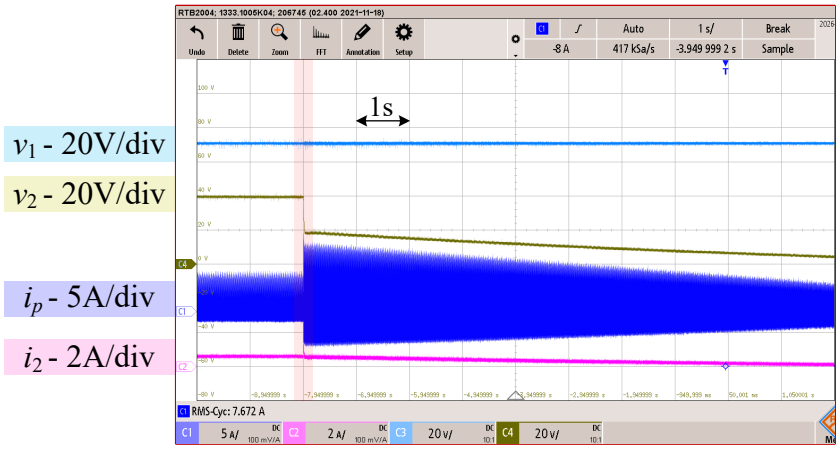

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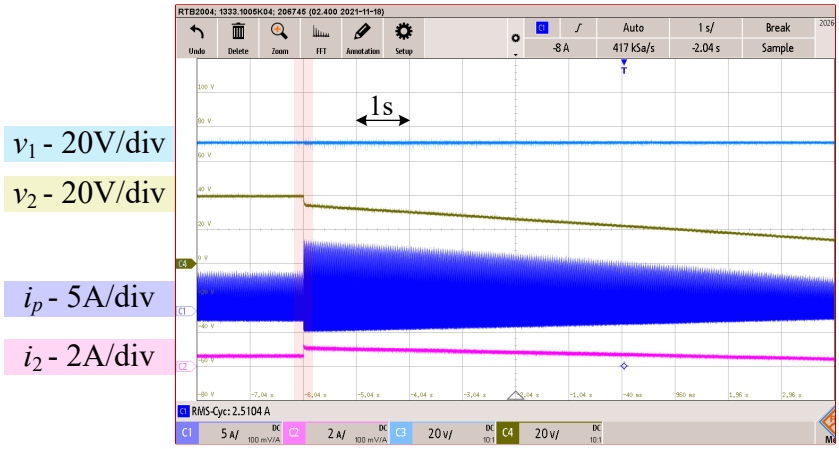

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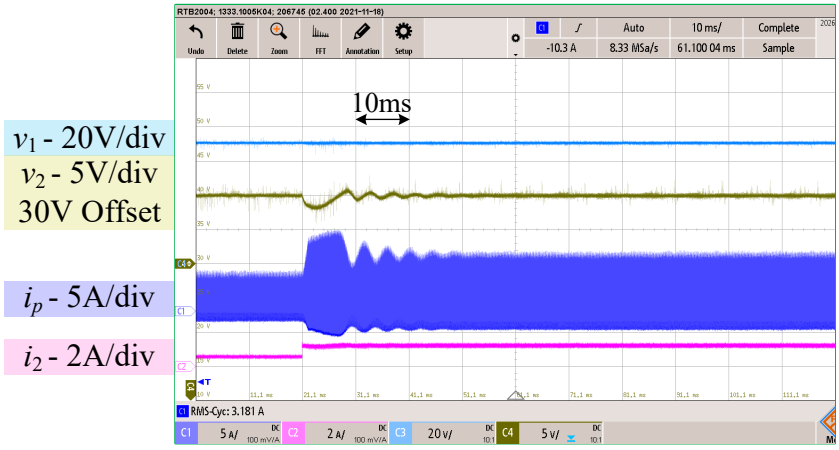

(**c**)

Figure 8. Dynamic comparison of the DAHB converter under a load step from 25% P_{rated} to 50% P_{rated}: (**a**) based on the traditional ESC with fixed phase shift angle saturation; (**b**) based on the traditional ESC with time-varying phase shift angle saturation; (**c**) based on the proposed EESC.

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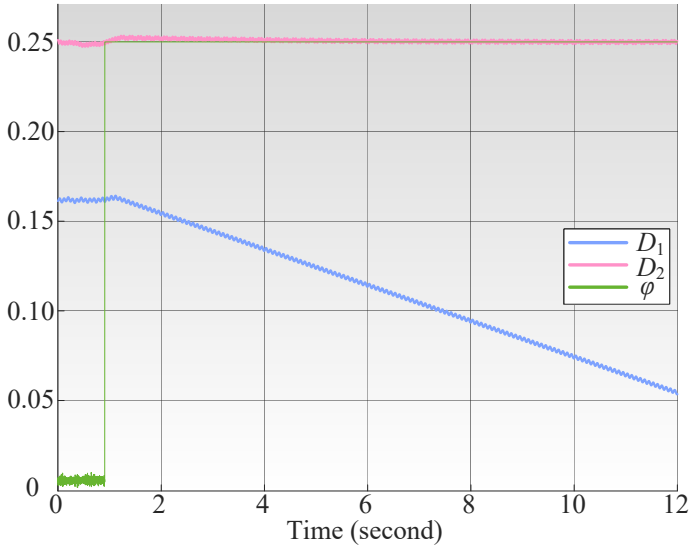
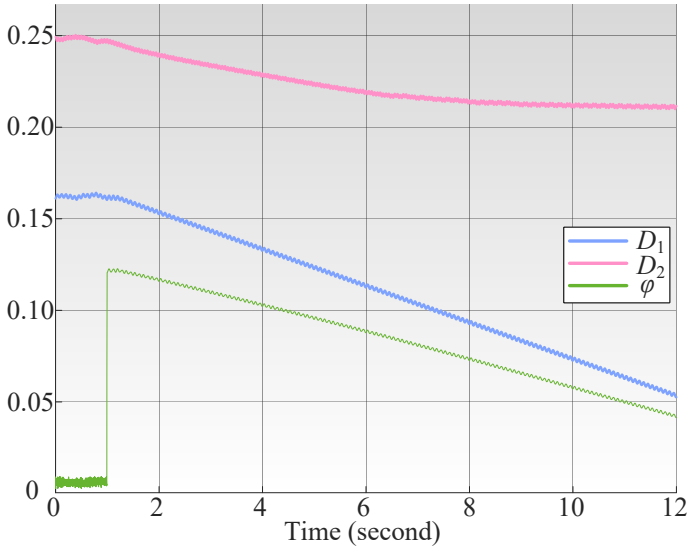
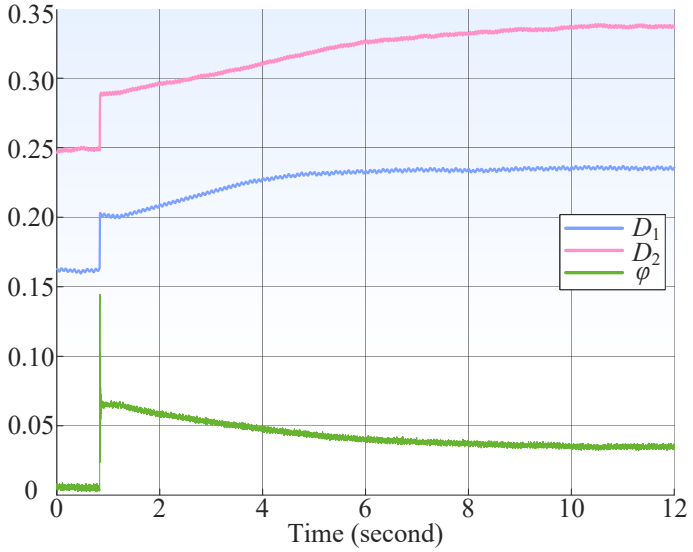


(**a**)



(**b**)



(**c**)

Figure 9. Trends of D_1, D_2, and ϕ during a load step from 25% P_{rated} to 50% P_{rated}: (**a**) based on the traditional ESC with fixed phase shift angle saturation; (**b**) based on the traditional ESC with time-varying phase shift angle saturation; (**c**) based on the proposed EESC.

 doi:10.20944/preprints202603.0464.v1

5. Conclusions

This paper reveals the phenomenon and underlying causes of dynamic output voltage collapse encountered by conventional extremum seeking control (ESC) under load transient conditions, using a DAHB converter as a representative example. To address this issue, an enhanced extremum seeking control (EESC) structure is proposed for dual-bridge converters, including DAHB and DAB converters. The EESC structure integrates two complementary mechanisms: a slow duty-cycle optimization aimed at minimizing the input current to improve converter efficiency, and a fast duty-cycle adjustment that rapidly responds to load transients by enhancing the power transfer capability. Theoretical analysis explains the coordination between these two control actions. Furthermore, comparative experimental results validate the output voltage collapse caused by the power transfer limitation of the conventional ESC and demonstrate that the proposed EESC not only eliminates output voltage collapse, but also preserves efficiency optimization during transient conditions.

Abbreviations

The following abbreviations are used in this manuscript:

DAB	Dual active bridge converter
DAHB	Dual active half-bridge converter
ESC	Extremum seeking control
EESC	Enhanced extremum seeking control
RMS	Root-mean-square

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