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Posted Date: 21 November 2025

doi: 10.20944/preprints202511.1641.v1

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Article

Universal Logic-In-Memory Gates using Reconfigurable Silicon Transistors

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Abstract

This study aims to implement universal logic gates using polarity control within a single silicon transistor structure. For this purpose, a reconfigurable transistor based on a p-i-n structure featuring two polarity gates (PGs) and one control gate was proposed, and its electrical characteristics and logic-in-memory (LIM) circuit operations were analyzed via two-dimensional technology computer-aided design simulations. The proposed device could be perfectly reconfigured into p-channel or n-channel modes because virtual doping effects could be induced according to the polarity of the PG voltage. Moreover, based on the positive feedback and latch-up phenomena, a steep subthreshold swing of approximately 1 mV/dec and a high ON/OFF current ratio of the order of 10^{10} were achieved. Building on these characteristics, we successfully verified NAND LIM operation in the p-channel mode and NOR LIM operation in the n-channel mode by connecting two of the proposed devices in parallel. The reconfigurable silicon transistor proposed in this study could perform both NAND and NOR LIM operations while sharing the same device structure and can be expected to play a key role in implementing high-density, low-power LIM systems in the future.

Keywords: polarity gate; control gate; universal logic-in-memory gate

1. Introduction

In modern computing, where data-intensive applications such as artificial intelligence and big data analytics are becoming increasingly important, the von Neumann architecture suffers from latency and high power consumption owing to frequent data transfers, resulting in a performance bottleneck [1]. This problem arises from the physical separation of the processor and memory inherent in the von Neumann architecture. Consequently, logic-in-memory (LIM) architectures have been explored [2–4]. LIM architectures enable both logic and memory operations within a single physical block, eliminating the need for frequent data movement and thereby improving computational speed and energy efficiency. This approach has garnered considerable attention as a promising strategy for next-generation, low-power, high-efficiency computing applications. Although various devices, such as resistive random-access memory and magnetic random-access memory, have been proposed for implementing LIM architectures, they suffer from high operating voltages and complex control mechanisms. Additionally, static random-access memory (SRAM)-based LIM structures offer the advantage of high-speed operation but are limited in terms of their integration density and leakage current [5,6]. Recently, feedback field-effect transistors (FBFETs) based on a positive-feedback mechanism have garnered attention as promising devices for LIM applications [7–10]. The positive-feedback mechanism controls the charge carrier injection according to the potential barrier, operating the device through the formation of a positive-feedback loop [11]. This mechanism enables FBFETs to achieve abrupt switching at low operating voltages while exploiting hysteresis characteristics for simultaneous memory operation [12–14]. Moreover, as shown in **Figure 1(a)**, the reconfigurable nature of the device—achieved by controlling the polarity of the

three gates—enables channel selection according to the majority carrier, making it suitable for LIM applications [15].

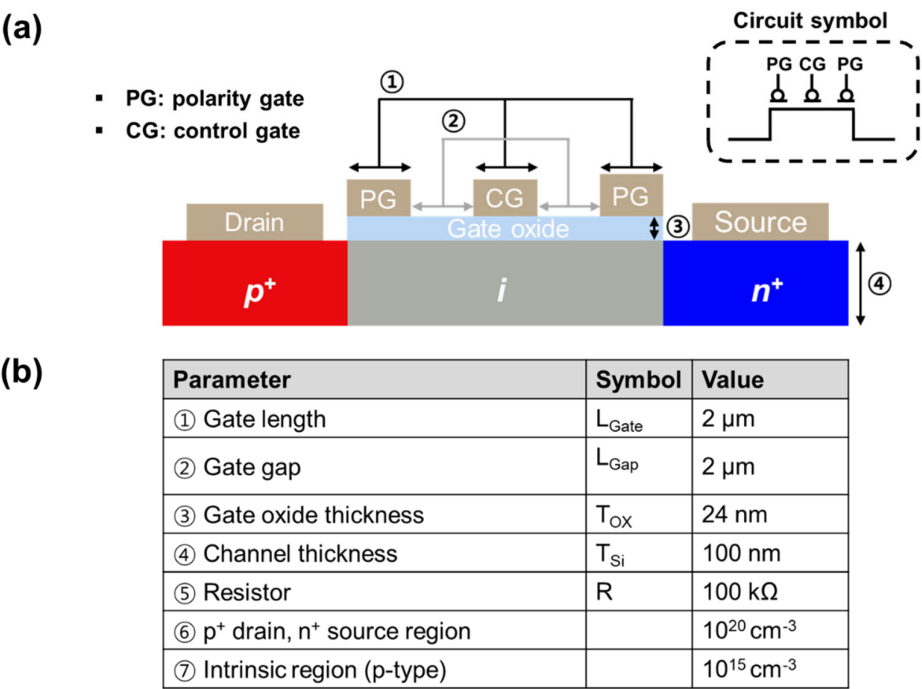


Figure 1. (a) Schematic cross-section and circuit symbols of the proposed reconfigurable silicon transistor. (b) Key structural and electrical parameters used in the TCAD simulation, including the gate length, oxide thickness, and doping concentrations.

In this study, we implemented NAND and NOR gates capable of simultaneous logic and memory operations using a three-gate transistor. The gates located at both ends of the transistor function as polarity gates (PGs) that determine the channel mode according to the polarity of the applied voltage. The centrally located gate serves as a control gate (CG), regulating the injection of charge carriers. The operation of the device is determined by the applied voltage. In p-channel mode, a positive voltage is applied to the drain, whereas in n-channel mode, a negative voltage is applied to the source. Using this operating scheme and configuring the transistor with a resistor in a pull-up and pull-down structure, logic functions, such as NAND and NOR, and memory operations can be simultaneously implemented within a single device.

2. Materials and Methods

The reconfigurable silicon transistor used in this study was based on a p-i-n structure, as illustrated in **Figure 1(a)**. It was fabricated on a p-type silicon substrate (doping concentration of 10¹⁵ cm⁻³) and featured a heavily doped p⁺ drain (10²⁰ cm⁻³), a heavily doped n⁺ source (10²⁰ cm⁻³), and an intrinsic silicon channel of thickness (T_{Si}) 100 nm. Two PGs and one CG were positioned on the gate oxide above the intrinsic channel. The gate oxide thickness (T_{ox}) was 24 nm. Both the gate length (L_{G}) for all gates and the gap between gates were 2 μm . Two-dimensional (2D) device simulations were performed using the Silvaco technology computer-aided design (TCAD) toolset to analyze the device characteristics. The device structure was generated using Silvaco Athena, and the electrical characteristics were simulated using Silvaco Atlas in mixed mode. The following physical models were employed in the simulations to ensure accuracy—that is, the Fermi-Dirac statistics [16] (Fermi), Lombardi mobility [17], parallel electric field dependence for high-field carrier velocity [18], bandgap

narrowing (BGN) [19], concentration-dependent Shockley–Read–Hall recombination, Auger recombination (Auger) [20], and Klaassen mobility [21] models.

3. Results and Discussion

Figure 2 illustrates a schematic of the device structure and energy-band diagrams for p-channel and n-channel operations, depending on the majority of the carriers. The transistor proposed in this study controls the ON/OFF behavior of the device by adjusting the potential barrier height of the charge using three gate voltages. In the OFF state, a potential barrier is formed for both electrons and holes, which inhibits the current flow. Conversely, in the ON state, this barrier is lowered, injecting electrons and holes into the channel region, and the interaction between them creates a positive-feedback loop. Additionally, the device can select the majority carriers as electrons or holes, depending on the voltage of the two PGs, enabling n-channel and p-channel operations, respectively.

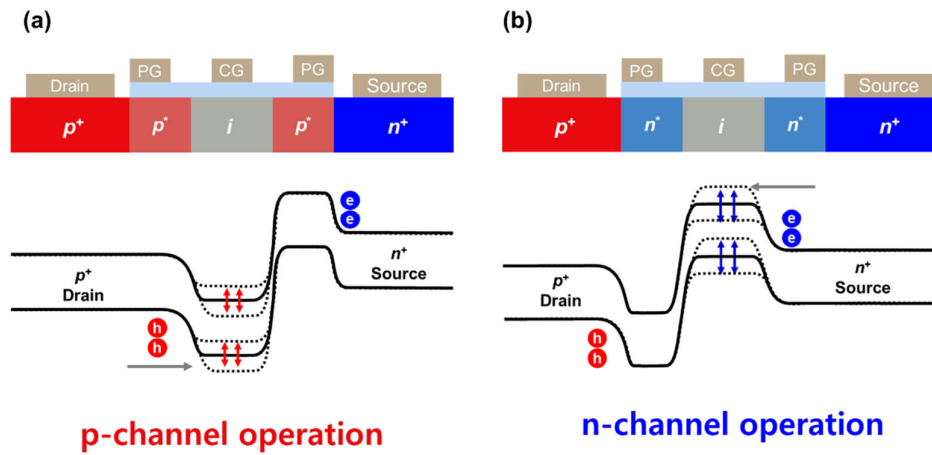


Figure 2. Operating mechanism of the reconfigurable transistor based on the voltage applied to V_{PG} , with device structure and energy-band diagrams for the (a) p-channel and (b) n-channel operations.

When a negative voltage is applied to V_{PG} ($V_{PG} < 0$), the lower energy band rises, resulting in the same effect as virtual p⁺-type doping of the area. Moreover, a potential barrier is formed for the hole, which inhibits its injection into the channel. As the voltage of the V_{CG} is swept from positive to negative, the hole barrier gradually decreases, and holes are injected from the drain into the channel area, accumulating in the potential well. Consequently, the potential barrier to electrons is lowered, and electrons are injected into the channel, resulting in p-channel behavior, in which holes are the majority carriers.

Conversely, when a positive voltage ($V_{PG} > 0$) is applied to V_{PG} , the energy band in the region decreases, inducing a virtual n-type doping effect. Consequently, a potential barrier is formed for the electrons, which inhibits their injection. When V_{CG} is swept from negative to positive, electrons are injected into the channel and accumulate in the potential well, decreasing the electron barrier. The hole barrier is then lowered and holes are injected, resulting in n-channel behavior, in which electrons are the majority carriers.

Figures 3(a) and 3(b) show the I_{DS} characteristics of V_{DS} in the n-channel and p-channel operations. Applying -3 V to V_{PG} results in the device being virtually doped as p⁺- p⁺- i- p⁺- n⁺. The potential barrier formed by the applied voltage prevents the injection of holes and electrons into the channels. In this configuration, sweeping V_{DS} from 0 to 5 V reduces the potential barrier for holes in the drain region. The injected holes accumulate in the potential well, lowering the potential barrier for electrons. This process initiates a positive-feedback loop, leading to an abrupt turn-on and latch-up.

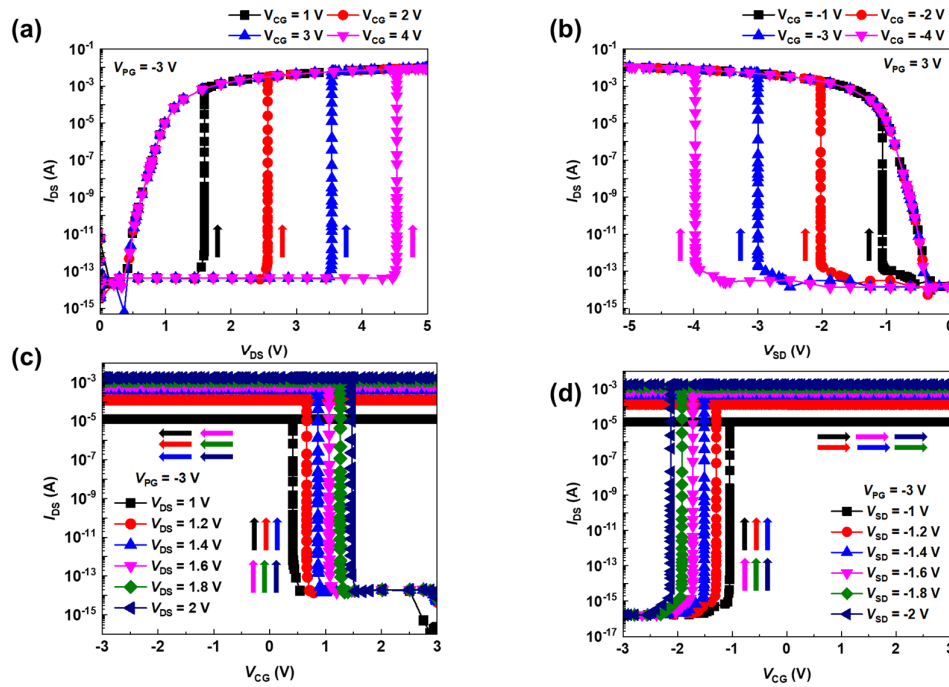


Figure 3. Electrical characteristics of the transistor: output characteristics for the (a) p-channel and (b) n-channel under different control gate voltages, and transfer characteristics for the (c) p-channel and (d) n-channel as a function of the drain–source voltage.

As shown in **Figure 3(a)**, varying V_{CG} from 1 to 4 V results in latch-up voltages of approximately 1.5, 2.5, 3.5, and 4.5 V, respectively. **Figure 3 (b)** shows a device virtually doped with $p^+ - n^* - i - n^* - n^+$ when 3 V is applied to V_{PG} . Sweeping V_{SD} from 0 to -5 V lowers the potential barrier for electrons in the source region, facilitating electron injection into the channel. These injected electrons accumulate in the potential well, thereby reducing the potential barrier for holes. Consequently, a positive-feedback loop is formed, leading to abrupt switching and latch-up behavior. The latch-up voltage increases with V_{CG} and was observed to be approximately -1 , -2 , -3 , and -4 V, respectively.

Figures 3 (c) and 3(d) show the I_{DS} characteristic according to V_{CG} for the p-channel and n-channel operations of the transistor, respectively. The two graphs show that the steep switching of the device and clear separation of the ON and OFF states are bistable. **Figure 3(c)** shows the I_{DS} transfer characteristics as a function of V_{CG} in the p-channel mode with V_{PG} fixed at -3 V. As V_{CG} decreases from 3 to -3 V, the potential barrier in the drain region initially suppresses hole injection, but the barrier is lowered with increasing V_{CG} , injecting holes into the channel region. Consequently, a positive-feedback loop is formed, leading to abrupt switching behavior with a subthreshold swing (SS) of approximately 1 mV/dec and an ON/OFF current ratio of the order of 10^{10} .

Figure 3(d) illustrates that, in n-channel mode, the device turns on more rapidly as V_{DS} increases. This behavior can be attributed to enhanced electron injection, which facilitates internal potential changes and, in turn, promotes more rapid formation of the feedback loop. Under these conditions, the ON/OFF current ratio exceeds 10^{10} , and the SS is below 1 mV/dec.

Figure 4(a) shows the NAND circuit constructed using two reconfigurable silicon transistors in a parallel configuration and a pull-down resistor. A common voltage of -3 V was applied to the PGs of both transistors to set them to operate in p-channel mode. To receive external inputs, the CG of the left transistor is defined as V_{IN1} , and the V_{CG} of the right transistor is defined as V_{IN2} . Voltage (V_{DD}) is applied to the drain side of the parallel transistor. The operation of the circuit is determined by the positive-feedback mechanism within the transistors.

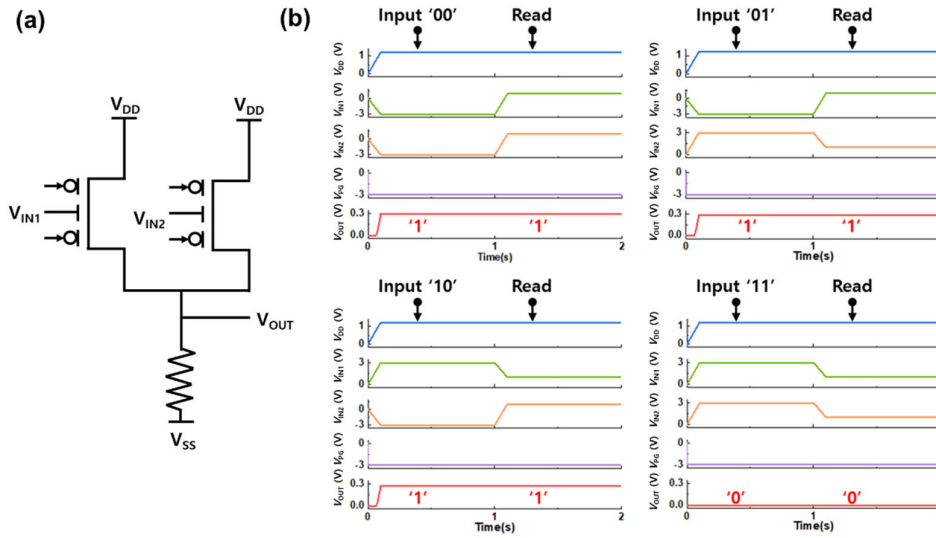


Figure 4. (a) Logic circuit diagram composed of two reconfigurable silicon transistors and a pull-down resistor. (b) AC simulation waveforms verifying the NAND LIM gate operation, showing the output signal V_{OUT} in response to the input signals V_{IN1} and V_{IN2} .

The AC simulation waveforms verified the NAND LIM operation, as shown in **Figure 4(b)**. When the voltage polarities of V_{PG} and V_{CG} are the same (e.g., $V_{PG} < 0$ and $V_{CG} < 0$), positive feedback is activated. If feedback is activated in at least one of the two transistors, the positive voltage V_{DD} applied to the drain side is transferred to the output terminal V_{OUT} , resulting in a positive output signal. This state is defined as logic “1.” Conversely, if the polarities of V_{PG} and V_{CG} are different for both transistors (e.g., $V_{PG} < 0$ and $V_{CG} > 0$), the feedback is deactivated. In this case, the V_{DD} voltage is blocked, and the circuit is pulled to the ground state by the pull-down resistor, resulting in an output of 0 V at V_{OUT} . This state is defined as logic “0.” The logical operation of the circuit corresponds to the truth table of the NAND gate. Based on the provided voltage conditions, a negative input (V_{IN}) is defined as logic “0” (–3 V), and a positive input is defined as logic “1” (3 V). A positive output (V_{OUT}) is defined as logic “1,” and an output of 0 V is defined as logic “0.” For input ‘00’ ($V_{IN1} = -3$ V, $V_{IN2} = -3$ V), the polarities of V_{PG} ($V_{PG} < 0$) and V_{CG} ($V_{CG} < 0$) are the same for both transistors, so the positive feedback is ON. Therefore, V_{DD} is transferred to V_{OUT} , resulting in a positive output (logic “1”). For input ‘01’ ($V_{IN1} = -3$ V, $V_{IN2} = 3$ V), the polarities of V_{PG} ($V_{PG} < 0$) and V_{CG} ($V_{CG} < 0$) are the same in the left transistor, so the feedback is ‘ON,’ and V_{OUT} is positive (logic “1”). Similarly, for input ‘10’ ($V_{IN1} = 3$ V, $V_{IN2} = -3$ V), the polarities of V_{PG} ($V_{PG} < 0$) and V_{CG} ($V_{CG} < 0$) are the same in the right transistor, activating the feedback and resulting in a positive output (logic “1”). Finally, for input ‘11’ ($V_{IN1} = 3$ V, $V_{IN2} = 3$ V), the polarities of V_{PG} ($V_{PG} < 0$) and V_{CG} ($V_{CG} > 0$) are different for both transistors, so the feedback is ‘OFF.’ Consequently, V_{DD} is blocked, and V_{OUT} is 0 V (logic “0”).

The NOR circuit was constructed using two reconfigurable silicon transistors and one pull-up resistor, as shown in **Figure 5(a)**. A common voltage of 3 V was applied to the PGs of both transistors to set them to operate in n-channel mode. The V_{CG} of the left transistor is defined as V_{IN1} , and the V_{CG} of the right transistor is defined as V_{IN2} to receive external inputs. The operation of the circuit is determined by the positive-feedback mechanism within the transistors.

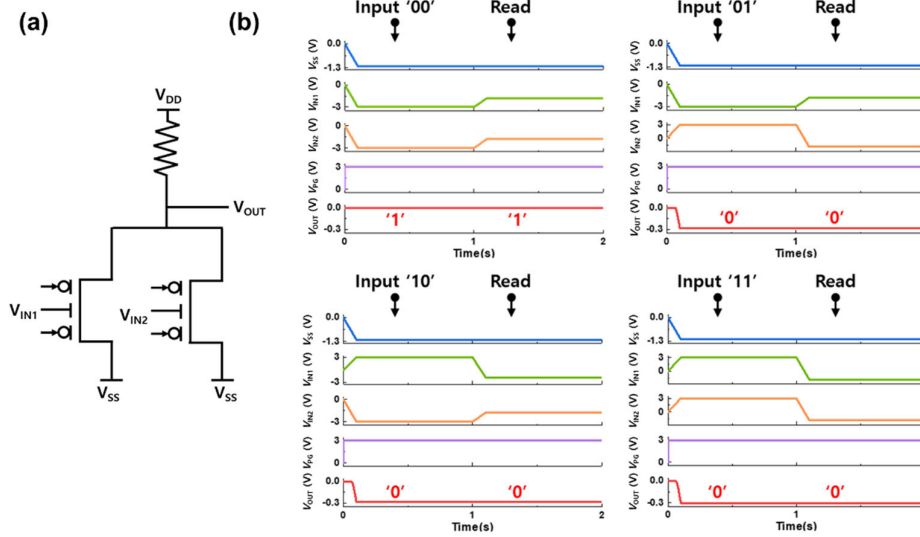


Figure 5. (a) Logic circuit diagram composed of two reconfigurable silicon transistors and a pull-up resistor. (b) AC simulation waveforms verifying the NOR LIM operation, showing the output signal V_{OUT} in response to the input signals V_{IN1} and V_{IN2} .

Figure 5(b) shows the AC simulation waveforms, which validate the operation of the NOR LIM. When the voltage polarities of V_{PG} and V_{CG} are the same (e.g., $V_{PG} > 0$ and $V_{CG} > 0$), positive feedback is activated. If feedback is activated in at least one of the two transistors, the negative voltage V_{SS} applied to the source side is transferred to the output terminal V_{OUT} , resulting in a negative output signal. This state is defined as logic “0.” Conversely, if the polarities of V_{PG} and V_{CG} are different for both transistors (e.g., $V_{PG} > 0$ and $V_{CG} < 0$), the feedback is deactivated. In this case, the V_{SS} voltage is blocked, and the circuit goes to the ground state, resulting in an output of 0 V at V_{OUT} . This state is defined as logic “1.”

Figure 5(b) shows the AC simulation results used to verify the logical operation of the circuit. A negative input (V_{IN}) is defined as logic “0,” and a positive input is defined as logic “1.” A negative output (V_{OUT}) of -0.3 V is defined as logic “0,” and an output of 0 V is defined as logic “1.” The simulation results were consistent with the NOR gate truth table. For input ‘00’ ($V_{IN1} = -3$ V, $V_{IN2} = -3$ V), the polarities of V_{PG} ($V_{PG} > 0$) and V_{CG} ($V_{CG} < 0$) are different for both transistors, so the positive feedback is ‘OFF,’ resulting in V_{OUT} being 0 V (logic “1”). For input 01 ($V_{IN1} = -3$ V, $V_{IN2} = 3$ V), the polarities of V_{PG} ($V_{PG} > 0$) and V_{CG} ($V_{CG} > 0$) are the same in the right transistor, so the feedback is ‘ON,’ and V_{OUT} is approximately -0.3 V (logic “0”). Similarly, for input 10 ($V_{IN1} = 3$ V, $V_{IN2} = -3$ V), the polarities of V_{PG} ($V_{PG} > 0$) and V_{CG} ($V_{CG} > 0$) are the same in the left transistor, activating feedback and resulting in V_{OUT} being approximately -0.3 V (logic “0”). Finally, for input ‘11’ ($V_{IN1} = 3$ V, $V_{IN2} = 3$ V), the polarities of V_{PG} ($V_{PG} > 0$) and V_{CG} ($V_{CG} > 0$) are the same for both transistors, so the feedback is ‘ON,’ and V_{OUT} is approximately -0.3 V (logic “0”).

4. Conclusions

In this study, we demonstrated a reconfigurable silicon transistor based on a p-i-n structure, aimed at implementing an LIM architecture to overcome the limitations of the von Neumann structure, and verified its superior characteristics using 2D TCAD simulations. The proposed device could be perfectly reconfigured into p-channel and n-channel modes solely by controlling the polarity of the PG voltage. This reconfigurable operation provided hardware-level flexibility, which reduced the circuit complexity and improved the integration density. Moreover, based on the positive feedback and latch-up phenomena, the device achieved a steep SS of approximately 1 mV/dec and a high ON/OFF current ratio of the order of 10^{10} , signifying that a clear switching operation was

possible under ultralow power conditions. Building on these characteristics, we successfully implemented a universal logic gate by connecting two identical devices in parallel, demonstrating NAND LIM operation in p-channel mode and NOR LIM operation in n-channel mode within a single-device structure. In conclusion, the proposed device is highly suitable for LIM operations and enables computational and memory functions without requiring data movement. It provides a universal gate that is hardware-reconfigurable and possesses ultralow-power switching characteristics. The findings of this study are expected to contribute to the core device technology for future high-density, low-power next-generation computing systems.

Author Contributions: Conceptualization, S. H.; Methodology, S. H., N. H., and Y. Y.; Validation, S. H., N. H., and Y. Y.; Formal Analysis, S. H., N. H., and Y. Y.; Investigation, S. H., N. H., and Y. Y.; Writing—Original Draft, S. H. and N. H.; Writing—Review and Editing, D. L.; Visualization, S. H., N. H., Y. Y., and D. L.; Supervision, D. L.; Project Administration, D. L. All authors have read and agreed to the published version of this manuscript.

Funding: This work was supported by the Korea Collaborative & High-Tech Initiative for Prospective Semiconductor Research (1415187357, RS-2023-00230336, 23004-15TC) funded by the Ministry of Trade, Industry, and Energy (MOTIE, Korea) and a National Research Foundation of Korea (NRF) grant funded by the Korean Government (MSIT) (Grant No. RS-2023-00217791).

Data Availability Statement: Data are contained within the article

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

BGN	Bandgap narrowing
CG	Control gate
FBFET	Feedback field-effect transistor
LIM	Logic-in-memory
PG	Polarity gate
SS	Subthreshold swing
TCAD	Technology computer-aided design

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