Review

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A Review of Double Pulse Test Techniques for GaN Power Devices in High-Frequency Power Converters

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Abstract

The growing demand for high-efficiency, high-power-density converters in data centers, electric vehicle chargers, and renewable energy systems has accelerated the adoption of wide bandgap (WBG) devices. Gallium nitride (GaN) transistors offer superior switching speed, lower losses, and higher power density compared with Silicon (Si) devices. Accurate characterization of GaN switching dynamics is essential due to parasitic effects and transient phenomena affecting performance and reliability. The Double Pulse Test (DPT) is widely used to quantify critical parameters, including switching energy losses, dynamic $R_{DS(on)}$ and transient voltage and current waveforms. This paper reviews DPT techniques for GaN devices, focusing on measurement methodologies, parasitic mitigation, and reliability considerations, providing practical guidance for optimizing high-frequency GaN-based power converters.

Keywords: wide bandgap semiconductors; Gallium Nitride (GaN); high-efficiency power conversion; switching speed; thermal management; reliability; GaN HEMTs; power electronics; double pulse test

1. Introduction

The demand for highly efficient and compact power conversion systems continues to increase with the rapid growth of applications such as data center power supplies, electric vehicle charging infrastructure, renewable energy systems, and telecommunication equipment [1,2]. In these applications, improving converter efficiency while reducing system size and weight has become a primary design objective [3]. Increasing the switching frequency of power converters is an effective strategy for achieving higher power density, as it allows the use of smaller passive components and enhances the system's dynamic performance [2]. However, the performance of conventional silicon (Si) power devices is limited under high-frequency switching conditions due to relatively large switching losses and material constraints [3]. Wide bandgap (WBG) semiconductors, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), have therefore attracted significant attention for next-generation power electronic systems. GaN power transistors provide superior switching performance due to their high electron mobility (μ_n), large critical electric field (E_c), and low parasitic capacitances whereas SiC devices are better suited for high-voltage applications because of their high thermal conductivity (λ) and strong material robustness [4]. These characteristics allow GaN devices to operate at significantly higher switching frequencies with reduced switching losses compared with traditional silicon (Si) devices, making them suitable for high-efficiency and high-power-density converter applications [5,6]. The very fast switching transitions of GaN devices, however, introduce challenges in accurately evaluating their dynamic performance [5]. High dv/dt and di/dt during switching can interact with parasitic inductances and capacitances in the test circuit, which may cause

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voltage overshoot, current oscillation, and measurement uncertainty [7]. For this reason, reliable experimental techniques are required to characterize the switching behavior of GaN power devices under controlled conditions [8]. Double Pulse Test (DPT) has become a widely accepted method for analyzing the switching characteristics of power semiconductor devices [9]. By generating two controlled switching pulses, this technique allows the evaluation of Turn-on (T_{ON}) and Turn-off (T_{OFF}) behavior, switching energy losses (E_{SW}), and dynamic device characteristics [10,11]. Consequently, DPT plays an important role in the experimental investigation and design optimization of GaN-based high-frequency power converters [12,13]. This paper reviews DPT techniques used for the switching characterization of GaN power transistors and discusses key considerations related to test circuit configuration, switching performance evaluation, and measurement reliability [14,15].

In GaN power transistors, charge trapping effects represent a critical phenomenon that directly influences the dynamic electrical characteristics of the device shown in Figure 1 [16–19]. Due to the heterostructure nature of GaN-based high-electron-mobility transistors (HEMTs), various trap states can exist at the surface, within the buffer layer, or at material interfaces [17–20]. During device operation, particularly under high drain bias and switching conditions, electrons can be captured by these trap states, leading to a redistribution of the internal electric field within the device structure. The presence of trapped charges reduces the density of the two-dimensional electron gas (2DEG) channel that is responsible for current conduction [19–21]. As a result, channel conductivity temporarily degrades, producing an increase in the effective ON-state resistance during dynamic operation. This phenomenon, commonly referred to as current collapse, has been widely reported as a key reliability and performance concern in GaN power devices. The magnitude of the trapping effect depends strongly on operating conditions such as drain bias voltage, switching frequency, temperature, and device architecture [2,22]. Under practical switching conditions, these trap-related mechanisms can significantly influence dynamic parameters including dynamic on resistance ($R_{DS(on)}$), switching transition behavior, and conduction losses. In high-frequency power converters, an increase in dynamic ON-state resistance caused by trapping can lead to additional power dissipation and reduced converter efficiency [23]. Therefore, the dynamic behavior of GaN devices under realistic switching conditions including effects from electron trapping, parasitic capacitances, and switching losses have become essential for advancing modern power electronics. Pulse-based experimental techniques are extensively utilized to characterize transient phenomena, owing to their capability to accurately capture switching behavior while suppressing the effects of device self-heating [21,24].

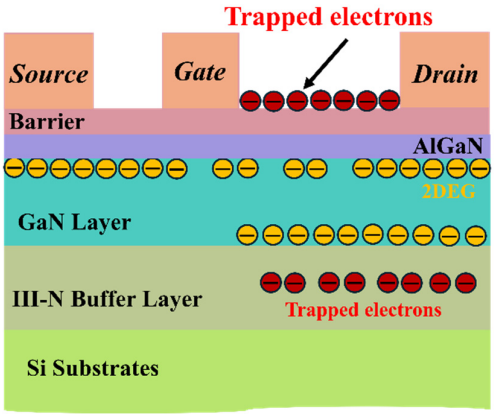

Figure 1. Electron Trapping Effects and Charge Accumulation in GaN Power Device.

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2. Double Pulse Test (DPT)

The DPT is a standard experimental technique used to evaluate the dynamic switching performance of power semiconductor devices, particularly GaN transistors, under realistic operating conditions in Figure 2. In this method, two consecutive gate pulses are applied to the device under test (DUT) [20,21]. The first pulse is applied to establish the required current in the inductive load, whereas the second pulse is used to initiate the switching transient for detailed characterization and analysis. This method allows precise observation of both T_{ON} and T_{OFF} switching events while reducing the impact of device self-heating [22]. During the test, high-bandwidth measurements of drain-source voltage (V_{DS}) and drain current (I_{DS}) are captured to analyze transient switching behavior [20]. From these waveforms, key parameters such as switching energies (E_{ON} and E_{OFF}), rise (t_r) and fall (t_f) times, dynamic $R_{DS(on)}$, voltage overshoot, and switching rates (dv/dt and di/dt) can be extracted [23]. The technique also allows the observation of threshold voltage (V_{TH}) variations under fast switching conditions. Because GaN devices operate with extremely fast switching speeds, precise characterization of transient effects is essential [24]. The DPT provides controlled conditions for analyzing these high-speed transitions and for evaluating the influence of parasitic elements in the gate and power loops [22,25]. Therefore, it is widely used for device characterization and for optimizing the design of high-frequency, high-efficiency power converters [20,23,26]

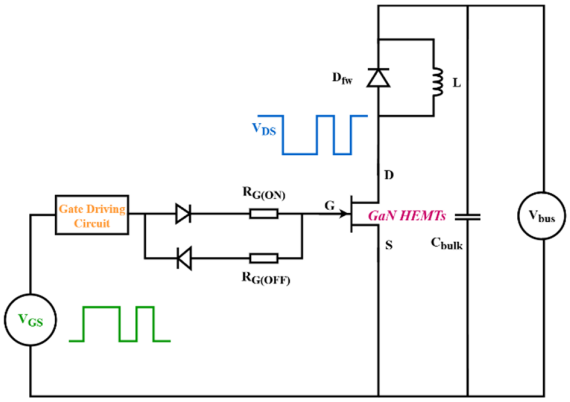

Figure 2. Schematic of the Double Pulse Test circuit with GaN HEMTs.

2.1. Waveform Responses in Double Pulse Testing

The dynamic behavior of the GaN device during the DPT can be systematically interpreted by examining the current flow and switching waveforms at three critical instants: t_0, t_1, and t_2. These time instants represent the temporal evolution of the first pulse and serve to establish the initial electrical conditions governing the subsequent switching transition.

A. Switching Response at t_0 (Initial Turn-ON Transition)

At time t_0, the gate driver applies a positive gate–source voltage V_{GS}, initiating the turn-on of the GaN HEMTs in Figure 3. As the device enters conduction, the drain–source voltage V_{DS} rapidly decreases from the DC bus voltage V_{bus} toward its low on-state value [26]. Simultaneously, the inductor current I_L begins to increase linearly, governed by the applied voltage across the inductance. During this interval, the freewheeling diode (D_{fw}) remains reverse-biased, and current flows entirely through DUT [24,26]. The rate of change of current di/dt is determined by the inductance and applied voltage, while the voltage transition dv/dt is influenced by intrinsic capacitances C_{GD}, C_{GS}, C_{DS} and parasitic elements in the loop [2,20]. This instant captures the initial switching transient, where displacement currents through parasitic capacitances and gate-drain coupling effects dominate [15,17]. Any existing trapped charges or interface states may begin to influence the channel formation, affecting the early-stage conduction behavior [19].

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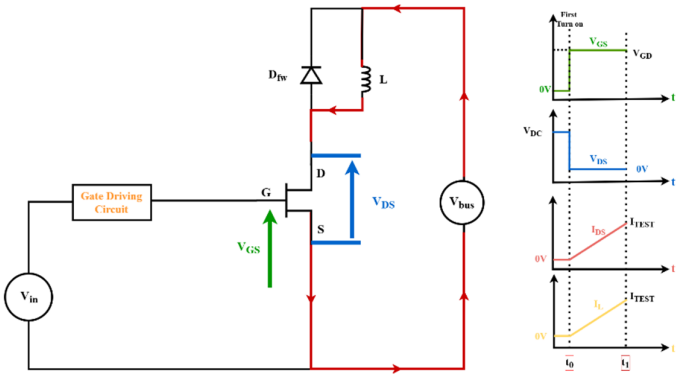

Figure 3. Turn-ON initiation of the GaN HEMTs at t_0 during the 1st pulse, showing initial current conduction and rapid V_{DS} transition.

B. Switching Response at t_1 (Current Build-Up and Steady Conduction)

At t_1, the device is fully enhanced, and V_{DS} stabilizes at its on-state voltage. The inductor current continues to rise linearly, reaching the predefined test current level I_{TEST}. The current path remains through DUT, with negligible contribution from the freewheeling diode. In this region, the switching transition is complete, and the system operates in a quasi-steady conduction state [22,25,26]. The slope of I_L remains constant, indicating that the applied voltage across the inductor is stable in Figure 4. The influence of parasitic inductances becomes less pronounced, while conduction characteristics such as on-resistance begin to dominate [18]. This interval establishes the initial current condition required for the second pulse. Additionally, any dynamic effects such as charge trapping during the transient turn-on may modify effective channel conductivity, influencing the subsequent switching behavior [10,14].

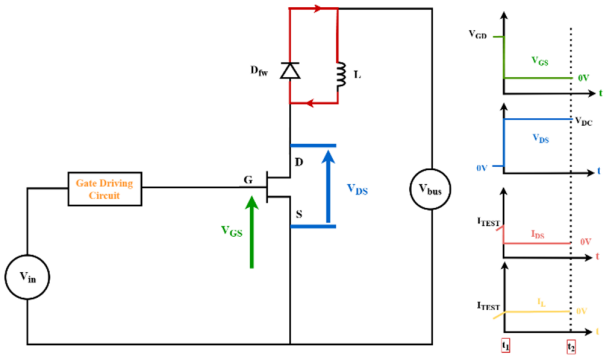

Figure 4. Current build-up and steady conduction at t_1, illustrating linear inductor current increase and stabilized on-state operation.

C. Switching Response at t_2 (Turn-OFF Transition and Energy Dissipation)

At t_2, the V_{GS} is reduced below the threshold level, initiating device turn-off in Figure 5. The channel conductivity collapses, causing the drain–source voltage to rise rapidly toward V_{bus}. Due to the energy stored in the inductance, the current cannot change instantaneously and is commuted to the freewheeling diode [23]. The overlap of rising voltage and falling current produces switching loss, which is a critical parameter extracted from DPT measurements [23,26]. High dv/dt and di/dt during this interval interact with parasitic elements, resulting in voltage overshoot and oscillatory behavior. This interval therefore defines the device's turn-off energy, transient stress limits, and susceptibility to electromagnetic interference.

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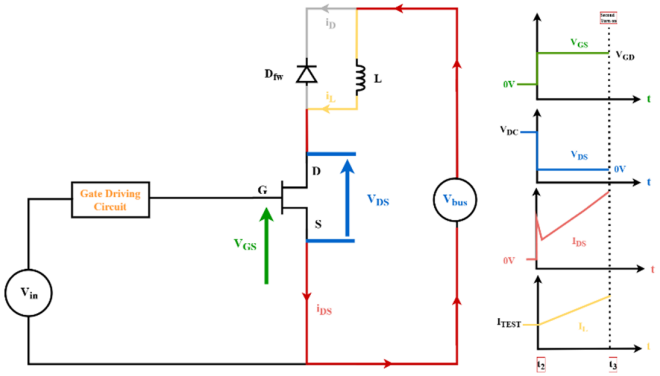

Figure 5. Turn-off transition at t_2, showing current commutation to the freewheeling diode and rapid rise of V_{DS}.

D. Interpretation of the Complete DPT Waveform

The complete DPT waveform represents a controlled switching sequence consisting of an initial current buildup stage followed by subsequent switching transitions, as illustrated in Figure 6 [27–29]. During the first pulse, the inductor current is established under well-defined electrical conditions. The second pulse then allows precise characterization of the device turn-on and turn-off transients at a predetermined current level [27]. The measured waveforms of V_{DS}, I_D, and V_{GS} allow direct extraction of switching energy, transient dynamics, and the impact of parasitic elements [28]. By correlating measured waveforms with circuit operating conditions, DPT separates intrinsic device behavior from external parasitic effects, enabling accurate assessment of GaN switching performance [29].

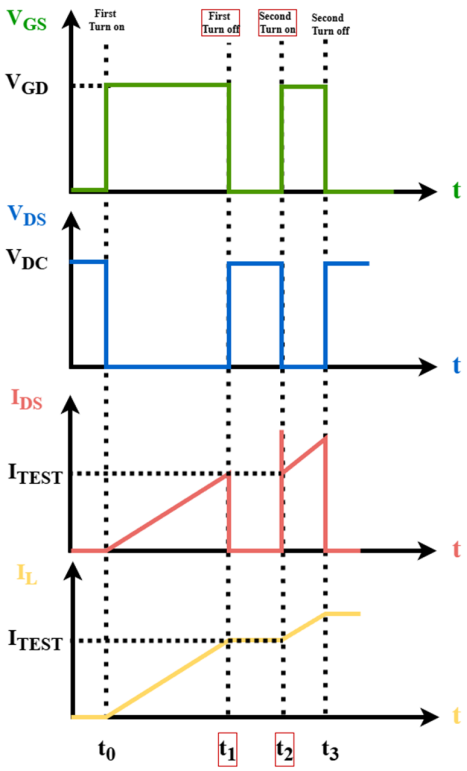

Figure 6. Ideal switching waveforms in a single-launch DPT GaN HEMTs.

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2.2. First Pulse (T_1): Current Initialization and Preconditioning

The T_1, a positive gate–source voltage V_{GS} is applied by the gate driver, turning the GaN HEMTs into the ON-state [28]. As illustrated in Figure 3, the device conducts, allowing the DC bus voltage V_{bus} to be imposed across the inductive load L, which results in a linear increase in the inductor current I_L [29]. In this interval, the freewheeling diode D_{fw} remains reverse-biased, and the drain–source voltage V_{DS} collapses to its low on-state value [28]. The primary function of the first pulse is to establish a well-defined current level required for the subsequent switching event. The current rise is governed by the applied voltage and inductance, while the voltage transition is influenced by the charging dynamics of the intrinsic capacitances C_{GD}, C_{GS}, C_{DS} [29]. The interaction between high dv/dt and parasitic inductances introduces non-ideal effects such as voltage ringing and transient oscillations [30]. To minimize self-heating while ensuring stable current initialization, the duration of T_1 is kept sufficiently short. For typical 650 V GaN devices, the pulse width is selected in the range of 10-50 ns, depending on gate driver capability, external gate resistance, and circuit parameters [31]. During this interval, key electrical quantities including I_D, V_{DS}, dv/dt, and di/dt are monitored to assess the initial switching response [26]. In addition to current establishment, the first pulse provides insight into early-stage dynamic effects. Charge trapping at surface or buffer-related states may alter the channel conductivity, leading to variations in the effective on-state resistance [32,33]. These effects influence the initial conditions of the second pulse and must be considered for accurate interpretation of switching performance [33].

2.3. Second Pulse (T_2) – Full Switching Observation

The second pulse is applied after the inductor current reaches the specified level, allowing accurate characterization of turn-on and turn-off transients under controlled operating conditions [12,13,21]. During the transition, rapid variations in $V_{DS}(t)$ and $I_D(t)$ produce a temporal overlap that defines the switching energy. The corresponding losses, E_{ON} and E_{OFF} are obtained by integrating the instantaneous power over the switching interval [10,12]. For typical 650V GaN devices at moderate current levels, switching energies are in order of tens of microjoules, with rise and fall times spanning a few to several tens of nanoseconds [5,22,26]. The high dv/dt inherent to fast switching operation improves conversion efficiency but simultaneously exacerbates the influence of parasitic inductances and capacitances, resulting in voltage overshoot and oscillatory ringing. Consequently, careful circuit design and optimized layout are essential to limit transient voltage stress. This switching interval further reveals dynamic phenomena not observable under steady-state conditions. Charge trapping and de-trapping effects induce variations in $R_{DS\,(on)}$ and V_{TH}, which critically affect transient behavior as well as long-term device reliability [29,30].

2.4. Switching Time and Energy Loss

This parameter describes the transient switching behavior in terms of rise and fall times and the corresponding voltage and current slew rates, which directly govern switching energy dissipation. These transitions are defined by finite voltage and current slopes determined by device capacitances and external parasitic elements. Switching energy is obtained from the instantaneous power overlap of voltage and current during the switching interval. The turn-on and turn-off energies are calculated as the time integral of instantaneous power over the respective switching transitions are given by

$$E_{ON} = \int_{t_{on}} V_{DS}(t)\, I_D(t)\, dt$$

$$E_{OFF} = \int_{t_{off}} V_{DS}(t)\, I_D(t)\, dt$$

The total switching energy per cycle and corresponding power loss are

$$E_{SW} = E_{ON} + E_{OFF}, P_{SW} = f_s \cdot E_{SW}$$

where f_s is the switching frequency. These formulations are widely adopted in high-speed switching characterization of GaN devices under DPT conditions [21,24,25].

The current transition is primarily limited by the external inductance L, yielding

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$$\frac{dI_D}{dt} \approx \frac{V_{bus}}{L}$$

while the voltage transition is dominated by the charging and discharging of the nonlinear device capacitances. The effective slope can be approximated as

$$\frac{dV_{DS}}{dt} \approx \frac{I_G}{C_{eq}}$$

where C_{eq} represents the combined effect of C_{GS}, C_{GD}, and C_{DS}. In particular, the Miller capacitance C_{GD} plays a dominant role during the plateau region, limiting the rate of voltage change [21,34].

Figure 7 illustrates the typical switching waveforms of a GaN HEMTs and defines the key timing intervals used for extracting switching losses. The turn-on transition starts when the gate–source voltage V_{GS} exceeds the threshold voltage, leading to an increase in drain current I_D with a defined current slope [24]. During this current-rise phase, the drain-source voltage V_{DS} remains close to the bus voltage. Once I_D reaches the load current, the voltage fall commences, limited by the gate current charging the Miller capacitance C_{GD} [22]. The overlap between V_{DS} and I_D during intervals t_r (current rise) and t_f (voltage fall) determines the turn-on energy E_{ON} [24,25]. In turn-off, V_{GS} falls to the Miller plateau, the voltage rises as C_{GD} is discharged, and subsequently the current falls. The overlap during voltage rise and current fall gives E_{OFF}. The Figure 7 also indicates the 10% and 90% points conventionally used to define transition durations, ensuring consistent comparison. Notably, parasitic inductance in the commutation loop causes voltage overshoot at turn-off, visible as a spike superimposed on V_{DS} when di/dt is high. This overshoot, increases stress and may elevate switching loss due to ringing [25].

$$V_{overshoot} \approx Lp \cdot \frac{dI}{dt}$$

Therefore, Figure 7 reinforces that accurate loss extraction requires careful identification of the overlap intervals, and that measured switching energy inherently includes the influence of parasitics and gate drive conditions.

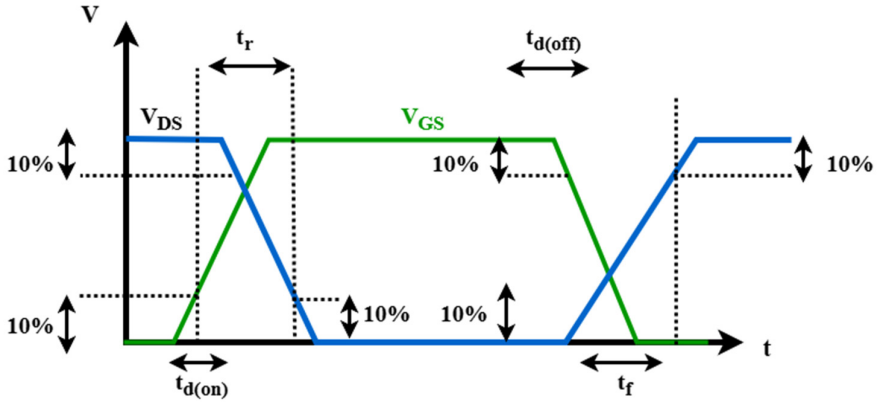

Figure 7. Waveforms and positions of switching times extractions of GaN HEMTs.

Table 1 presents the test conditions used in DPT studies to evaluate the switching performance of GaN devices. The reviewed devices include E-mode and p-GaN HEMTs, GaN GITs, and other GaN configurations, with voltage ratings from 80 V to 650 V. Key parameters such as switching time, energy loss, and gate charge are measured under different operating conditions [34,35]. The main variables investigated are gate resistance, gate-source voltage, DC bus voltage, load current, and temperature. In most studies, load current and DC voltage are varied to analyze their effect on switching energy, while temperature is considered to assess thermal dependence. However, some works do not fully report gate conditions, leading to variations in comparison [35]. Overall, the table highlights the common use of DPT for switching analysis and the influence of test parameters on device performance.

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Table 1. Test Conditions of Reviewed Double Pulse Tests for Switching Performance of GaN Devices.

Ref.	Switching ParametDevice (DUT)	Rated Voltage / Current	Parameters Evaluated	Variables Investigated	$R_{g,on}/R_{g,off}$ (Ω)	V_{GS} (V)	V_{DC}(V)	I_L(A)	T(°C)
[36]	GS66516T	650 V / 60 A	Switching time, loss	I_L	Rg,on=10 Ω	9	400	5-30 A (step 5 A)	25 °C
[37]	IGO60R070D1	650 V / 31 A	Switching loss	V_{DC}, I_L	Rg,on=10 Ω	0–8	0–400	0-15 A	25 °C
[38]	p-GaN HEMTs	650 V / 13 A	Switching speed, energy loss	V_{GS},V_{DC},I_L	Rg,on=10 Ω	4–6	50–400	2-10	25 °C
[39]	E-mode GaN HEMTs	650 V / 30 A	Switching time	V_{DC},I_L,T	Not reported	Not reported	300–400	1-10	25-150 °C
[40]	GaN GIT (Panasonic)	600 V / 10–15 A	Switching time, loss	T,I_L	Rg,on=33 Ω	3.5	500	4-10	25 °C, 125 °C
[41]	GaN devices	200 V class	Switching speed	Rg	Rg,on=10 Ω Rg,off=1.2 Ω	Not reported	Not reported	20-110 A (sweep)	25 °C
[42]	Normally-on/off GaN	600 V class	Switching, gate charge	Device type	Rg,on=10 Ω	Not reported	300	10 A	25 °C
[36]	E-mode GaN HEMT	80 V / 90 A	Switching loss	I_L			30	10 A, 30 A	25 °C

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	Not reported	Not reported

2.5. Dynamic $R_{DS(on)}$ and Threshold Voltage (V_{TH}) Stability

The dynamic variation of on-state resistance and threshold voltage in GaN devices originates from charge trapping phenomena within the device structure. These effects are closely related to the heterostructure nature of GaN HEMTs, where a two-dimensional electron gas forms the conduction channel [43,44].

The on-state resistance is defined as

$$R_{DS(on)} = \frac{V_{DS}}{I_D}$$

Under switching conditions, electrons can be trapped in surface states, buffer layers, or interface defects when the device is subjected to high drain bias. These trapped charges locally modify the electric field and reduce the 2DEG carrier density. As a result, effective resistance increases during subsequent conduction, described as

$$R_{DS(on,dyn)} = \frac{V_{DS,dyn}}{I_D}$$

The relative increase is expressed as

$$\Delta R_{DS(on)} = \frac{R_{DS(on,dyn)} - R_{DS(on,stat)}}{R_{DS(on,stat)}}$$

From a physical standpoint, this degradation is associated with partial depletion of the channel due to trapped negative charge, which reduces carrier mobility and conductivity. The effect becomes more significant with higher drain voltage, longer off-state duration, and increased switching frequency [41,45].

The threshold voltage is similarly affected by charge redistribution in the gate region. It is defined at a reference current level as

$$V_{TH} = V_{GS} \quad \text{at} \quad I_D = I_{ref}$$

Under dynamic conditions, a shift occurs

$$\Delta V_{TH} = V_{TH,dyn} - V_{TH,stat}$$

This shift arises from trapped charges altering the effective gate electric field. A positive shift reduces the gate overdrive $(V_{GS}-V_{TH})$, slowing down channel formation, whereas a negative shift may increase leakage or induce unintended turn-on [25,41]. The increase in dynamic on-resistance directly impacts conduction loss and contributes to efficiency degradation under high-frequency operation.

$$P_{cond} = I_D^2 \cdot R_{DS(on,dyn)}$$

The DPT facilitates direct evaluation of these effects by comparing conduction characteristics across successive pulses under identical current conditions. Owing to the short measurement interval, thermal contributions are minimized, allowing clear identification of trapping-related phenomena [43,45,46]. In GaN HEMTs, charge trapping in surface and buffer states perturbs the two-dimensional electron gas, leading to transient modulation of channel conductivity. Therefore, stability of $R_{DS(on)}$ and V_{TH} is critical for ensuring consistent switching behavior, limiting conduction loss, and maintaining reliable operation in high-frequency power conversion systems [44,46].

Table 2 Summarizes the experimental conditions used in DPT-based studies to investigate dynamic $R_{DS\,(on)}$ and threshold voltage stability in GaN devices. The reported devices include E-mode and p-GaN HEMTs, GaN GITs, and GaN-on-GaN structures, with voltage ratings up to 650 V [47]. The measurements are conducted over a wide range of gate bias, DC-link voltage (50–500 V), load current, and temperature (room temperature to 150 °C). The primary focus of these studies is the evaluation of charge trapping effects under different stress conditions, including OFF-state drain bias, gate bias stress, high current operation, and temperature variation [46–48]. Pulse width and blocking time are carefully selected, typically in the microsecond range, to capture transient trapping and recovery behavior while minimizing thermal influence. Variations in these parameters directly affect

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the observed dynamic $R_{DS(on)}$ and V_{TH} shift [48]. Overall, the table highlights that dynamic degradation is strongly dependent on drain voltage, stress duration, and temperature, while inconsistencies in reported gate conditions and timing parameters can influence comparison across studies. The DPT remains an effective method for isolating trapping-induced effects and assessing the reliability of GaN devices under realistic switching conditions [22].

Table 2. Test Conditions of Reviewed Double Pulse Tests for Dynamic $R_{DS\,(on)}$ and Threshold Voltage Stability in GaN Devices.

Ref.	Device Type	Rated Voltage / Current	V_{GS} (V)	V_{DC} (V)	I_L (A)	Temperature (°C)	Stress Conditions	Pulse Width	Blocking Time	Key Focus
[49]	E-mode GaN HEMT / GaN GIT	650 V / 13 A	6	50–400	0–20	25	OFF-state stress	2 µs	2 µs	Dynamic R_{DS}(on)
[50]	p-GaN HEMT	650 V / 13 A	4.5–6	400	step (few A)	25	Gate stress	164 µs + 3 µs	—	Trap effects
[51]	GaN HEMT	200 V / 32 A	100	150	20–100	25	High current stress	—	1.04 µs	Conduction behavior
[52]	Normally-OFF GaN	600 V / 50 mΩ	—	100–300	5–14	25–150	Thermal + OFF-state	3–4 µs	1 µs	Temperature effect
[53]	Enhancement-mode GaN	650 V / 30 A	−1.5 to 6	380	7–15	25	Gate bias stress	—	—	VTH shift
[54]	E-mode GaN	650 V / 30 A	—	200–400	10–20	25–150	Temperature sweep	2 µs	2 µs	Dynamic R_{DS}(on)
[55]	p-GaN HEMT	650 V / 13 A	—	100–400	10–22	25–150	OFF-state trapping	1–2 µs	—	Trap recovery
[36]	GaN HEMT / GaN GIT	650 V / 50 A	—	100–400	20	25–125	Device comparison	30 ns–5 µs	50 µs	Technology impact
[56]	GaN-on-GaN	650 V	—	50–500	0.2–1	25–150	Blocking voltage	—	10^{-6}–10^{-3} s	Long-term trapping

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[57]	GaN HEMT	600 V / 13 A	—	200 – 500	30	RT	Switching stress	—	up to 100 µs	Switching condition
[36]	Various GaN	350 V	—	50–350	3–6	RT	Manufacturer comparison	5 µs	2 µs	Device variation
[58]	p-GaN / D-mode GaN	650 V / 15 A	5–7	200 – 400	8	RT	Gate bias	10 µs	—	Gate effect
[59]	E-mode GaN	650 V / 8 A	5	200	20	RT	Switching	—	—	Basic DPT
[36]	E-mode GaN	100 V / 16 A	—	25–75	20	RT	Low-voltage test	56 µs	10 µs	Scaling behavior

2.5. Clamping Circuits in Double Pulse Testing of GaN HEMTs

The design of the clamping circuit (CC) is critical for accurately capturing the ON-state voltage of DUT within a very short interval after turn-on. An effective CC must ensure high sensing speed, minimal delay, and negligible measurement distortion. Representative CC topologies (CC1–CC8) are illustrated in Figure 8, and their characteristics are summarized as follows.

CC1 represents Figure 8a, the most basic passive clamp, where a diode-resistor network captures the clamped voltage. Its operation relies on charging and discharging through an RC path, which inherently limits the transient response [60]. The presence of leakage current through the diode introduces a voltage drop across the resistor, resulting in systematic measurement errors. Moreover, the large RC time constant restricts its applicability in high-frequency GaN switching environments.

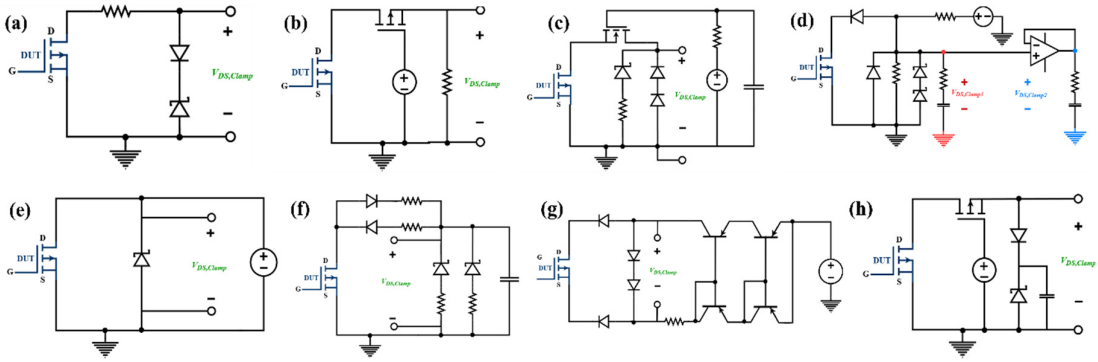

Figure 8. Clamping circuits. (a) CC1. (b) CC2. (c) CC3. (d) CC4. (e) CC5. (f) CC6. (g) CC7. (h) CC8.

CC2 improves upon CC1 by replacing the resistive element with a depletion-mode active device, thereby providing a lower impedance path during the transient interval in Figure 8b. This modification reduces the effective time constant and accelerates the clamping action [60]. However, the nonlinear behavior and parasitic capacitances of the active device can introduce voltage spikes and ringing, which degrade measurement fidelity.

CC3 combines [61] passive and active elements to achieve a compromise between speed and stability. The active device Figure 8c enhances the transient response, while the diode network suppresses excessive overshoot. Nevertheless, the clamping dynamics remain dependent on the charging characteristics of the diode and the operating point of the active device. Under varying load

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currents and DUT $R_{DS(on)}$, the sensing accuracy may deteriorate [62]. In addition, diode leakage currents and threshold variations introduce offset errors, necessitating calibration.

CC4 introduces a two-stage architecture consisting of a fast-sensing path and a dedicated filtering network in Figure 8d. The sensing branch ensures rapid voltage capture immediately after turn-on, while the filtering branch attenuates high-frequency oscillations caused by parasitic inductances [62]. This decoupled approach effectively improves both response speed and signal integrity.

CC5 simplifies the passive clamping structure by reducing component count and optimizing current paths shown in Figure 8e. Its performance relies heavily on minimizing loop inductance and careful PCB layout. When properly designed, it achieves moderate response speed with reduced implementation complexity, making it suitable for high-frequency testing setups [63].

CC6 employs a fully passive configuration incorporating Zener diodes for voltage clamping. While eliminating active components simplifies implementation and enhances robustness, the response speed is constrained by the Zener diode's reverse recovery and junction capacitance in Figure 8f. Consequently, high-frequency operation results in delayed clamping and potential distortion of the measured waveform. To overcome these limitations, advanced CC topologies have been proposed with improved dynamic performance [64]. A modified CC3 utilizing an enhancement-mode GaN transistor significantly reduces parasitic capacitances and improves switching speed, enabling voltage sensing within tens of nanoseconds. This highlights the advantage of using wide-bandgap devices within the sensing path itself.

CC7 is derived from a current mirror-based sensing mechanism, offering improved bandwidth and more precise voltage replication in Figure 8g. By establishing a controlled current path, it enables faster tracking of the DUT voltage. However, its performance is strongly dependent on external measurement equipment, particularly the bandwidth and common-mode rejection capability of differential probes [65]. Furthermore, the multi-node structure increases susceptibility to electromagnetic interference and layout-induced parasitics.

CC8 represents a hybrid active-passive topology incorporating an auxiliary MOSFET and a speed-up capacitor in Figure 8h. The capacitor provides a transient current injection that accelerates the clamping action, while the active device stabilizes the clamped voltage. This configuration effectively suppresses voltage overshoot without sacrificing response time, achieving sub-50 ns sensing capability [66].

From a circuit perspective, the evolution from CC1 to CC8 reflects a clear transition from purely passive, delay-limited designs toward hybrid and active-assisted structures that address the stringent requirements of GaN-based switching characterization. The key design challenges remain the mitigation of parasitic inductance, suppression of oscillations, reduction of leakage-induced errors, and maintaining high bandwidth under extreme switching conditions.

3. Reliability Issues Under Switching Stress

The reliability of GaN power devices under high-frequency switching is strongly influenced by electric field stress, current transients, charge trapping, and thermal effects [20,32,41]. These mechanisms are closely coupled under fast switching conditions and can significantly affect device stability and long-term performance [57,60]. The DPT provides a controlled platform to evaluate these effects by isolating transient switching behavior under well-defined electrical conditions. In particular, the OFF-state high drain voltage combined with rapid switching transitions promotes charge injection into defect states located at the surface, buffer layer, and heterointerface [65]. These trapped charges perturb the electrostatic equilibrium of the device, resulting in temporary or long-term degradation of electrical parameters [66,67]. Among the various reliability concerns, dynamic on-resistance degradation, commonly referred to as current collapse, represents one of the most critical issues affecting GaN device performance in practical power conversion systems [67]. Therefore, understanding the physical mechanisms governing trapping, de-trapping, and their

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dependence on voltage and time is essential for accurate reliability assessment under realistic switching conditions.

3.1. Dynamic $R_{DS\,(on)}$ Degradation Due to Charge Trapping

The dynamic increase in ON-state resistance in GaN HEMTs originates from charge trapping phenomena associated with the heterostructure device architecture [18,41]. In these devices, current conduction occurs through 2DEG formed at the AlGaN/GaN interface. Under OFF-state conditions, when a high drain-to-source voltage is applied, electrons are injected into trap states located at the surface, within the buffer layer, or at material interfaces [41]. The accumulation of trapped negative charge modifies the local electric field distribution and partially depletes the 2DEG channel, thereby reducing the effective carrier density available for conduction [32,57]. As a result, when the device is subsequently turned ON, the channel conductivity is temporarily degraded, leading to an increase in the effective on-state resistance, defined as dynamic $R_{DS(on)}$. This phenomenon is inherently transient, as the trapped charges gradually release over time depending on the trap energy levels and thermal conditions [66]. However, under repetitive switching operation, the continuous trapping process can lead to significant performance degradation, increased conduction losses, and reduced system efficiency.

The dependence of dynamic $R_{DS(on)}$ on electrical stress conditions is illustrated in Figure 9a. It can be observed that the normalized on-resistance increases with increasing OFF-state drain voltage, indicating that higher electric fields enhance electron trapping in deep-level states [68]. This behavior is primarily attributed to the increased probability of carrier injection into trap sites under strong electric field conditions. Furthermore, the time-dependent nature of the trapping process is demonstrated in Figure 9b. where the normalized $R_{DS(on)}$ is shown as a function of stress time. As the blocking duration increases, more charge is accumulated in the trap states, leading to a progressive increase in dynamic resistance. This confirms that charge trapping in GaN devices is not only field-dependent but also strongly influenced by the duration of the applied stress. The combined effect of voltage and time highlights the complex nature of trapping dynamics in GaN HEMTs, where both electric field strength and trapping duration play a critical role in determining device reliability. Consequently, accurate evaluation of dynamic $R_{DS(on)}$ requires carefully controlled DPT conditions that account for both voltage stress and blocking time.

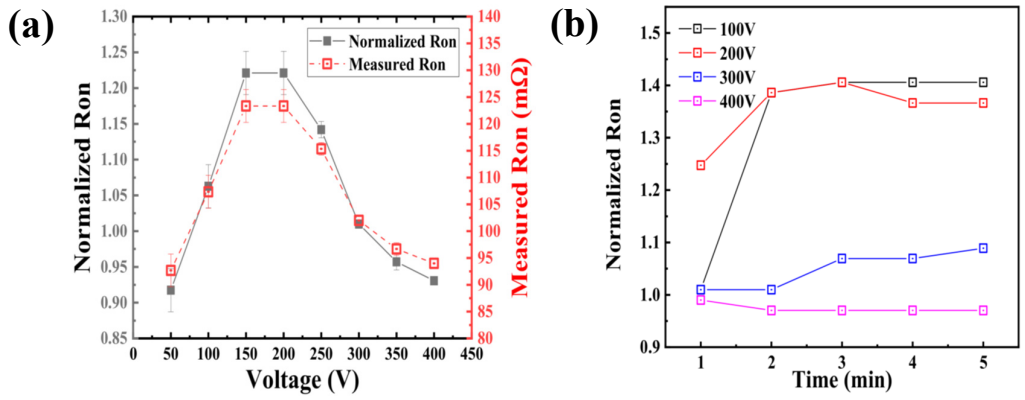

Figure 9. Normalized dynamic $R_{DS(on)}$ as a function of OFF-state (a) drain voltage, illustrating the increase in on-resistance with increasing electric field due to enhanced charge trapping. (b) stress time under different OFF-state voltages, demonstrating the time-dependent accumulation of trapped charges [68].

3.2. Current Collapse (Transient Conductivity Loss)

Current collapse in GaN HEMTs is a transient reduction in drain current observed between successive switching pulses, as shown in the multi-pulse DPT results in Figure 10. This effect is

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characterized by a lower I_{DS} in later pulses compared to the initial pulse under identical bias conditions, indicating a degradation in dynamic conduction capability [68]. The phenomenon is primarily caused by charge trapping during the OFF-state under high drain bias. Electrons are injected into surface states, buffer traps, and interface defects, where they remain partially trapped during the subsequent ON-state [57]. These trapped charges distort the local electric field, leading to partial depletion of the 2DEG channel and an increase in dynamic on-resistance. In the first pulse, the device exhibits near-intrinsic conduction behavior. However, in subsequent pulses, incomplete de-trapping results in reduced channel charge density and a measurable drop in I_{DS}. This pulse-to-pulse degradation defines current collapse and is a critical indicator of trapping-induced reliability concerns in GaN power devices. The severity of current collapse depends strongly on OFF-state voltage stress, blocking time, and switching frequency. Higher drain voltage enhances trap occupation, while insufficient recovery time at high frequency aggravates charge accumulation, leading to increased dynamic $R_{DS(on)}$ and elevated switching losses. Figure 10 presents the measured multi-pulse DPT waveforms under continuous operation, including V_{GS}, V_{DS}, I_{DS}, and extracted dynamic on-resistance, clearly demonstrating the reduction in drain current across successive pulses due to trapping effects [68]. Figure 10 presents the measured multi-pulse DPT waveforms under continuous operation, including V_{GS}, V_{DS}, I_{DS}, and extracted dynamic on-resistance. The progressive reduction in I_{DS} across successive pulses highlights trapping-induced transient effects and directly reflects current collapse under practical operating stress.

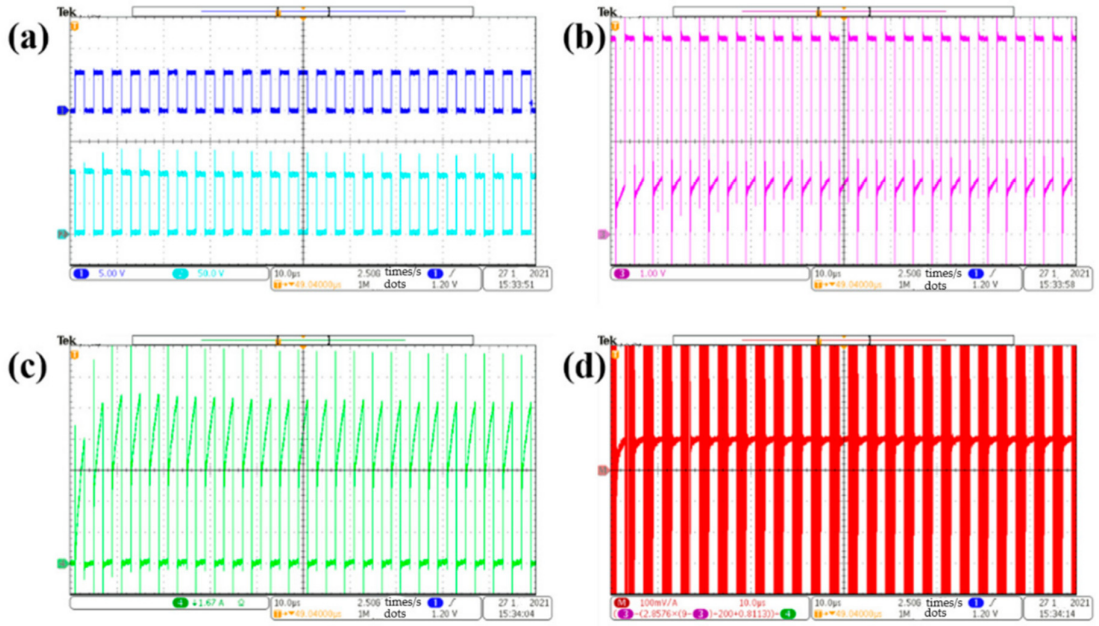

Figure 10. Multi-pulse switching waveforms of a GaN HEMT at 100 V and 250 kHz: (a) V_{GS} and V_{DS}; (b) measured drain voltage V_{DS}, (c) drain current I_{DS}, (d) dynamic $R_{DS(on)}$. The reduction in I_{DS} across successive pulses demonstrates current collapse caused by charge trapping under OFF-state high-voltage stress [68].

3.3. Hot Electron Effect (High Electric Field Reliability)

Hot electron degradation is a dominant high-field reliability mechanism in GaN HEMTs under repetitive switching stress [49,69]. During DPT, the device is subjected to high OFF-state drain bias followed by fast turn-on transitions, creating a strong electric field near the gate–drain region. This condition, channel electrons gain sufficient to become "hot" and are injected into surface states, AlGaN barrier traps, or buffer-related defect states [70]. This process modifies the local electric field and leads to a progressive degradation of dynamic device characteristics [71]. The trends observed in Figure 11a,b indicate that the normalized dynamic $R_{DS(on)}$ initially increases due to combined self-

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heating and fast trapping effects [69]. After the sensor temperature reaches steady state, $R_{DS(on)}$ is expected to stabilize; however, a continued increase is clearly observed. This post-stabilization degradation confirms the presence of field-driven mechanisms, primarily hot electron injection and defect activation, rather than purely thermal effects. Clear technology-dependent behavior is evident. The Schottky-gate p-GaN HEMTs exhibits severe degradation, reaching nearly 1000% increase in dynamic $R_{DS(on)}$ within tens of hours, whereas the ohmic-gate device shows a significantly lower degradation (~25% over longer stress duration). This difference is attributed to stronger electric field concentration at the Schottky gate interface, which enhances carrier acceleration and increases the probability of hot electron injection into trap states [69]. The impact of switching conditions further supports this mechanism. A reduced dV_{DS}/dt (lower slew rate) increases the overlap duration of high voltage and current during turn-on, thereby increasing carrier energy and injection probability. Experimental results show that slower switching transitions lead to substantially higher long-term degradation, despite only a modest increase in steady-state temperature. This indicates that electric field exposure time, rather than temperature alone, governs the degradation process. From a reliability perspective, hot electron effects result in cumulative trapping and possible generation of new defect states, leading to irreversible shifts in $R_{DS(on)}$ and V_{TH} [70,71]. The DPT methodology allows clear identification of this mechanism by decoupling thermal stabilization from time-dependent electrical degradation under controlled stress conditions.

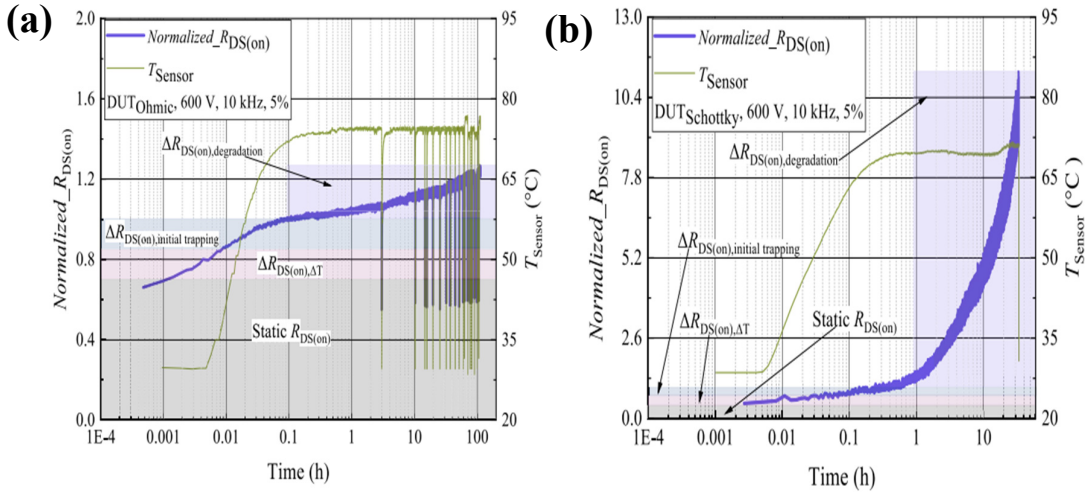

Figure 11. Long-term evolution of normalized dynamic $R_{DS(on)}$ under repetitive DPT stress (600 V, 10 kHz, 5% duty): (a) ohmic-gate p-GaN HEMT shows minimal degradation after thermal stabilization, while (b) Schottky-gate p-GaN HEMT exhibits significant degradation due to hot-electron injection. Stabilized T_{sensor} confirms dominance of high-field effects over self-heating [69].

3.4. Gate Reliability and Voltage Overshoot

Gate reliability in p-GaN HEMTs is strongly governed by the electric field distribution in the gate–drain access region and the applied OFF-state gate bias [72–74]. The impact of gate bias is illustrated in Figure 12 where the dynamic $R_{DS(on)}$ is evaluated under different $V_{GS,OFF}$ conditions [75]. A clear increase in degradation is observed as the gate bias becomes more negative, particularly at higher drain bias. This behavior indicates enhanced electric field concentration near the gate edge, which promotes carrier injection into trap states located in the p-GaN layer and at the AlGaN interface. From a physical standpoint, a more negative $V_{GS,OFF}$ increases band bending in the gate region and facilitates hole accumulation and trapping. These trapped charges alter the local electrostatics, leading to partial depletion of the channel and a subsequent increase in dynamic $R_{DS(on)}$. The observed dependence on both V_{DS} and $V_{GS,OFF}$ confirms that gate-controlled electric field plays a dominant role in degradation. In practical DPT operation, the gate is additionally subjected to

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transient stress due to voltage overshoot [75]. During high dv/dt switching, displacement current through the Miller capacitance C_{GD} induces a transient increase in gate voltage. This overshoot can momentarily exceed the intended gate drive level, especially in the presence of common source inductance and gate loop parasitics. Unlike static bias stress, this is a dynamic and repetitive stress mechanism, which accelerates degradation of the gate interface and may lead to increased leakage or premature failure. Therefore, gate reliability in GaN HEMTs is determined by the combined influence of OFF-state gate bias–induced electric field stress and transient gate voltage overshoot during switching [73–75]. The former governs long-term trapping and degradation, while the latter introduces additional dynamic stress that must be considered in high-frequency converter operation.

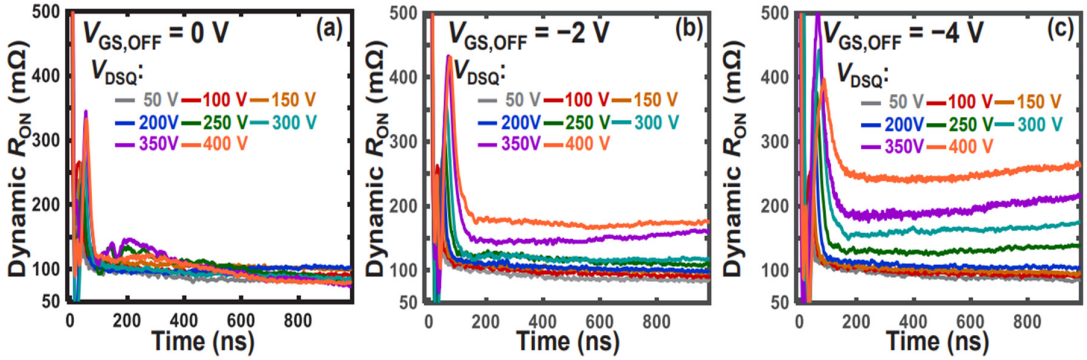

Figure 12. Dynamic $R_{DS(on)}$ of p-GaN gate HEMT under varying OFF-state gate bias conditions. Increased degradation with more negative $V_{GS,OFF}$ and higher drain bias indicates enhanced electric field stress and gate-related trapping effects, highlighting the role of gate bias in device reliability [75].

3.5. Parasitic-Induced Stress (Overshoot & Ringing)

Parasitic elements in the commutation loop critically influence the switching behavior of GaN HEMTs under high-speed operation. During DPT, the interaction between loop inductance and device capacitances forms a resonant network, leading to voltage overshoot and high-frequency ringing superimposed on the switching waveforms [77–79]. Figure 13 illustrates the switching behavior with a snubber network at I_L =20A and loop inductance L_{loop} = 45.3nH. During the turn-off transition, a sharp increase in V_{DS} is observed due to the rapid current commutation [76]. The associated current slew rate interacting with loop inductance produces a voltage spike, consistent with $V_{overshoot} \propto L_{loop} \cdot \frac{dI}{dt}$. Superimposed oscillations indicate underdamped resonance between parasitic inductance and nonlinear capacitances C_{DS} and C_{GD}. The waveform further shows that the inclusion of a snubber effectively suppresses the oscillation amplitude and limits the peak drain voltage. This damping action reduces the energy stored in the resonant loop and mitigates repetitive electrical stress on the device [80]. In addition to drain voltage stabilization, the reduction of oscillatory behavior also minimizes coupling into the gate loop, thereby lowering the risk of unintended gate excitation [80,81]. From a reliability perspective, uncontrolled overshoots can exceed the safe operating voltage of GaN devices, which inherently lack avalanche robustness. Persistent ringing contributes to additional switching loss, electromagnetic interference, and long-term degradation [81]. Therefore, minimization of parasitic inductance and proper damping through snubber design are essential for ensuring stable and reliable high-frequency operation.

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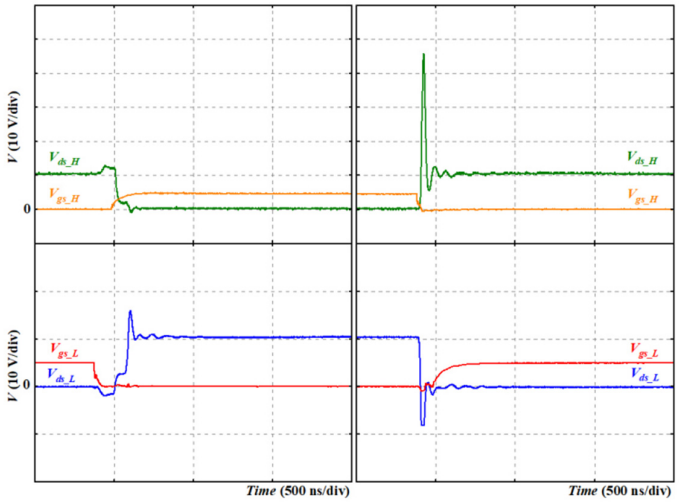

Figure 13. Switching waveforms of GaN HEMT with snubber network at I_L =20A and L_{loop} = 45.3nH. Reduced voltage overshoot and suppressed high-frequency ringing are observed due to damping of the parasitic LC resonance, indicating improved switching stability and reduced electrical stress [76].

3.6. Thermal and Time-Dependent Trapping

The coupled influence of switching dynamics and thermal effects on long-term degradation is illustrated in Figure 14 where the normalized $R_{DS(on)}$ and sensor temperature are monitored under different turn-on slew rates. Initially, the increase in $R_{DS(on)}$ is dominated by self-heating, as the device temperature rises and carrier mobility decreases. Once thermal steady state is reached, the temperature stabilizes; however, the continued increase in $R_{DS(on)}$ indicates that additional degradation mechanisms are active [49]. The dependence on slew rate reveals a key physical mechanism. A lower turn-on slew rate 10 V/ns increases the duration of overlap between high drain voltage and high current during switching [69]. This extended overlap enhances carrier energy and promotes charge injection into deep trap states located in the p-GaN layer and buffer region [66]. As a result, the slower switching condition leads to significantly higher long-term degradation compared to the faster transition 22 V/ns [69].

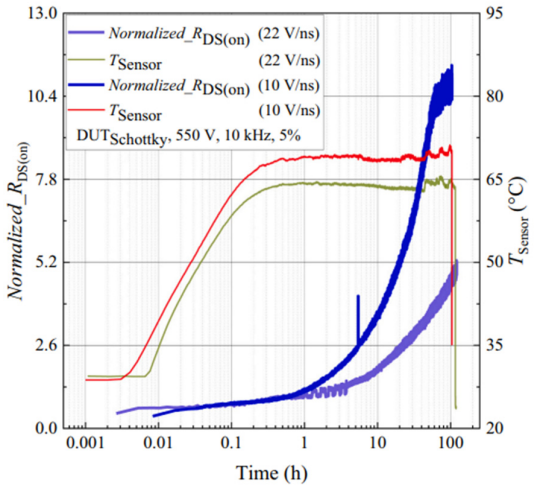

Figure 14. Long-term evolution of normalized $R_{DS(on)}$ and sensor temperature under varying turn-on slew rates, highlighting increased degradation at lower slew rates due to enhanced high-field stress and time-dependent charge trapping [69].

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Although the device operating at lower slew rate exhibits only a modest increase in steady-state temperature, the observed degradation is substantially larger, confirming that thermal effects alone cannot account for the behavior. Instead, the results indicate that time-dependent trapping driven by high-field stress during switching is the dominant mechanism. The progressive increase in $R_{DS(on)}$ over-time reflects the accumulation of trapped charge, which perturbs the channel electrostatics and reduces effective conductivity [69]. In the later stage of operation, deviation in the degradation trend is observed due to the action of the clamping circuit, which limits the maximum voltage stress and modifies the switching condition [70]. This highlights that external circuit elements can influence the apparent degradation behavior and must be considered when interpreting long-term reliability data [82,83].

Recent studies indicate that reliability degradation in GaN HEMTs is fundamentally governed by trap-assisted charge dynamics and high-field carrier injections, particularly under repetitive switching stress [83,84]. Therefore, future research is increasingly focused on electric-field engineering and trap suppression at the device level. Advanced structures such as multi-gate and field-plate designs allow more uniform field distribution, thereby reducing hot electron injection and localized trapping [67,69]. In parallel, gate-stack innovation using dielectric integration (e.g., MOS-HEMT) has shown strong potential to suppress gate leakage and improve long-term stability under dynamic stress conditions. From a physics perspective, controlling the interaction between high electric field, carrier energy, and trap states remains the key challenge [38]. Future reliability improvement will rely on co-optimization of material quality, electrostatics, and switching conditions, enabling reduced trapping, suppressed hot carrier effects, and stable operation in high-frequency power conversion systems [49].

4. Applications of GaN Switching Characterization

Switching characterization of GaN HEMTs establishes a direct link between device physics and converter-level performance, showing accurate evaluation of high-frequency power electronic systems [10,22,26]. Using Double Pulse Testing key dynamic parameters such as switching energies (E_{ON}, E_{OFF}), dv/dt, di/dt, dynamic $R_{DS(on)}$, and voltage overshoot are extracted under controlled switching conditions [2,44,49]. These parameters are essential for quantifying switching losses, transient behavior, and reliability limitations, thereby supporting optimized converter design [38,43]. In high-frequency power factor correction (PFC) and LLC resonant converters, switching characterization is used to analyze efficiency–EMI trade-offs [50,68,69]. Although GaN HEMTs devices support high-frequency operation, excessive dv/dt and di/dt can induce ringing and parasitic losses [70,78,79]. The obtained characterization data is used to optimize gate resistance, dead-time, and snubber networks for improved efficiency and stable switching behavior [84–87]. For data center power supply units (PSUs), switching characterization enables high-efficiency and high-power-density design [76]. Measurement of dynamic $R_{DS(on)}$ and current collapse under realistic switching conditions allows accurate estimation of conduction and switching losses, which is critical for thermal design and long-term reliability assessment under hard-switching operation [88]. In automotive and high-voltage systems, characterization is crucial for evaluating device robustness under extreme electrical stress. Parameters such as voltage overshoot, gate transient response, and short-circuit behavior are analyzed to ensure safe operation within device limits, given the limited avalanche capability of GaN devices [89,90]. This supports the development of protection strategies including active gate control and fault handling. Additionally, switching characterization supports device–package co-design by correlating measured transient waveforms with parasitic inductance and capacitance [90–92]. This allows optimization of PCB layout and packaging to reduce ringing and improve switching performance. Overall, GaN switching characterization is a key enabler for translating device-level advantages into system-level gains in efficiency, power density, and reliability across modern power electronic applications [91–93].

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5. Conclusions

This review presented the DPT method for GaN power devices, covering its principle, sampling methods, reliability aspects, and converter-level applications. DPT is widely used to extract dynamic switching parameters, including dynamic $R_{DS(on)}$, under hard-switching conditions for evaluating GaN HEMTs performance. Measurement accuracy depends strongly on reducing parasitic inductance and improving layout design in the test setup. GaN devices are affected by trapping effects, gate stress, and transient overvoltage, which influence dynamic conduction and switching behavior. These factors should be considered when using DPT results for reliability and lifetime analysis. In practical applications, DPT results are used in the design of high-frequency PFC, LLC converters, and power supply systems to reduce switching loss and improve efficiency and thermal performance. Main limitations include measurement bandwidth constraints, parasitic effects, and the lack of standardized testing procedures for GaN devices, which leads to variation in reported results. Future work should focus on low-parasitic test structures, improved high-speed measurement techniques, and standardized DPT procedures. Integration of devices, packages, and circuit design will be important for accurate switching characterization in next-generation power converters.

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