Temperature-Dependent Electro-Thermal Characteristics of E-Mode GaN HEMTs with Ohmic and Schottky Gates

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Article

Temperature-Dependent Electro-Thermal Characteristics of E-Mode GaN HEMTs with Ohmic and Schottky Gates

Minji Kim [1], Jiun Oh [1], Younghun Han [2], June-O Song [2] and Joon Seop Kwak [1,*]

[1] Department of Energy Engineering, Korea Institute of Energy Technology, Naju, Republic of Korea
[2] R&D Center, Wavelord Inc., Hwaseong, Republic of Korea
* Correspondence: jskwak@kentech.ac.kr

Abstract

p-GaN gate enhancement-mode GaN HEMTs are promising normally-off power devices, but their high-temperature reliability is strongly affected by the gate contact scheme. This study compares Pd-ohmic and Ni-Schottky p-GaN gate HEMTs fabricated on the same GaN-on-Si epitaxial platform by combining temperature-dependent electrical characterization, post-temperature-dependent-test (TDT) room-temperature recovery analysis, and thermoreflectance thermal mapping. Electrical measurements were performed from room temperature to 500 °C using gate leakage, transfer, and output characteristics, while thermal maps were obtained before and after TDT under identical bias conditions. The Pd-ohmic devices exhibited higher initial current drive but larger operating gate-current penalty and stronger degradation of normalized on-state characteristics at elevated temperature. After TDT, reduced transconductance and maximum drain current were accompanied by weaker active-channel heating, indicating degradation-type cooling associated with reduced gate-channel modulation efficiency. In contrast, the Ni-Schottky devices showed lower gate-current penalty and better normalized output retention up to approximately 300 °C; however, post-TDT increases in transconductance and drain current occurred together with degraded subthreshold swing and persistent localized heating, indicating apparent on-state activation with weakened gate/depletion control. These results show that p-GaN gate reliability should be assessed through coupled electrical and thermal signatures rather than single electrical or thermal metrics.

Keywords: p-GaN gate HEMT; GaN power devices; Ohmic gate; Schottky gate; thermoreflectance; thermal mapping; high-temperature reliability; gate leakage; electro-thermal degradation

1. Introduction

GaN-based high electron mobility transistors (HEMTs) are attractive for power electronics because the AlGaN/GaN heterointerface supports a highly conductive two-dimensional electron gas(2DEG), enabling high current density and low on-state resistance [1,2]. However, conventional AlGaN/GaN HEMTs are inherently depletion-mode devices because the polarization-induced 2DEG exists even at zero gate bias. For power switching applications, enhancement-mode operation is generally preferred to ensure fail-safe behavior and to simplify gate-driven design [3–6].

Among the normally-off approaches, p-GaN gate technology has become one of the most practically important solutions. The p-GaN cap lifts the conduction band beneath the gate and depletes the 2DEG at equilibrium. A positive gate bias restores the channel, enabling normally-off operation [5,6]. The gate contact scheme, however, plays a decisive role in determining threshold voltage, gate leakage, gate-drive window, and reliability. Depending on the metal/p-GaN barrier

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profile, p-GaN gate HEMTs can be broadly classified into ohmic-gate and Schottky-gate devices [7–10].

In Ohmic-gate or gate-injection type devices (GIT), forward gate bias can induce hole injection from the p-type gate region into the heterostructure. This hole injection increases the electron density in the channel through conductivity modulation, thereby enhancing the drain current while maintaining normally-off behavior [9]. In Schottky-gate devices, the metal/p-GaN Schottky barrier suppresses gate injection and reduce gate current. Schottky-gate p-GaN HEMTs typically offer higher threshold voltage, higher gate-breakdown voltage, and larger gate-voltage swing than Ohmic-gate p-GaN HEMTs, but the allowable long-term gate bias remains limited by gate/p-GaN interface degradation under high electric field [7,9,10].

Previous studies have clarified several important aspects of these two gate schemes. Comparative studies have shown that the gate current magnitude differs strongly between Ohmic and Schottky p-GaN gate HEMTs, with Ohmic-gate devices generally exhibiting larger turn-on gate current [9]. Other works have examined p-GaN related gate optimization, Schottky gate leakage mechanisms, gate breakdown, and p-GaN-related current instability in high temperature [11–14]. Nevertheless, the spatial consequence of electrical degradation remains insufficiently resolved. In particular, it remains unclear how post-temperature dependent test (TDT) changes in transfer and output characteristics are linked to changes in heat-source topology observed by thermal mapping.

In this study, we address this gap by correlating electrical degradation parameters with thermoreflectance thermal maps in Pd-ohmic and Ni-Schottky p-GaN gate e-mode HEMTs. The central hypothesis is that gate-contact-dependent degradation is not only reflected in scalar electrical parameters, such as gm, Ron, IG/ID, SS, and Ioff, but also in the spatial redistribution framework in which electrical changes and thermoreflectance signatures are interpreted as coupled reliability indicators.

2. Experimental

2.1. Device Fabrication

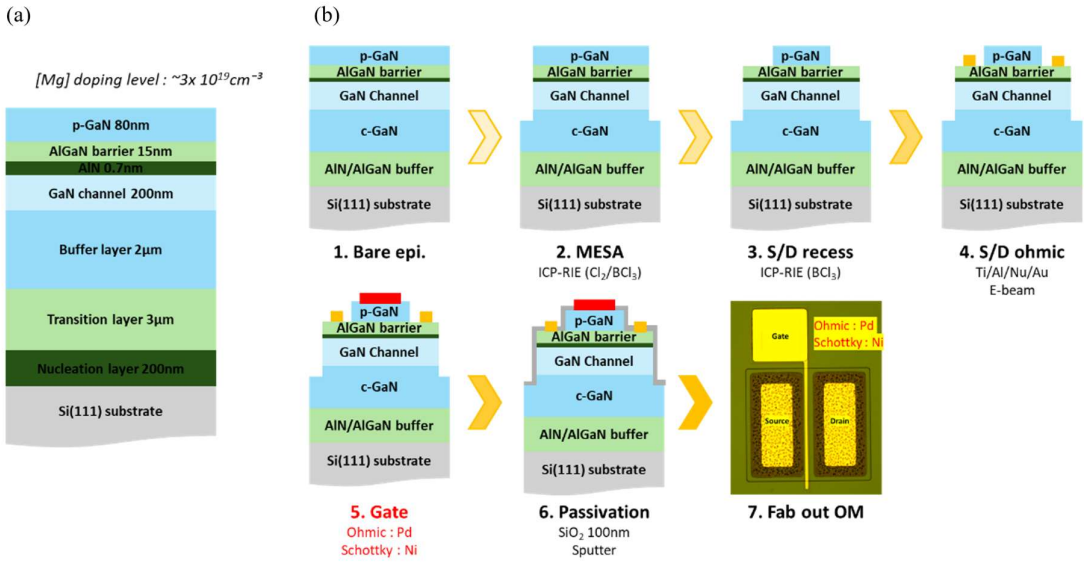

Figure 1. (a) Epitaxial structure of p-GaN HEMTs; (**b**) Fabrication process and fab-out image of the device.

Two p-GaN gate enhancement-mode HEMT structures were fabricated: a Pd-based Ohmic-gate device and a Ni-based Schottky-gate device. The devices investigated in this work were fabricated on an GaN HEMT-on-Si epitaxial wafer in Figure 1 (a). The epitaxial structure consisted of, Si(111) substrate, a 200nm nucleation layer, a 3000nm transition layer, a 2000nm high-resistivity buffer layer,

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a 200nm GaN channel layer, a 0.7nm AlN spacer, a 15nm AlGaN barrier with an Al composition of 20%, and an 80nm p-GaN cap layer. The same epitaxial platform was used for both Pd-ohmic and Ni-Schottky gate devices, allowing the effect of the gate contact scheme to be compared without changing the underlying channel and buffer structures.

The fabrication process as depicted in Figure 1(b) was designed to isolate the gate-contact effect while maintaining identical source/drain and passivation processes. First, mesa isolation was performed by inductively couple plasma reactive-ion etching (ICP-RIE) using a Cl_2/BCl_3 chemistry. The source/drain access regions were then recessed by ICP-RIE using BCl_3 to remove the p-GaN cap in the source/drain contact regions. Source and rain ohmic contacts were formed by electron-beam evaporation of Ti/Al/Ni/Au (20/100/50/50nm), followed by rapid thermal annealing at 850°C for 30s. The gate metal was subsequently defined with two different metallization schemes: Pd for the ohmic-gate device and Ni for the Schottky-gate device. No post-metallization annealing was performed after gate metal deposition. Finally, a 100nm SiO_2 passivation layer was deposited by sputtering.

The fabricated devices had the same lateral geometry for both gate-contact schemes. The source-to-gate spacing, gate length, gate-to-drain spacing, and gate width were 5μm, 5μm, 13μm, and 200μm, respectively. Theis identical layout enables direct comparison of the electrical and thermal responses of the Pd-ohmic and Ni-Schottky p-GaN gate HEMTs.

The distinct gate-contact characteristics were verified using transmission-line-method(TLM) structures and structural characterization of the gate metal on GaN. The Pd contact exhibited an approximately linear current-voltage behavior, consistent with Ohmic-type conduction, whereas the Ni contact showed rectifying behavior characteristic of a Schottky-type gate. X-ray diffraction measurements further indicated preferential Pd(111) alignment on GaN, supporting the formation of the Pd-based Ohmic gate contact. By contrast, the Ni-gate was used as the rectifying Schottky gate contact in the comparative devices.

2.2. Temperature-Dependent Electrical Characterization

Electrical measurements were performed before TDT, during temperature-dependent characterization and after post-TDT recovery to room temperature. Gate leakage measured at V_{DS}=0V was treated as intrinsic gate-stack leakage, whereas gate current obtained during transfer measurements at finite V_{DS} was treated as the operating gate-current penalty. This distinction is essential because the gate current under shorted drain-source conditions does not necessarily represent the gate-current burden during transistor operation [12–14].

The experimental workflow was designed to correlate the electrical degradation of the two gate-contact schemes with their corresponding thermal signatures. The electrical and thermal datasets were integrated using a common set of degradation and localization metrics. Electrical characterization, including the temperature-dependent test (TDT), and thermoreflectance thermal imaging were therefore treated as complementary measurements rather than independent analyses.

Temperature-dependent electrical characterization was carried out using a Keysight B1505A power device analyzer and a vacuum chamber. The devices were measured sequentially at room temperature, 100°C, 200°C, 300°C, 400°C, and 500°C. At each temperature, the devices were allowed to stabilize for more than 30min before electrical measurements were performed. After the high-temperature sequence, the devices were naturally cooled down inside the vacuum chamber and then measured again at room temperature to distinguish reversible temperature-dependent changes from residual degradation after TDT.

Three electrical measurement modes were used. First, gate leakage characteristics were measured under shorted drain-source conditions, with V_{DS}=0V and V_{GS} swept from -8 to 6V. This measurement was used to evaluate intrinsic gate-stack conduction through the metal/p-GaN/AlGaN gate structure. Second, I_{DS}-V_{GS} were measured at VDS=10V while sweeping V_{GS} from -8 to 6V. From these data, I_{DS}, I_{GS}, I_{GS}/I_{DS}, threshold voltage (V_{TH}), transconductance (gm), subthreshold swing (SS), and off-state current were extracted. Third, output characteristics were measured with VDS swept from 0V to 10V and Vg varied from -4V to 6V in 2V steps. The output curves were used to assess on-

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state current capability and on-resistance. To minimize the influence of self-heating induced current collapse during the electrical measurements, the transfer and output characteristics were measured under pulsed-bias conditions.

2.3. Thermoreflectance Thermal Imaging

Thermoreflectance thermal imaging was performed using a TRM250 system from Nanoscopesystems. Thermoreflectance is an optical thermometry technique based on the temperature dependence of the optical reflectance of a material. When the temperature changes by delta T, the refractive index and optical constants of the probed surface change slightly, producing a corresponding change in the reflected intensity[15–17]. For small temperature excursions, the normalized reflectance change is linearly related to the local temperature rise through the thermoreflectance coefficient, C_{TR}:

$$\frac{\Delta R}{R} = C_{TR} \times \Delta T \quad (1)$$

Here, C_{TR} represents the temperature sensitivity of the measured surface reflectance at a given wavelength and material region. Since both the magnitude and sign of C_{TR} depend on the material, surface conditions, and illumination wavelength, the experimentally calibrated C_{TR} value was used directly for temperature conversion[17].

A 365nm wavelength was used to probe the GaN region, and the thermal maps were acquired using a 20x objective lens. The use of near-ultraviolet illumination is appropriate for GaN because the photon energy at 365 nm is close to the GaN bandgap and can therefore probe the near-surface GaN region rather than being fully transparent to the semiconductor[15].

The thermoreflectance coefficient calibration was performed from 25°C to 95°C with a 10°C interval, yielding a CTR value of -2×10^{-3}. Temperature was calculated using an asynchronous thermoreflectance technique. The pre- and post-TDT thermal maps were acquired under the same electrical bias condition, VGS=6V and VDS=10V. Therefore, the observed changes in the thermal maps reflect the combined influence of electrical degradations, modified current transport, and heat-source redistribution under identical external bias conditions.

3. Results and Discussion

3.1. Gate Leakage Characteristics

The gate leakage characteristics in Figure 1 were first examined under V_{DS}=0V to evaluate the intrinsic gate-stack conduction of each gate-contact scheme. This measurement condition isolates the metal/p-GaN/AlGaN gate stack from drain-induced channel conduction and therefore provides a direct comparison of the leakage behavior of the Pd-ohmic and Ni-Schottky gates.

At the initial room-temperature state, the Pd-ohmic gate exhibited a substantially larger gate leakage than the Ni-Schottky gate. At $V_{GS} \approx 6$V, the gate leakage current was 20.69mA/mm for the Pd-ohmic gate and 6.24mA/mm for the Ni-Schottky gate. At VGS=4V, the difference was even more pronounced, with 15.18 mA/mm for the ohmic gate and 1.05mA/mm for the Schottky gate. This confirms that the Pd gate provides an injection-capable gate contact, whereas the Ni gate suppresses gate conduction through a rectifying Schottky-type barrier.

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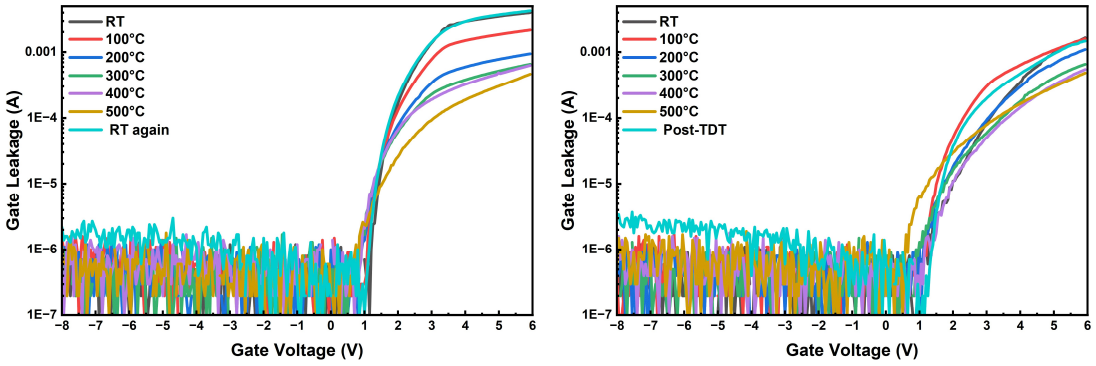

(**a**) (**b**)

Figure 2. Gate leakage characteristics of (**a**) Pd-ohmic gate; (**b**) Ni-Schottky gate.

The temperature dependence of gate leakage showed different trends for the two gate types. For ohmic gate, the leakage current at $V_{GS} \approx 6V$ decreased from 20.69mA/mm at room temperature to 2.24mA/mm at 500°C. This decrease indicates that the high-temperature behavior of the ohmic gate is not governed simply by thermally enhanced emission. Instead, the effective gate injection may be limited by increased p-GaN resistance, altered voltage partitioning within the gate stack, or weakening of the effective injection path at high temperature. For the Ni-Schottky gate, the leakage current was 6.24 mA/mm at room temperature, increased slightly to 7.22 mA/mm at 100 °C, and then decreased to 2.46 mA/mm at 500 °C. After cooling back to room temperature, the leakage current was 6.71 mA/mm, slightly higher than the initial value, suggesting a residual modification of the Schottky gate stack after TDT.

Table 1. Gate leakage onset voltage defined at I_{GS}=0.5mA/mm.

Temperature	Pd-ohmic gate	Ni-Schottky gate
RT	1.78V	3.42V
100°C	1.85V	2.58V
200°C	2.11V	3.37V
300°C	2.27V	3.81V
400°C	2.33V	3.91V
500°C	3.08V	3.17V
Post-TDT	1.75V	2.53V

As described in Table.1, the leakage onset voltage, defined here as the gate voltage at which IG reaches 0.5 mA/mm, also revealed gate-stack modification after TDT. Initially, the onset voltage was 1.78 V for the ohmic gate and 3.42 V for the Schottky gate. The higher onset voltage of the Schottky gate confirms its stronger gate-current blocking capability at the initial state. However, after TDT, the onset voltage of the Schottky gate decreased from 3.42 V to 2.53 V, indicating that the Schottky barrier or leakage path became easier to activate after high-temperature exposure.

3.2. Transfer Characteristics

The temperature-dependent transfer (Id-Vg) characteristics were summarized using four key parameters extracted at V_{DS}=10V: V_{TH}, gm, SS, and the operating gate-current ratio (I_G/I_D). The resulting trends are shown in Figure 3.

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Figure 3(a) shows that V_{TH} increases monotonically with temperature for both gate-contact schemes. At room temperature, all devices exhibit similar V_{TH} values of approximately 1.6-1.7V, confirming comparable normally-off behavior before high-temperature exposure. As the temperature increases, V_{TH} gradually shifts toward positive values and reaches approximately 3.4-3.8V at 500°C. This positive V_{TH} shift indicates that a larger gate bias is required to restore the 2DEG channel at elevated temperature. The trend is observed in both ohmic and Schottky devices, suggesting that the dominant origin is not solely the metal/p-GaN contact type but also temperature-dependent channel depletion, p-GaN potential modulation, and increased series resistance in the gate/channel access path.

Figure. 3(b) shows a strong reduction in gm with increasing temperature. The gm values are normalized to their room-temperature values in the plot, and all devices decrease rapidly from unity at room temperature to less than approximately 0.1 at 400-500°C. This reduction is attributed primarily to modulation at high temperature. The similarity of the decreasing trend in both gate types indicates that high-temperature carrier transport degradation in the AlGaN/GaN channel and access regions dominates the transconductance loss. However, the post-TDT recovery behavior must still be interpreted together with the contact-specific gate-current and off-state degradation signatures.

Figure 3(c) compares the subthreshold swing normalized to the room-temperature value. In general, SS increases with temperature, indicating degraded subthreshold gate control at elevated temperature. The increase is modest up to approximately 300°C for most devices but becomes more pronounced at 400-500°C. The device-to-device scatter is larger in SS than in VTH and gm, especially at high temperature, implying that the subthreshold regime is more sensitive to local trap states, leakage paths, and gate-stack nonuniformity. The Schottky devices show strong SS degradation at intermediate-to-high temperatures, whereas the ohmic devices exhibit a sharp SS increase near 500°C. This behavior indicates that both gate schemes lose electrostatic control in the extreme-temperature regime, although the detailed degradation path differs between the two contact types.

Figure 3(d) shows the operating gate-current ratio. It evaluates the gate-current burden under actual transistor operation rather than under gate-leakage conditions (V_{DS}=0V). At room-temperature, the Schottky devices exhibit much lower I_G/I_D than the ohmic devices, confirming the superior gate-current blocking capability of the Schottky contact. With increasing temperature, gate-current ratio increases for all devices, reflecting the combined effect of reduced drain current and non-negligible gate current. Near 500°C, the Schottky devices show a pronounced increase in I_G/I_D, reaching values comparable to or larger than those of the ohmic devices. This indicates that the low-gate-current advantage of the Schottky gate collapses in the extreme-temperature regime.

After TDT and natural cooling to room temperature, the gate-current ratio decreases markedly in the Schottky devices and returns close to the initial low range, while the ohmic devices remain at several percent. However, this apparent recovery of I_G/I_D should not be interpreted alone as full recovery of gate reliability, because the post-TDT electrical data also show degraded SS and increased I_{off} in the Schottky devices. Therefore, the transfer-parameter trends indicate that the Schottky gate is advantageous at low-to-moderate temperature due to its low operating gate-current penalty, whereas both gate types enter a severe degradation regime at 400–500 °C where gm collapse, SS degradation, and increased IG/ID must be considered simultaneously.

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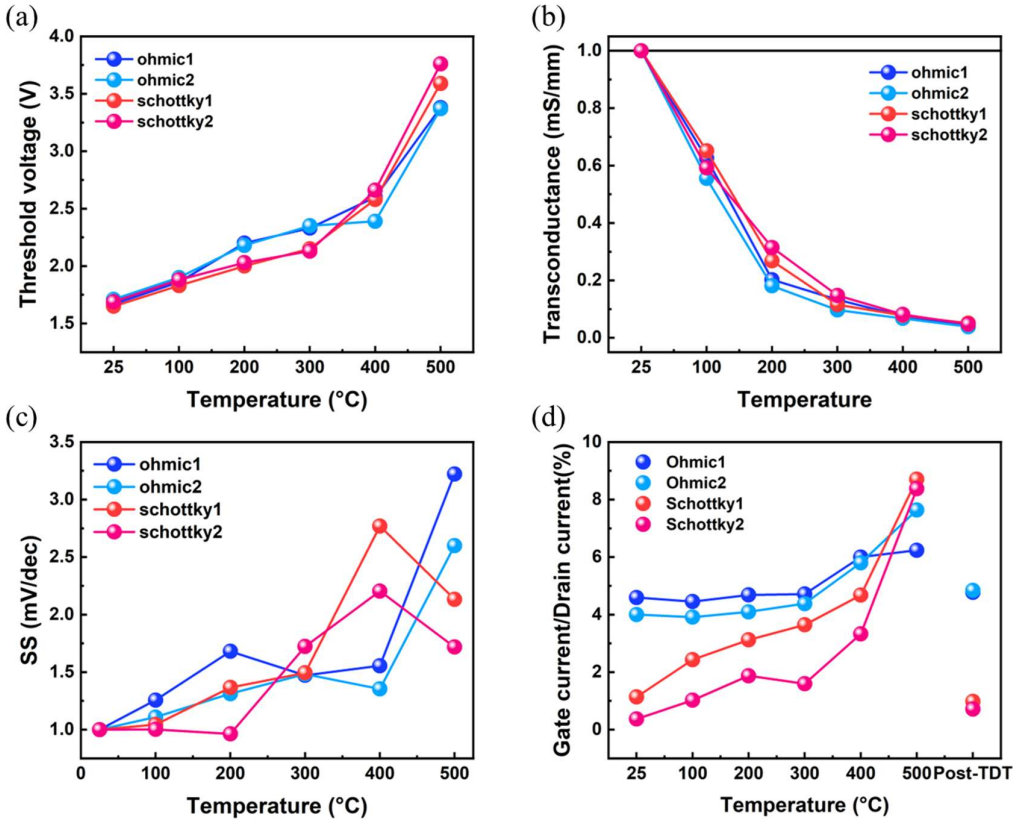

Figure 3. Temperature-dependent parameters (**a**) Threshold voltage; (**b**) normalized transconductance; (**c**) normalized subthreshold swing; (**d**) operating gate-current ratio.

3.3. Output Characteristics

After the transfer analysis established the progressive loss of gate modulation capability with increasing temperature, the output characteristics were examined to evaluate how this degradation is reflected in the on-state conduction path. The output behavior was summarized using normalized on-resistance and normalized maximum drain current, as shown in Figure 4. Normalization to the room-temperature value allows the relative thermal stability of each gate-contact scheme to be compared independently of the initial ab-solute current difference between the ohmic and Schottky devices.

Figure 4(a) shows the normalized on-resistance, $R_{ON,norm}$, as a function of temperature. For all devices, $R_{ON,norm}$ increases monotonically with temperature, indicating progressive degradation of the on-state conduction path. This increase is consistent with reduced carrier mobility, enhanced phonon scattering, and increased channel/access resistance at elevated temperature. However, the slope of degradation differs between the two gate-contact schemes. The ohmic devices show a steeper increase in $R_{ON,norm}$, particularly above 300 °C, reaching approximately 7.4–7.9 times their room-temperature values at 500 °C. By contrast, the Schottky devices show a more moderate increase, reaching approximately 4.3–5.0 times their room-temperature values at 500 °C. This result indicates that, although the Pd-ohmic devices provide strong initial current drive, their on-state resistance is more strongly affected by high-temperature operation.

Figure 4(b) presents the normalized maximum drain current, $I_{D,max,norm}$. The drain current decreases systematically with temperature for both gate-contact schemes, reflecting the loss of current-driving capability under high-temperature operation. The decrease is most rapid from room temperature to 200°C and continues more gradually at higher temperatures. Consistent with the $R_{ON,norm}$, the Schottky devices retain a larger fraction of their initial drain current over most of the measured temperature range. In the 200–500 °C range, the normalized $I_{D,max}$ of the Schottky devices

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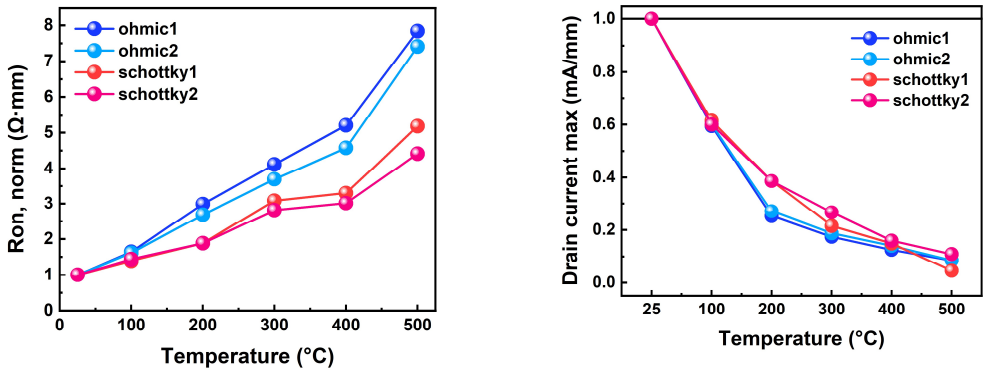
remains higher than that of the ohmic devices, indicating superior relative current retention under thermal stress.

The transfer data showed that gm collapses and I_G/I_D increases as temperature rises, especially in the extreme-temperature regime. The normalized output data further show that the degradation is not limited to gate modulation but also extends to the lateral conduction path. The ohmic gate devices exhibit stronger relative degradation in R_{ON} and $I_{D,max}$, suggesting that the injection-assisted current advantage observed at lower temperature becomes increasingly ineffective as the channel/access resistance increases. Conversely, the Schottky devices show better relative preservation of on-state conduction, even though their gate-current advantage also weakens at high temperature.



(**a**) (**b**)

Figure 4. Temperature dependence of output parameters: (a) normalized on-resistance; (b) normalized maximum drain current.

3.4. Post-TDT Electrical Signatures

The residual electrical changes after TDT were evaluated by comparing the initial room-temperature parameters with those measured after natural cooling to room temperature, as summarized in Figure 5. The ohmic devices show a clear reduction in current-modulation capability after TDT: the transconductance decreases from 83.3 to 52.2 mS/mm and from 107.2 to 89.95 mS/mm for ohmic devices, while $I_{D,max}$ decreases from 201.8 to 163.3 mA/mm and from 200.65 to 195.75 mA/mm, respectively. Although R_{ON} decreases after TDT in both Ohmic devices, from 17.65 to 14.16 Ω·mm and from 18.93 to 14.13 Ω·mm, this reduction does not indicate full recovery or improved gate control because it occurs simultaneously with a decrease in gm and $I_{D,max}$. Therefore, the dominant post-TDT signature of the ohmic gate is not on-state activation but degradation of gate-channel modulation efficiency. In other words, the ability of the Pd gate to translate forward gate bias or gate injection into effective 2DEG modulation becomes weaker after high-temperature exposure.

In contrast, the Schottky devices exhibit apparent on-state activation after TDT. The transconductance increases from 87.45 to 109.4 mS/mm and from 84.25 to 112.45 mS/mm for Schottky devices, while $I_{D,\ max}$ increases from 175.55 to 205.7 mA/mm and from 165.1 to 211.25 mA/mm, respectively. R_{ON} also decreases strongly, from 27.21 to 15.53 Ω·mm and from 27.97 to 15.04 Ω·mm. However, this apparent improvement is accompanied by a pronounced degradation in subthreshold swing, which increases from 129.9 to 189.7 mV/dec and from 146 to 239.6 mV/dec. Thus, the post-TDT Schottky behavior should not be interpreted as beneficial annealing. Instead, the simultaneous increase in gm and $I_{D,max}$, decrease in R_{ON}, and degradation of SS indicate weakened Schottky-barrier or p-GaN depletion control, which makes the channel easier to turn on but degrades off-state electrostatic control. This distinction motivates the thermal-map analysis in the following sections, where the electrical signatures are correlated with heat-source redistribution under identical bias conditions.

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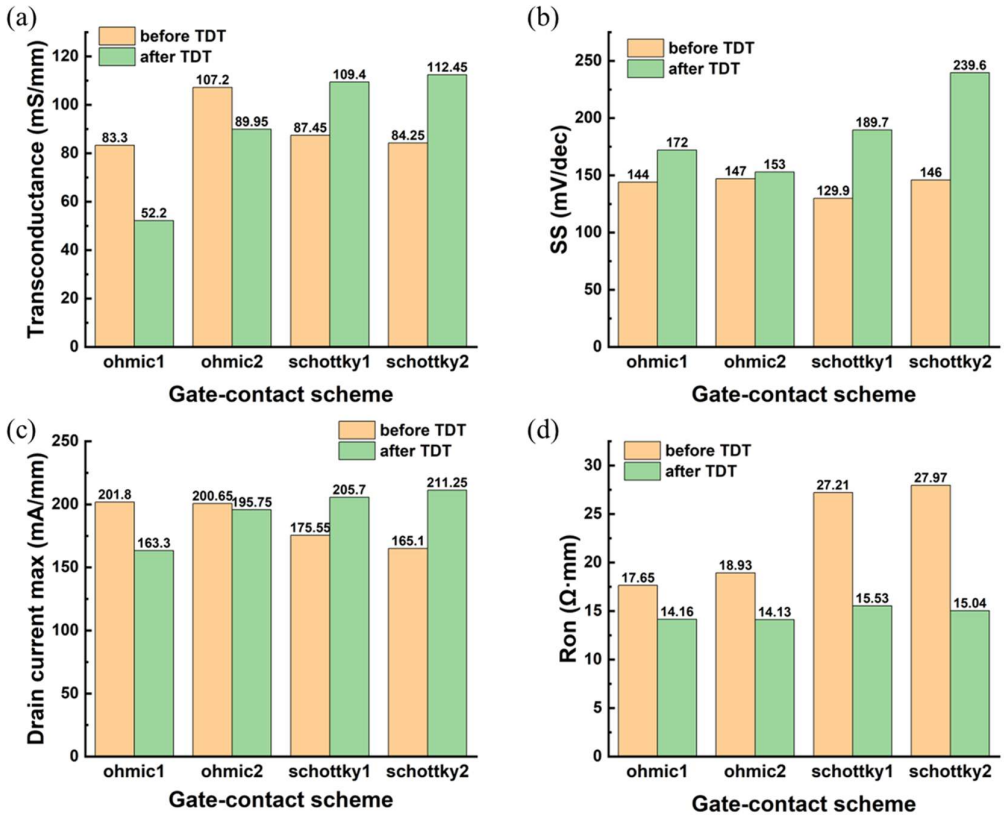

Figure 5. Initial and post-TDT room-temperature electrical: (**a**) transconductance; (**b**) subthreshold swing; (**c**) maximum drain current; (**d**) on-resistance.

3.5. Temperature-Dependent Trade-Off between Ohmic and Schottky Gates

The electrical characteristics show that the preferred gate-contact scheme depends on both temperature and reliability metric. At low temperatures, the ohmic devices provide higher absolute current drive through injection-assisted channel modulation, but this benefit is accompanied by a larger operating I_G/I_D ratio. In contrast, the Schottky devices show lower initial current but substantially reduced gate-current burden. Therefore, from RT to approximately 100 °C, the Schottky gate is more favorable when gate-drive efficiency and leakage suppression are prioritized, whereas the ohmic gate is advantageous only when maximum on-state current is the primary criterion.

In the 100–300 °C range, the Schottky devices provide the more balanced response. They maintain lower I_G/I_D ratio and better normalized retention of $I_{D,max}$ and R_{ON}, indicating that the Schottky barrier remains effective while the dominant degradation is still associated with thermally induced mobility reduction and access-resistance increase. Above approximately 300 °C, however, both gate schemes show severe gm degradation, increasing SS, and rising I_G/I_D ratio. In this regime, Schottky devices may still retain favorable normalized output behavior, but the post-TDT SS degradation indicates that apparent on-state improvement can coincide with weakened gate or depletion control.

At 400–500°C, both gate-contact schemes enter an extreme degradation regime, characterized by strong current reduction, sharp R_{ON} increase, and large I_G/I_D. The low-gate-current advantage of the Schottky gate is no longer decisive because the degraded drain current amplifies the relative gate-current penalty. Thus, operation near 500°C should be regarded as a failure-precursor regime rather than a stable operating window for either contact scheme. Overall, Schottky gates are preferable up to approximately 300°C for leakage suppression and gate-drive efficiency, whereas ohmic gates

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provide stronger initial current drive but are more vulnerable to thermally induced loss of gate-channel modulation efficiency.

Table 2. Temperature-regime-dependent interpretation of ohmic and Schottky p-GaN gate HEMTs..

Temperature range	Dominant electrical behavior	More favorable gate contact
RT-100°C	Ohmic: higher current; Schottky: lower gate leakage	Ohmic for maximum current; Schottky for gate efficiency
100-300°C	Schottky retains lower I_G/I_D and better normalized output	Schottky
300-400°C	gm collapse and SS degradation emerge	Application-dependent
400-500°C	Severe current degradation, high R_{ON}, and large I_G/I_D	No clearly stable option
Post-TDT RT	Ohmic: modulation loss; Schottky: apparent activation with SS degradation	-

3.6. Thermoreflectance Thermal Maps before and after TDT

Figure 6 shows the thermoreflectance thermal maps measured under the identical bias condition of V_{GS}=6V and V_{DS}=10V. The grayscale image indicates the device metallization layout, while the overlaid color map represents the temperature distribution in the GaN active region. The source and drain electrodes are located on the left and right sides of the central channel region, respectively, and the thermal response is therefore interpreted mainly along the narrow vertical active region between the source and drain metallization. Since the maps were acquired under identical external bias rather than identical dissipated power, the observed change in temperature distribution reflects the combined effects of post-TDT electrical degradation, modified channel current, and heat-source redistribution.

The ohmic device exhibits a clear reduction in active-channel heating after TDT. Before TDT, Figure 6(a) shows a continuous hot stripe along the central channel, with the highest temperature contrast concentrated near the gate-edge/channel region. This behavior is consistent with injection-assisted channel conduction in the ohmic gate device, where forward gate bias enhances the channel charge and produces an extended Joule-heating profile. After TDT, as shown in Figure 6(b), the hot stripe becomes weaker, and the high-temperature region is less pronounced. This reduction should not be interpreted as improved thermal stability. Rather, it is consistent with the post-TDT decrease in gm and $I_{D,max}$. Under the same V_{GS} and V_{DS}, the reduced thermal contrast indicates that a smaller fraction of the applied gate bias is effectively converted into channel modulation and drain current. Therefore, the post-TDT cooling of the Pd-ohmic device is a thermal signature of degraded gate-channel modulation efficiency.

In contrast, the Schottky device maintains a stronger and more localized hot stripe after TDT. Before TDT, Figure 6(c) shows a sharp high-temperature stripe along the central gate-edge/channel region, indicating localized heat generation under Schottky-gate operation. After TDT, Figure 6(d) still shows a pronounced localized heating profile, although the spatial contrast becomes slightly redistributed along the channel. This behavior is consistent with the post-TDT electrical signature of the Schottky devices: gm and $I_{D,max}$ increase, while SS strongly degrades. Therefore, the persistent hot stripe should not be regarded as evidence of beneficial recovery. Instead, it suggests that high-temperature exposure weakens the Schottky-barrier or p-GaN depletion control, allowing the channel to turn on more easily under the same external bias while degrading off-state electrostatic control.

Overall, the thermoreflectance maps reveal that the two gate-contact schemes undergo different heat-source transformations after TDT. The ohmic gate shows degradation-type cooling associated with reduced modulation efficiency, whereas the Schottky gate shows persistent localized heating

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associated with apparent on-state activation and degraded subthreshold control. Thus, the thermal maps provide spatial evidence that complements the electrical analysis: post-TDT reliability cannot be judged from the absolute temperature rise alone, but must be interpreted together with the direction of change in gm, $I_{D,max}$, R_{ON}, and SS.

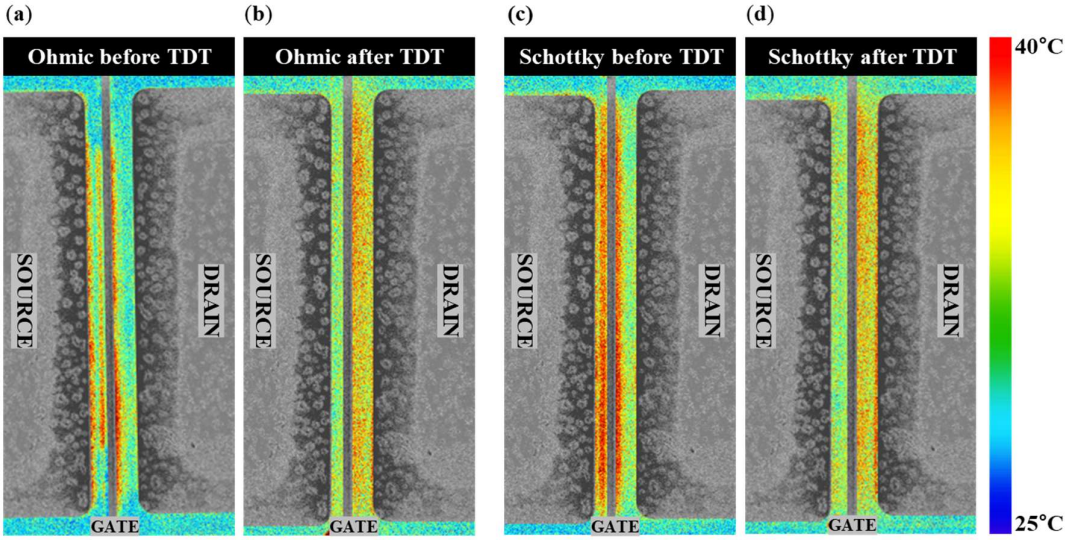

Figure 6. Thermoreflectance thermal imaging (a) ohmic before TDT; (b) ohmic after TDT; (c) Schottky before TDT; (d) Schottky after TDT. The color scale represents the temperature distribution in the GaN active region, while the grayscale image shows the device metallization layout.

4. Conclusions

This study compared Pd-ohmic and Ni-Schottky p-GaN gate HEMTs fabricated on the same GaN-on-Si epitaxial platform by combining temperature-dependent electrical characterization, post-TDT room-temperature recovery analysis, and thermoreflectance thermal imaging. The results show that the relative advantage of each gate-contact scheme depends strongly on the temperature regime and on the metric used for evaluation. The Pd-ohmic devices provide higher initial current drive through injection-assisted channel modulation, but this benefit is accompanied by a larger operating gate-current penalty. In contrast, the Ni-Schottky devices suppress the gate-current burden and retain normalized output characteristics more effectively up to approximately 300°C. At higher temperatures, however, both gate types show severe degradation in gate modulation and on-state conduction, indicating that operation near 500°C should be regarded as an extreme-stress or failure-precursor regime rather than a stable operating window.

The post-TDT results reveal that apparent improvements in individual electrical parameters can be misleading unless on-state, off-state, and thermal signatures are interpreted together. In the Pd-ohmic devices, the post-TDT reduction in gm and $I_{D,max}$, together with the weakened active-channel thermal contrast, indicates a loss of gate-channel modulation efficiency. The resulting decrease in thermal signal is therefore interpreted as degradation-type cooling rather than improved thermal stability. In the Ni-Schottky devices, the post-TDT increase in gm and $I_{D,max}$ and the reduction in R_{ON} occur simultaneously with pronounced SS degradation and persistent localized heating. This behavior indicates apparent on-state activation associated with weakened Schottky-barrier or p-GaN depletion control, rather than beneficial recovery.

Overall, this work demonstrates that high-temperature reliability in p-GaN gate HEMTs cannot be assessed using a single scalar parameter such as $I_{D,max}$, R_{ON}, gate leakage, or peak temperature. A physically meaningful assessment requires separating intrinsic gate-stack leakage from transfer-condition gate-current penalty and correlating electrical degradation with spatial heat-source redistribution. By linking post-TDT electrical shifts with spatial changes in thermoreflectance maps,

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this study provides a gate-contact-resolved view of reliability degradation in p-GaN HEMTs. The results suggest that ohmic and Schottky gates do not merely differ in leakage magnitude or initial current capability but follow different electro-thermal degradation pathways: reduced modulation efficiency in the former and easier channel activation with compromised off-state control in the latter. This interpretation offers a practical basis for temperature-regime-dependent gate-contact selection and highlights the broader need to treat gate-stack stability, heat-source topology, and high-temperature reliability as coupled design parameters in GaN and ultrawide-bandgap power devices.

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Abbreviations

The following abbreviations are used in this manuscript:

HEMT	High electron mobility transistor
2DEG	Two-dimensional electron gas
TDT	Temperature-Dependent Test
TR	Thermoreflectance
SS	Subthreshold swing
V_{TH}	Threshold voltage
R_{ON}	On-state resistance
RT	Room-Temperature
C_{TR}	Thermoreflectance coefficient

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