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Design and Analysis of a High Gain, Low-Noise and Low-Power Analog Front End for ECG Acquisition in 45nm Technology Using Gm/Id Method

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Abstract: In this work, an analog front-end (AFE) circuit for Electrocardiogram (ECG) detection system has been designed, implemented, and investigated in an industry-standard Cadence simulation framework using advanced technology node of 45 nm. The AFE consists of an instrumentation amplifier, a Butterworth band-pass filter (with fifth-order low-pass and second-order high-pass sections), and a second-order notch filter- all are based on two-stage, Miller-compensated operational transconductance amplifiers (OTA). The OTAs have been designed employing the g_m/I_D methodology. Both the pre-layout and post-layout simulation were carried out. The layout consumes an area of 0.0058 mm^2 without the resistors and capacitors. Analysis of various simulation results were carried out for the proposed AFE. The circuit demonstrates a post-layout bandwidth of 239 Hz with a variable gain between 44 to 58 dB, a notch depth of -56.4 dB at 50.1 Hz, a total harmonic distortion (THD) of -59.65 dB (less than 1%), an input referred noise spectral density of $< 34\ \mu$Vrms$/\sqrt{Hz}$ at the pass-band, and a total power consumption of 10.88 μW with a supply of $\pm$0.6 V. Hence, the AFE exhibits a promise of high-quality signal acquisition capability required for portable ECG detection systems in modern healthcare.

Keywords: operational trans-conductance amplifier; Op-amp; ECG; bio-medical applications; filter; low-power CMOS circuits; Gm/Id method; layout; parasitic extraction

1. Introduction

In the last two decades, tremendous and rapid technological advancement has been observed in the world of electronics. The shrinking of feature size (i.e., channel length of a transistor) is a testament to this advancement. Although digital circuits has already been working on technology nodes (interchangeable with channel length) lower than 5nm[1,2], their analog circuit counterparts did not advance at the same pace. For the past two decades, most of the analog circuits has been developed using 180 nm node or above [3–16] because of some benefits enjoyed by the larger technology nodes, for example, ease of design, larger amplification etc. However, in mixed-signal circuits, analog circuits need to be fabricated with the digital circuits on the same chip to meet various purposes[17]. One such analog circuit is an operational amplifier (OPAMP), which usually has two inputs and a single output.

OPAMPs are versatile integrated circuits (ICs) widely used in various applications, including small-signal amplification, filtering, wave generations, arithmetic operations, and analog-to-digital (ADC) and digital-to-analog (DAC) conversion. In recent years, novel OPAMP architectures have emerged [18–21] aiming to enhance their functionality for specific domains. One such critical domain is biomedical electronics, where OPAMPs play a crucial role[22] and serve as fundamental building blocks. In biomedical electronic circuits, OPAMPs need to address the unique features demanded by bio-potential signals (i.e. ECG), which include high amplification (as these signals are inherently weak), low noise levels (to ensure accurate signal acquisition and subsequent processing), and low power consumption. These features become indispensable for portable medical devices such as ECG monitors, where OPAMPs are commonly used for acquiring ECG signals generated by heart

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[23] to enable precise monitoring and diagnosis. OPAMPs are also extensively employed in other medical platforms, including diagnostics, therapy, imaging, and instrumentation. The versatility and adaptability of OPAMPs continue to drive innovation in healthcare technology [24].

Figure 1 shows a typical block diagram of an Analog Front End (AFE) for an ECG acquisition system. This work focuses on the blocks highlighted in this figure.

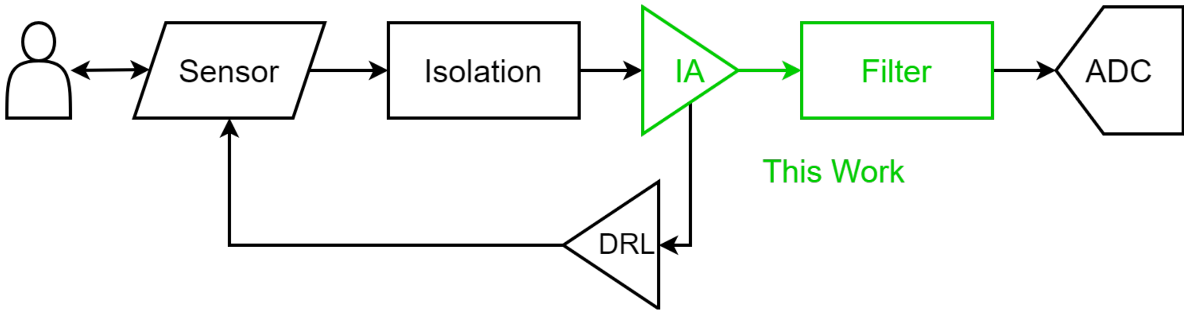

Figure 1. Typical block diagram of AFE for ECG signal acquisition

In comparison with analog circuits, designing digital circuits requires less effort as the input signals are limited to only two voltage levels- logic 1 (HIGH) and logic 0 (LOW). Indeed, digital circuit design principle utilizes the switching (ON or OFF) concept which can be easily realized by transistors, like MOSFET or BJT. But on the other hand, analog circuits deal with continuous signals, comprising of infinite voltage levels. This increases complexity in design. Analog circuits mostly use transistors to amplify signals. Multiple transistors are used to design a circuit that can implement mathematical functions on signals, known as OPAMP. Most of the studies focus on design of OPAMP in larger nodes : on the likes of 180nm or more. Very few study can be found for design in 90nm[25] and 45nm[26,27]. It is due to the fact that below 180nm channel length the transistors suffer greatly from short channel effects. This effect is not accounted for, in widely used long channel model (also known as Ideal or Shockley model). This adds to the design complexity. But lower technology nodes (smaller channel length) can offer great benefits in terms of performance parameters. The long channel model, which is widely used for analog circuit design, is not very accurate for lower nodes. There are other models, such as EKV, BSIM, etc., that can better predict the transistor behavior in lower nodes, but they are too complex to use for analog circuit design, as they involve too many variables and also lacks well established design flow.

The g_m/I_D method can simplify the design process for the designers [28], as g_m/I_D parameter is not dependent on any model equation and is applicable in all regions of operation. For this semi-empirical approach, the necessary curves are generated directly from the simulator, which closely matches the actual measurement. In [29], design and analysis of different OPAMP architectures are discussed, where long-channel MOSFET models are used. It is very difficult to design circuits in low technology nodes (channel length $\leq$ 180 nm) using the long-channel model. The g_m/I_D method explained in [28] provides various examples of design with MATLAB scripts. The method utilizes Look-Up Table (LUT), but it lacks the analysis of circuit to meet multiple specifications such as power, Gain-Bandwidth product (GBW), Power Supply Rejection Ratio (PSRR), Common Mode Rejection Ratio (CMRR) etc. Also, no specific design methodology is discussed in this work and searching values from a table can become tedious and time consuming. The work in [30] describes the use of a licensed software called 'Analog Designer's Toolbox' in short ADT. To use the toolbox, the user needs to provide MOSFET model parameters in written form. The integrated circuit designer's usually have access to realistic models provided by manufacturing companies (such as TSMC). Deriving necessary parameters from these realistic models for the ADT toolbox adds more design complexity. The authors in [31], discuss the design of differential amplifier circuit using g_m/I_D methodology. This work assumes some specifications. The design process involves solving a number of equations using the specifications. In solving these equations, a lot of the unknown variable values are required. In

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finding those variable values, the authors needed more characteristic curves. The work of [32] focuses on design of CMOS Telescopic OTA. The authors only mentioned a design flow using g_m/I_D but didn't explain the flow. The selection of design parameters from g_m/I_D curves or LUT were not demonstrated. All the cited works except [32] lack usage of realistic MOSFET models of various technology nodes (such as 45 nm, 90 nm, 180 nm etc. models from TSMC) resulting in inaccuracy in design to some extent.

In this work, the characteristic curves generated from the simulator (Cadence) using realistic MOSFET model from TSMC (45 nm) are used. 'SPICE' simulators can also be used to generate the curves. An efficient script which can be used to generate all the necessary curves at once is developed. This script can be used inside the simulator. We have developed a design methodology which involves analysis of the selected circuit (2 stage OTA) to meet multiple specifications (Power, GBW, CMRR, PSRR, Noise etc.) through a step-by-step design process using the g_m/I_D curves and optimization approaches. In the proposed design flow, the usage of design equations is minimized, which eliminates the determination of unknown variable values from characteristic curves. As a result, the number of the necessary characteristic curves are minimized. The proposed design flow is presented through a flow chart for better understanding. Using this systematic design process flow, an OTA (interchangeable with OPAMP) in 45 nm technology node is designed, which is used to implement the various blocks - an instrumentation amplifier, a notch filter, a low-pas filter, and a high-pass filter of the proposed ECG acquisition system as shown in Figure 2. The target performance metrics are verified through various simulations which includes transient, ac, stability, noise, common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), total harmonic distortion (THD) etc.

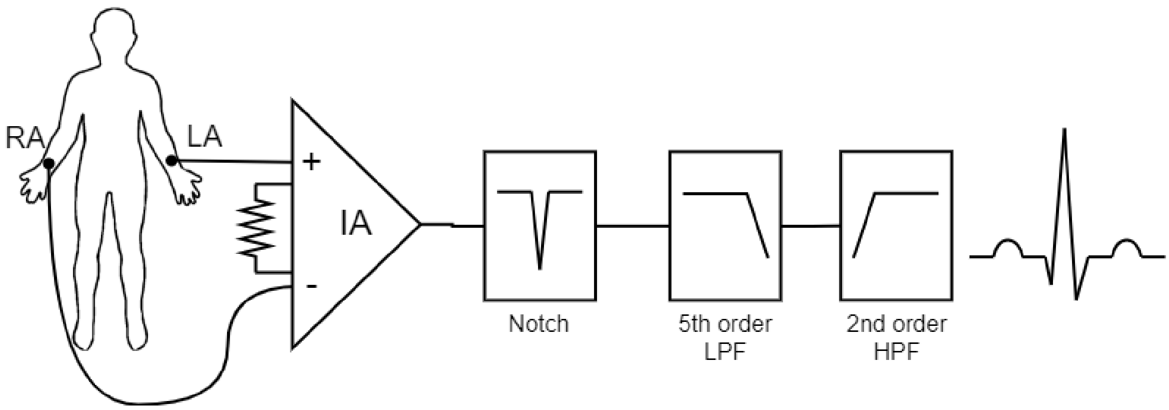

Figure 2. Simplified block diagram of the work in this paper

The paper is structured as follows. Section 2 presents the detail explanation of the developed methodology which includes analysis and design of the OTA. Design constraints and design of ECG acquisition system is explained in Section 3. A simple and brief review on various types of analyses required for analog integrated circuits are mentioned in section 4.1. Section 4.2.1 explains the schematic level simulations of the designed OTA and compares the result with contemporary designs. ECG acquisition system simulations are shown and analysed in Section 4.2.2. Section 4.3 presents the layout implementation and also demonstrates the post-layout simulations of both the OTA and the whole ECG acquisition system. Conclusions of the work are drawn in Section 5. This section includes the comparison with recent reported works.

2. Methodology

This section is divided into two sub-sections. In Section 2.1, a detailed analysis of the OTA circuit is presented and a conclusion is drawn for each MOSFET device's required inversion region, area and g_m/I_D to meet the various specifications. In Section 2.2, the design procedure and optimization of the OTA circuit is explained followed by the design of the AFE system.

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2.1. Analysis of circuit

There are several architectures for OTA [18–21,33]. We have chosen two-stage miller compensated OTA for it's simplicity, robustness and popularity [34]. This architecture can deliver high gain and output swing. Figure 3 depicts the two-stage Miller-compensated OTA circuit. In this OTA, a differential input stage ($M_1 - M_2$) amplifies the input signal, and a common-source output stage ($M_6 - M_7$) provides a high output impedance. A capacitor C_c, following the Miller compensation technique, is inserted between the output and input of the second stage to ensure the stability of the proposed OTA. C_c lowers the gain at high frequencies and reduces the phase shift caused by the parasitic capacitance. Current through M_1-M_3 branch is copied into M_2-M_4 branch through current mirror action of M_3-M_4 load MOS pair. The signal is further amplified by the output stage formed by M_6-M_7 MOSFETs. I_{BIAS} is copied through the current mirror action of M_8-M_5 and M_7-M_5.

An OTA designed for the portable ECG system must provide low-power, low-noise, and high gain[35]. Low power ($V_{supply} \times I_{total}$) demands for lower supply voltage and lower bias current (I_{bias}). Since the proposed OTA is intended to be implemented in 45 nm process technology, a bias of $\pm$0.6 V has been chosen. To ensure lower power, a total current $\leq$1 μA is preferable. Through specification aware analysis of the circuit, the required inversion region can be predicted. Typically, the transistors are kept in the saturation region for amplification purpose. To maintain the MOSFET device operation in the saturation region, Equation (1) needs to be satisfied.

$$|V_{DS}| \geq |V_{GS} - V_{TH}| \tag{1}$$

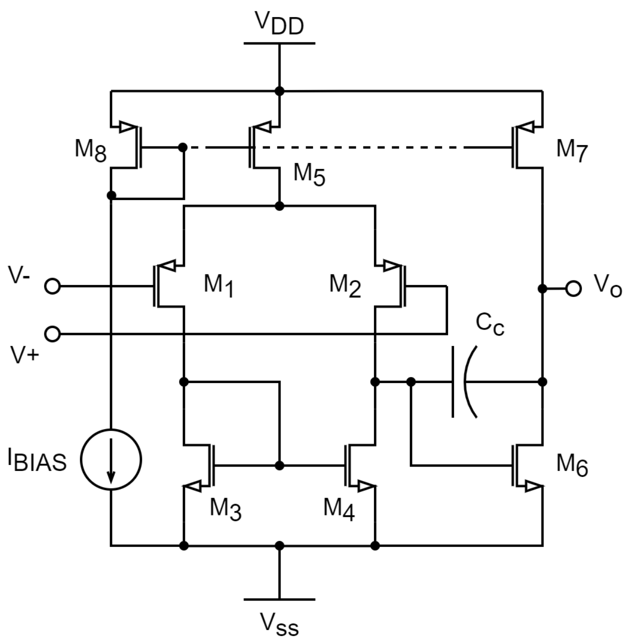

Figure 3. Two stage OTA with Miller Compensation

Power spectral density of the input-referred noise (IRN) voltage of a MOSFET is given by the following equation[36],

$$\frac{\bar{v_i^2}}{\Delta f} = 4kT\gamma\frac{1}{g_m} \tag{2}$$

and for the single-ended differential amplifier (1st stage), we can write from [36]

$$\frac{\bar{v_i^2}}{\Delta f} \propto \frac{g_m \text{ of load}}{g_m \text{ of input}} = \frac{g_{m3}}{g_{m1}} \tag{3}$$

Equation 2 suggests, if g_m is lowered, IRN will increase. However from [36],

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$$g_m \propto I_D, Area \tag{4}$$

So area (WxL) of the active loads should be minimized while area of the input drivers (M_1, M_2, M_6) should be maximized. p-channel MOSFET as input driver was chosen, as it gives less flicker noise compared to it's counterpart n-channel device [37]. For lower power, I_D should be kept small. So the width (W) can be increased to increase g_m, which results in an increase of g_m/I_D, hinting towards the weak or moderate inversion region of the driver MOSFETs.

Again, GBW is related to g_m/I_D through Equation 5[29]. Therefore a high g_m/I_D value required for the weak inversion region causes the GBW to drop.

$$GBW \propto \frac{1}{g_m/I_D} \tag{5}$$

According to Equation 6[29], a higher value of g_m/I_D can cause higher THD.

$$THD \propto g_m/I_D \tag{6}$$

For bio-potential signal acquisition circuits, it is important to keep the THD as low as possible to ensure linear amplification. Thus, a trade-off between noise and THD has to be made. But for the higher gain, g_m/I_D must be increased, as the parameter is related in proportion to intrinsic gain g_m/g_{ds}.

From Equation 7, for a high CMRR, a high value of g_m is preferred to keep a smaller current mismatch between the input drivers M_1, M_2. Also, keeping the device larger reduces the mismatch and short channel effects [38].

$$CMRR \approx \frac{g_m}{\Delta g_m}(1 + 2g_m R_{ss}) \tag{7}$$

For a higher PSRR, it is imperative to have a higher gain for the OTA as per Equation 8 [29],[36].

$$PSRR = \frac{\Delta V_{DD}}{\Delta Vout} = g_{m2} g_{m6} (r_{02}||r_{04})(r_{06}||r_{07}) \tag{8}$$

To realize an OTA for low power with a balanced THD, noise, gain, CMRR and PSRR performance, we have chosen a low bias current (I_{BIAS}), moderate g_m/I_D (moderate inversion) region for the driver MOSFETs and strong inversion for the rest of the devices. Although weak inversion (sub-threshold region) can give higher g_m for a given I_D and hence, higher gain with lower power [39], this region is highly sensitive to the gate voltage and can limit the linearity of the device gain[40]. To reduce the channel length modulation effect we have used higher channel lengths for the devices. Table 1 summarizes the necessary inversion region, area and g_m/I_D for all the devices.

Table 1. Summary of design requirements for individual MOSFETs of the 2 stage miller compensated OTA.

MOSFET	Inversion region	Area	g_m/I_D
M_1, M_2	Moderate	Large	High to Medium
M_3, M_4	Strong	Small	Low
M_5, M_8	Strong	Small	Low
M_6	Moderate	Large	High to Medium
M_7	Strong	Small	Low

The design equations 9 and 10 [29] are used in calculation of g_m/I_D for driver MOSFETs and choosing I_D and Cc of the circuit.

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$$(g_m/I_D)_{1,2} = 4\pi GBW/SR \tag{9}$$

$$GBW = g_{m1,2}/C_C \tag{10}$$

To attain a phase margin of 60 degree, equations 11 and 12 from [29] are manipulated.

$$g_{m6} = 10 * g_{m2} \tag{11}$$

$$C_c \geq 0.22 * C_L \tag{12}$$

where C_L is load capacitance and is a design specification.

2.2. Design Procedure

In the context of the sub-micron design and design complexity, design with available models such as - EKV (Enz-Krummenacher-Vittoz), long-channel (square law) etc. may become difficult. Therefore, we utilized the g_m/I_D method. The developed design and optimization flow implementing the g_m/I_D method is displayed in Figure 4. The inclusion of first decision block (diamond shaped) in the flow-chart, offers greater accuracy of the design.

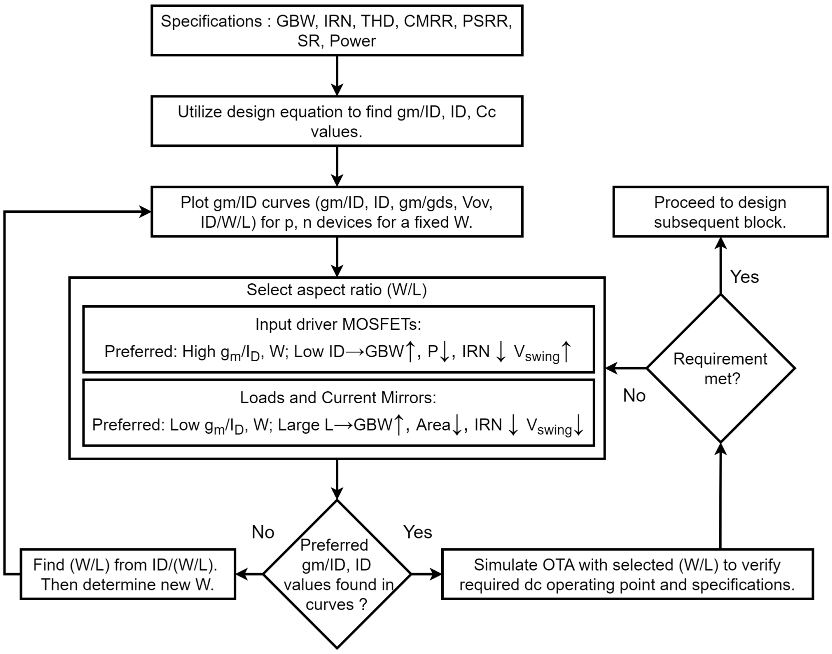

Figure 4. Design flow for design and optimization of OTA.

2.2.1. Parameter Extraction from Literature

The first step in designing the OTA starts with extraction of the specifications from literature review. In order to design a low power OTA, we have chosen a total current of 800 nA and a supply of ±0.6 V. The selected values keep the power of the OTA below 1 μW. In the works of [18–20] the designed OTAs yield gain values between 31.1 to 47.6 dB, the PSRR and the CMRR range between 37.2 to 70 dB and 65 to 105 dB respectively, the THD values were $<$ 1% and the input referred noise spans between 0.12 to 174 $\mu V/\sqrt{Hz}$. In [41], authors investigated various segments of ECG wave and reported minimum required slew rate of < 1 V/s or 1 $\mu V/\mu S$. In this work, we have selected a gain of 60 dB (1000 in linear) and -3 dB frequency of 1.25 kHz for the OTA, as the OTA for ECG acquisition system is designed for a bandwidth of 150 to 1 kHz depending upon it's usage [42]. This produces a

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gain bandwidth product of 1.25 MHz. The slew rate of 0.67 $V/\mu s$ is chosen for design convenience. The load capacitance (C_L) is considered as 2 pF. The specifications chosen for the design of OTA are listed in Table 2.

Table 2. Design specification for the 2 stage miller compensated OTA.

Parameter	Value
V_{DD}	$\pm$0.6 V
I_{BIAS}	200 nA
GBW	1.25 MHz
Slew Rate	0.67 $V/\mu s$
CMRR	High ($\geq 60dB$)
PSRR	High ($\geq 60dB$)
THD	Low ($\leq$ 1%)
C_L	2 pF

2.2.2. g_m/I_D Curve Generation

The schematics of Figure 5 are used for p-channel and n-channel MOSFET's characteristic curves generation. 'vdc' parameter of 'V0' dc source (gate source voltage, V_{GS}) is swept from 0.1 to 0.9 V. The drain to source voltage controlled by 'v1' source, of the MOSFET is kept constant. We set the 'half supply' variable as 0.6 for M_5, M_6, M_7, M_8 and 0.3 for M_1, M_2, M_3, M_4 MOSFETs. The source on the right 'V2' is used only to view the width value of the MOSFET as legend for the generated curves and has no effect on these curves.

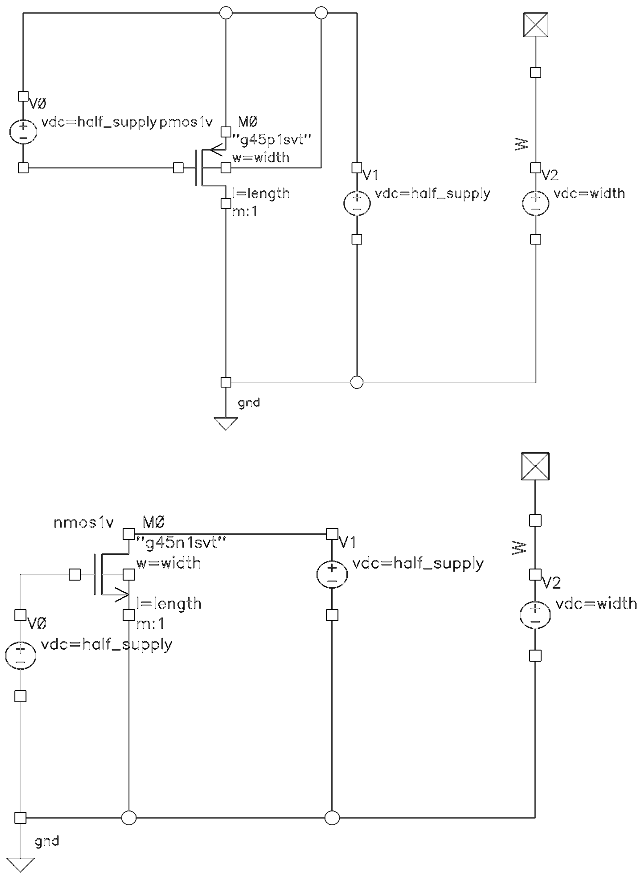

Figure 5. Schematic diagrams for gm/I_D method curve generation. **(Left)** P- channel MOSFET. **(Right)** N-channel MOSFET.

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Variables regarding g_m/I_D method such as g_m (trans-conductance), g_m/I_D (trans-conductance efficiency), g_m/g_{ds} (intrinsic gain), ω_T (transit frequency) and I_D, I_D/(W/L) (current density) are plotted against V_{GS} for various channel lengths (495n, 1u, 5u, 10u) through parametric sweep for both n-channel and p-channel MOSFETs while keeping the width (1u) and drain-source voltage ('half supply' variable) fixed. V_{GS} acts as a common variable between all the other plots. Cross-plotting of the various variables (such as g_m/I_D vs g_m/g_{ds} or I_D or V_{OV} (overdrive voltage) etc.) is done. Figure 6 displays only the g_m/I_D vs V_{OV} plot for L=1μ, 5μ, 10μ. In 45 nm technology node, the simulated Figure 6 shows that the g_m/I_D value varies from 8 to 36. Generally, a lower g_m/I_D refers to the strong inversion region and a higher value refers to the weak inversion region. The moderate inversion region starts from V_{OV} ≥0 mV where g_m/I_D value is nearly 30 $\mu S/\mu A$ for the simulated channel lengths.

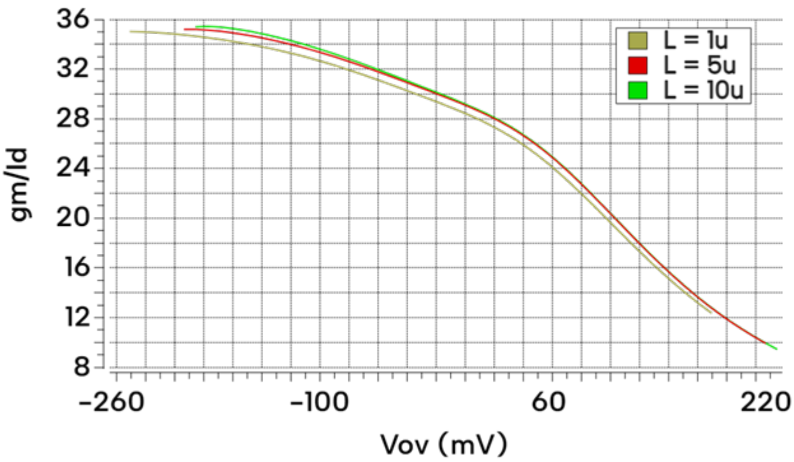

Figure 6. g_m/I_D vs Vov plot for p-channel MOS device at W=1μ and L=1μ, 5μ, 10μ

Although aspect ratio of MOSFETs can be calculated from current density plot (if I_D is known or assumed), we have observed that plotting for a required or selected 'width' gives more accuracy in circuit level simulation. In our case, we have chosen 100 nA current to flow through driver M_1 and M_2. We developed an 'ocean script' to generate the various plots. The script can be loaded using 'load' command from 'virtuoso' command window and also from 'SKILL IDE'. 'SKILL' function such as 'ocnYvsYplot(?wavex Id ?wavey gmoverId)' in ocean script will do a cross-plot of 'Id' in Y-axis and 'gmoverId' in X-axis for W = 1 µm. A sample ocean-script has been provided in appendix A where only the g_m/I_D vs I_D plot of pMOS was generated using the schematic in Figure 5(Left). It should be mentioned that the schematic must be simulated beforehand. Then the script can be utilized.

2.2.3. Aspect Ratio Selection from g_m/I_D Curves

In order to determine the aspect ratio, we have selected the drain to source voltage, V_{DS} of each MOSFET. A good distribution of total supply (0.6 + 0.6 = 1.2 V) at the first stage would be as follows : 0.6 V to M_5, 0.3 V for M_1, M_2 and 0.3 V for M_3, M_4. For the second stage, the distribution of the total supply may be equal (in M_6, M_7), as it will ensure no off-set voltage at the output. The TSMC 45nm (gpdk45) technology file has a maximum limit of channel length value of 10µm. The aspect ratio has been selected considering this constraint.

Aspect Ratio for Input Pairs (M_1, M_2):

For a GBW of 1.25 MHz and SR of 0.67 V/μs, the value of 23.6 $\mu S/\mu A$ for g_m/I_D is calculated from Equation 9. From the g_m/I_D vs I_D curve in Figure 7(a), a g_m/I_D value of 23.769 (close to 23.63) for 100 nA is selected for L=5 µm. So, g_{m1} becomes 2.37 μS for 100 nA. In the first stage, we wish to

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achieve a gain (A_{V1}) of at least 30 dB (33 in linear) so that the remaining gain can be achieved from the next stage. The calculated ($g_{ds1} + g_{ds3}$) for a gain of 33 is 71.8 nS according to equation 13 [29].

$$A_{V1} = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \tag{13}$$

To achieve a gain of at least 30 dB, the denominator must be $\leq$ 71.8 nS. If we distribute 71.8 nS equally in the two terms in the denominator, we find g_{ds1} = 35.9 nS. So the requirement for g_m/g_{ds} of M_1, M_2 is 66. Using the g_m/g_{ds} vs g_m/I_D curve for the selected L=5 µm, the g_m/g_{ds} is found as 52.5 from Figure 7b, which is closer to the requirement (<66). This gives a g_{ds} value of 45.1 nS. The Vov value is obtained from Figure 7c as 70.22 mV for g_m/I_D = 23.769 $\mu S/\mu$A and L = 5 µm. This value helps determine the required dc bias voltage at the gates of the input pairs. The selected width is 1 µm.

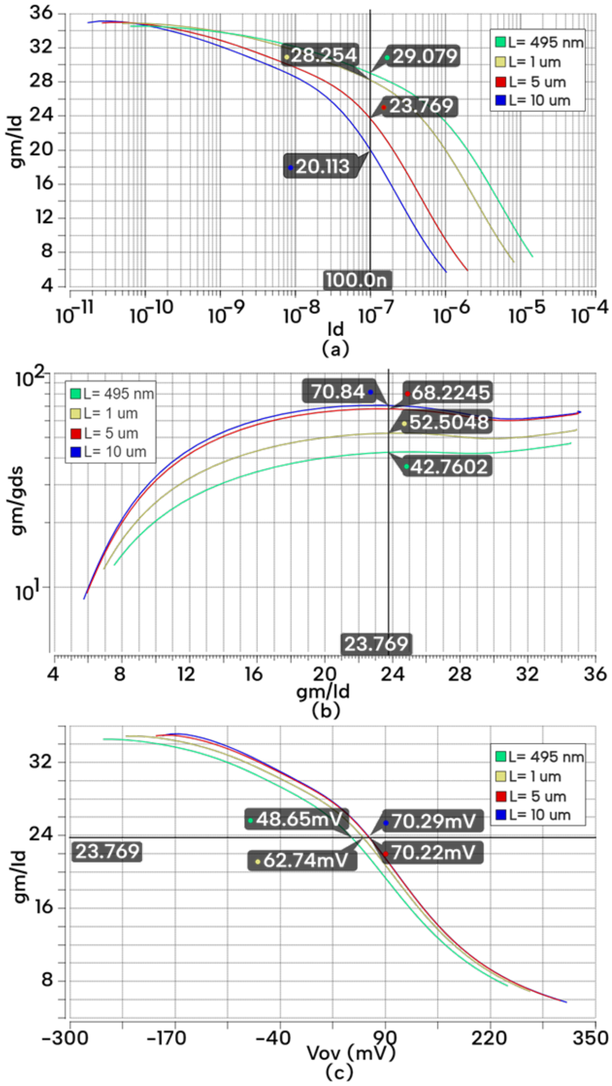

Figure 7. Characteristic curves for the input pairs (M_1, M_2). (**a**) g_m/I_D vs I_D for W=1 µm. (**b**) g_m/g_{ds} vs g_m/I_D for W=1 µm. (**c**) g_m/I_D vs Vov for W=1 µm.

Aspect Ratio for First Stage Active Loads (M_3, M_4):

To satisfy the gain requirement of the first stage, the g_{ds} of M_3, M_4 must be $\leq$ (71.8 nS - 45.1 nS) = 26.7 nS. Also the analysis in the previous sub-section 2.1 sub-section indicates a selection of strong inversion (low g_m/I_D) region for M_3, M_4. From Figure 8a, the g_m/I_D is found as 17.11 $\mu S/\mu A$ for 100 nA drain current at L = 10 µm and for the same length and g_m/I_D value, the g_m/g_{ds} is obtained as 49.6

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from Figure 8b. The calculated gm and gds values are 1.711 uS and 34 nS respectively. Although the gds value is higher than the requirement (>26.7 nS), we have proceeded with this value for the first iteration. The selected width is 1 μm.

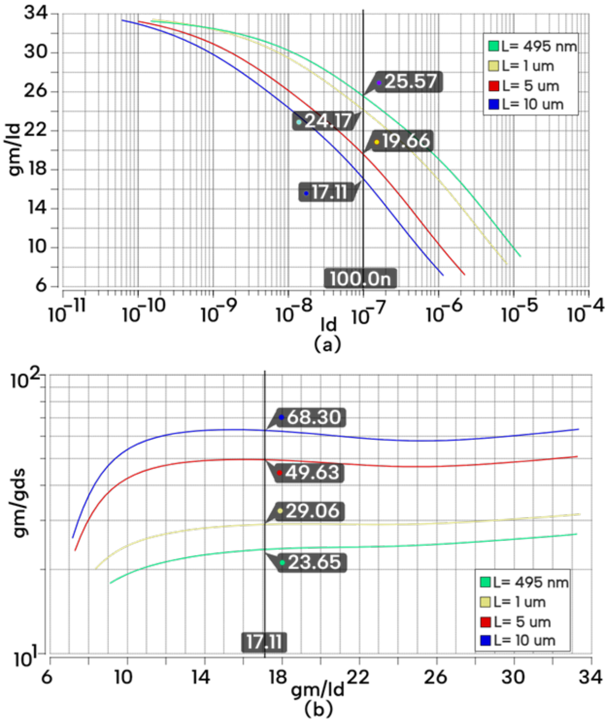

Figure 8. Characteristic curves for the active loads (M_3, M_4). (**a**) g_m/I_D vs I_D for W=1 μm. (**b**) g_m/g_{ds} vs g_m/I_D for W=1 μm.

Aspect Ratio for Tail Current Source (M_5, M_8):

The tail current source must be designed to provide a current of 200 nA. When designing the tail current source, choosing the overdrive voltage is crucial. As per our analysis, we need strong inversion region which means a lower g_m/I_D for the current source. Equation 14 [36] establishes an inverse relationship between g_m/I_D and V_{OV}. So, we will choose a high V_{OV}.

$$g_m/I_D = \frac{2}{V_{OV}} \tag{14}$$

By choosing a high V_{OV}, a more stable current can be achieved regardless of the small variations at the gate voltage. This will lead to more symmetrical operation of the input pairs and less current mismatch between them. As a result, differential gain (A_D) will increase while lowering the common-mode gain (A_{CM}). This leads in achieving a high CMRR as suggested by the Equation 15 [36] .

$$CMRR = \frac{A_D}{A_{CM}} \tag{15}$$

From Figure 9a, for a 200 nA current, the lowest g_m/I_D is found as 15.78 $\mu S/\mu A$ for L=10 μm. This g_m/I_D value provides a g_m/g_{ds} of 85.39 from Figure 9b and a V_{OV} of 137.3 mV from Figure 9c for the same length. **Aspect Ratio for Second Stage Input Driver (M_6):**

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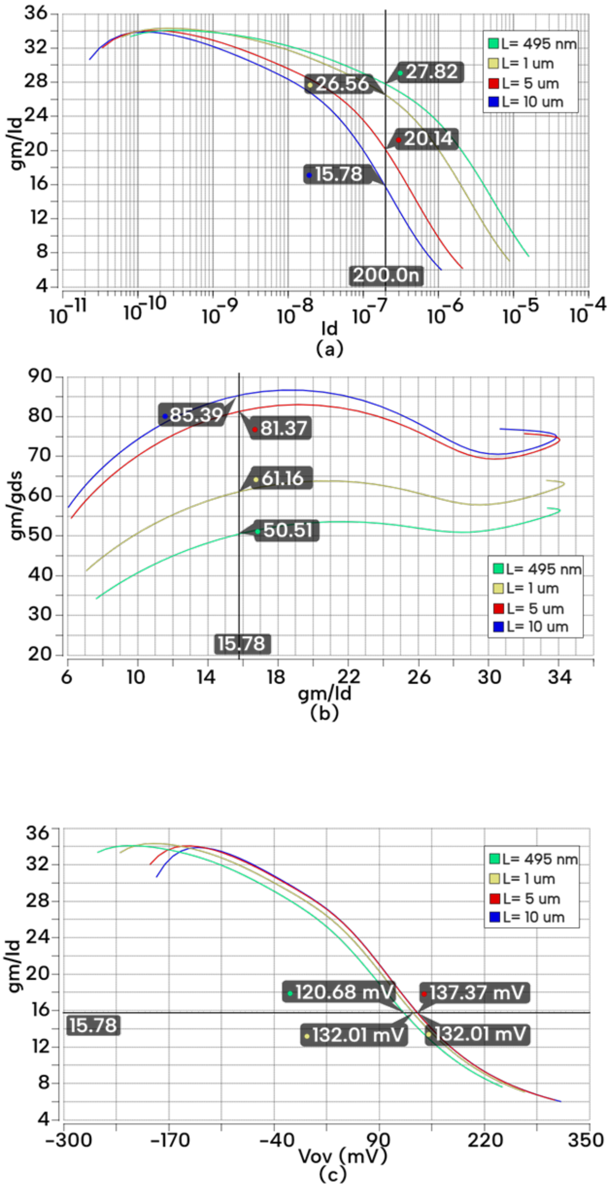

Figure 9. Characteristic curves for M_5 and M_8. (**a**) g_m/I_D vs I_D for W=1 µm. (**b**) g_m/g_{ds} vs g_m/I_D for W=1 µm. (**c**) g_m/I_D vs Vov for W=1 µm.

The simulation carried out only for the first stage using the chosen aspect ratios provides 385.7 mV as the biasing voltage (V_{GS}) of second stage input driver MOSFET (M_6). Also a gain of 38.21 dB (81.38 in linear) is acquired at the output of the first stage. For the requirement of a gain of at least 1000 (60 dB), at least a gain of 12.29 at the second stage is needed. The requirement of g_m/I_D for M_6 is same as the input pairs i.e. g_m/I_D = 23.76 $\mu S/\mu A$.

Using the Figure 10c, a drain current of ~550 nA (close to the requirement of 600 nA) for V_{GS} = 385.7 mV has been selected. The channel length at this condition is obtained as 495 nm from this figure. A g_m/I_D value of 21.01 (close to 23.76) and a g_m/g_{ds} value of 24.082 are obtained at this channel length from Figure 10a and Figure 10b respectively. The gm6 value is then calculated as 11.55 μS. The second stage gain is given by the equation 16 [36].

$$A_{V2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} \tag{16}$$

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Using equation16, the calculated $(g_{ds6} + g_{ds7})$ = 940 nS. If $g_{ds6} = g_{ds7}$ is assumed, then $g_{ds6} = g_{ds7}$ = 470 nS and, the required g_{m6}/g_{ds6} is 24.5 , which is slightly higher than the selected value of 24.082. The width of M6 is 1 µm.

Aspect Ratio for Second Stage Active Load (M_7): The first stage simulation delivers a bias voltage, V_{GS} of 424.8 mV for M_7. The analysis of circuit favors the use of strong inversion for M_7. From Figure 11c, the length of M7 is chosen as 3 um for the desired current value of 550 nA at VGS = 424.8 mV. This channel length gives g_m/I_D = 17.15 $\mu S/\mu A$ from Figure 11a and g_m/g_{ds} = 77.84 from Figure 11b. The necessary gm is calculated as 9.43 uS and the gds is 122 nS (< 470 nS). This yields a gain larger than the preferred gain of 12.29 at the second stage. The width is 1 µm.

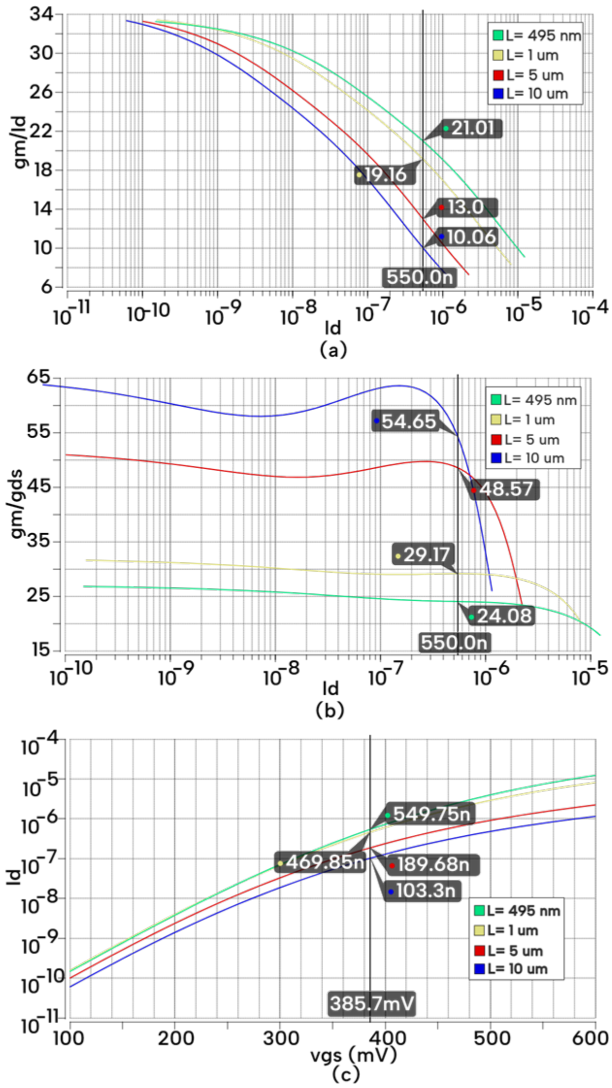

Figure 10. Characteristic curves for the input driver (M_6). (**a**) g_m/I_D vs I_D for W=1 µm. (**b**) g_m/g_{ds} vs I_D for W=1 µm. (**c**) I_D vs Vov for W=1 µm.

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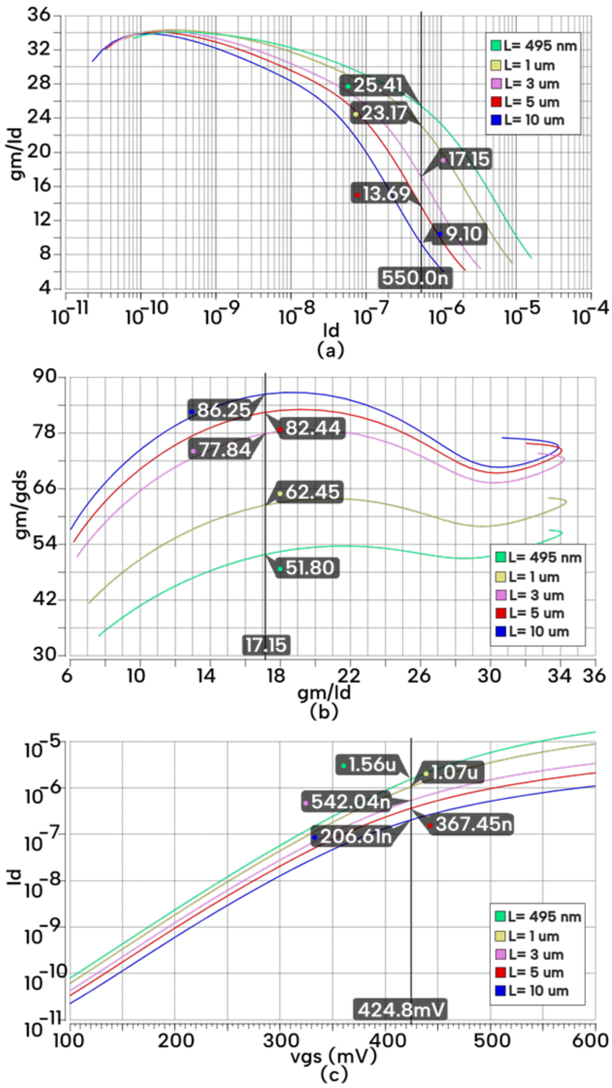

Figure 11. (Characteristic curves for the active load (M_7). **a**) g_m/I_D vs I_D for W=1 µm. (**b**) g_m/g_{ds} vs g_m/I_D for W=1 µm. (**c**) I_D vs Vgs for W=1 µm.

2.2.4. OTA Circuit Simulation and Optimization

The OTA in Figure 3 has been designed in Cadence 'virtuoso' using the selected aspect ratios, as shown in Table 3 and simulated using 'spectre'. The frequency response of the simulated OTA is shown in Figure 12. The simulated gain is 64.5 dB and obtained GBW is 954 kHz which are close to the chosen gain ($\geq 60dB$) and GBW (1.25 MHz) respectively.

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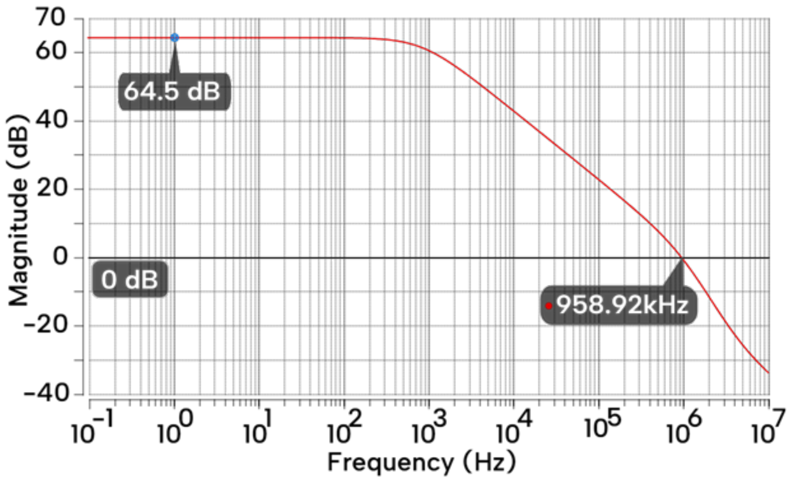

Figure 12. Frequency response of designed OTA for the first iteration.

The Figure 13 shows the dc operating points of each MOSFET devices after simulation. In the first stage, the tail current source drain current (I_{D5}) is I_{D5} = 203.05 nA and in the second stage, the output current (I_{D7}) is 573.036 nA. The simulated drain currents are close to the chosen value (I_{D5} = 200 nA and I_{D7} = 600 nA).

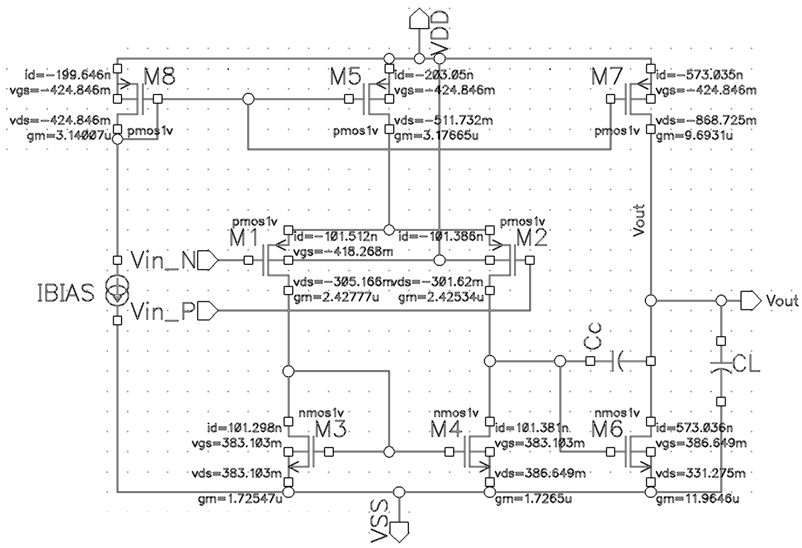

Figure 13. DC operating points of the OTA circuit from simulation.

The dc operating points of the circuit is summarised in Table 3. The simulated g_m/I_D values are consistent with the selected values from the curves.

Table 3. Summary of dc operating point of each MOSFET device for the first iteration.

MOSFET	Aspect Ratio (W/L)	V_{DS}	I_D	g_m/I_D
M_1, M_2	1/5	-301.62 mV	101.38 nA	23.91
M_3, M_4	1/10	386.64 mV	101.38 nA	16.96
M_5	6/10	-511.73 mV	203.05 nA	15.61
M_6	7/5	331.27mV	573.03 nA	20.87
M_7	5/1	-868.72 mV	573.03 nA	16.91
M_8	6/10	-424.84 mV	199.64 nA	15.73

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In order to improve noise performance and to increase V_{DS6} and $I_{D6,7}$, we have re-designed M_6 and M_7 device by increasing their area. Also, at the first stage, we need to match the g_m/I_D of the input drivers perfectly and increase V_{DS5}. Therefore, we re-distributed the voltage as following : V_{DS5} = 0.575 V, $V_{DS1,2,}$ = 0.25 V and $V_{DS3,4}$ = 0.375 V and re-calculated the aspect ratios.

Figure 14 reveals the new choice (final iteration) of g_m/I_D, VOV and g_m/g_{ds} selection for input pairs. The shaded region depicts the moderate inversion region. This can be confirmed from the Figure 15 showing the $fTxg_m/I_D$ vs Vov plot which has a bell shaped curve. The peak value at V_{OV} = 135 mV lies inside the moderate inversion region. It should be noted that the moderate inversion region starts from Vov = 0. The operating point for the driver MOSFETs is 66.85 mV, which is inside the moderate inversion region.

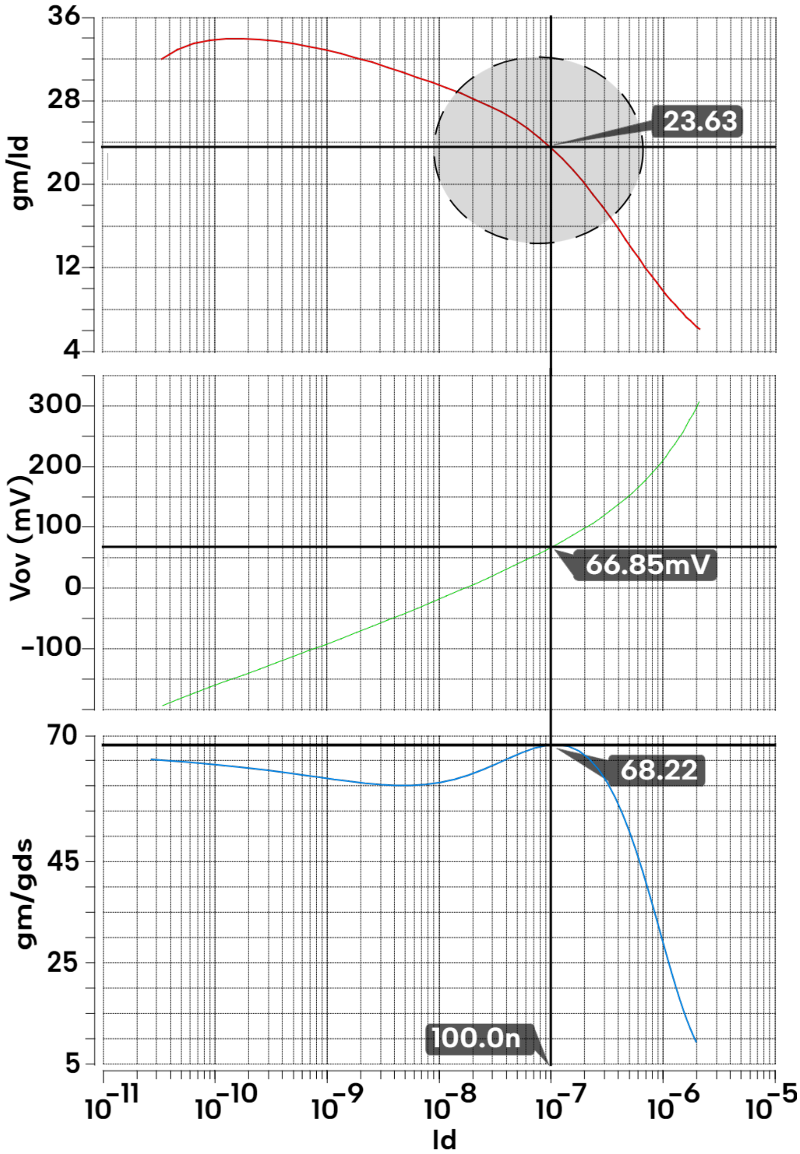

Figure 14. g_m/I_D, Vov and g_m/g_{ds} vs I_D figures for p-channel MOS devices M_1, M_2 for W=1 µm and L=5 µm.

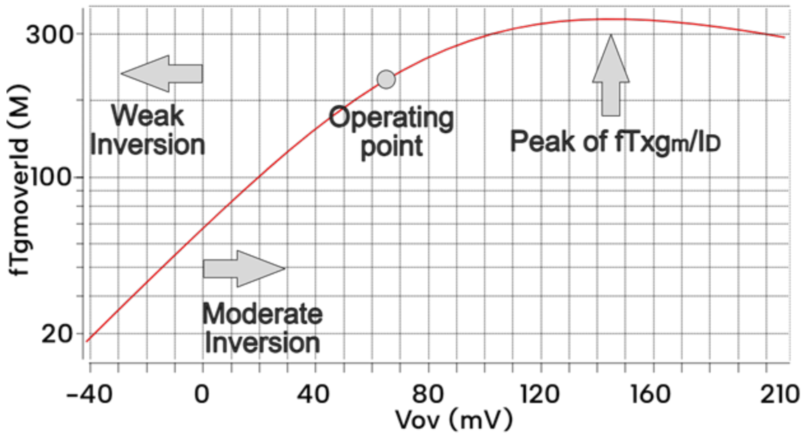

Figure 15. ft x g_m/I_D vs Vov plot for p-channel MOS device at W=1μ and L=5μ.

We have finalized the design after a few iteration. We simulated the OTA for dc, transient, ac, noise, input-output wave shape similarity, gain, power-consumption and input-referred noise analyses. We have tweaked the aspect ratio to meet the requirements (if not met) further and re-ran the simulations. Table 4 summarizes the finalized design of OTA.

Table 4. Design parameters for the 2 stage miller compensated OTA of instrumentation amplifier.

Parameter	Value
V_{DD}	±0.6 V
I_{BIAS}	200 nA
$(W/L)_{M1,M2}$	1 µm/5µm
$(W/L)_{M3,M4}$	1 µm/10 µm
$(W/L)_{M5,M8}$	6 µm/10 µm
$(W/L)_{M6}$	7 µm/10 µm
$(W/L)_{M7}$	5 µm/1 µm
C_c	500 fF

2.2.5. Instrumentation Amplifier and Filter Circuits Simulation and Optimization

We have selected the circuit topology (for individual block) from the literature review and ease of design perspective. Active RC filters were chosen for this work and subsequently Low pass, high pass, notch filters and instrumentation amplifier (IA) circuits were separately designed and simulated. For each individual circuits, the desired gain and component values (resistor and capacitor) were decided from design equation, component sweep and parametric analysis. Initially, the -3 dB (cut-off) frequency was derived from specification. Using the design equations, all the component values were calculated. Then applying sweep and parametric analysis (keeping the calculated values inside the sweep range), we have selected the optimized component values. The design and optimization flow is displayed in Figure 16.

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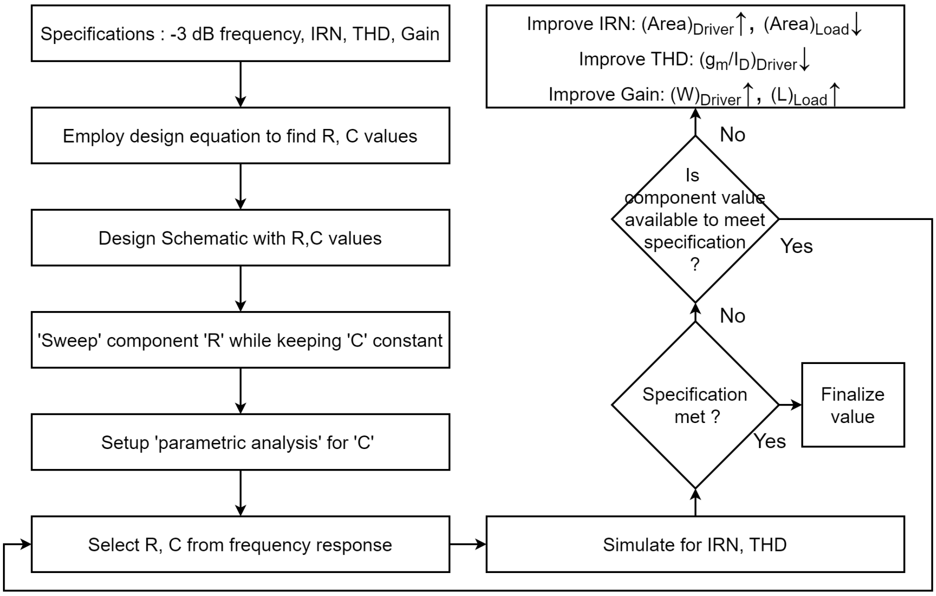

Figure 16. Design flow for design and optimization of filters.

All the individual circuits were tested for ringing-free (oscillation-free) operation, which is ensured by (closed-loop phase margin $\geq 60^o$) transient and ac simulations.

2.2.6. Trade-Off and Optimization for the AFE

Eventually, the individual circuits were cascaded for the realization of the whole system (AFE). We simulated all the necessary analyses to check and verify the operation of the AFE. For the final trade-off and optimization, we analysed the simulated circuit. Minute changes were made to optimize (reduce IRN, power) the individual circuits. For optimization the developed flow of work was followed. Table 5 summarizes the optimized OTAs for different circuits.

Table 5. Finalized aspect ratios for the optimized OTAs.

Parameter	IA	LPF	HPF	Notch
$(W/L)_{M1,M2}$	1 μm/5μm	2.5μm/5μm	1μm/10μm	1μm/5μm
$(W/L)_{M3,M4}$	1 μm/10 μm	1μm/10μm	1μm/10μm	1μm/10μm
$(W/L)_{M5,M8}$	6 μm/10 μm	6μm/10μm	6μm/10μm	6μm/10μm
$(W/L)_{M6}$	7 μm/10 μm	1μm/10μm	1μm/5μm	5μm/5μm
$(W/L)_{M7}$	5 μm/1 μm	0.9μm/0.9μm	10μm/1μm	7μm/1μm

3. ECG Acquisition System Design

Figure 17 shows the full circuit diagram for the proposed AFE for ECG signal acquisition. The system contains a band pass filter with a notch. Two stage OTA's (un-buffered) were utilized instead of 3 stage OTA's (buffered) to reduce the transistor count. As the final stage of the OTA is a common source amplifier, it provides high output impedance. Thus design of filters must employ very high resistance values in order to avoid loading effect. 3 stage would reduce the resistor values but it is difficult to design for necessary phase margin.

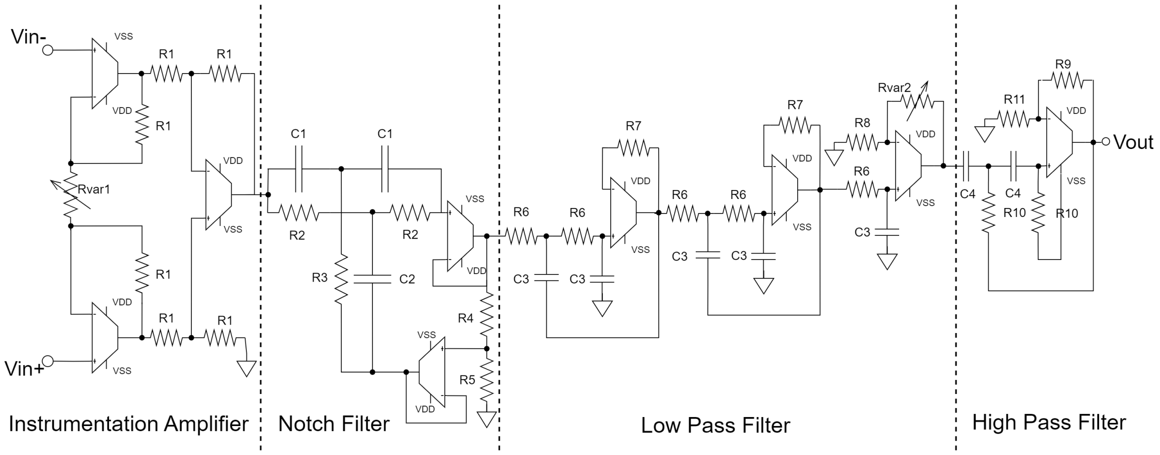

Figure 17. Proposed ECG acquisition circuit diagram.

ECG signal mostly varies from $10\mu V - 5mV$ in amplitude and mostly concentrated between 0.05Hz - 35 Hz frequency[43]. According to [44–46], 0.2mV - 5mV voltage range is considered for the design. Frequency ranging from 0.05Hz - 250 Hz is chosen for design as per [44,47]. [4,48]. The constraints for filters of ECG acquisition system are: (1) Low input-referred noise density (<400μVrms/$\sqrt{Hz}$), (2) High order, (3) Low THD (<-50 dB) and (4) Low power consumption (<50μW) [35]. For the filters, Active-RC topology was used, though Gm-C filter might seem preferable[49]. Gm-C filter can accommodate higher bandwidth but is sensitive to parasitics[50]. In [51], a comparison shows that the Active-R filter performed slightly better than Gm-C filter. In [50], the authors found Gm-assisted Active-RC's linearity is better than Gm-C. The tunability of Active-RC for gain and bandwidth is much easier[52].

An instrumentation amplifier with low noise performance is added as input stage. The gain of the instrumentation amplifier helps the overall noise to decrease[53]. A total of 9 OTA's were used for the 4 blocks.

3.1. Instrumentation Amplifier

Instrumentation amplifier (IA) is used to subtract the two input signals while providing a suitable gain to the whole system. 3 OTA's and 7 resistors (6xR1, Rvar1) are required for the design of IA. 'Rvar1' (R_{gain}) variable resistor can be adjusted to control gain.

$$A_V = 1 + \frac{2R}{R_{gain}} \tag{17}$$

Utilizing the design equation 17 [54], the value of the resistors are determined for a specific gain. To avoid loading effect, R and R_{gain} are selected to be greater than 10 times at least.

3.2. Notch Filter Design

The 2nd block of the circuit is a second-order active Twin-T topology notch filter. 2 OTA's, 3 capacitors (2xC1, C2) and 5 resistors (2xR2, R3, R4, R5) are required in the design of this block. This type of filter usually provides no gain.

$$\begin{aligned} f_N &= \frac{1}{4\pi RC} \\ Q &= \frac{f_N}{BW} \\ K &= 1 - \frac{4}{Q} \end{aligned} \tag{18}$$

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Applying equations in 18 [54], resistors and capacitors value were determined for a high-Q high notch-depth.

3.3. Low Pass Filter Design

The 3rd block of the circuit is a fifth-order butterworth low pass filter. Cascaded topology was used in realizing fifth-order. Though function replacement realization is preferred over other topology[35], cascade active topology is easier to design for required band and additional gain. Two second-order filters followed by a first order filter provide a fifth order filter. To ensure ringing-free operation, a minimum of 45 degree phase margin is required while 60 degree is preferable in the closed loop systems [29,36]. The two second-order sections gain was chosen 0 dB. This ensures more than 60 degree phase margin in the closed loop system. The final section is a first-order section with a gain >0 dB. The 'Rvar2' is a variable resistor to control gain. The LPF block comprises of 3 OTA's, 5 capacitors (5xC3) and 9 resistors (5xR6, 2xR7, R8, Rvar2). The LPF is designed for a higher cut-off frequency of 250Hz which is a requirement of ECG acquisition system.

$$f_c = \left(\frac{1}{2\pi RC}\right) \tag{19}$$

Using the equation 19 [54], capacitor (C) and resistor (R) value are calculated.

3.4. High Pass Filter Design

The final block of the circuit is a second order butterworth high pass filter. For proper biasing condition the inverting input is connected to 'VSS' instead of 'gnd' through R10. This block contains 1 OTA, 2 capacitors (2xC4) and 4 resistors (R9, 2xR10, R11). Ideally for an ECG signal the lower cut-off frequency is 0.05Hz.

$$f_c = \left(\frac{1}{2\pi RC}\right) \tag{20}$$

Employing the design equation 20 [54], capacitor value (C) was calculated after careful selection of resistor value (R).

The designed parameters (resistors and capacitors) of the whole system is summarised in Table 6. The large resistors can be substituted by MOSFETs (operating as resistors).

Table 6. Design parameters for the proposed ECG acquisition system.

Parameter	Value
R1	300 MΩ
R2	32 MΩ
R3	16 MΩ
R4	10 MΩ
R5	99 MΩ
R6	190 MΩ
R7	400 MΩ
R8	900 MΩ
R9, R10	3.5 GΩ
R11	1 GΩ
Rvar1	60 MΩ
Rvar2	200 MΩ
C1	99.2 pF
C2	198.4 pF
C3	1.4 pF
C4	900 pF

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4. Simulation and Results

The section portrays the various simulation results and discusses the findings. A brief introduction to various 'analyses' is given first in Section 4.1. Then pre-layout simulations of the OTA and the proposed ECG acquisition system are shown in Section 4.2, followed by the post-layout simulations in Section 4.3. A comparison with the recent works is stated in Section 4.4. Here, all the simulations were carried out in Cadence virtuoso software using the 45 nm MOSFET model by TSMC.

4.1. Analyses and Test-Bench

A 'symbol' view is given to the schematic of Figure 3. The 'symbol' view contains 7 pins. The view is used to prepare a test-bench schematic (as shown in Figure 18) for various analyses i.e. dc, ac, noise, pole-zero etc.

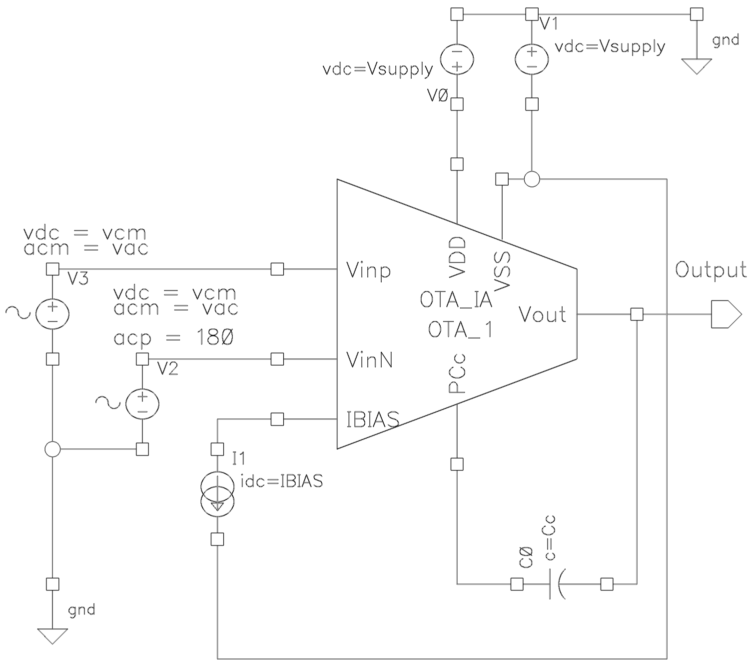

Figure 18. Test-bench for dc, ac, transient, noise, pole-zero analyses.

DC analysis: The dc analysis reveal the biasing (operating) condition of all the MOSFET devices. By this we will be able to verify whether a device is operating in cut-off or, triode or saturation region. Variable 'vdc' is set to common-mode voltage while 'acm' variable is set to 0. Proper biasing current is applied using 'IBIAS' variable. Using 'Vsupply' variable supply voltage is provided. 'Cc' variable sets the coupling capacitor value. These parameter values will be required for most of the analyses.

Transient analysis: Transient analysis is performed to check the circuit operation for change of inputs with time. Proper bias condition parameters are given as in stated in DC analyses. Additionally, for the two inputs (inverting, non-inverting) the 'vsin' source parameter 'Amplitude' and 'Frequency' are set to 1m V and 20 Hz respectively for our simulation. 'Initial Phase for Sinusoid' for inverting source is set to 180. The time-domain output is observed at the 'Output' pin.

AC analysis: With the help of ac analyses, the ac performance metrics such as gain, phase, -3dB frequency (cut-off) and unity gain bandwidth (UGBW) can be measured. Variables 'vdc', 'IBIAS', 'Cc' and 'Vsupply' are set to proper values. 'acm' parameter is set to 1m. The inverting input source 'acp' parameter is set to 180 degree. This sets the two ac inputs to 180 degree out of phase. To observe gain and phase, 'AC Gain & Phase' from 'Direct plot' can be used.

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Pole-zero analysis: For 'pz' analysis, the positive output, negative output and input voltage parameter from 'pz' analysis window are set. The dc biasing is given. Then pole-zero summary can be observed or plotted using 'Main form'.

Noise analysis: One of the key parameter of the system is input-referred noise. It can be measured using the test-bench. Proper biasing needs to be given. 'acm' variable must be set-up for one of the inputs. This input source generate the noise. Then in 'Noise' analyses form, that source must be selected as input. In 'Direct plot', the 'Main form' has the option for noise related curve generation. 'Noise summary' is also an excellent option for input-referred noise measurement.

CMRR analysis: A different test-bench schematic is developed for the CMRR analysis where two same OTA connections are given. One connection is similar to the test-bench shown in Figure 18 and the other has the two inputs tied together to a 'vdc' source only (no 'vsin') to provide a common-mode voltage. CMRR expression is evaluated. Virtuoso calculator is used to create the expression. Usually a higher CMRR is desirable.

PSRR analysis: A different test-bench schematic is developed for the PSRR analysis where output is connected to inverting input via 'iprobe' cell from 'analogLib'. 'xf' analysis is selected for the purpose.

Monte Carlo: This simulation provides the statistical report of different outcomes due to process, variation and temperature (PVT). For the schematic in Figure 18, we choose 'vth' parameter to be evaluated for the variations. The 'dc' parameter expressions can be extracted using 'calculator'. For this simulation, we use 'ADE XL'. The result can be observed in histograms.

4.2. Schematic Level Simulation

4.2.1. Operational Trans-Conductance Amplifier (OTA)

The designed OTA is simulated using 'spectre' using TSMC's 45nm pdk technology with supply voltage of ±0.6 V. The dc analysis confirms the operating condition of all the MOSFET device in the required inversion/saturation region. Figure 19 shows the magnitude response of the OTA which shows that the low frequency (dc) gain is 64.5 dB or 1679 (65.69 at the 1st stage and 25.56 at the 2nd stage), -3dB frequency (cut-off) is at 864 Hz and a unity gain-bandwidth is 1.24 MHz. The choice of 'moderate inversion' region for the driver MOSFET's (M1, M2, M6) with a higher g_m/I_D than in 'strong inversion' region assures the high gain. The 1st stage gain is very close to the chosen g_m/g_{ds} value (68.22 in Figure 14).

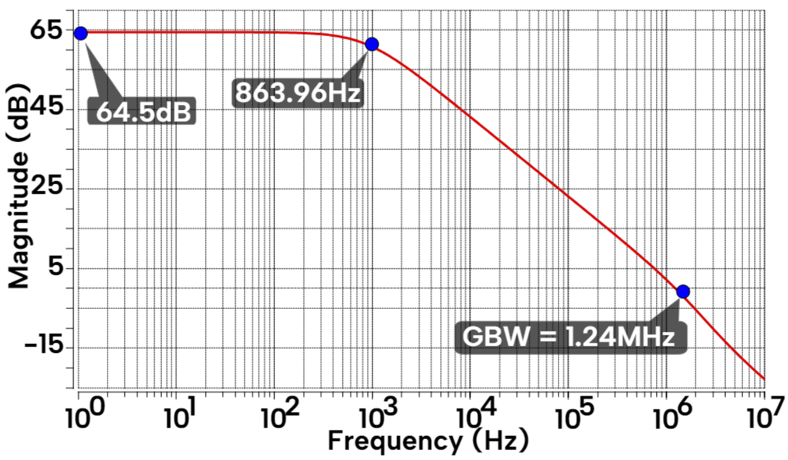

Figure 19. Magnitude response of the designed OTA.

From pole-zero analysis presented in Figure 20, the dominant pole approximately at 843 Hz sets the -3dB frequency. In total 4 poles and 3 zeros are observed. No right half poles but one right half

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zero is observed. The poles are from the input (P4), mirror (P3), first stage output (P2) and the second stage output (P1).

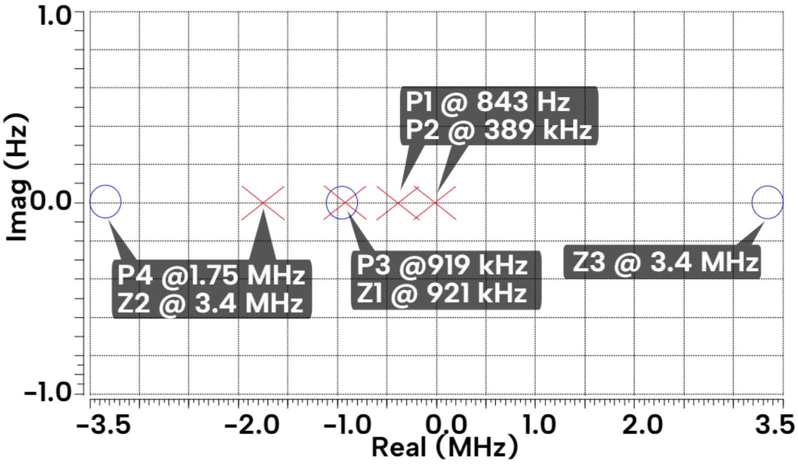

Figure 20. Pole zero map of the OTA.

From the pole-zero diagram, P3 and Z1 nullify each other. The gain starts to decay at frequency 843 Hz (P1) which is further enhanced by the pole P2 at 389 KHz. The gain reaches 0 dB at 1.24 MHz. The pole P4 further increases the negative slope of gain at 1.75 MHz. Taking Bode's approximation into account, the 3 poles before 3.4 MHz create a slope of -60 dB/decade where the two zeros increase the slope to -20 dB/decade. The system shows a phase margin of an acceptable 34 degree.

A common mode rejection ratio (CMRR) of 66.52 dB over a bandwidth of more than 10 kHz is observed in Figure 21 which confirms an attenuation of more than 1000 times for the common noise coming through the two inputs. This is due to the high differential gain from high g_m/I_D value. The low mismatch in g_m values of M_1, M_2 also contributes to this findings. Power Supply rejection ratio (PSRR) of -53.17 and -76.55 dB within 1 kHz bandwidth for positive and negative sources noise are observed in Figure 22. If any noise appear at the power supply, the OTA will attenuate that noise by at least 456 times.

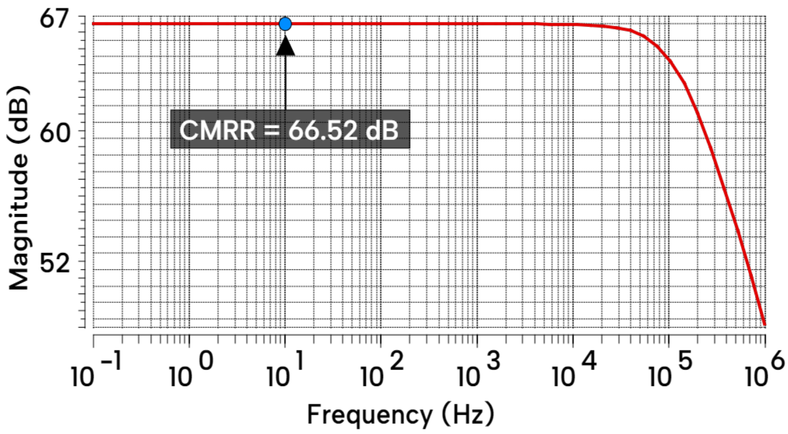

Figure 21. CMRR waveform vs. frequency.

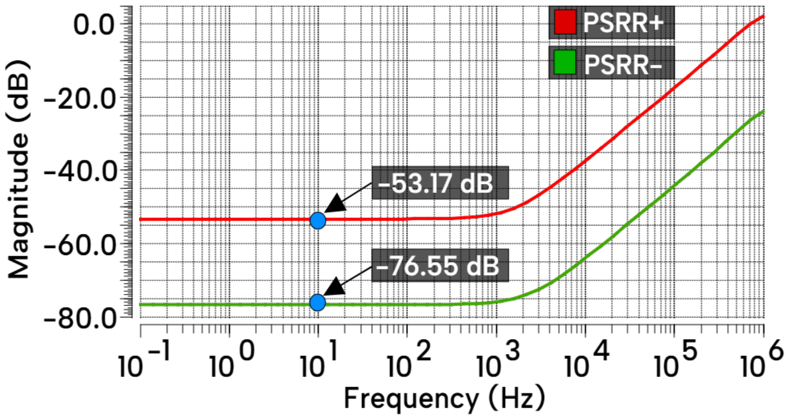

Figure 22. PSRR waveform vs. frequency.

The transient analysis with the given test-bench can be used utilized for THD calculation. This can be done from 'Virtuoso Visualization and Analysis' (also known as 'ViVA' window) in 'Measurements' from Spectrum. Figure 23 displays a Total Harmonic Distortion (THD) of -114.9 dB (less than 1%) for 400 μV peak to peak (p-p) signal at 100 Hz. The THD here is a 2^{nd} order harmonic. Due to differential input, rest of the even order harmonics are nullified.

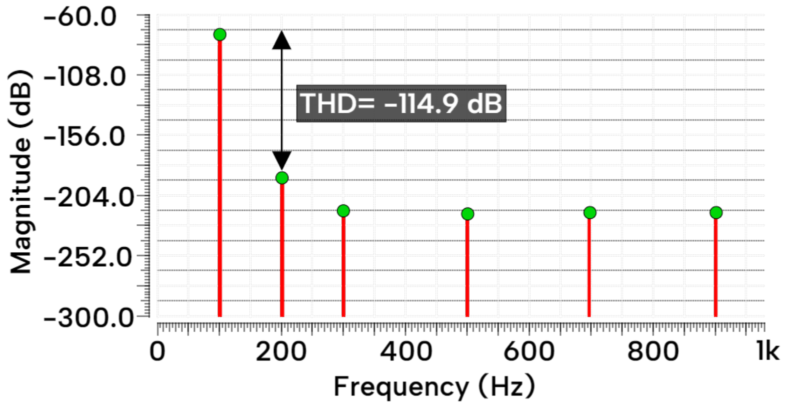

Figure 23. Output voltage spectrum of the designed OTA for an input sinusoidal of 100 Hz and 0.4 mV p-p.

The OTA gives out an output impedance of 2.06 MΩ and a large input impedance of 5.13 GΩ inside the frequency of interest, as seen from Figures 24 and 25. For output impedance measurement, a voltage source is added to OTA's output node. Current is measured at the same node while frequency is varied.

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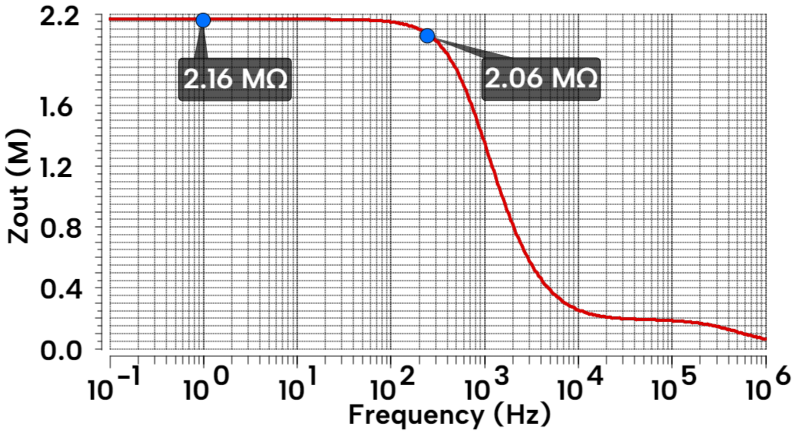

Figure 24. Output impedance of the Operational Trans-conductance Amplifier.

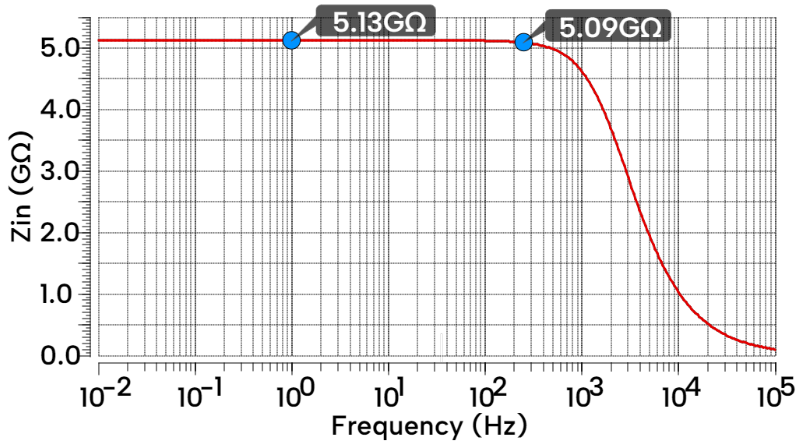

Figure 25. Input impedance of the Operational Trans-conductance Amplifier.

Table 7 summarizes a performance comparison of the proposed OTA with the state-of-the art OTAs. Considering the lowest technology node, the proposed OTA gives the best gain and PSRR, and a comparable power, CMRR, THD, IRN and Zin.

Table 7. Performance comparison of the proposed OTA with previously reported work.

Parameter	This Work	[18]	[19]	[20]
Tech [nm]	45	350	180	180
Topology	Miller-OTA	CR-OTA[1]	GBFC-IBL[2]	MI-OTA[3]
Supply [V]	±0.6	2	± 0.75	± 0.5
I_{Total} [A]	816n	160n	570n	200n
Power [nW]	980	320	855	267.5
Gain [dB]	64.5	39.8	47.6	31.17
PSRR [dB]	76.55	70	-	37.26
CMRR [dB]	66.55	65	105.6	90.05
THD [%]	<1	<1	<1	<1
IRN [μV]	15.9	2.05	0.12 (PSD)	174
Zin [$G\Omega$]	5.1	-	0.3	-

[1]CR-OTA = Current Re-used Operational Trans-conductance Amplifier [2]GBFC-IBL = Gain-boosted folded-cascode with Impedance Boosting Loop [3]MI-OTA = Multiple-Input Operational Trans-conductance Amplifier

The process variation of the technology can change the performance of the OPAMP[55], which in turn can change the response of the circuit. Figure 26 illustrates the Monte Carlo histograms at T=27 ^{o}C for 100 points of threshold voltage parameter. A deviation of nearly $\pm$20 mV is observed from the mean value. The OTA designed in this work has a 72.3 mV difference in gate to source voltage. This ensures appropriate region operation of the MOSFETs. The designers may opt for PVT simulations as it reveals biasing related challenges.

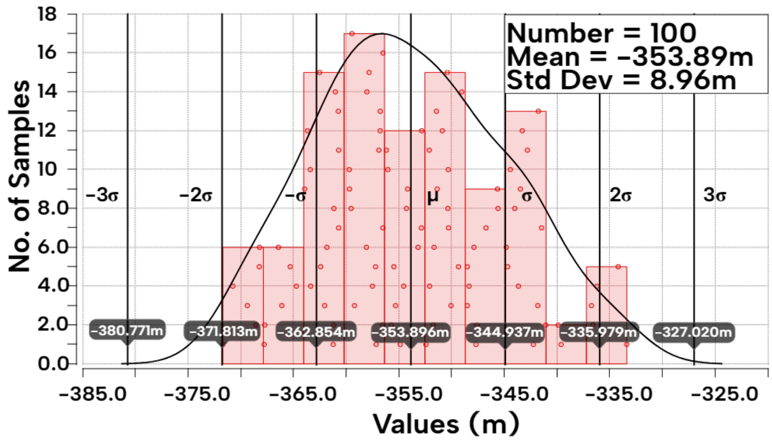

Figure 26. Threshold voltage deviation distribution

4.2.2. ECG Acquisition System

All the filters and instrumentation amplifier are simulated separately before forming the whole ECG system. Various performance parameters, figures are obtained via dc, ac, transient, xf, noise analyses using spectre simulator.

Table 8 summarizes the various performance parameters of the High Pass filter (HPF), Notch filter and Low Pass Filter (LPF) designed for the ECG system. All the individual parameter is within the acceptable value mentioned in [35]. As the first block is an instrumentation amplifier and provides gain, the input-referred noise is reduced for the whole system.

Table 8. Input-Referred Noise, Power Consumption and Total Harmonic Distortion for the filters.

Parameter	2^{nd} order HPF	Notch Filter	5^{th} order LPF
Input-Referred Noise	70.1μVrms/$\sqrt{Hz}$	14μVrms/$\sqrt{Hz}$ @ PB	130μVrms/$\sqrt{Hz}$
Power Consumption	2.034 μW	2.67 μW	1.21 μW
Total Harmonic Distortion	-92.5 dB	-52.1 dB	-112.2 dB

Figure 27 shows the schematic used as the test-bench for the ecg acquisition system. Supply voltages (VDD, VSS) are given as 'stimuli'.

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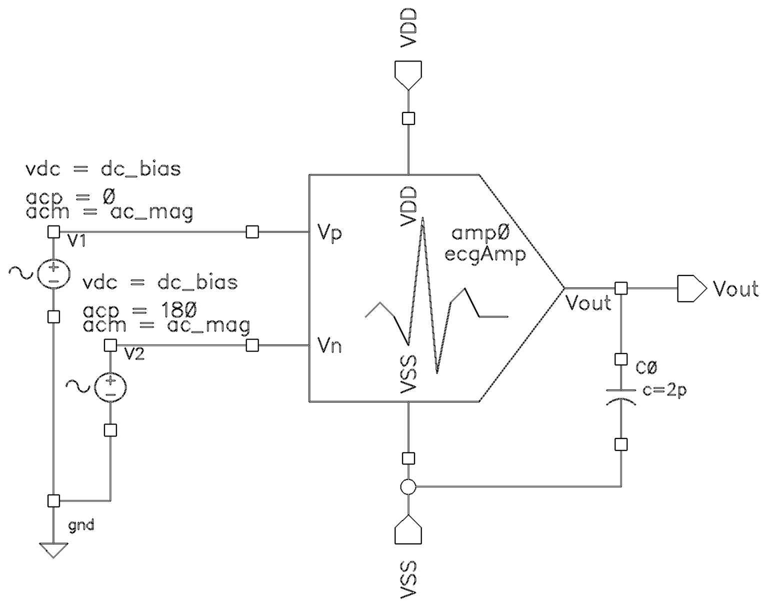

Figure 27. Test-bench for the final ECG acquisition system.

Figure 28 shows the magnitude response of the ECG system. The pass-band gain of the system is 58 dB. The lower cut-off is at 82.24 mHz resulting from the 2nd order HPF poles and the higher cut-off is at 248.15 Hz which is due to the poles of 5th order LPF. Cut-off's of notch filter are at 41.38 Hz and 60.78 Hz. The notch depth is 56.4 dB at 50.1 Hz. These results confirm that the ECG designed in this work can function within the specified bandwidth of the ECG signals, where the 50 Hz power line frequency is selectively notched out.

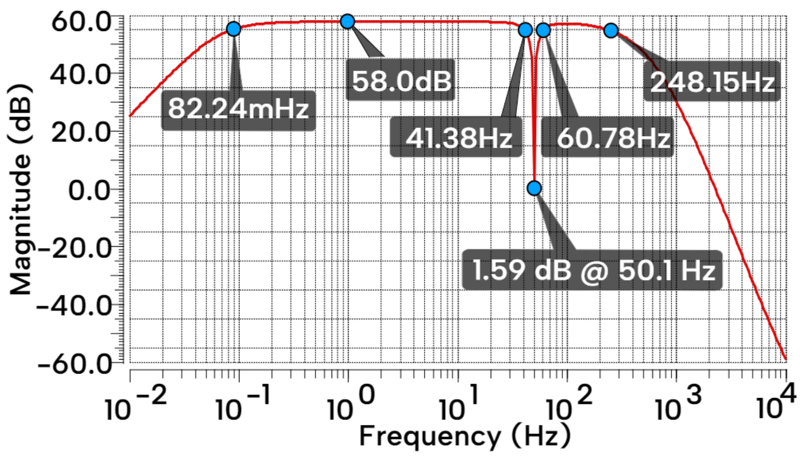

Figure 28. Magnitude Response of the whole ECG system.

Figure 29 verifies the stability performance of the whole system through a pole-zero map. All the poles are situated inside the left half plane (LHP), while few zeros are located at the right half plane (RHP). While Right half plane poles makes the system unstable but zeros don't. Right half plane zeros provides a +20dB/decade gain and -90 degree phase change. This makes it difficult to achieve the desired phase margin, as the gain will increase at that frequency but phase decreases which will reduce the phase margin (total phase change from 0 or 180 degree till 0 dB gain). Since the proposed system reaches 0dB gain near 1 kHz frequency, the effects of the RHP zeros becomes insignificant.

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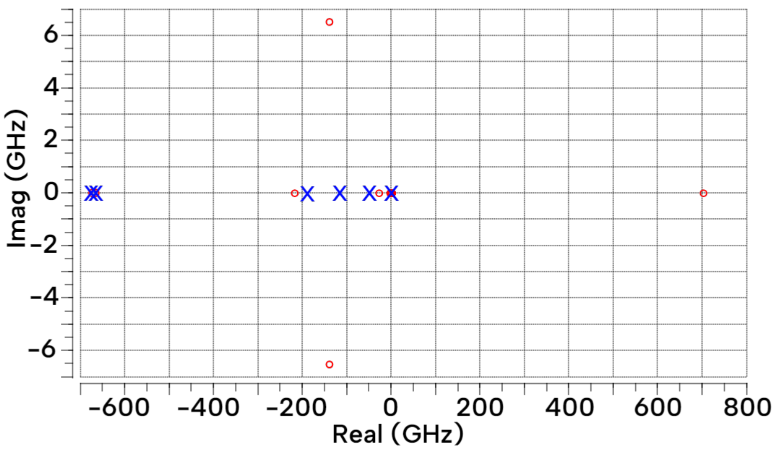

Figure 29. Pole-zero locations of the ECG system.

The input referred noise is demonstrated in Figure 30. Flicker noise is typically a low frequency noise and is high at low frequencies. It decreases with the increase in frequency. From 0.01 to 0.1 Hz, the noise decreases which is a typical behaviour of flicker noise. The notch filter attenuates signal by nearly 56 dB at 50.1 Hz. This will make the signal weak but strong noise at that frequency. Similar behaviour was observed from the figure which shows a large spike of 927.452u input referred noise at 50.11 Hz.

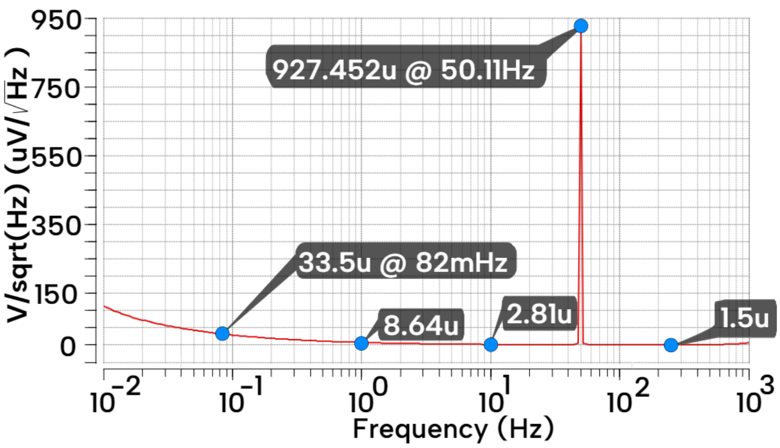

Figure 30. Input referred noise density.

Using MIT-BIH data-set, an ECG signal[56] with added noise at 50 Hz and 500 Hz is fed to ECG system. The overall gain of the system is set to 46 dB by changing the value of variable resistances for gain control. The ECG signal voltage spectrum is shown in Figure 31 (Left) with externally added noise at 50 and 500 Hz. In typical ECG signal spectrum, most of the considerable signal is within 35 Hz range. This can be confirmed by the magnitude from 0 to 35 Hz, which is ranging in between 25-500 μV. The output voltage spectrum of the ECG system is shown in Figure 31 (Right), where it can be seen that noise at 50 Hz is not visible and noise at 500 Hz is reduced while the magnitude of the signal is increased to a maximum value of nearly 26 mV.

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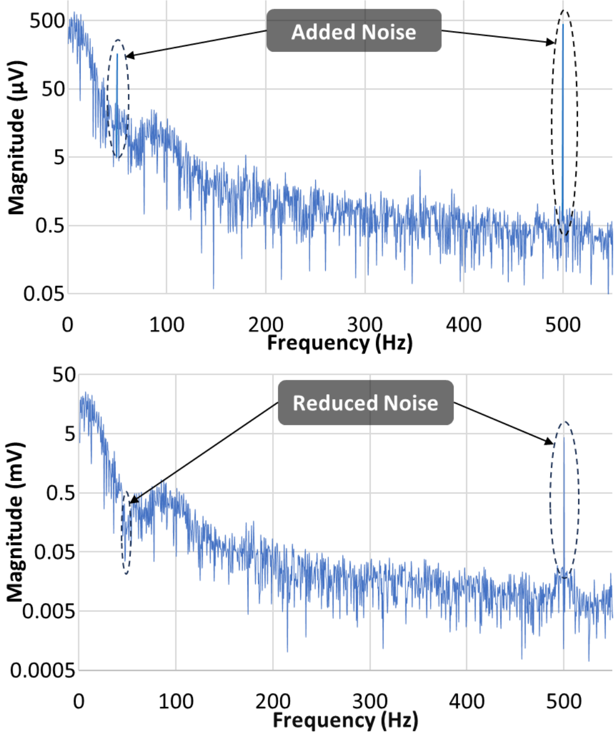

Figure 31. (**Left**) ECG spectrum with added noise at 50 Hz and 500 Hz. (**Right**) Output voltage spectrum of the designed ECG acquisition system.

Figure 32 depicts the time domain signals, where VL (green) and VR (blue) are input signals from electrodes of left arm and right arm respectively. Vout (red) is the output signal from the ECG system. As demonstrated, the noise at the output signal is minimized and can be understood by comparing the haziness of the VL, VR and Vout signals.

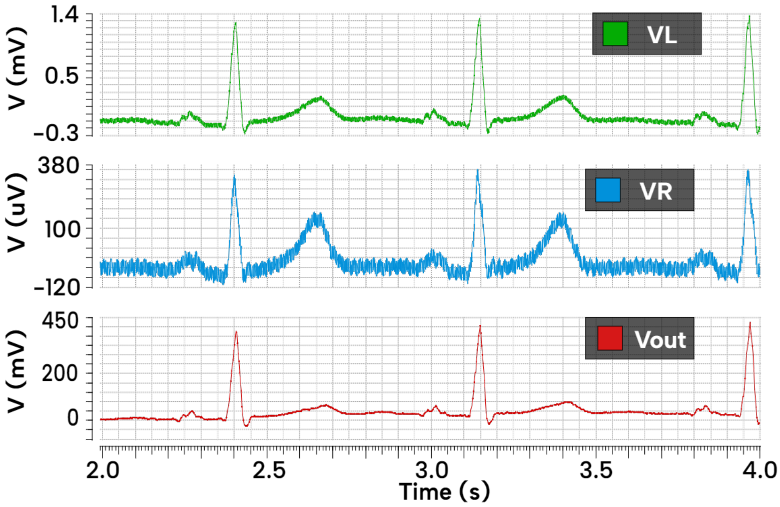

Figure 32. Output of ECG the system for noisy inputs.

THD values in Figure 33 represents system's performance within the range. All THD values are less than - 50 dB. For the ECG signal range (0.2mV - 5mV), the designed system provides good linearity and providing 158 - 797 times larger signal at the output. It is worthy of mentioning that the dc analysis of the whole system has been done to ensure appropriate region of operation of all the transistors.

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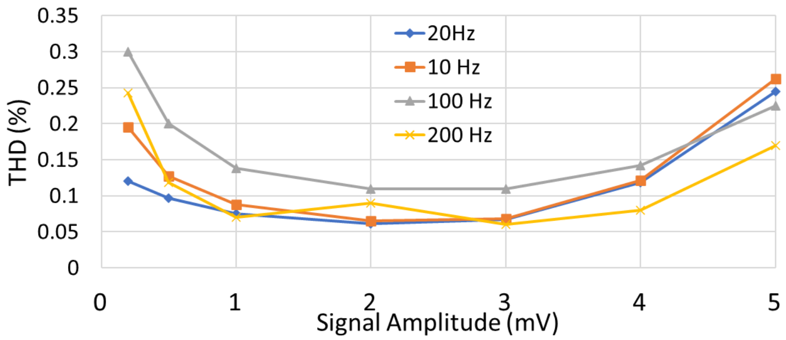

Figure 33. THD for various amplitude and frequency.

4.3. Post Layout Simulation

All the OTA's are design-rule-checked, layouted and extracted using Cadence virtuoso's 'Layout XL' tool (PVS, QRC plugins). For post-layout simulation, a 'config' view is created for the test bench circuit ('schematic' view). The 'config' view is also known as hierarchy editor. From 'config' view, all the OTA's are set to 'av-extracted' view. This 'av-extracted' view contains all the parasitic resistances and capacitance's formed after the layout. Then the test bench 'schematic view' and ADE L (Analog Design Environment) are opened from 'config' view. Again 'spectre' is chosen as simulator for the ADE L. Using the same 'states' from pre-layout simulation (saved previously), simulations are carried out for various analyses.

For the ECG system layout, only the OTA's (total 9) of various blocks (IA, filters - Notch, LPF, HPF) and interconnection between them are considered. All the R, C components are excluded from the layout. Figure 34 and 36 show the proposed layout view of the instrumentation amplifier OTA and ECG system respectively.

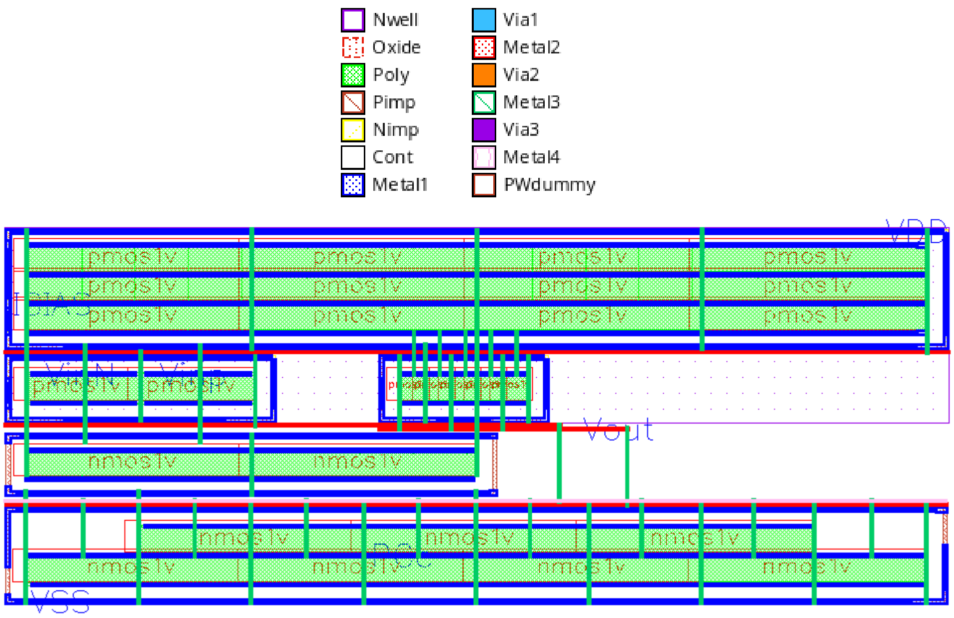

Figure 34. (**Left**) Layers used in layout. (**Right**) Post layout view for the instrumentation amplifier OTA.

Advance layout technique such as common-centroid method is applied for both differential pairs and current mirror inside the OTA's. This helps to reduce mismatch. No dummies are used. But sufficient space is kept for dummies, if required. The used layers for layout is shown in Figure 34 (Left). For routing purpose, only metal 2, 3 and 4 are used, as higher metals have lower resistivity. This reduces voltage drop in interconnects. The direction for metal 1, 3 is kept vertical and for metal 2,

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4 is horizontal. No metal jogging is done. Multiple via's are placed wherever possible. This allows for better signal strength. For block to block inter-connection metal 4 is used. Devices with width greater than 1 µm are broken into smaller multiple devices with width of 1 µm. Guard ring for pMOS and nMOS devices are used to prevent latch-up issue. All the pMOS devices of OTA share a common 'nwell' while nMOS devices share a common 'pdummy'. Top half of the layout is used for pMOS devices and bottom for nMOS devices. Routing symmetry is maintained between M_1, M_2 pairs and M_5, M_8 pairs. This helps in matching. The IA-OTA poses a dimension of 42.58µm x 16.995µm (W x H). The dimension could have been reduced with less gaurd rings and a more compact floor-plan (placement of devices). Though capacitors are not included in the layout, 'mimcap's can be used to implement such capacitors. 'pmoscap' would reduce the area but also reduces the performance of the system, as it incorporates resistance along with it. In 45 nm node, the sheet resistance of various metals would cause a very large area for resistors only. Consequently, we opt for off-chip resistor and capacitor.

Four different layouts and PEX for IA-OTA, Notch-OTA, LPF-OTA, HPF-OTA are done. Figure 35 shows the post-layout magnitude response of the IA-OTA. The gain is slightly increased while -3dB frequency is reduced due to the added parasitics. These changes do not vary much and can be deemed as acceptable.

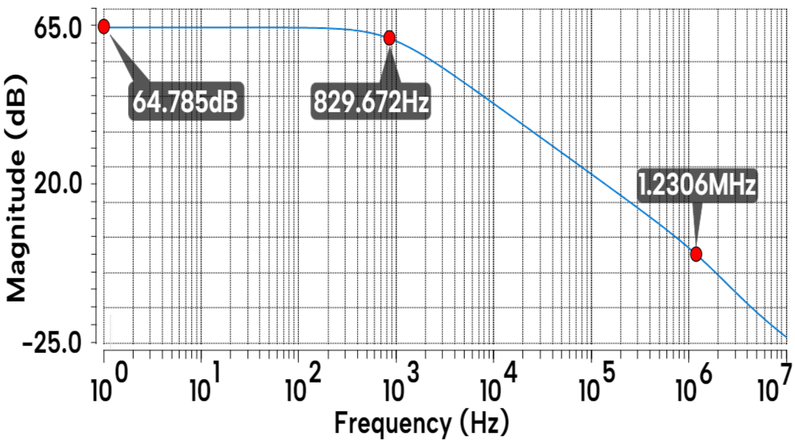

Figure 35. Post layout magnitude response of the instrumentation amplifier OTA.

Finally, layout of the ECG system is designed with the OTA's, as shown in Figure 36. The red marked region is IA, blue is Notch, yellow is LPF and green is HPF block. The layout dimension is 85.62µm x 67.79µm (W x H), occupying an area of 0.0058mm^2.

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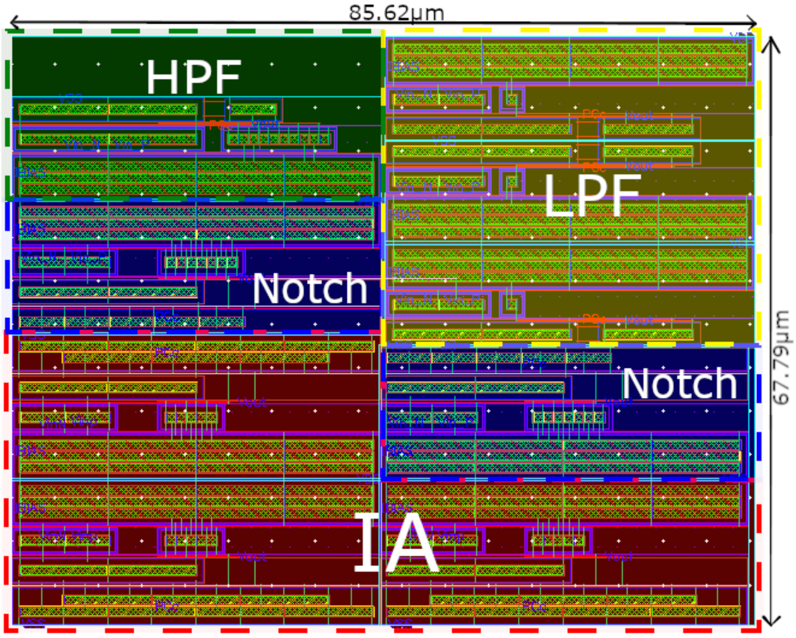

Figure 36. The proposed ECG filter circuit layout.

Figure 37 demonstrates the post-layout frequency response of the ECG acquisition system, where no significant changes are observed. The new bandwidth is approximately 239 Hz, which is only 7 Hz lower than that obtained from the schematic-level simulation.

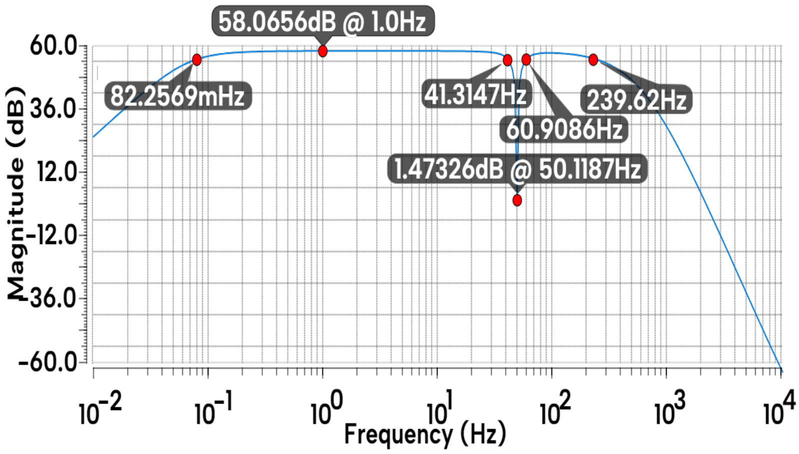

Figure 37. The proposed ECG acquisition system post layout frequency response.

Figure 38 verifies a good similarity in noise performance with the pre-layout simulation. This justifies that the layout has less parasitic effects.

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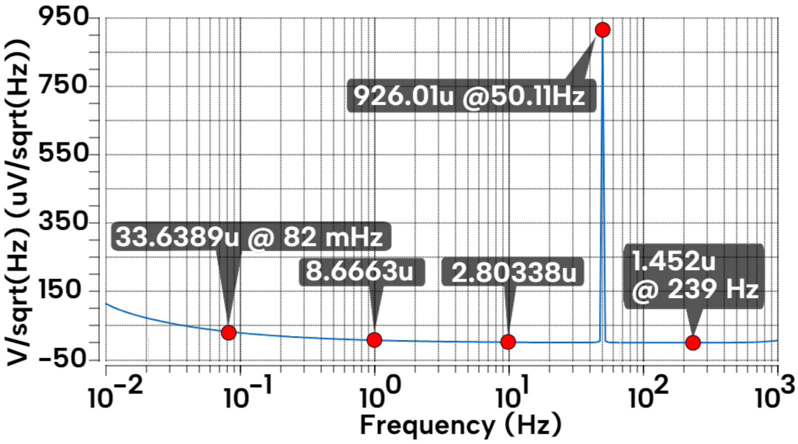

Figure 38. The proposed ECG acquisition system post layout input referred noise.

4.4. Comparison with State-of-the-Art Designs

Table 9 summarizes a comparison of the performance metrics with state-of-the-art designs for ECG acquisition systems. Among the mentioned works, this work utilizes the smallest technology node (45 nm). The order of the filter and gain of the system designed here are the highest among the reported works. This work has the smallest chip area, one of the best input-referred noise with power-line-interference removal capability. Rest of the parameters are comparable. These results highlight the fact that the g_m/I_D methodology developed in this work can be utilized in designing OTA with reduced time and effort.

Table 9. Performance comparison of the designed ECG acquisition system with contemporary designs.

Parameters	This Work[1]	[57][1]	[20][1]	[58][1]	[59][1]	[60][2]
Technology [nm]	45	180	180	180	180	180
Supply [V]	±0.6	1.8	± 0.25	0.5	0.5	1
Order	HPF-2nd, LPF-5th	LPF-2nd	BPF-3rd	LPF-4th	BPF-2nd	LPF-5th
Power [μW]	10.88	19.4	.161	0.003	0.0313	0.041
Gain [dB]	58.06	34.5	0	-5.6	37.1	-7
BW [Hz]	.08-239.6	1.7-352	.1-250	200	1.5-112	250
IRN [μV]	33.6	3.47	198	91.9	17.9	134
PLI Removal	Notch	No	Notch	No	No	No
Area [mm^2]	0.0058 (off-chip RC)	156.25	0.0528 (off-chip cap)	0.074	0.167	0.24

[1] Post-layout simulated.
[2] Measured

5. Conclusions

This paper focuses on the design flow for a low power, low noise and a high gain ECG acquisition system. A two stage OTA is successfully designed using the developed g_m/I_D methodology. All the blocks are designed and simulated separately. Finally they are cascaded to form the band pass filter with a notch (ECG system) to remove power line interference (PLI). The designed ECG acquisition system is simulated at T=27^o C using TSMC 45nm technology in Cadence virtuoso. DC, AC, transient, power, CMRR, PSRR, noise, pole-zero and THD are analyzed. The design is layouted and to fortify confidence in the design, post layout simulations after parasitic extraction (PEX) are done. The AFE successfully de-noised a noisy ECG signal (MIT-BIH dataset). Comparison of the performance metrics with state-of-the designs for both the OTA and the ECG acquisition system implemented in this work shows their superiority considering the lowest technology node used herein. Therefore, the proposed design in this work has excellent promises in the realization of ECG acquisition system for the modern healthcare.

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Abbreviations

The following abbreviations are used in this manuscript:

TSMC	Taiwan Semiconductor Manufacturing Company
MOSFET	Metal Oxide Semi-conductor Field Effect Transistor
OTA	Operational Trans-conductance Amplifier
OPAMP	Operational Amplifier
IA	Instrumentation Amplifier
ECG	Electrocardiogram
CMRR	Common-Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
PEX	Parasitic Extraction
GBW	Gain Band Width Product
SR	Slew Rate
PVS	Physical Verification System
QRC	Quantus RC Extraction
IRN	Input-referred noise
PVT	Process, Variation and Temperature

Appendix A

```
; //SAMPLE OCEAN-SCRIPT FOR GM/ID CURVE GENERATION//
; DESIGN, RESULT, DEFINITION, MODEL FILE DIRECTORY
simulator( 'spectre )
design(  "/home/simulation/pmos_char/spectre/schematic/netlist/netlist")
resultsDir( "/home/simulation/pmos_char/spectre/schematic" )
modelFile(
    '("/pkg/eee/cadence/tech/gpdk045_v_5_0/..
    /models/spectre/gpdk045.scs" "mc")
)
definitionFile(
    "/home/work/save_op.scs"
)
```

```
;DC SWEEP
analysis('dc ?saveOppoint t  ?dev "/V0"  ?param "dc"
?start ".1"  ?stop ".6"  ?lin "50"  )
desVar(   "half_supply" 300m ) ; M1, M2
desVar(   "length" 45n )
desVar(   "width" 1u )
envOption(
'firstRun  t
'analysisOrder  list("dc")
)

temp( 27 ) ; TEMPERATURE SET TO 27

;PARAMETRIC ANALYSIS - 'length' VARIED
paramAnalysis("length" ?values '(4.95e-07
1e-06 5e-06 10e-06)
)
paramRun()

;PARAMETER EQUATIONS
gmoverId =((-getData("M0:gm" ?result "dc"))/getData("M0:id" ?result "dc"))
Id = (- getData("M0:id" ?result "dc"))

;CROSS-PLOTTING
newWindow()
ocnYvsYplot(?wavex Id ?wavey gmoverId)
awvLogXAxis(currentWindow() t)
awvSetXAxisLabel(currentWindow() "Id")
awvSetYAxisLabel(currentWindow() 1 "gm/Id")
addSubwindowTitle("pMOS - gm/Id vs Id")
;//Script finish//
```

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