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*Article*

# Power Control in an On-Board PV Converter Using Disturbance Trend Prediction

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## Abstract

This paper presents a fast adaptive power control with implicit predictive behavior for an onboard power converter operating in support with a 400 Hz aircraft electrical network. Accurate control of active and reactive power in such high-frequency networks requires precise estimation of the network voltage phase, frequency, and amplitude. To achieve this, a novel adaptive phase-locked loop (PLL) algorithm is integrated with a proportional–resonant (PR) current controller. The adaptive PLL continuously estimates the instantaneous phase, frequency, and amplitude of the fundamental voltage component, enabling fast synchronization and dynamic adjustment of the PR controller resonant frequency. This combination familiarizes predictive characteristics into the control loop without the need for computationally intensive model predictive control algorithms. Simulation results demonstrate that the proposed method significantly reduces synchronization time, maintains high accuracy under frequency variations and harmonic distortion, and exhibits robustness against measurement noise. Furthermore, the algorithm's modular and computationally efficient structure makes it suitable for real-time FPGA implementation. The proposed approach provides an effective solution for high-performance power management in aircraft electrical systems, ensuring precise power control under hard dynamic conditions.

**Keywords:** adaptive phase-locked loop; adaptive power control; proportional–resonant controller; aircraft electrical network; 400 Hz power system; FPGA implementation; high-frequency power conversion; synchronization algorithm

## 1. Introduction

The increasing electrification of aircraft systems has led to the development of the so-called more-electric aircraft concept, in which many traditionally hydraulic or mechanical subsystems are replaced by electrically powered devices. This transition significantly increases the importance of power electronic converters in onboard electrical power systems, as they enable efficient power conversion, distribution, and control between different subsystems [1–3].

Aircraft electrical networks typically operate at a frequency of 400 Hz. Compared with conventional terrestrial power systems operating at 50 Hz or 60 Hz, higher-frequency grids enable significant reduction of the size and weight of magnetic components such as transformers and inductors. These advantages are particularly important in aviation applications, where minimizing weight and volume is a key design objective [4].

However, the higher operating frequency also introduces additional challenges for the control of power electronic converters. Because the period of a 400 Hz signal is only 2.5 ms, synchronization

algorithms must provide accurate phase and frequency estimation with very short response times. Even small synchronization delays may significantly degrade the performance of current and power control loops.

Accurate synchronization between power converters and the electrical network is typically achieved using phase-locked loop (PLL) algorithms. PLL structures allow real-time estimation of the phase angle and frequency of periodic signals and therefore play a fundamental role in grid-connected power electronic systems. In grid-interactive converters, synchronization errors may lead to instability or degraded power quality, particularly under conditions such as harmonic distortion, voltage imbalance, or frequency variations [5].

Among various PLL implementations, the synchronous reference frame PLL (SRF-PLL) is one of the most widely used synchronization methods. In this approach, the measured voltage is transformed into a rotating reference frame using the Park transformation, and the quadrature component of the voltage is used as an error signal to control the estimated phase. This structure provides good steady-state accuracy and relatively simple implementation, which has contributed to its widespread adoption in grid-connected converter systems [6].

Despite its popularity, the SRF-PLL may exhibit limitations in applications where the input signal contains harmonics, unbalanced conditions, or rapidly varying frequency [7]. Under such conditions, the PLL loop dynamics may introduce estimation errors that affect converter stability and power control performance. For this reason, various improved synchronization methods have been proposed, including adaptive PLL structures and orthogonal signal generation techniques.

In parallel with the development of advanced synchronization algorithms, significant research efforts have focused on improving current control strategies in grid-connected converters. One of the most widely used approaches for AC current control is the proportional–resonant (PR) controller [8,9]. Unlike conventional proportional–integral controllers, which are primarily designed for DC signals, PR controllers provide theoretically infinite gain at a selected resonant frequency, enabling accurate tracking of sinusoidal reference signals with zero steady-state error.

Because of this property, PR controllers have become a popular solution for current control in stationary reference frames for grid-connected converters and renewable energy systems. However, their performance strongly depends on the accuracy of the resonant frequency parameter. If the actual system frequency deviates from the nominal value, the controller performance may deteriorate significantly.

Recent research has therefore investigated adaptive control structures in which the resonant frequency of the PR controller is continuously updated using frequency estimates obtained from synchronization algorithms. Such approaches allow the control system to maintain optimal performance even under varying operating conditions [10,11].

Another important trend in modern power electronics is the increasing use of predictive control concepts. Adaptive control techniques aim to anticipate future system behaviour and adjust control actions accordingly, leading to faster transient response and improved dynamic performance [12,13]. However, classical model adaptive control algorithms often require significant computational resources and detailed system models, which may limit their applicability in real-time embedded implementations.

An alternative approach consists of introducing predictive characteristics indirectly through fast adaptive synchronization combined with dynamically tuned controllers. When the control system can rapidly estimate the instantaneous phase and frequency of the network voltage, it becomes possible to generate current references and control signals that effectively anticipate variations in the network conditions [14,15].

This concept is particularly relevant in high-frequency electrical systems such as aircraft power networks, where synchronization delays must be minimized to maintain stable operation [16]. In such systems, adaptive PLL algorithms combined with resonant current controllers may provide a practical solution for achieving adaptive power control with relatively low computational complexity [17].

In this paper, an adaptive power control strategy for an onboard power converter operating in a 400 Hz electrical network is presented. The proposed approach integrates an adaptive PLL algorithm with a proportional-resonant current controller in order to achieve accurate synchronization and dynamic power control. The adaptive PLL continuously estimates the instantaneous phase, frequency, and amplitude of the network voltage, enabling real-time adjustment of the resonant controller parameters.

The main contribution of this work lies in the integration of the proposed adaptive synchronization method with a power control system designed for aircraft electrical networks. The proposed solution introduces predictive characteristics into the control loop while maintaining computational simplicity suitable for FPGA-based implementations.

The structure of the paper is organized as follows. Section 2 presents the theoretical background of synchronization algorithms used in grid-connected converters. Section 3 describes the system model and control structure of the onboard converter. Section 4 introduces the adaptive frequency estimation algorithm used in the proposed PLL. Section 5 discusses implementation aspects of the algorithm in FPGA-based control systems. Section 6 presents simulation results and performance evaluation under various operating conditions. Finally, Section 7 concludes the paper.

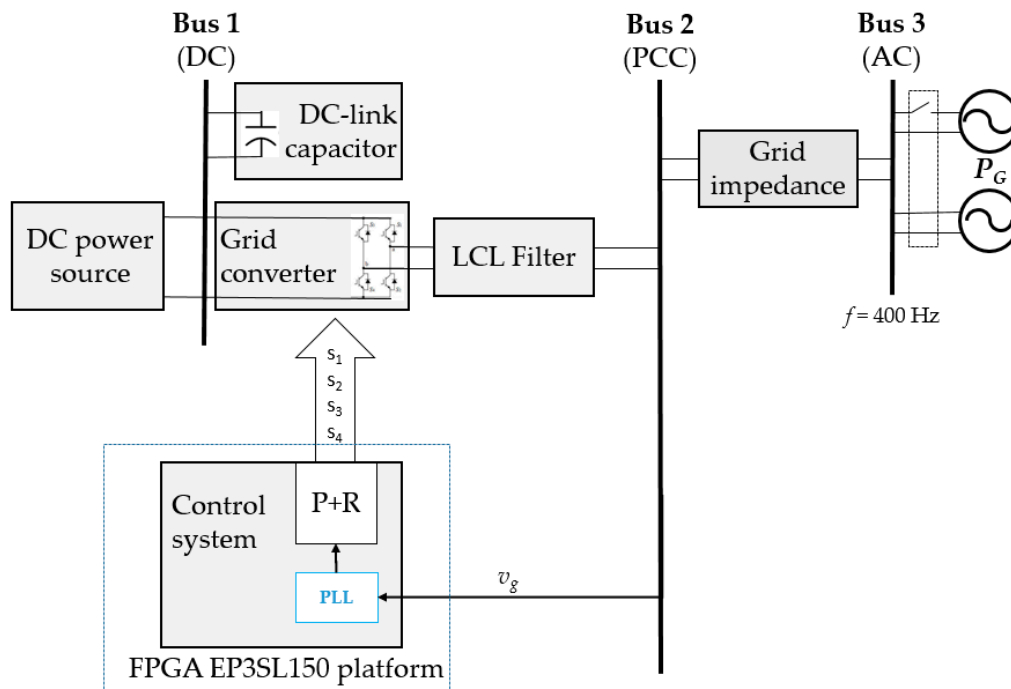
## 2. Materials and Methods

### 2.1. System Overview

The study presented in this paper concerns adaptive power control in an onboard power converter operating in cooperation with a 400 Hz electrical network. Such networks are widely used in airborne electrical power systems due to their favourable power-to-weight ratio and reduced size of passive components compared to conventional 50/60 Hz systems. In modern aircraft electrical architectures, onboard power converters are responsible for interfacing various subsystems with the primary power distribution network. These converters must operate reliably under dynamic operating conditions while maintaining strict requirements regarding power quality, synchronization accuracy, and dynamic response.

The control of active and reactive power exchanged between the converter and the onboard grid requires accurate estimation of the fundamental component of the grid voltage. In particular, precise knowledge of the instantaneous phase and frequency of the network voltage is necessary for effective implementation of synchronous control strategies.

In this work, adaptive power control is achieved through the integration of a novel adaptive phase-locked loop (PLL) structure with a proportional-resonant (PR) control system. The proposed PLL provides real-time estimation of the instantaneous phase, frequency, and amplitude of the fundamental component of the network voltage. These quantities are subsequently used by the power control algorithm to regulate the converter output currents and achieve the desired power exchange with the onboard electrical network.



**Figure 1.** Block diagram of the onboard converter with the main control board.

The block diagram of the investigated structure is shown in Figure 1. The proposed approach allows the adaptive behaviour of the control system to be obtained without the need for complex model predictive control algorithms. Instead, adaptive properties emerge from the fast adaptive synchronization mechanism combined with the resonant characteristics of the PR controller.

### 2.2. Onboard 400 Hz Power System Characteristics

Aircraft electrical power systems differ significantly from conventional terrestrial grids. One of the key distinguishing features is the operating frequency of the onboard power network, which is typically equal to 400 Hz.

The higher operating frequency offers several advantages, including reduced size and weight of transformers, filters, and other passive components. However, it also imposes more stringent requirements on control algorithms and synchronization systems used in power electronic converters.

In particular, the fundamental period of a 400 Hz signal is only  $T=2.5$  ms which means that synchronization algorithms must operate significantly faster than those used in standard 50 Hz or 60 Hz power systems. Even small delays in phase estimation may lead to noticeable errors in current control and power regulation.

Furthermore, onboard electrical networks are often subject to dynamic disturbances caused by rapidly changing loads, power electronic interfaces, and variable-speed generators. These conditions require synchronization methods capable of maintaining stable operation even under rapidly changing frequency and amplitude conditions.

For these reasons, conventional synchronization algorithms designed for low-frequency power systems may exhibit insufficient dynamic performance when applied to 400 Hz networks. Therefore, the development of faster and more adaptive synchronization techniques is essential for high-performance control of onboard power converters.

### 2.3. Adaptive Power Control Structure

The proposed control system aims to regulate the active power exchanged between the onboard power converter and the aircraft electrical network. The control strategy is based on synchronous



reference frame concepts combined with adaptive estimation of the network voltage phase and frequency.

The converter output current is controlled using a proportional–resonant (PR) regulator operating in the stationary reference frame. The PR controller is particularly well suited for sinusoidal reference tracking because it provides theoretically infinite gain at the resonant frequency corresponding to the fundamental component of the signal.

The transfer function of the proportional–resonant controller can be expressed as

$$G_{PR}(s) = K_p + \frac{K_r s}{s^2 + \omega_0^2} \quad (1)$$

where  $K_p$  is the proportional gain,  $K_r$  is the resonant gain, and  $\omega_0$  represents the angular frequency of the fundamental component of the network voltage.

In the proposed control scheme, the resonant frequency of the PR controller is not fixed. Instead, it is continuously updated using the frequency estimate provided by the adaptive PLL algorithm described in the following sections.

As a result, the resonant controller automatically tracks variations in the network frequency, ensuring accurate current control even when the system frequency deviates from its nominal value.

This adaptive interaction between the PLL and the PR controller introduces predictive characteristics into the control system. Because the PLL rapidly estimates the instantaneous phase and frequency of the network voltage, the controller can respond to dynamic changes before large phase errors accumulate in the system.

Consequently, the power regulation process becomes significantly faster compared with conventional fixed-frequency control schemes.

#### 2.4. Role of the Adaptive PLL in the Control Loop

The adaptive PLL proposed in this work plays a central role in the overall adaptive power control strategy. The algorithm continuously estimates the instantaneous phase, frequency, and amplitude of the fundamental component of the network voltage. These estimated parameters are used in several parts of the control system. First, the phase estimate allows synchronization of the converter current with the network voltage, which is necessary for precise control of active and reactive power. Second, the frequency estimate is used to dynamically tune the resonant frequency of the PR controller. This ensures that the controller remains perfectly aligned with the fundamental component of the network voltage even when frequency deviations occur. Third, the amplitude estimate allows accurate reconstruction of the fundamental sinusoidal component of the network voltage, which can be used in feedforward control paths or adaptive estimation mechanisms.

Because the PLL structure employs an adaptive frequency update law based on the quadrature component of the Park transformation, the synchronization process exhibits very fast dynamic response. This property is particularly beneficial in 400 Hz systems where the signal period is short and synchronization errors must be minimized.

The interaction between the adaptive PLL and the PR controller forms the basis of the adaptive power control strategy investigated in this study.

#### 2.5. Adaptive Characteristics of the Control Loop

An important feature of the proposed control structure is its predictive behaviour resulting from the interaction between the adaptive PLL and the resonant current controller. In conventional grid-synchronized converters, the controller operates based on phase information obtained from synchronization algorithms that may introduce delays. These delays can lead to transient power oscillations and slower dynamic response. In contrast, the adaptive PLL used in this work provides fast estimation of the instantaneous phase and frequency of the network voltage. Because the phase estimate is continuously updated, the current reference signal generated by the control system closely follows the fundamental component of the network voltage. Furthermore, the resonant controller dynamically adjusts its internal frequency using the PLL output. This mechanism effectively

anticipates variations in the network frequency and allows the controller to maintain accurate current tracking even during transient operating conditions. As a result, the overall control system exhibits predictive characteristics without requiring explicit model adaptive control algorithms.

To enable analytical treatment of the adaptive and predictive behavior described above, a mathematical representation of the input signal is introduced. This formulation allows direct characterization of phase, frequency, and amplitude dynamics. It also facilitates the analysis of the interaction between the adaptive PLL and the resonant controller within a unified framework. A discrete-time representation is adopted to reflect practical digital implementation constraints. The resulting model accounts for the fundamental component as well as harmonic distortion and measurement noise. The input of the system is a single-phase sinusoidal signal, subject to noise and harmonic distortion:

$$x(t) = A(t)\sin(\phi(t)) + \sum_{h=2}^H A_h \sin(h\phi(t) + \psi_h) + n(t) \quad (2)$$

where  $A$  is the instantaneous amplitude,  $\phi(t) = \int_0^t \omega_{in}(\tau) + \phi_0$  is the instantaneous phase,  $\omega_{in}$  is angular frequency,  $A_h$  and  $\psi_h$  are the amplitudes and phases of the  $h$ -th harmonic, and  $n(t)$  is additive noise, modelling measurement or grid disturbances. For digital processing, the signal is sampled at a frequency  $f_s$  with sampling interval  $T_s=1/f_s$ , yielding the discrete-time sequence  $x[n] = x(nT_s)$ . This model is general enough to represent grid voltages, power electronics outputs, or communication carriers. In practice,  $A(t)$  and  $\omega_{in}(t)$  may vary slowly or rapidly, and the system must track both parameters in real time.

For single-phase signals, an orthogonal reference  $y[n]$  is constructed via a Hilbert transform or quadrature oscillator, producing an  $\alpha\beta$  vector:

$$\mathbf{v}[n] = \begin{bmatrix} x[n] \\ y[n] \end{bmatrix}. \quad (3)$$

This allows the system to perform phase and amplitude estimation in a two-dimensional stationary plane, where the phase angle corresponds to the instantaneous position of the input signal vector. The  $\alpha\beta$  representation facilitates decoupling amplitude and phase dynamics, implementing discrete-time rotational transformations, and linearizing the frequency error around the synchronous frame.

To facilitate adaptive frequency estimation, the input signal is transformed into the  $\alpha\beta$  stationary reference frame, or equivalently, treated as in-phase ( $d$ ) and quadrature ( $q$ ) components if an orthogonal reference is available. The Park transformation is applied to rotate the reference frame in synchrony with an estimated phase  $\theta[n]$ :

$$\begin{bmatrix} d[n] \\ q[n] \end{bmatrix} = \begin{bmatrix} \cos\theta[n] & \sin\theta[n] \\ -\sin\theta[n] & \cos\theta[n] \end{bmatrix} \begin{bmatrix} x[n] \\ y[n] \end{bmatrix}. \quad (4)$$

In equation (4),  $d[n]$  represents the component in-phase with the estimated signal, ideally equal to the amplitude  $A[n]$ , while  $q[n]$  represents the quadrature component, proportional to the instantaneous phase/frequency error. This transformation enables linear adaptive control, because the error dynamics can be directly mapped to  $\Delta\omega$ . This transformation yields the following properties:

- Unitary rotation which preserves magnitude  $\|\mathbf{v}[n]\| = \sqrt{d[n]^2 + q[n]^2}$ .
- Phase error encoding with small deviations of  $\theta[n]$  from the true phase lead to  $q[n] \approx A[n] \cdot (\theta_{true}[n] - \theta[n])$ .
- Noise attenuation: harmonics and high-frequency noise project onto both  $d[n]$  and  $q[n]$ ; subsequent filtering isolates the fundamental.

Assuming a slowly varying amplitude  $A[n]$  and instantaneous frequency  $\omega_{in}[n]$ , the discrete-time dynamics of the d-q frame are:

$$d[n+1] = A[n]\cos(\Delta\theta[n]) \approx A[n]\left(1 - \frac{1}{2}(\Delta\theta[n])^2\right), \quad (5)$$

$$q[n+1] = A[n]\sin(\Delta\theta[n]) \approx A[n]\Delta\theta[n], \quad (6)$$

where  $\Delta\theta[n] = \theta_{in}[n] - \theta[n]$  is the phase error. For small phase deviations,  $q[n]$  is linearly proportional to frequency error, forming the basis for the adaptive law:

$$\Delta\omega[n] = k_\omega \cdot q[n]. \quad (7)$$

This linearization is central to stability analysis and predictive behavior.

Sampling introduces several practical effects:

- Aliasing:  $f_s$  must satisfy the Nyquist criterion for the highest frequency component, including harmonics.
- Integrator resolution:  $\theta[n+1] = \theta[n] + \omega[n] \cdot T_s$  requires fixed-point or floating-point representation; saturation or modulo arithmetic may be necessary.
- Delay: each block introduces one-sample delay; cumulative delay affects convergence time and must be considered in  $k_\omega$  selection.

Discrete-time modelling ensures that the PLL remains stable under real-world sampling and FPGA/DSP constraints.

Amplitude is estimated from  $d[n]$  using a discrete low-pass filter:

$$A[n+1] = A[n] + k_A(d[n] - A[n]), \quad (8)$$

where  $k_A$  is chosen based on desired tracking speed and noise rejection. For noisy or harmonically distorted signals, this filtering ensures smooth amplitude estimates, preventing spurious scaling of the output sinusoid.

The predicted sinusoid is reconstructed as:

$$\hat{x}[n] = A[n]\sin(\theta[n]). \quad (9)$$

The error  $q[n]$  feeds back into the frequency integrator, closing the loop. In this predictive model, the system anticipates changes in the input frequency and adjusts  $\theta[n]$  and  $\omega[n]$  before the phase error becomes large, ensuring fast locking.

## 2.6. Adaptive Frequency Estimation

The primary goal of the adaptive PLL is to generate a frequency estimate  $\omega[n]$  that rapidly converges to the true input frequency  $\omega_{in}[n]$  while ensuring fast convergence (the estimated frequency  $\omega[n]$  quickly locks to the actual input frequency), stability (oscillations and overshoot are minimized), and robustness (the system remains reliable in the presence of noise, harmonic distortion, and large frequency steps). In the d-q frame, the quadrature component  $q[n]$  encodes the frequency error:

$$q[n] \approx A[n](\theta_{in}[n] - \theta[n]) \approx A[n](\Delta\omega[n] \cdot T_s), \quad (10)$$

For small phase deviations, where  $\Delta\omega[n] = \omega_{in}[n] - \omega[n]$ . This relation allows linear adaptive control.

In the proposed system, the quadrature component  $q[n]$  serves as the primary error signal. A simple yet effective adaptive law updates the estimated frequency using:

$$\Delta\omega[n] = k_\omega q[n], \quad (11)$$

$$\omega[n+1] = \omega[n] + \Delta\omega[n]. \quad (12)$$

where  $k_\omega$  is the loop gain coefficient determining the adaptation rate, chosen to balance speed and overshoot. This method avoids nonlinear operations like division or arctangent, which are sensitive



to noise and quantization, and the integrator update form is straightforward to implement in fixed-point arithmetic. Unlike normalized or division-based phase detectors, this linear formulation avoids numerical instability and is straightforward to implement in fixed-point arithmetic on FPGA.

To improve convergence during rapid input frequency changes, a feedforward term is proposed:

$$\Delta\omega_{ff}[n] = k_{ff} \cdot (q[n] - q[n-1]), \quad (13)$$

yielding the updated frequency estimate:

$$\omega[n+1] = \omega[n] + \Delta\omega[n] + \Delta\omega_{ff}[n]. \quad (14)$$

Saturation limits  $\omega_{\min} \leq \omega[n+1] \leq \omega_{\max}$  are applied to prevent integrator wind-up and ensure safe operation over a wide frequency range. This approach reduces effective settling time, compensates for the lag introduced by the discrete-time integrator, and improves tracking of step changes and ramps in  $\omega_{in}$ .

The linear law can be interpreted as a gradient descent on a phase error function [18]:

$$J(\theta[n]) = \frac{1}{2} q[n]^2, \quad (15)$$

$$\frac{\partial J}{\partial \theta[n]} = q[n] \Rightarrow \Delta\omega[n] = -k_{\omega} \frac{\partial J}{\partial \theta[n]}. \quad (16)$$

Minimizing  $J(\theta[n])$  drives  $q[n]$  to 0, effectively synchronizing the PLL. This perspective provides a theoretical justification for stability and convergence speed.

Discrete-time implementation must meet a number of requirements:

- **Sampling and Quantization:**  $q[n]$  must be computed with sufficient resolution; insufficient word length can introduce limit cycles and fixed-point implementation typically must use 16–24 bits, with scaling to maintain numerical stability.
- **Integrator Design:** saturation or modulo arithmetic is essential to prevent overflow during large frequency excursions.
- **Time-Delay Effects:** each block introduces a one-sample delay; careful selection of  $k_{\omega}$  and  $k_{ff}$  compensates for this.

While the linear law works for moderate frequency changes, adaptive gain scheduling improves response for large variations:

$$\mu[n] = \text{sat} \left( \frac{|q[n]|}{A[n]} \right), \quad (17)$$

$$\Delta\omega[n] = k_{\omega} \mu[n] q[n]. \quad (18)$$

where  $\mu[n]$  scales the adaptation rate based on instantaneous phase error magnitude, and saturation prevents excessive response and preserves stability. This approach is similar to variable step-size gradient descent, common in adaptive filtering.

Real signals often contain thermal or measurement noise (additive noise), harmonics (integer multiples of the fundamental frequency, and amplitude modulation (slow variations of  $A[n]$ ). The PLL must be robust, which has been achieved by d–q transformation, which decouples phase and amplitude, allowing  $q[n]$  to predominantly encode frequency error, low-pass filtering of  $q[n]$  which smooths rapid oscillations due to harmonics or noise, and feedforward terms to compensate predictable changes without amplifying high-frequency components. For very fast inputs, multi-rate processing improves convergence computing  $q[n]$  at a higher sampling rate than the main NCO update, and integrate an adaptive estimator of future  $\omega[n+1]$  based on recent slope:

$$\omega_{pred}[n+1] = \omega[n] + \Delta\omega[n] + \Delta\omega[n] - \Delta\omega[n-1]. \quad (19)$$

This reduces effective phase error before it accumulates, enhancing lock-in speed.

The hardware-oriented considerations for this task are as follows:

- **Fixed-point scaling**  $-k_{\omega}$ ,  $k_{ff}$ , and  $T_s$  must be chosen to maximize resolution and avoid overflow.

- Pipeline structure — d-q transformation,  $q[n]$  computation,  $\Delta\omega[n]$  update, and  $\omega[n+1]$  integration can be parallelized in FPGA.
- Lookup tables for sine/cosine — minimizes computational cost for  $\theta[n]$  updates.
- Latency minimization — critical for high-frequency signals (>10 kHz), can be achieved by fully combinatorial logic for d-q transformation.

### 2.7. Phase Tracking

Phase tracking is the core function of any phase-locked loop. Its goal is to generate an internal phase  $\theta[n]$  that matches the instantaneous phase of the input signal  $\theta_{in}[n]$ . The input is modelled as:

$$x[n] = A \sin(\theta_{in}[n]) + \text{noise} + \text{harmonics}. \quad (20)$$

The phase error is defined as:

$$\tilde{\theta}[n] = \theta_{in}[n] - \theta[n]. \quad (21)$$

In the d-q Park frame, the quadrature component  $q[n]$  is approximately:

$$q[n] \approx A[n] \sin(\tilde{\theta}[n]) \approx A[n] \tilde{\theta}[n], \quad (22)$$

for small  $\tilde{\theta}[n]$ . Hence,  $q[n]$  serves as a phase error indicator, forming the basis for phase tracking.

Once  $\omega[n]$  is estimated, the phase is updated using a discrete-time integrator (numerically controlled oscillator, NCO):

$$\theta[n+1] = \theta[n] + \omega[n+1] \cdot T_s. \quad (23)$$

The precision of  $\theta[n+1]$  depends on the word length in fixed-point arithmetic. Finite resolution can introduce quantization error, accumulating as a phase drift. Sampling interval  $T_s$  determines the step size of phase update; smaller  $T_s$  reduces phase error but increases computational load. Accurate phase tracking relies on accurate  $\omega[n+1]$ , as a consequence the errors in frequency estimation manifest as linear phase drift over time. Assuming small phase error  $\tilde{\theta}[n]$ , the update law can be linearized:

$$\tilde{\theta}[n+1] \approx \tilde{\theta}[n] - k_\omega T_s \tilde{\theta}[n], \quad (24)$$

where  $k_\omega$  is the loop gain from the frequency adaptation law. This linearization yields a first-order discrete-time system with eigenvalue  $1 - k_\omega T_s$ . As a consequence it can be obtained overdamped response for  $0 < k_\omega T_s < 1$ , convergence rate directly controlled by  $k_\omega$ , and predictable settling time, critical for real-time systems. For rapidly varying input frequency, an adaptive correction term improves phase tracking:

$$\theta[n+1] = \theta[n] + \omega[n+1] T_s + k_p (q[n] - q[n-1]), \quad (25)$$

where the term  $k_p (q[n] - q[n-1])$  acts as a phase rate predictor, compensating for expected phase changes in the next sampling step. This approach reduces overshoot and accelerates lock-in.

The phase tracking can be interpreted as a discrete-time proportional-derivative (PD) controller:

$$\Delta\theta[n] = k_p q[n] + k_d (q[n] - q[n-1]), \quad (26)$$

where  $k_p$  corresponds to proportional correction,  $k_d$  corresponds to derivative (predictive) action, and together, they enable faster settling and reduced oscillations. The PD formulation allows the designer to tune phase error damping independently of frequency adaptation gain.

The synchronized output sinusoid is reconstructed as:

$$\hat{x}[n] = A[n] \cdot \sin(\theta[n]), \quad (27)$$

with amplitude  $A[n]$  estimated separately. This architecture guarantees that the predicted sinusoid closely follows the input signal in both phase and frequency, even under large and rapid variations.

## 2.8. Amplitude Estimation

The amplitude of the input sinusoidal signal, is a critical parameter for reconstruction and adaptive control. After d-q transformation, the in-phase component  $d[n]$  aligns with the instantaneous input amplitude, while  $q[n]$  encodes frequency/phase error. For small  $\tilde{\theta}[n]$

$$d[n] \approx A[n], \quad q[n] \approx A[n]\tilde{\theta}[n]. \quad (28)$$

Thus, amplitude estimation can be performed directly from  $d[n]$ . A simple first-order low-pass filter is applied to remove high-frequency noise:

$$A[n+1] = A[n] + k_A \cdot (d[n] - A[n]), \quad (29)$$

where  $k_A$  is the amplitude adaptation coefficient. This approach avoids costly square root operations while providing smooth and reliable amplitude tracking. The filtered amplitude is subsequently used to scale the reconstructed output sinusoid.

For signals with rapid amplitude modulation, a variable step-size improves responsiveness:

$$k_A[n] = k_{A0} \cdot \text{sat}\left(\frac{|d[n] - A[n]|}{A[n]}\right), \quad (30)$$

$$A[n+1] = A[n] + k_A[n] \cdot (d[n] - A[n]). \quad (31)$$

When the error is small,  $k_A[n]$  decreases to reduce oscillations. When the error is large (e.g., sudden amplitude step),  $k_A[n]$  increases for faster convergence. As a consequence the saturation ensures numerical stability in fixed-point hardware.

Due to the amplitude estimation is affected by additive noise, harmonics, and phase error coupling at small  $\tilde{\theta}[n]$  the advanced strategy to estimate  $A[n]$  from magnitude of d-q vector is proposed:

$$A[n] \approx \sqrt{d[n]^2 + q[n]^2} \approx d[n] + \frac{q[n]^2}{2d[n]}, \quad (32)$$

which reduces sensitivity to small phase errors. This method, though slightly more computationally intensive, improves accuracy for high-precision applications.

For systems with rapid amplitude variation, the multi-rate and adaptive estimation compute  $A[n]$  at a higher internal sampling rate and predict next sample using slope:

$$A_{pred}[n+1] = A[n] + (A[n] - A[n-1]), \quad (33)$$

reducing tracking lag.

The comparative analysis of proposed algorithms is presented in Table 1.

**Table 1.** The comparative analysis of proposed algorithms.

| Method                 | Complexity | Accuracy  | Noise rejection | Covergence |
|------------------------|------------|-----------|-----------------|------------|
| LPF on $d[n]$          | Low        | Moderate  | Good            | Moderate   |
| Variable step-size LPF | Medium     | High      | Very good       | Fast       |
| Magnitude-based        | High       | Very High | Excellent       | Moderate   |
| Adaptive multi-rate    | High       | High      | Very good       | Very fast  |

Based on comparative analysis it can be concluded that the LPF is simplest and adequate for most grid application, while adaptive methods are recommended when amplitude changes faster than the sampling period.

### 2.9. Stability Considerations

The closed-loop dynamics of the adaptive PLL can be approximated as a second-order linear system:

$$\theta[n+1] = \theta[n] + T_s \cdot k_\omega q[n], \quad (34)$$

$$q[n+1] \approx q[n] - T_s \cdot k_\omega q[n]. \quad (35)$$

Global stability is ensured if the loop gain satisfies:

$$0 < k_\omega T_s < 1. \quad (36)$$

Empirically,  $k_\omega T_s \approx 0.2$  provides a trade-off between fast convergence and minimal overshoot. The feedforward term further reduces the effective settling time, allowing the PLL to track frequency steps within one or two signal periods.

### 2.10. Linearization Around Equilibrium

The stability analysis of the adaptive PLL relies on linearizing the discrete-time system around the equilibrium point. The equilibrium occurs when the estimated frequency  $\omega[n]$  exactly matches the input frequency  $\omega_{in}[n]$ , and the phase error  $q[n]$  tends to zero. Denoting the small deviation from equilibrium as  $\tilde{q}[n]$  and  $\tilde{\omega}[n] = \omega[n] - \omega_{in}$ , the discrete-time dynamics of the loop can be approximated as:

$$\tilde{\omega}[n+1] = \tilde{\omega}[n] + k_\omega \tilde{q}[n] T_s, \quad (36)$$

$$\tilde{q}[n+1] \approx \tilde{q}[n] - k_\omega \tilde{q}[n] T_s. \quad (37)$$

This linearization assumes that the amplitude  $A[n]$  is slowly varying and the phase deviation  $\tilde{q}[n]$  remains small. The result is a first-order discrete-time system, where the eigenvalue associated with the error dynamics is  $1 - k_\omega T_s$ .

### 2.11. Stability Criterion

The system is globally stable if the magnitude of the eigenvalue lies strictly within the unit circle:

$$|1 - k_\omega T_s| < 1 \Rightarrow 0 < k_\omega T_s < 2. \quad (38)$$

In practice, values  $0 < k_\omega T_s < 1$  are chosen to ensure overdamped response, minimizing oscillations and avoiding overshoot. This criterion directly links the loop gain  $k_\omega$  with the sampling interval  $T_s$ , providing a clear design guideline for discrete-time implementation.

The linearization allows the designer to predict settling time and overshoot analytically. The system behaves as a first-order stable integrator with tunable time constant  $\tau = 1/k_\omega$ . Because the dynamics are linearized around the instantaneous frequency, even large step changes in  $\omega_{in}$  produce bounded responses, provided the integrator saturation limits are enforced. The linear model avoids division operations and nonlinear trigonometric functions (except NCO sine/cosine), which is ideal for FPGA or DSP implementation. Incorporating the term  $\Delta\omega_{ff}[n] = k_{ff}(q[n] - q[n-1])$  effectively cancels the dominant component of the error for fast frequency variations, reducing the effective eigenvalue and accelerating convergence.

Alternatively, stability can be interpreted using a Lyapunov function [19]:

$$V[n] = \frac{1}{2} \tilde{q}[n]^2 + \frac{1}{2k_\omega} \tilde{\omega}[n]^2. \quad (39)$$

where  $V[n] > 0$  for all nonzero deviations. The discrete-time derivative  $\Delta V = V[n+1] - V[n]$  satisfies  $\Delta V < 0$  if  $0 < k_\omega T_s < 1$ . This guarantees monotonic decrease of the energy function, confirming global asymptotic stability of the PLL. This Lyapunov-based view provides rigorous proof of stability, complementing the linearized eigenvalue analysis.

The proposed method is characterized by linearized first-order discrete-time dynamics around the equilibrium phase and frequency, eigenvalue-based stability criterion directly linking loop gain and sampling interval and predictable, non-oscillatory convergence for small loop gains, adjustable via  $k_\omega$ . Optional feedforward term improves response to rapid frequency variations, and Lyapunov function confirms global asymptotic stability, making the approach robust and suitable for FPGA/DSP implementations.

### 3. Implementation on FPGA

The proposed adaptive PLL algorithm is well suited for implementation on reconfigurable hardware platforms due to its relatively low computational complexity and highly parallel structure. Field-programmable gate arrays (FPGAs) provide deterministic timing, low latency, and the possibility of extensive pipelining, which makes them particularly attractive for real-time signal processing applications such as frequency tracking and signal reconstruction.

The overall architecture of the FPGA implementation follows the signal processing chain described in previous sections. The system processes the sampled input signal  $x[n]$  at a fixed sampling frequency  $f_s$ , and internally computes the orthogonal signal components, the Park transformation, and the adaptive estimation of frequency, phase, and amplitude.

The principal computational blocks are:

- Orthogonal signal generation
- Park transformation
- Phase detector
- Adaptive frequency estimation block
- Phase accumulator
- Amplitude estimator
- Sinusoidal signal reconstruction

These blocks form a fully synchronous digital processing pipeline. Each stage operates on data sampled at the system clock rate, and intermediate results are stored in registers between pipeline stages in order to maintain high operating frequency. The proposed system is particularly suited for fixed-point implementation on FPGA with key considerations:

- Fixed-point representation:  $d[n]$ ,  $q[n]$ ,  $A[n]$ ,  $\Delta\omega[n]$ , and  $\theta[n]$  can be represented with 16–24 bits to balance precision and hardware resources.
- Discrete integrators: implemented using accumulators; saturation logic ensures safety.
- Lookup tables for sin/cos:  $\theta[n]$  to sin/cos conversion is implemented via LUTs, avoiding expensive real-time computations.
- Parallel processing: all blocks can operate concurrently for minimal latency, crucial for 10 kHz sampling rates.

### 4. Simulation and Experimental Validation

#### 4.1. Test Setup

The performance of the proposed adaptive phase-locked loop (PLL) was evaluated through a series of simulation studies designed to assess the robustness, accuracy, and dynamic response of the algorithm under realistic operating conditions. The simulations were conducted using a discrete-time model of the signal processing chain, including the Park transformation, adaptive frequency estimation, phase tracking, and amplitude estimation blocks.

The input signal was sampled with a sampling frequency of  $f_s=10$  kHz which corresponds to a sampling period  $T_s=100$   $\mu$ s. The nominal input frequency was set to  $f_0=400$  Hz with the corresponding angular frequency  $\omega_0=2513.27$  rad/s. The adaptive frequency update law used in the simulations is given by  $\omega[n+1]=\omega[n]+k_\omega q[n]$ , while the phase estimate is obtained from  $\theta[n+1]=\theta[n]+\omega[n]T_s$ . The



amplitude estimation block follows the recursive relation  $A[n+1]=A[n]+k_A(d[n]-A[n])$ . All simulations were performed using fixed-point arithmetic consistent with the intended FPGA implementation.

The following test scenarios were considered:

- frequency step response
- frequency ramp tracking
- harmonic distortion robustness
- noise robustness
- amplitude variation tracking

Each experiment evaluates a different aspect of the algorithm's behaviour and demonstrates its suitability for real-time signal synchronization.

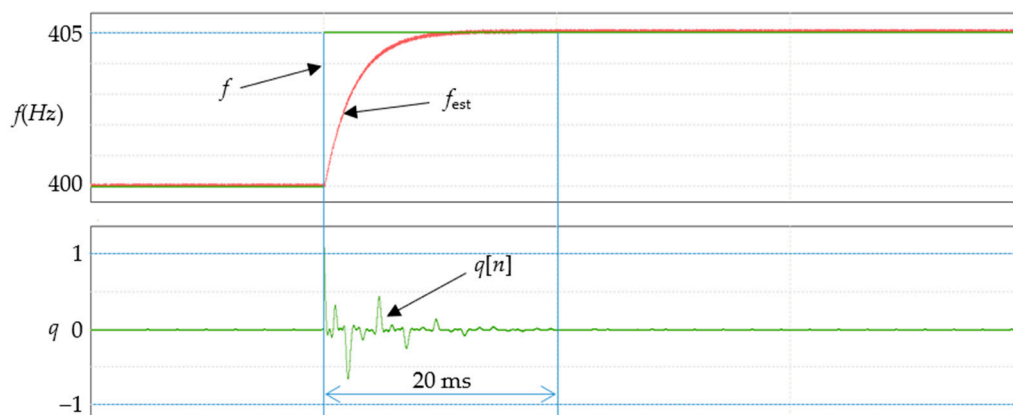
#### 4.2. Frequency Step Response

The first experiment evaluates the dynamic response of the PLL to sudden frequency changes. The input signal frequency was modified according to the following step function:

$$f_{in} = \begin{cases} 400 \text{ Hz}, & t < 0.02s \\ 405 \text{ Hz}, & t \geq 0.02s \end{cases} \quad (40)$$

This test represents a common scenario in power systems where grid frequency may deviate due to load disturbances or generation imbalance.

Figure 2 illustrates the estimated frequency  $f_{est}$  together with the actual input frequency. Immediately after the frequency step occurs, the phase detector produces a non-zero quadrature component  $q[n]$ , which drives the adaptive frequency estimator.



**Figure 2.** Estimated frequency  $f_{est}$ , the actual input frequency  $f$  and the quadrature component  $q$  during a frequency step.

The proposed PLL demonstrates a rapid convergence to the new frequency value with minimal overshoot. The settling time of the algorithm is approximately one fundamental period of the signal, which confirms the effectiveness of the adaptive frequency update mechanism.

The steady-state frequency error is negligible once the synchronization process is complete.

#### 4.3. Frequency Ramp Tracking

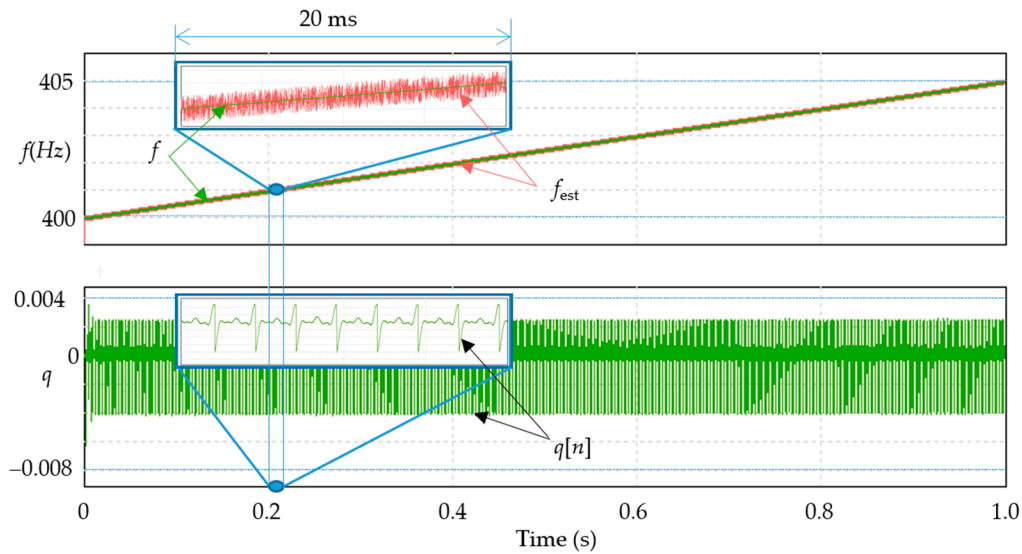
To evaluate the tracking capability under continuously varying frequency conditions, a ramp frequency profile was applied to the input signal:

$$f_{in}(t) = 400 + 405t. \quad (41)$$

which corresponds to a frequency increase from 400 Hz to 405 Hz within one second.

This scenario represents situations encountered in variable-speed drives, renewable energy converters, or islanded microgrids where the system frequency may vary dynamically.

Figure 3 presents the comparison between the true frequency and the estimated frequency. The results demonstrate that the adaptive PLL accurately follows the frequency ramp with only a small tracking error.



**Figure 3.** Estimated frequency  $f_{est}$ , the actual input frequency  $f$  and the quadrature component  $q$  for a frequency ramp.

The instantaneous tracking error

$$e_f[n] = f_{est}[n] - f_{in}[n], \quad (42)$$

remains small throughout the experiment, confirming the ability of the algorithm to adapt to continuous frequency variations without loss of synchronization.

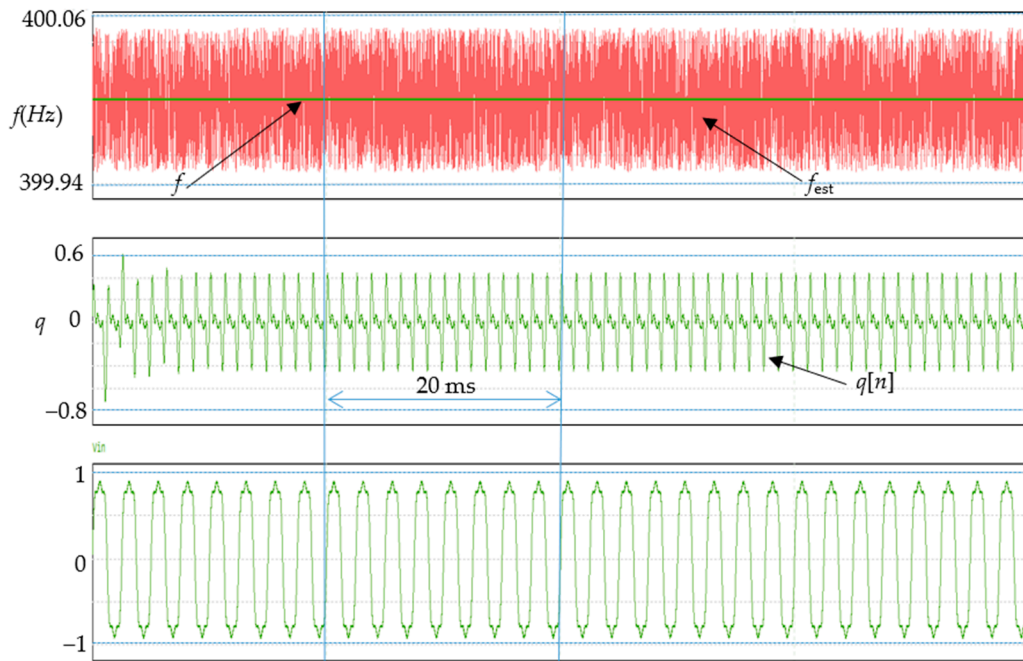
#### 4.4. Harmonic Distortion Test

Real-world signals often contain harmonic components caused by nonlinear loads, power electronic converters, or measurement imperfections. Therefore, the robustness of the algorithm against harmonic distortion was investigated. The input signal was constructed as

$$x(t) = A\sin(\omega t) + 0.2A\sin(3\omega t) + 0.1A\sin(5\omega t), \quad (43)$$

which corresponds to a signal containing: 20% third harmonic, and 10% fifth harmonic. Such distortion levels are typical in power systems with nonlinear loads.

Figure 4 shows the behaviour of the estimated frequency and the quadrature error signal  $q[n]$ . Despite the presence of significant harmonic distortion, the proposed PLL maintains stable operation and accurately estimates the fundamental frequency component.



**Figure 4.** Estimated frequency  $f_{est}$ , the actual input frequency  $f$ , the quadrature component  $q$  and input signal  $v_{in}$  defined by (43).

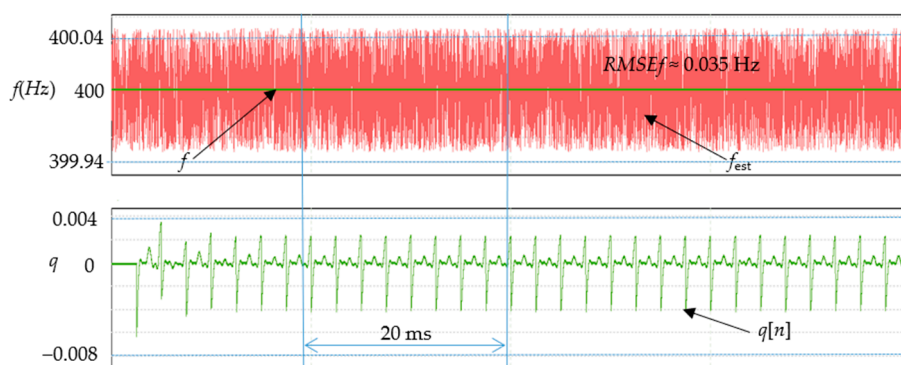
The Park transformation effectively separates the fundamental component from harmonic disturbances, while the adaptive filtering inherent in the frequency estimator suppresses high-frequency error components. As a result, the algorithm exhibits strong immunity to harmonic interference.

#### 4.5. Noise Robustness

To analyse the effect of measurement noise, white Gaussian noise was added to the input signal. The following signal-to-noise ratios (SNR) were considered: 40 dB, 30 dB, 20 dB. These noise levels represent typical conditions encountered in measurement systems and digital signal acquisition.

Figure 5 presents the estimated frequency under noisy conditions. Although the quadrature error signal becomes noisier as the SNR decreases, the frequency estimate remains stable due to the inherent filtering properties of the adaptive loop. The estimation accuracy was quantified using the root-mean-square frequency error

$$RMSE_f = \sqrt{\frac{1}{N} \sum (f_{est} - f_{in})^2} \quad (44)$$



**Figure 5.** Estimated frequency  $f_{est}$ , the actual input frequency  $f$  and the quadrature component  $q$  under noisy conditions.

The RMSE was calculated over  $N=4000$  samples corresponding to the steady-state interval of the simulation.

The results indicate that even under severe noise conditions (SNR = 20 dB), the frequency estimation error remains within acceptable limits.

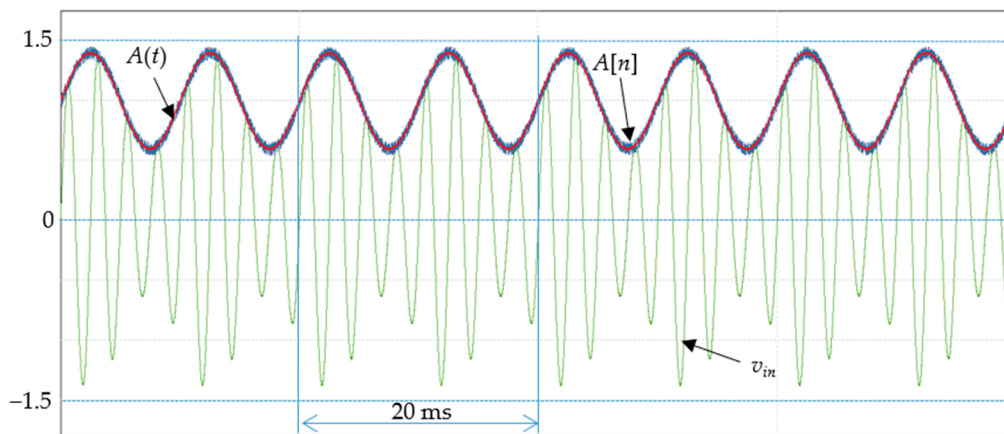
#### 4.6. Amplitude Variation Tracking

The final experiment evaluates the amplitude estimation mechanism. In many practical applications, the amplitude of the input signal may vary over time due to load changes, modulation processes, or measurement scaling. To simulate this behaviour, the amplitude of the input sinusoid was modulated according to

$$A(t) = 1 + 0.4\sin(2\pi 100t). \quad (45)$$

The (45) corresponds to a sinusoidal amplitude variation at 100 Hz.

Figure 6 compares the true amplitude  $A(t)$  with the estimated amplitude  $A[n]$ . The results demonstrate that the recursive amplitude estimator successfully tracks the amplitude modulation with minimal delay.



**Figure 6.** Estimated amplitude  $A[n]$ , the actual amplitude  $A[t]$  and the input, modulated signal  $v_{in}$ .

Furthermore, the reconstructed sinusoidal signal  $y[n] = A[n]\sin(\theta[n])$  remains well aligned with the fundamental component of the input signal. This confirms that the algorithm is capable of accurately reconstructing the fundamental waveform even when both frequency and amplitude vary over time.

#### 4.7. Discussion

The conducted experiments demonstrate that the proposed adaptive PLL architecture exhibits robust synchronization capabilities under a wide range of operating conditions. The algorithm successfully tracks abrupt frequency changes, continuous frequency ramps, harmonic distortion, and measurement noise. In addition, the amplitude estimation mechanism allows accurate reconstruction of the fundamental sinusoidal component of the input signal. The results confirm that the proposed method is suitable for real-time signal synchronization and waveform reconstruction applications, particularly in power electronics, grid synchronization, and digital signal processing systems implemented on FPGA platforms.

4.8. Comparison with Conventional PLL Methods

To evaluate the effectiveness of the proposed adaptive synchronization algorithm, its performance was compared with two widely used synchronization methods commonly employed in power electronics and signal processing applications:

- the synchronous reference frame PLL (SRF-PLL)
- the second-order generalized integrator PLL (SOGI-PLL)

The SRF-PLL is one of the most commonly used synchronization algorithms in grid-connected converters. It relies on Park transformation to generate the quadrature error signal, which is then processed by a proportional–integral (PI) controller to estimate the signal phase and frequency. The SOGI-PLL introduces an orthogonal signal generator based on a second-order resonant filter, allowing accurate extraction of the fundamental component even in the presence of harmonic distortion. Although both approaches provide reliable synchronization, they may suffer from limited dynamic performance when the input frequency varies rapidly.

The proposed algorithm differs from these classical approaches in that it directly adapts the estimated frequency using an adaptive update law driven by the quadrature error signal. This structure allows faster frequency convergence without requiring a classical PI loop filter.

All synchronization methods were evaluated under identical simulation conditions. The following parameters were used in the experiments:

Table 2. Parameters used in the experiments.

| Parameter           | Value              |
|---------------------|--------------------|
| Sampling frequency  | 10 kHz             |
| Nominal frequency   | 400 Hz             |
| Frequency step      | 400 to 405 Hz      |
| Noise level         | 30 dB SNR          |
| Harmonic distortion | 20% third harmonic |

Each algorithm was tuned to achieve stable operation and comparable steady-state accuracy. The following performance indicators were used to evaluate the synchronization quality:

- frequency settling time
- maximum overshoot
- steady-state frequency error
- robustness to harmonic distortion.

The first comparison concerns the response of the synchronization algorithms to a sudden frequency step. Figure 7 presents the estimated frequency for all three methods when the input frequency changes from 400 Hz to 405 Hz. The SRF-PLL shows a relatively slow response due to the dynamics of the PI loop filter.

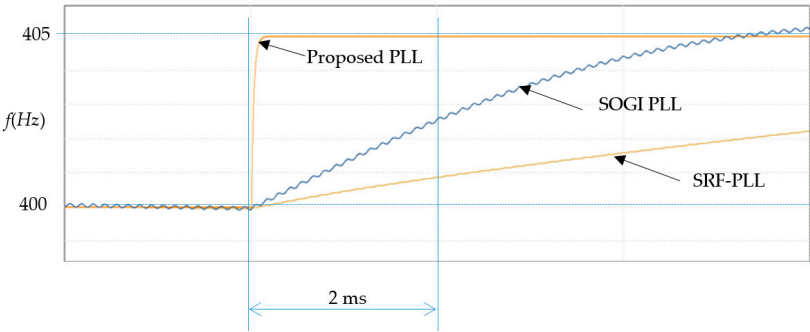
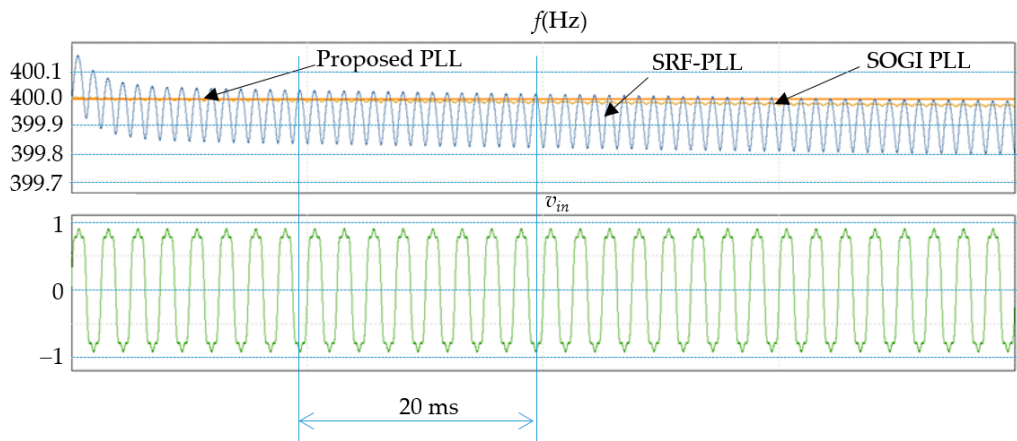


Figure 7. Estimated frequency for SRF-PLL, SOGI PLL, and proposed PLL methods when the input frequency changes from 400 Hz to 405 Hz.



The SOGI-PLL shows improved stability but still requires several signal periods to fully converge to the new frequency. In contrast, the proposed adaptive PLL demonstrates significantly faster convergence. Because the frequency update law directly adjusts the estimated frequency based on the quadrature error signal, the algorithm rapidly compensates for the phase mismatch introduced by the frequency step. As a result, the synchronization time of the proposed method is substantially shorter than that of the conventional PLL structures.

Another important comparison concerns the performance of the synchronization algorithms in the presence of harmonic distortion. In this experiment, the input signal contained both third and fifth harmonic components. Figure 8 shows the estimated frequency signals calculated by the three algorithms.



**Figure 8.** Estimated frequency for SRF-PLL, SOGI PLL, and proposed PLL method in the presence of harmonic distortion.

The SRF-PLL is particularly sensitive to harmonic distortion because the quadrature error signal contains harmonic components that propagate through the PI controller. This may introduce oscillations in the estimated frequency. The SOGI-PLL performs significantly better in this scenario due to the inherent filtering properties of the resonant structure. However, the presence of harmonics still influences the transient behaviour. The proposed algorithm exhibits comparable or improved robustness compared with the SOGI-PLL. The adaptive frequency update mechanism naturally filters high-frequency error components, which reduces the influence of harmonic disturbances on the frequency estimate.

The algorithms were also evaluated under noisy measurement conditions. White Gaussian noise was added to the input signal to achieve a signal-to-noise ratio of 30 dB.

Despite the increased noise level, the proposed adaptive PLL maintained stable operation. The estimated frequency signal remained smooth, and the synchronization process was not significantly affected. The SRF-PLL showed slightly increased jitter due to noise amplification in the PI controller. The SOGI-PLL exhibited improved filtering properties but at the cost of slower dynamic response. Overall, the proposed method provides a good compromise between noise robustness and fast dynamic performance.

Table 3 summarizes the key performance indicators obtained from the conducted simulations.

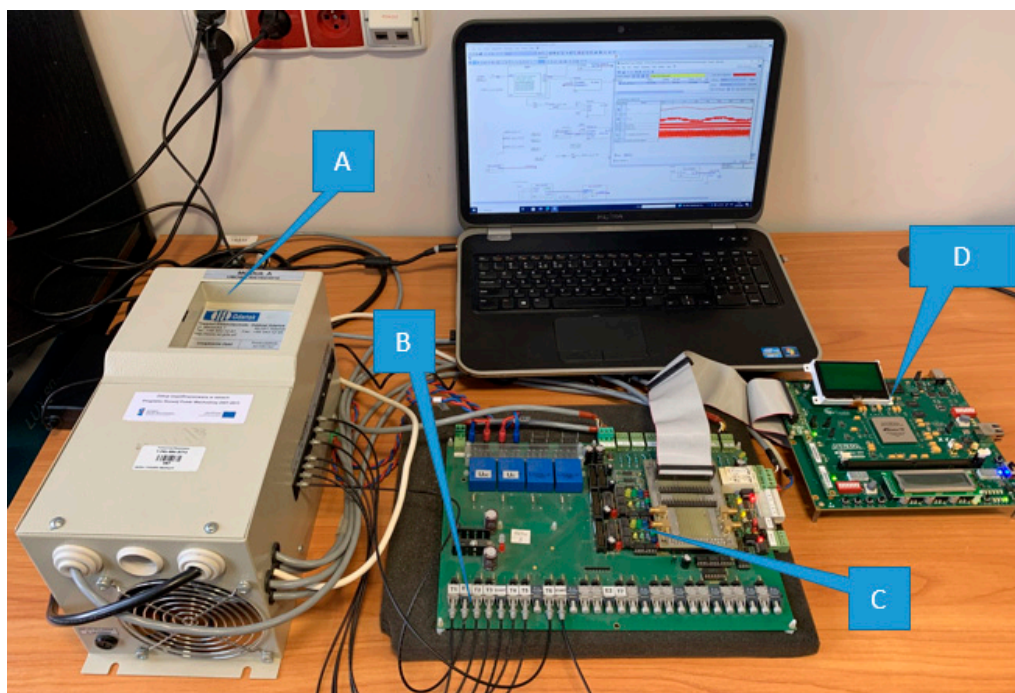
**Table 3.** key performance indicators obtained from the conducted simulations.

| Method          | Settling time | Overshoot  | Frequency error |
|-----------------|---------------|------------|-----------------|
| SRF-PLL         | Highest       | Moderate   | Very small      |
| SOGI-PLL        | Medium        | Small      | Very small      |
| Proposed Method | Lowest        | Very small | Very small      |

The results clearly indicate that the proposed synchronization algorithm achieves the fastest convergence while maintaining high steady-state accuracy. The comparison results highlight several advantages of the proposed adaptive synchronization method. First, the direct adaptive frequency update law enables faster convergence compared with conventional PLL structures that rely on PI controllers. Second, the algorithm maintains good robustness against harmonic distortion and measurement noise. Finally, the computational complexity of the proposed approach remains relatively low, making it well suited for real-time FPGA implementations. These characteristics make the method particularly attractive for applications requiring fast and reliable synchronization, such as grid-connected converters, power electronics systems, and real-time signal processing platforms.

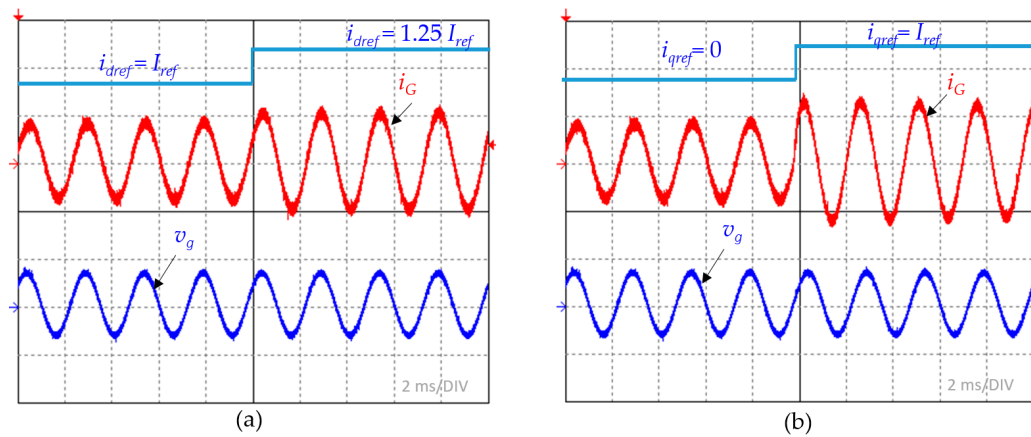
#### 4.9. Hardware Tests

The proposed adaptive control algorithm was validated using a hardware-based implementation targeting a field-programmable gate array (FPGA) platform. The experimental setup consisted of a real-time control system interfacing with a simulated or laboratory power stage representing an onboard 400 Hz electrical grid. The control algorithm, including the adaptive phase-locked loop (PLL), proportional-resonant (PR) controller, and power regulation loops, was implemented using fixed-point arithmetic to ensure efficient utilization of FPGA resources. The system was designed to operate at a sampling frequency of  $f_s=10$  kHz, which provides sufficient temporal resolution for accurate control of a 400 Hz signal. The FPGA implementation was based on a pipelined architecture to minimize computation latency and ensure deterministic execution of all control tasks within a single sampling period. The control loop included: signal acquisition and preprocessing, Park transformation, adaptive PLL estimation, PR current control, reference signal generation. All modules were executed sequentially within a single control cycle, ensuring synchronized operation of the entire control system. The photograph of the experimental setup is shown in Figure 9, where: A—grid inverter, B—fiber-optic coupling, C—main onboard board, D—CPU based on FPGA EP3SL150F1152C2N of Stratix III family board.



**Figure 9.** Photograph of the hardware test bench.

The dynamic behavior of the control system was evaluated by applying step changes in the reference power.



**Figure 10.** Grid current  $i_G$  and voltage  $v_g$  for: step change in active power (a); step change in reactive power (b).

Figure 10 (a) shows the grid current and voltage waveforms in response to a step change of the active current component by 25%, resulting in a variation of the active power. The active current component directly influences the active power exchange with the system. Figure 10 (b) illustrates the system response to a step change in the reactive current component. This change leads to a corresponding variation in reactive power while having a negligible effect on the active power.

The experimental results show that: the system exhibits fast transient response, overshoot is limited due to adaptive synchronization, steady-state error remains negligible. The integration of the adaptive PLL with the PR controller enables precise current tracking, resulting in accurate power regulation even under rapidly changing conditions.

## Conclusions

This paper presented an adaptive synchronization algorithm designed for accurate estimation of the fundamental component of a sinusoidal signal. The proposed method combines the Park transformation with adaptive frequency and amplitude estimation mechanisms to enable robust tracking of signals whose parameters vary over time.

Unlike conventional phase-locked loop structures, the proposed approach directly updates the estimated frequency using an adaptive correction term derived from the quadrature component of the transformed signal. This structure eliminates the need for a classical proportional–integral loop filter and simplifies the overall control architecture while maintaining stable and accurate synchronization.

The algorithm simultaneously estimates the instantaneous phase, frequency, and amplitude of the input signal. The phase estimate is obtained through a discrete-time phase accumulator driven by the adaptive frequency estimator, while the amplitude is determined using a recursive estimation mechanism based on the direct-axis component of the Park transformation.

A series of simulation experiments was conducted to evaluate the performance of the proposed method under various operating conditions. The obtained results demonstrate that the algorithm is capable of accurately tracking sudden frequency changes, continuous frequency ramps, amplitude variations, and signals corrupted by noise or harmonic distortion.

In particular, the proposed method exhibits significantly faster convergence compared with conventional synchronization algorithms such as the synchronous reference frame PLL and the second-order generalized integrator PLL. The adaptive frequency update law enables rapid compensation of phase errors, leading to shorter synchronization times without sacrificing steady-state accuracy.

Furthermore, the algorithm maintains robust operation in the presence of harmonic distortion and measurement noise. The inherent filtering properties of the adaptive loop reduce the impact of high-frequency disturbances, resulting in stable frequency and phase estimates even under challenging signal conditions.

Another important advantage of the proposed approach is its suitability for efficient hardware implementation. The algorithm relies primarily on simple arithmetic operations and can be implemented using fixed-point arithmetic on FPGA platforms. Its modular structure allows straightforward pipelining, enabling high sampling rates and deterministic real-time operation.

These characteristics make the proposed synchronization technique particularly attractive for applications in power electronics, grid-connected converters, digital signal processing systems, and real-time monitoring platforms.

Future research may focus on extending the proposed method toward multi-phase systems, improving harmonic rejection capabilities, and exploring machine-learning-assisted parameter tuning for adaptive synchronization in highly dynamic environments.

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