Article

Multicell Power Supplies for Improved Energy Efficiency in the Information and Communications Technology Infrastructures

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Abstract: The rapid growth of the Information and Communications Technology (ICT) sector requires additional infrastructure, such as more micro-datacenters and telecom stations, to support the higher internet speeds and low latency requirements of 5G networks. The increased power requirements of the new ICT technologies necessitate the proposal of new power supplies in an attempt to retain the increase in energy demand and running costs. This work provides an in-depth theoretical analysis on the losses of the individual stages of commercially available PSU and proposes a new multicell PSU, Buck-PFC converter, which offers a higher overall efficiency at varying load levels. The theoretical results are verified using simulation results, via PSIM Thermal Module, and using experimental data. The results indicate that multi-cell structures can improve the overall PSU efficiency by 1.2% at 50% rated power and more than 2.1% at full power. Finally, taking into consideration the economic implications of this study, it is shown that the proposed multicell structure may increase the PSU costs by 10.78% but the payback period is in the order of just 3.3 years .

Keywords: MICRO-DATACENTRES, INFORMATION AND COMMUNICATIONS TECHNOLOGY (ICT), EFFICIENCY, POWER SUPPLY UNIT, MULTICELL.

1. Introduction

The 5G network requirements for the Information and Communication Technology (ICT) sector has caused a continuous demand growth in micro-datacentre and Telecommunication Stations (TS) [1], [2].   Datacentres accommodate the ICT data storage and processing equipment such as servers, hubs, hard discs, ICT racks etc. A micro-datacentre (μDC) is a datacentre of size smaller or equal to one rack. The growth of datacentres and micro-datacentres is huge nowadays and they have great impact on global electricity consumption. In 2016, more than 1.8% of the global electrical energy was consumed by datacentres and this will keep increasing [3]. The higher speeds of radio frequency bands (such as 4G and 5G) tend to have shorter area coverage and as a result more TS are needed. The increased number of TS and μDC will unavoidably lead to increased energy consumption.

The impact of the power supply system to the overall energy efficiency of datacentres and TS has pushed several energy agencies to develop strict efficiency requirements such as Energy Star and EPRI [4], [5]. In the last two decades, the telecommunications industry adopted equipment supplied by 48 V DC. In the Information Technology (IT) and Datacentre industries though, the preferred voltage system over the last decades was 230 V AC, with integral secondary power supplies for converting the AC 230 V to 12 V DC. With the IT and Telecom industry convergence of the last few years, both AC 230V and DC 48V systems were used with a debate as to which system would dominate the market. Over the last few years, Facebook initiated the "open compute project" and other organizations have joined such as Google and Microsoft for promoting the 48 V DC distribution topology for the IT industry as well because of its improved performance [6-7].

Multicell Structures have been utilized in the last two decades for several applications but the main objectives were the improvement of the voltage gain in the input or the output of a circuit and the component stress decrease. There are four different topologies of multicell structures which are:

- Input in Series Output in Series (ISOS)

- Input in Series Output in Parallel (ISOP)

- Input in Parallel Output in Series (IPOS)

- Input in Parallel Output in Parallel (IPOP)

Aiming for higher efficiency, Kasper et al. [8] suggested a 6-cell converter system which showed the highest efficiency conversion above 1 kW however, the suggested converter [8] has great efficiency only in specific loading conditions. Furthermore, the 6-Cell ISOP converter creates additional complexity to the system and reduced reliability since failure of one of the cells could lead to overall system failure especially as cells are connected in series at the input. Multicell structures have been used in various studies but not primarily for energy efficiency improvement. Arezki Fekik et al. [9] proposes a three-cell DC to DC structure for Off-Grid PV systems for improved robustness using ISOS structure but the study does not include an experimental verification and although simulation results are promising in terms of Maximum Power Point Tracking (MPPT) function, the efficiency is not validated. Furthermore, the reliability of the three-cell DC to DC structure is reduced since failure of one of the three cells leads to overall system failure. ISOS structures in both AC to DC and DC to DC conversion stages do not significantly improve the efficiency and have much more complicated load sharing control [10, 11]. The IPOS structure proposed in [12] in order to improve efficiency and output voltage, reduces the overall system efficiency (maximum efficiency of 91%) and increases the complexity of the system.

The paper analyses and compares multicell topology structures (ISOS, IPOS IPOP or ISOP) and the way that these can lead to energy efficiency improvements by investigating each stage of conversion (Rectification, Power Factor Correction and DC to DC stage through LLC and PSFB converters). The work verifies through simulations and experimental measurements that IPOP structures can lead to improved energy efficiency conversion and proposes a new Multicell Buck PFC structure to increase the energy conversion efficiency. Furthermore, the work presents a technoeconomic evaluation of multi-cell structures compared to single structure Power Supply Units.

The introduction section of the work is followed by section two which presents the structure of AC/DC 48 V power supplies. The section identifies and analyzes the three individual conversion stages and specifies single stage and two stage conversion alternative topologies. In section three, the multicell structure topologies are introduced and analyzed. This analysis is subsequently followed by section four, the experimental setup and verification. The proposed multicell Buck-PFC converter is presented in section five and a technoeconomic analysis follows in section six. The last section of the paper, section 7, is the conclusion.

2. Structure of AC to DC 48 V Power Supplies

Power Supply (PS) systems tend to have low efficiency under low loading conditions. It is for this reason that modular PS systems are commonly used within TS and datacentres to overcome the problem of oversized PS systems. A DC PS system may be composed of a number of Power Supply Units (PSU), frequently called "modules", that work in parallel to feed a DC bus, creating in this way a scalable PS system. A PSU consists of three main stages: (a) The AC to DC rectification, (b) the Power Factor Correction (PFC) stage, and (c) the DC to DC stage to step-down the voltage to the desired 48 V DC, Figure 1. A μDC should have a capacity of up to 20 kW and thus a modular μDC should have PSU modules of less than 10 kW (at least 2 modules) $P_{module} \leq (P_{rack-max} / 2)$. The rectifier stage of the PSU consists of a bridge rectifier with switches (MOSFETs, IGBT, Thyristors, etc.) or diodes. The power factor correction system is used to ensure conformity with EN61000 and that there are no excessive harmonics in the AC supply from the UPS system. The third stage of a PSU is needed to step-down the voltage from the rectification stage to the desired 48 V DC. The rectification is common in all systems but there are two options used to get the desired 48 V DC and to satisfy the input power quality requirements. The

first option is to use a two-stage process with Boost PFC and DC to DC step-down converter. The second option is to use the buck PFC single-stage circuit solution (PFC and DC to DC step-down circuits combined). In a single-stage conversion circuit it is very difficult to control both the input current quality, the output voltage level at different loads and at the same time achieve high conversion efficiency. The two-stage conversion is therefore preferred as a solution for loads above 1 kW [13], [14].
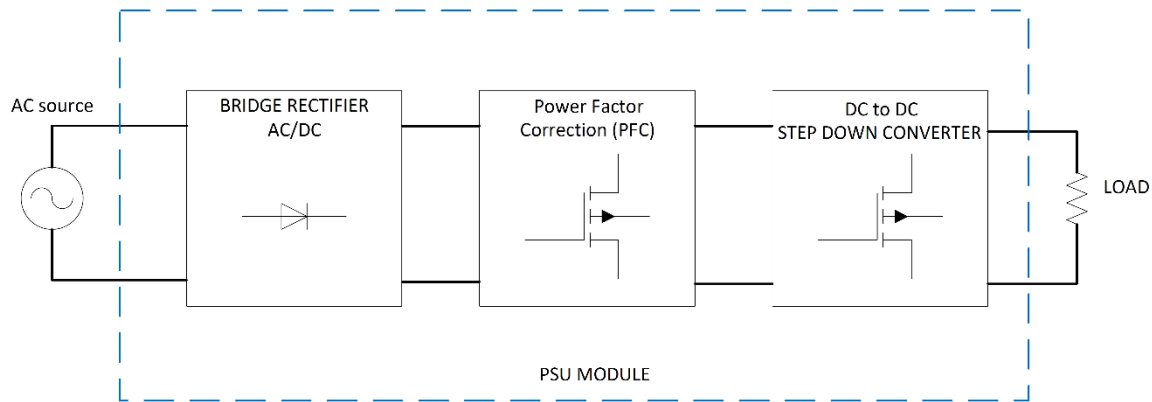

Figure 1. Block diagram of PSU.

2.1. Single-Stage PSU

The single-stage PSU is a Buck PFC system with a bridge rectifier. Buck PFCs are used in low power applications since their structure creates dead angles at the input current waveform. Dead angles are generated from the switching of the input rectified waveform. Boost PFC circuits have the switching device in the output of the circuit and thus have higher THD and is therefore preferred for high power applications [13], [14]. On the contrary, since Buck PFCs are only single-stage conversion systems they present higher efficiency than Boost converters at low power applications. Is not easy to get rid of dead angles in Buck PFCs. Several researchers aimed to minimize their impact such as Saeed Sharifi et al. [15], who introduced a new Buck PFC circuit with a Z-source network that smooths out the switching effect on the input power quality, Figure 4. The Z-Source circuit was initially proposed by B. Axelrod et al. [16] with its main target to increase the voltage gain in Buck converters. Fortunately, the new circuit introduces a new input inductor that not only increases the gain but also minimizes the stress on the switch and smooths out the input current dead zones.

2.2. Two-Stage PSU solution

The two-stage solution includes the AC to DC Boost PFC which converts the AC input voltage to 380-400 V DC and maintains input power quality and a DC to DC step-downconverter to step-down the voltage to the desired level. Due to imperfect switching (especially for high power applications), high switching losses occur in the converters. To step-down the voltage from 380-400 V to 48 V DC as previously described, a DC to DC step-down converter is needed. Since high energy efficiency and power density is required for such converter systems, the most commonly used low power (under 1 kW) converter circuit is the LLC Half or Full-Bridge Converter [17-19]. These converters are resonant converters that adopt Zero Voltage Switching (ZVS) techniques in order to minimize switching losses, something that improves the efficiency of conversion. LLC half or full bridge converters however incorporate transformers in their structure that create no-load losses and therefore have low efficiency on low loads.

3. Multicell Structures

A multicell structure, is a structure made of multiple converter systems (cells) put together and working in parallel or in series to form a new larger converter system as shown in Figure 2. This work aims to prove that combining multiple converters (multicells) in series or in parallel can lead to overall energy efficiency improvements. Since conversion from AC 230 to DC 48 V includes more than one conversion step, multicell efficiency improvements need to be analysed per stage (AC to DC, PFC stage and DC to DC step-down stage).
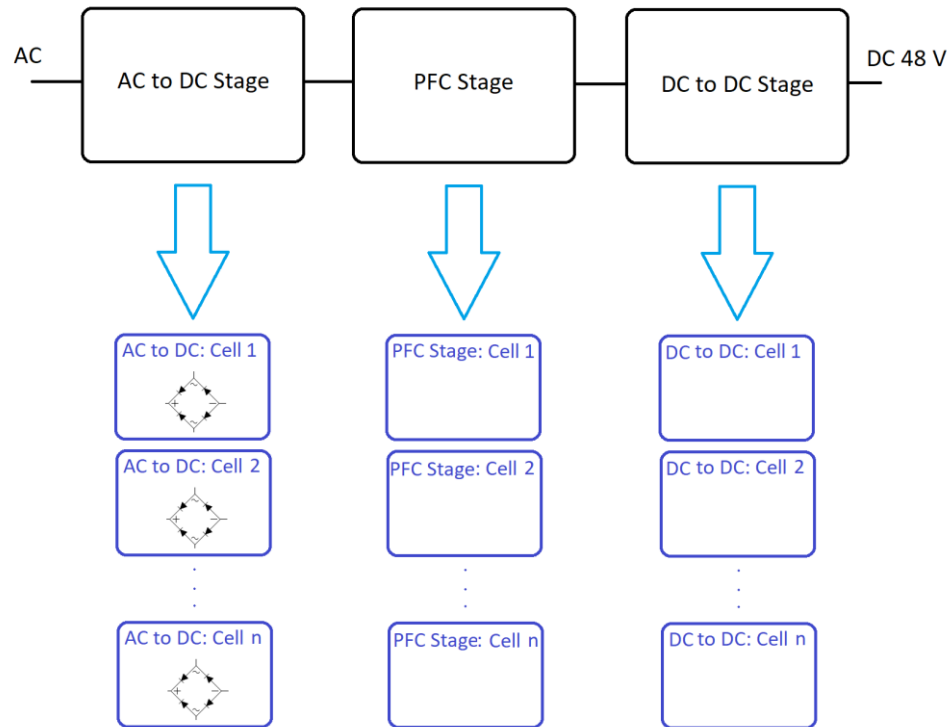
Figure 2. Block diagram of a multicell structure.

3.1.   The Multicell AC to DC Rectification stage

A multicell rectification can be constructed either with diodes or switches (MOSFETs, IGBTs etc) as previously mentioned. A strategy to minimize the losses in the rectification stage is to use parallel diode bridge rectifier systems [20]. Considering that each bridge circuit is a cell, using multiple bridges a multicell structure is formed. According to [20], parallel diode bridge rectifiers lead to lower losses because diodes with lower maximum current currying capacity have less forward voltage drop although this stands only for specific applications.   The power losses are mainly generated as a result of the conduction and the switching of the diodes or the switches. Due to the low switching frequency (50 Hz or 60 Hz), the switching losses are almost negligible and the resultant losses of each of the two bridge rectifier legs arise mainly due to conduction. The use of IGBT switches would not benefit such systems since IGBT losses are similar and higher than diodes for similar power applications. GaN MOSFETs tend to have lower switching losses than silicon MOSFETs despite their higher conduction resistance (on-resistance $R_{DS\text{-}On}$).

For the diode case, the conduction losses are given by:

$$P_{Dloss} = I_{rms}.V_d \tag{1}$$

Where V_d is the diode voltage drop and I_{rms} is the average current passing through bridge leg.

For the MOSFET switch case, conduction losses are given by:

$$P_{Loss} = I_{rms}^2.R_{DS-On} \tag{2}$$

Where $R_{DS\text{-}On}$ is the on-resistance of the MOSFET switch.
Connecting bridge rectifier cells in ISOS or IPOS would imply that the output voltage is a multiple of 325 V (V_{peak} of AC input). This would require a very high gain to reduce it to 48 V and thus higher power losses in the secondary circuits to step down the voltage. Additionally, a high voltage at the output of the bridge rectification stage would need switches that withstand higher voltage. Since $R_{DS\text{-}On}$ is proportional to voltage, this would result in higher power losses. Therefore, the multicell bridge would not have better efficiency if connected in ISOS or IPOS. The ISOP structure with MOSFET switches would not improve the efficiency either since the series switches

would increase the conduction losses. Considering however that the breaking voltage is proportional to $R_{DS\text{-}On}$, switches with lower withstand voltage would have lower conduction losses. Replacing therefore one MOSFET switch with two switches of smaller $R_{DS\text{-}On,}$ could in theory result in better efficiency. Examining however the characteristics of available MOSFET switches, those with breaking voltage of 50 V have an $R_{DS\text{-}On}$ as low as 3.3 mΩ (IFR3805), while switches with breaking voltage of 200 V have an $R_{DS\text{-}On}$ as low as 4 mΩ (IXFK300N20X3). Therefore, no energy efficiency improvement could be achieved with ISOP and MOSFETs for this type of power supply. Analysing the circuit further, it can be seen that the ISOP structure of the bridge rectification part would not provide any energy efficiency improvement with diodes either, since in each cycle of the AC source only two switches/diodes conduct, Figure 3, as in the single cell structure, namely D_{1a} and D_{2b} in the positive cycle and D_{3b} and D_{4a} in the negative cycle. In the IPOP structure with diodes, the voltage drop is increased as the number of cells is increased. Efficiency is therefore slightly improved as a result of lower heat dissipation. For the case of the IPOP structure with MOSFETs, the voltage stress on the switches remains the same and the current passing through the system is divided in the parallel cell bridges, something that may lead to significant energy efficiency improvements.
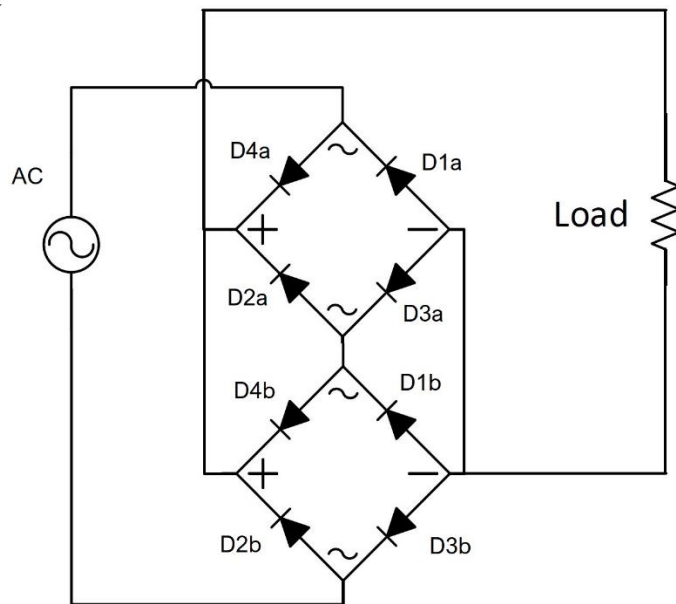

Figure 3. Multicell Bridge ISOP circuit

For instance, in a two-cell rectifier bridge system, the current in the two legs is halved (assuming MOSFETs with the same $R_{DS\text{-}On}$) and since $2\,(I/2)^2 < I^2$, it can be easily proven that parallel bridge structures lead to overall energy savings. For N cells, it can be shown that:

$$N \left[\frac{I}{N}\right]^2 . R_{DS-On} < I^2 . R_{DS-On} \qquad (3)$$

3.2. The Multicell PFC stage

There are different PFC structures. For single stage converters, Buck PFC can be used. For dual stage converters, the boost PFC is widely used as well as some modified boost PFC circuits. All PFC circuits are always following the AC to DC rectification, or they are incorporated into it.

3.2.1. Multicell Buck PFC

As discussed in the previous sections, to improve the power factor of the Buck PFC circuits, the Z-source Buck PFC circuit is proposed in [11] by adding a Z-source network in front of the Buck converter. As seen in Figure 4, the circuit has two switches SW1 and SW2. The losses arising in such a circuit are mainly as a result of conduction and switching as well as due to the inductor at the input. Conduction losses are given by equation (3) and the switching losses are given by equation (4).

$$P_{sw} = V_{in} \cdot I_{out} \cdot f_{sw}(t_r + t_f) \qquad (4)$$

Where f_{sw} is the switching frequency, t_r is the rising time the transistor needs to switch on and t_f is the falling time needed to switch off.
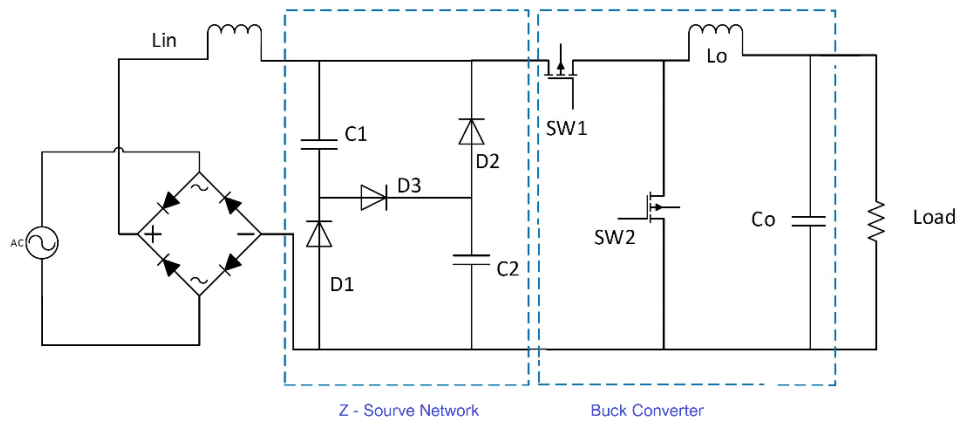

Figure 4. The Z source Buck PFC

In a multicell parallel input configuration such as IPOP and IPOS, the input peak voltage would be 325 V DC (with ripple). For parallel cell circuits, the current in each of the parallel circuits would be split equally and the conduction losses would therefore decrease. The switching losses on the other hand cannot decrease. Considering the use of switches with lower drain current, faster response and thus lower t_r and t_f, they could potentially lead to better efficiency. Using however switches with lower t_r and t_f and at the same lower maximum drain current capability, this may negatively affect the R_{DS-On} (i.e. conduction losses).

Connecting the multiple cells in series would require higher gain at the output. As a result, bigger inductor and capacitor at the output would be required that would lead to higher losses especially on low loads. Therefore, the IPOP is the only parallel input configuration that should be examined. In a parallel configuration, the inductor winding losses are also less since the current passing through them is divided by the number of cells and despite that core losses of inductors can increase, they are negligible compared to winding losses. The inductor size in the split cells would not be affected since the output and input voltages as well as switching frequency remain the same. The equation for calculating the inductor size is given by:

$$L = V_{out} \cdot \frac{(V_{in} - V_{out})}{\Delta I_L} f_{sw} \cdot V_{in} \qquad (5)$$

Where ΔI_L is the ripple current and is proportional to the output current of each cell.

Connecting multiple Buck-PFC cells in series at the input (ISOP or ISOS) causes higher overall R_{DS-On} resistance during the ON state. The switching losses on the other hand are multiplied by the number of cells but the voltage input is divided by the number of cells (assuming exactly the same R_{DS-On}). The rising and falling times of the switches in the multicell ISOP and ISOS structures can be minimized since switches with lower voltage breaking capacity tend to have lower falling and rising times. Silicon MOSFETs can have R_{DS-On} as low as 3.5 mΩ, with rising and falling times of about 170 nS (IXFN300N20X3), while GaN MOSFETs can have 12.4 ns rising and 24 ns falling time with R_{DS-On} of 25mΩ (GS66516). On the other hand, inductor losses are increased if the inductor size is not reduced from the single cell design. Since voltage gain is reduced in the ISOP and ISOS structures, the inductor size can also be significantly reduced. Therefore, ISOP or ISOS structures lead to reduced inductor losses but with insignificant switching loss improvement. The overall improvements are minor in relation to the complexity and increase in cost.

3.2.2. Multicell Boost PFC

The losses in the Boost PFC circuit (as in the Buck PFC) are mainly due to switching and conduction loss of the MOSFETs, the input inductor and the output capacitor. Because however of the higher voltage stress applied on the switches of the Boost PFC compared with that applied on the Buck PFC, higher conduction losses occur. ISOS and ISOP structured Boost PFC would lead to increased losses in MOSFET devices since will they be

connected in series, even if lower $R_{DS\text{-}On}$ MOSFET switches are used. Since in ISOP and ISOS structures the inductors are in series, the overall DC resistance and hence inductor losses will increase. Considering the inductor size needed to form a multicell ISOP or ISOS structure compared to single cell, it can be concluded that the ISOP case would lead to reduced losses compared to ISOS, but both cases would not lead to a significant reduction in the inductor overall size and power losses (6), (7) &(8) . The single cell Boost PFC inductor value is given by [20]:

$$L = \frac{T}{\%Ripple} \cdot \frac{V^2_{ac-min}}{P_o} \cdot \left[1 - \frac{\sqrt{2} \cdot V_{ac-min}}{V_o}\right] \tag{6}$$

In a Multicell ISOP Boost PFC the inductor value per cell is calculated by:

$$L = \frac{T}{\%Ripple} \cdot \frac{V^2_{ac-min}}{P_o \cdot N} \cdot \left[1 - \frac{\sqrt{2} \cdot V_{ac-min}}{V_o \cdot N}\right] \tag{7}$$

In a multicell ISOS Boost PFC the inductor value per cell is:

$$L = \frac{T}{\%Ripple} \cdot \frac{V^2_{ac-min}}{P_o \cdot N} \cdot \left[1 - \frac{\sqrt{2} \cdot V_{ac-min}}{V_o}\right] \tag{8}$$

For IPOS and IPOP structures as in the Buck-PFC case, the current is split between cells something that as previously mentioned, reduces both inductor and MOSFET losses.

3.3. *The Multicell DC to DC voltage step-down in two stage conversions*

The most common type of circuit for high efficiency DC to DC step-down conversion is the resonant converter such as LLC [17], [18] and Phase Shift Full Bridge converters (PSFB). The presence of the transformer in these circuits provides magnetic isolation to the connected load. The losses for these types of converter circuits are again down to the switches, the inductors, the capacitors and the transformers. These circuits use Zero Voltage Switching (ZVS) techniques to minimize the switching losses. These techniques do not influence however the conduction losses. The losses because of the inductors and the transformers are a result of the core and I^2R of windings. The core losses are given by:

$$P_{core} = P_{hysterisis} + P_{eddy} \tag{9}$$
$$P_{hysterisis} = K_h f B^n V_e \tag{10}$$
$$P_{eddy} = K_e f^2 B^2 V_e t^2 \tag{11}$$

Where K_e and K_h are the eddy and hysteresis loss constants, P_{eddy} is the eddy current power loss (W), B is the flux density (Wb/m^2), f is the frequency of magnetic reversals per second (Hz), t is the core material thickness (m), V is the volume of core (m^3) and n is the Steinmetz exponent (ranges from 1.5 to 2.5 depending on material)

Core losses are not proportional to the current passing through the coils. In inductors, the core losses are proven to be negligible compared to winding losses. In transformers however, the larger core size the higher the core losses even without any load. Paralleling transformers would reduce winding losses but would increase core losses and the overall losses would therefore also increase.

4. Experimental verification of multicell

This experimental verification work validates the use of parallel converter cells within a PSU system for improved overall energy efficiency. To experimentally validate this proposal, a small-scale experimental setup was implemented with 3 Buck conversion cells of maximum power output of 18 W, input voltage of 24 V DC and output 5 V DC connected in IPOP structure.

Initially the setup was simulated in PSIM thermal module for comparison of theoretical and experimental results. The setup consists of 3 Buck converter cells, a 3-pole switch for switching of the 3 parallel cells, variable loads, and two power meters measuring input and output voltage, current and power. The Buck Cells used are commercially available and they employ the LM2596 controller. Photo of the experimental setup is shown in Figure 5 and Figure 6 shows the respective schematic diagram. The input power meter used is a Lucas-Nulle Analog/digital multimeter, wattmeter and power-factor meter model SO5127-1Z with measurement accuracy of 2% with capability to work with voltages of up to 600V and current range 0-20A. The meter used in the output of

the multicell conversion system is Fluke 345 PQ meter with accuracy in current measurement of ±0.2A or ±1.5% and accuracy of voltage measurement of ±1%. It is worth to mention here that since the measurements with 3 cells, 2 cells and 1 cell are comparative, the efficiency improvement could be easily verified. As it can be seen in Figure 5, for 17 W load output, the power input with 3 buck cells is 22.8W. For instance, at the same load (of 17W) with 2 cells, the input power was 23.1W. The voltage input to the 3 cells was 23.56V and current input 0.97A.
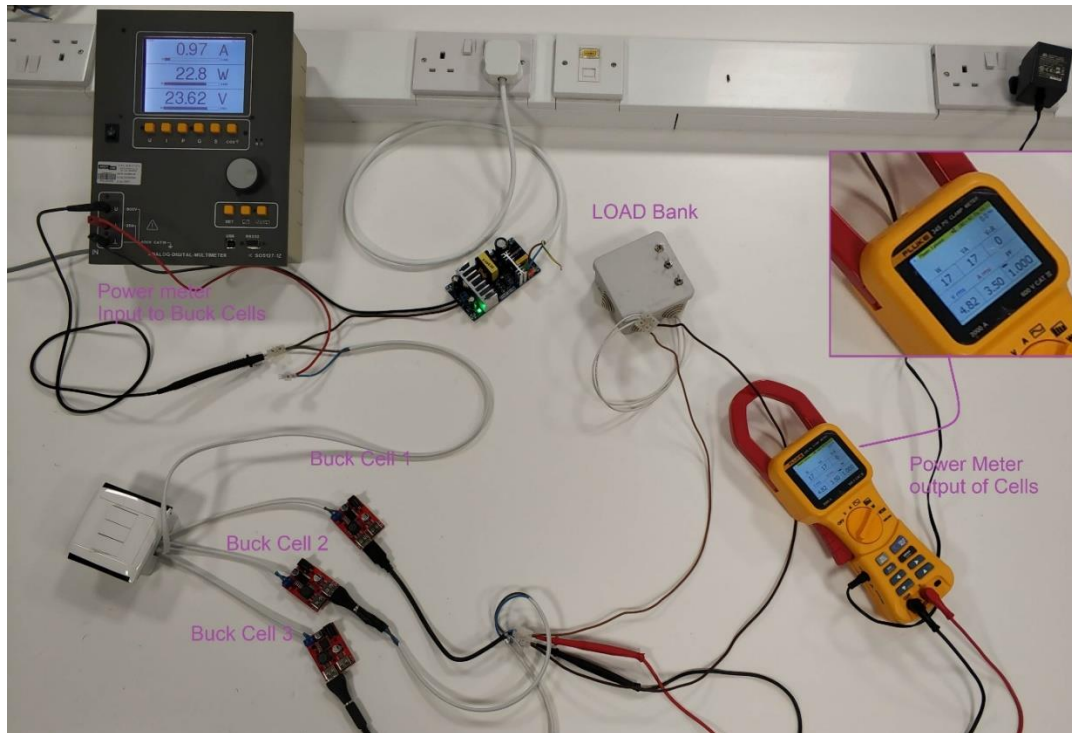

Figure 5. Experimental setup with parallel buck converter cells.

The efficiency of the single buck cell at different load conditions was measured and graphically analysed and used as a baseline for energy efficiency. Following the experimental measurements with one Buck converter cell, two and subsequently three similar Buck converter cells were used. Repeating the same methodology and measurement strategy, the load-efficiency curve was constructed, Figure 7. It is worth mentioning, that the no-load consumption of one, two and three PFC circuits have an effect on the load-efficiency curves. As it can be seen in Figure 7, for loads corresponding to 10-20% of the full load (i.e. 1.8-3.6W), the efficiency of one Buck converter cell is higher than the case with two and three Buck converter cells. For instance, on 2 W load, the efficiency of 1 cell was 72.76% and with 3 cells 70.63%. Additionally, on 3.6 W load, the efficiency with 1 cell was 72.5%, with 2 cells 72.32% and with 3 cells 72.07%. This is due to the no-load losses of the PSU modules arising mainly from the inductors and the control circuitry. The no-load loss of a single Buck converter cell is found to be 0.1904 W, that of two cells was equal to 0.238 W and for three cells 0.3094 W.
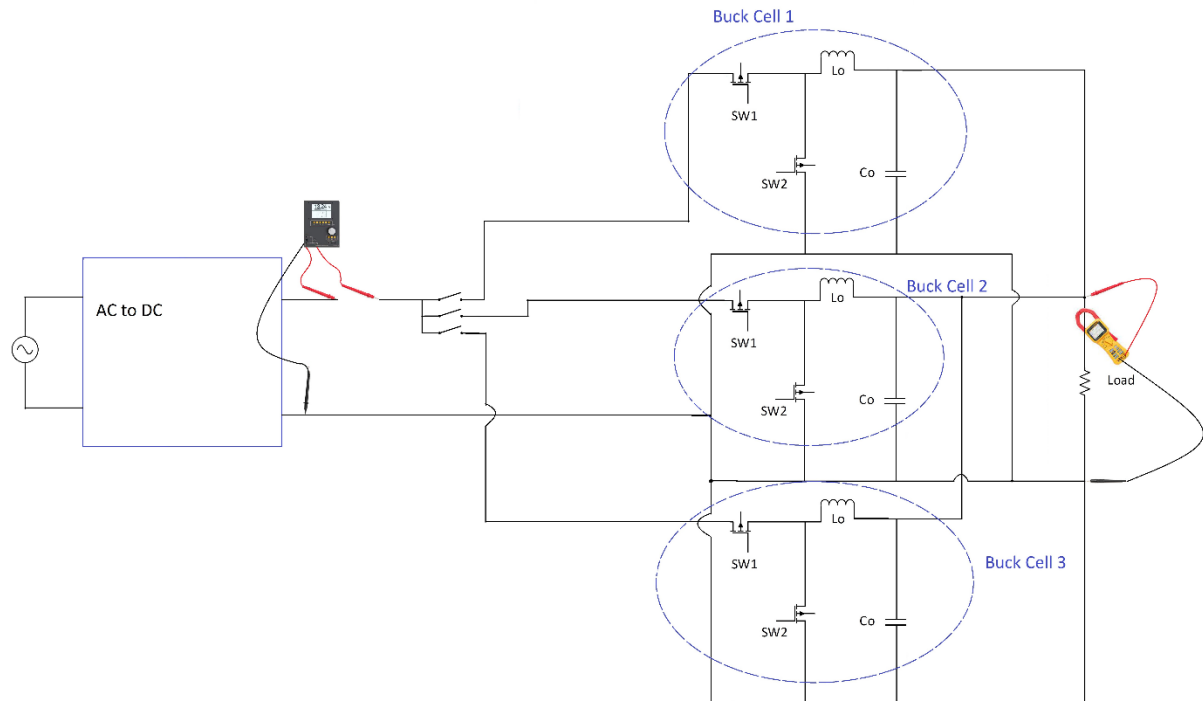
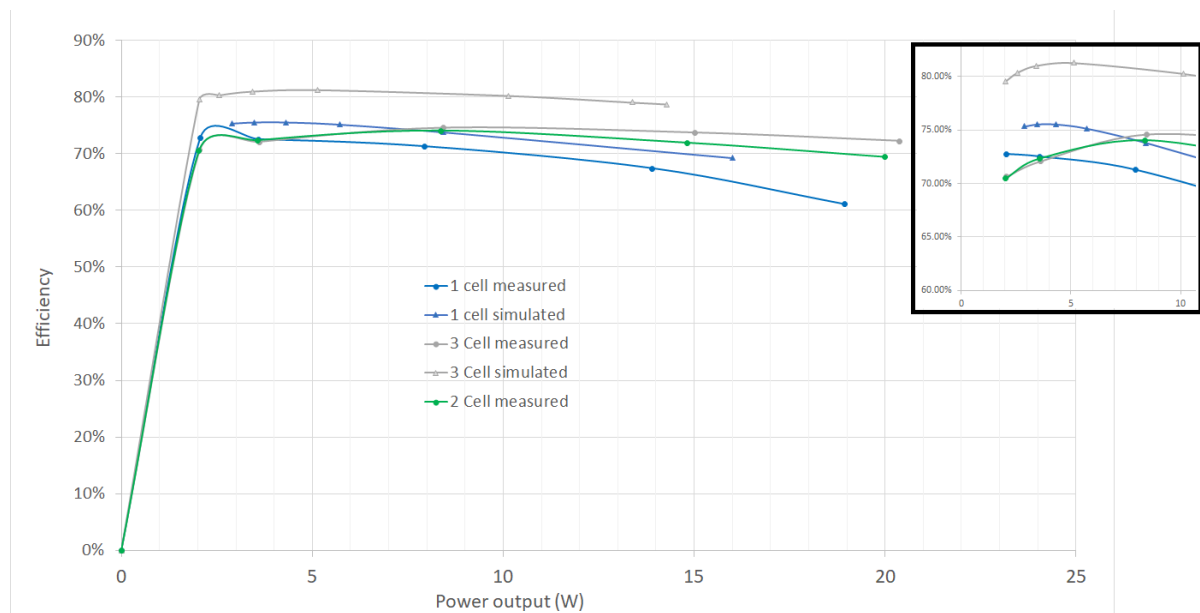**Figure 6**: Circuit diagram of experimental setup

Figure 7. Efficiency comparison of 1-cell and 3 cell multicell buck converters

It can be theoretically and experimentally shown that using parallel cells of the same converters type, size and brand, the load is equally shared between the number of parallel cells. Power converters or PSUs are voltage-controlled systems in which the controller must maintain the output voltage level within certain values for different loading conditions. Either in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), the small signal model of the Buck converter in the secondary (output) side of the converter, consists of DC sources and a series impedance/resistance. The voltage and resistance of CCM and DCM modes is of course different when analysing the small signal model. The equivalent simplified circuit for DC power supplies proposed from this work is shown in Figure 8. Using the circuit proposed, the equation of output power as a function of output voltage, load and internal resistance can be derived for different Cells and is given by:

$$P_{out-m} = \frac{V_{oc-m} - V_{out}}{r_m} \qquad (12)$$

For multiple and dissimilar in size and type cells, it can be shown that connecting "w" number of cells of type A and "q" number of cells of type B in parallel supplying a common load, the voltage at the output is given by:

$$V_{out} = \frac{\left[w\frac{V_{oc1}}{r_1}+q\frac{V_{oc2}}{r_2}-P_{out}\right]}{\frac{w}{r_1}+\frac{q}{r_2}} \tag{13}$$

Where: V_{oc1} and V_{oc2} are the cell type A and cell type B, open circuit voltage, V_{out} is the output voltage of the system, r_1 is the internal resistance of type A buck-cell and w & q are the number of buck-cells of type A and B respectively connected to the system. The Power output of the system consisting of "w" cells of type A and "q" cells of type B is given by:

$$P_{out} = w.P_{out1} + q.P_{out2} \tag{14}$$

It is obvious from (12), (13), and (14), that each cell shares a portion of the output load based on the internal resistance, the open circuit voltage and the total load. For IPOP structures with same type of converter cells, (in ideal conditions) it can be realized from equation (12) that Pout of each cell is equal. Measurements results for load sharing between cells are shown in Table 1. The current was measured using three clamp-on ammeters of brand and type CEM, DT-362. The input power is measured through a Lucas-Nulle Analog/digital multimeter of type SO5127-1Z. The experimental set-up is shown in Figure 9.

Table 1: Load Sharing between three Buck cells

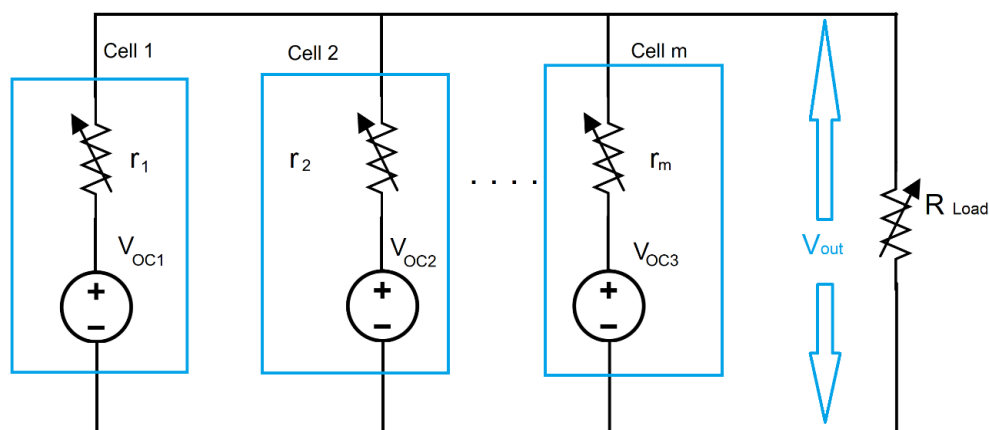| Power input cells (W)	Input current to Cell 1 (A)	Input current to Cell 2 (A)	Input current to Cell 3 (A)
10.9	0.16	0.17	0.17
21	0.31	0.33	0.3
30.7	0.46	0.46	0.43

Figure 8. Equivalent simplified circuit of parallel DC cells connected to a common variable load.

Figure 9. Experimental set-up of load sharing between parallel Buck cells

The no-load losses could not be measured by PSIM and this is why in Figure 7 the simulation results show higher efficiency in all load levels compared with the respective experimental ones. Under full load, an impressive 11.18% higher efficiency was measured with three cells compared to one cell. In addition to no-load losses, PSIM is unable to measure the capacitor losses, control system consumption and other losses arising from cabling, connections etc. Most industrial power supply units require high frequency transformers for isolation purposes that generate however excessive no-load losses. A single centralized transformer should be used in PSUs adopting the multicell circuitry structure. If each cell uses its own transformer this would result in increased losses and lower overall conversion efficiency. This can be proven experimentally by combining in parallel three complete PSUs including their individual transformer and measuring the efficiency for different loads. Three Eltek Valere Micro pack 250 W, 230 V AC input / 48 V DC output PSUs are used to perform this experiment. The input to the three PSUs was measured using a Lucas-Nulle Analog/digital multimeter measuring the input current, applied voltage and consumed power of the system. Each of the three PSU outputs was connected to "dummy loads" of different load values whilst measuring the output current and voltage. For every different load case, input and output parameters were measured so that the efficiency could be subsequently evaluated. The plot of efficiency versus load output is shown in Figure 10 from which is it seen that the efficiency decreases as the number of PSUs connected in parallel increases. The no-load consumption of the PSUs (mainly as a result of the transformers) was measured and found to be 5 W per PSU (i.e. 2% of efficiency at full load).
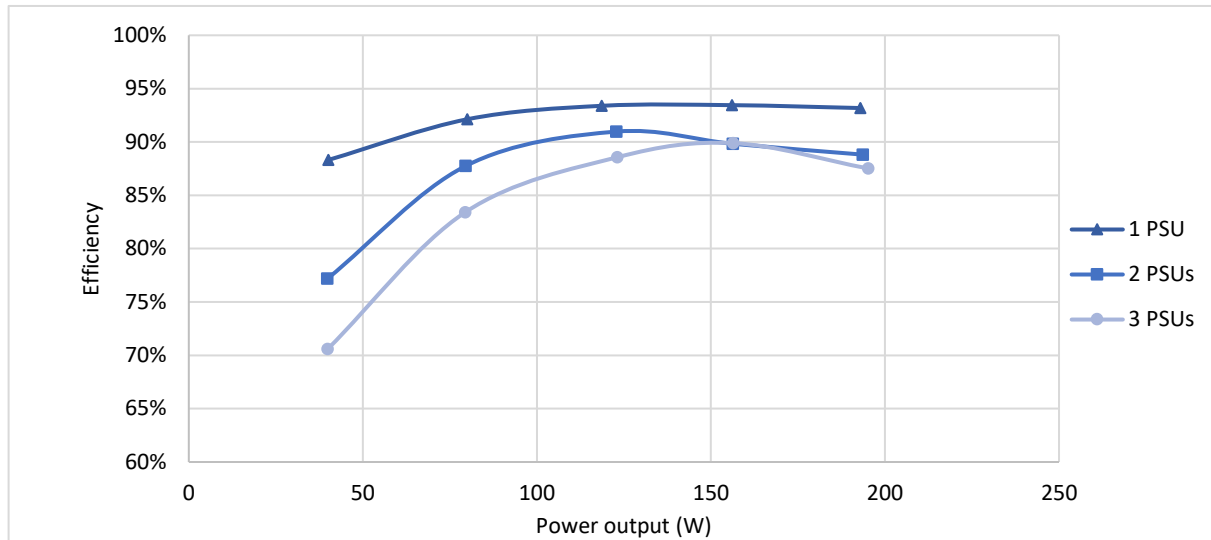
Figure 10. Efficiency against Power output of 1,2 and 3 PSUs working in parallel (with transformer)

5. Proposed Multicell Buck-PFC converter

5.1. Justification of AC to DC Multicell selection

In order to justify the selection and advantages of multicell structures, a high efficiency Z-source Buck PFC with power output of 1000 W was initially simulated. The proposed converter is a AC to DC step down conversion circuit with improved efficiency. Despite its single stage conversion structure, due to the Z-source filtering, it satisfies power supply regulation EN 61000-6-3. As a result, it is a transformer-less single stage conversion system that can be used with ISOP structures and with an improved energy conversion efficiency.

The results with the losses at different power output level are shown in Table 2. It should be noted that the input inductor was 3 mH and the one at the output 92.4 µH. The output inductor design was optimized to minimize losses based on [21], [22]. Table 1 shows that the total converter losses for the 200 W load output are 8.38 W and the efficiency comes out therefore to be 95.81%. For the 1000 W load case, the total losses are 55.15 W and the efficiency is 94.485%. It is interesting to note that the losses for switch 1 losses are lower than those of switch 2 for small loads however, as the load increase the losses of switch 2 become greater. Furthermore, the losses of the PFC stage are more than 40% of total circuit loss and the output inductor losses are negligible.

Initially, the AC to DC part of the multicell rectifier was simulated with the remaining parts of the PSU in single-cell structure. The results are shown in Table 3. The results are very promising since the load losses at 1000 W are considerably minimized. As expected, since for both inductors and MOSFET switches the main losses are due to the internal resistance ($R_{indutor}$ and R_{DS-On} respectively), the three-cell Buck PFC has significantly lower losses (since $N(I/N)^2 . R < I^2 . R$)

Table 2 Simulated single cell Buck PFC results

Power output (W)	Total Losses (W)	Switch 1 Losses (W)	Switch 2 Losses (W)	Rectifier losses (W)	PFC losses (W)	L1 loss (W)	L2 loss (W)
200	8.38	1.46	0.51	1.28	4.91	0.19	0.03
300	12.51	1.89	1.08	2.04	6.98	0.44	0.08
400	16.85	2.39	1.88	2.88	8.79	0.78	0.13
500	21.89	3.02	2.93	3.8	10.7	1.23	0.21
1000	55.15	8.56	11.07	8.68	20.93	5.08	0.83

The significant savings affect the overall PSU energy efficiency by up to 0.79% as demonstrated in Table 3. In the proposed multicell bridge simulation that consists of a three-cell system, it is shown that increasing the

number of cells the efficiency improves. The efficiency improvement is significant, especially under bigger load conditions but as the load decreases, the efficiency gains are relatively reduced.

Table 3 Comparison of 1-cell and 3-cell Rectifier system

Power output (W)	Single cell Rectifier losses (W)	3 Cell Rectifier losses (W)	**Rectifier** efficiency improvement	**Overall** PSU efficiency improvement %
1000	8.68	0.00288	>99%	0.79%
500	3.8	0.0144	>99%	0.70%
400	2.88	0.01872	>99%	0.66%
300	2.04	0.0261	>98%	0.62%
200	1.28	0.03636	>97%	0.58%

5.2. Multicell Buck PFC

Simulating a two-cell Buck PFC in PSIM's thermal Module, it revealed that inductor losses were minimized by about 50% as shown in Table 4. The switching losses remained about the same with those of a single cell system, conduction losses however were minimized by 52-57% for different loads and inductor losses are improved by 50% with the overall results of the new system shown in Figure 11. The results indicate that when increasing the number of parallel cells, the conduction and inductor losses decrease proportionally. Switching losses on the other hand are not affected. Using therefore GaN switches that have low switching losses compared to silicon MOSFETs and minimizing also conduction losses through multicell, leads to considerable efficiency improvement. The simulated system diagram is shown in Figure 12.
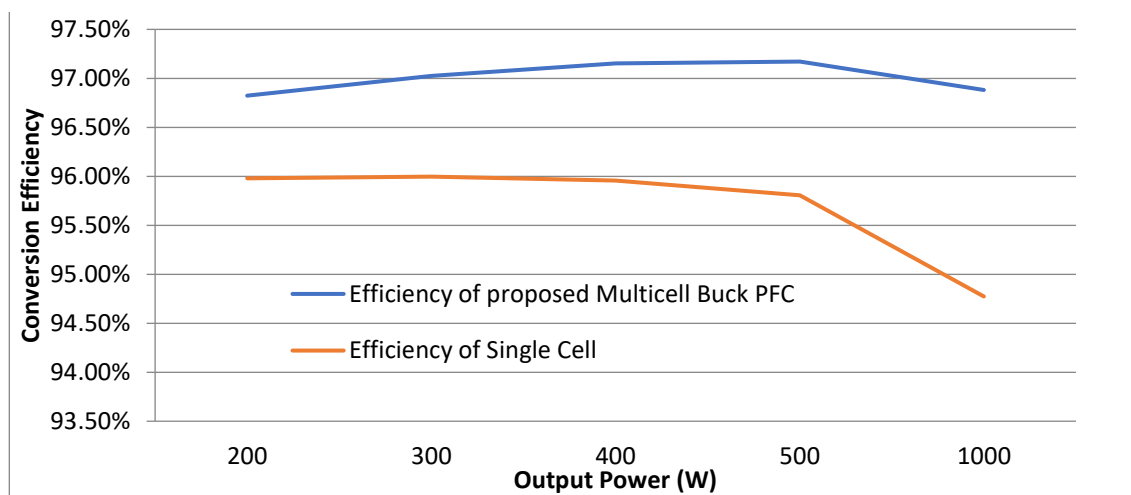

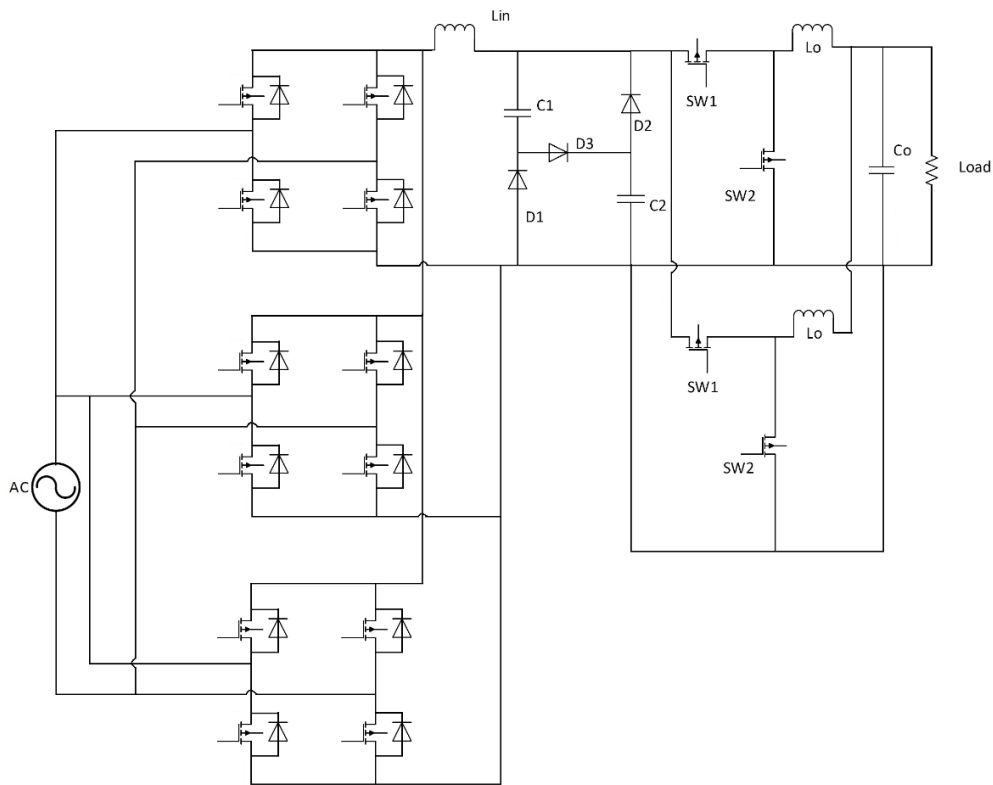**Figure 11.** Efficiency comparison of single-cell and multicell PSU

Figure 12. Multicell PSU circuit proposed

In order to simulate the thermal losses of the individual components of the circuit using PSIM's thermal module, each component was modeled with its equivalent circuit as shown in Figure 13. In the simulation the ambient temperature and the thermal resistance of each of the components is taken also into account. The flowchart in Figure 12 illustrates the procedure used for selecting the number of cells in the multicell structure ensuring no excessive cells are used. The first step is to identify the MOSFET switches with the lowest on-Resistance (R_{DS-On}).

All switches should have reverse voltage breaking capacity higher than the input voltage of the source. Since the price of the switches tends to be proportional to the output current, the flowchart in Figure 14 compares the system cost with the lowest cost switch and the system cost of a multicell structure with the lowest R_{DS-On} switches. The solution with the lowest system cost is selected from the product of number of cells and cost of switches.
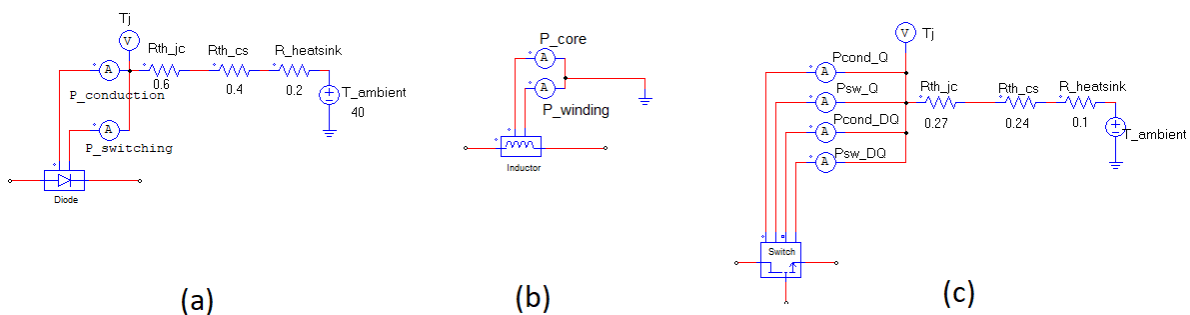

Figure 13. Equivalent circuits in PSIM thermal module for (a) Diode, (b). Inductor, (c). MOSFET
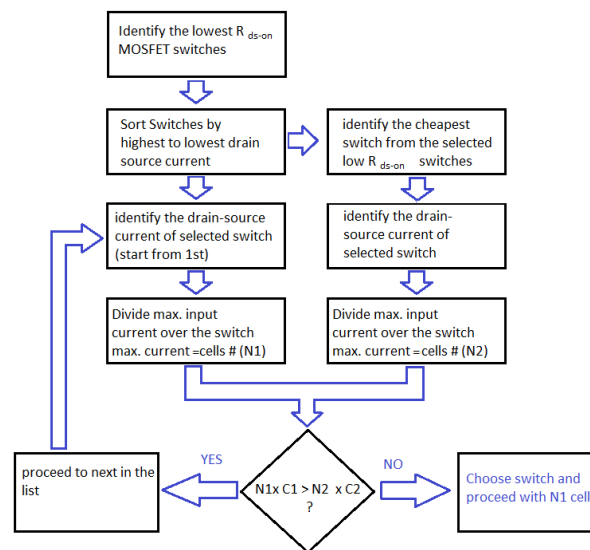
Figure 14: Procedure for cell/switch selection

6. Multicell PSU cost considerations

Of course, the improvement in efficiency comes at an extra cost as a result of the additional components used. The total manufacturing cost of a PSU system consists of the electronic components, the controller, the mounting, the enclosure and labour costs. A PSU consisting of multicell parts would have increased cost on components (cells) and labour costs but would not have increased cost on the controller, the mounting and the enclosure systems. Additionally, as earlier mentioned, the transformer systems which lead to a significant cost in PSU systems should be single (centralized) and thus no additional cost arise.

Analyzing the industry's readymade PSU prices, it can be observed that using smaller units (as those in multicell structures) for a 20 kW PSU (1 full rack) the cost is slightly higher. Table 4 compares the cost per watt using smaller PSUs for the same type and brand PSUs for different capacities.

The cost variation is in the order of 1-11%.   For example, constructing a 20 kW power supply system with 20 pieces of RCP-1000-48 would cost 10.78% more than using 10 pieces of RCP-2000-48. Using 4 Meanwell RST-5000-48 instead of 2 RST-10000-48, would cost 0.8% more, but using Jetpower SP60-48/CR4830 instead of SPS200-48/SR4850 systems would cost less per installed Watt.

Table 4 Comparison of cost per watt for different PSU systems

PSU brand	PSU model	Power output	PSU price	Cost per Watt	Reference
Mean well	RCP-1000-48	1000	$241.90	$0.2419	Jameco.com
Mean well	RCP-2000-48	2000	$436.69	$0.2183	Jameco.com
Mean well	RST-5000-48	5000	$1,193.00	$0.2386	Jameco.com
Mean well	RST-10000-48	10000	$2,366.00	$0.2366	Jameco.com
Jetpower	SPS60-48/CR4830	3000	$360.00	$0.1200	Alibaba.com
Jetpower	SPS200-48/SR4850	10000	$1,250.00	$0.1250	Alibaba.com

7. Conclusion

The results presented in this study demonstrate that using low-power modules such as the multicell structure for high-power PSU systems improves the energy efficiency. Using three rectifier cells and two Buck PFC cells, a more efficient power supply system can be constructed for the same power output. Efficiency

improvements of more than 1.2% can be achieved for 50% of the load and more than 2.1% efficiency improvement under full load. The concept of multicell efficiency improvement is experimentally proven through the testing of a three-cell, a two-cell and a single-cell Buck converter system. It is shown that efficiency improvement of up to 10% can be achieved for particular loads in the DC to DC conversion part.

The initial cost of a power supply system in a datacenter is about 5% of the total capital cost. A 10.78% increase in the power supply unit (i.e. the worst-case scenario) due to multicell structure compared to single cell, corresponds to an additional 0.5% increase in relation to the total capital cost. The respective savings however are in the order of 2.1% as previously mentioned. Looking ahead in the long-term, the cost benefit for this investment is viable as with simple calculations the payback period is in the order of just 3.3 years.

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