Brief Report

Self-rectifying Resistive Switching Memory based on Molybdenum disulfide for Low Power Synapse Array

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Self-Rectifying Resistive Switching Memory Based on Molybdenum Disulfide for Low Power Synapse Array

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Abstract: Resistive random-access memory has emerged as a promising non-volatile memory technology, garnering substantial attention due to its potential for high operational performance, low power consumption, and scalability. Two-dimensional nanostructured materials play a pivotal role in RRAM devices, offering enhanced electrical properties and physical attributes that contribute to overall device improvement. In this study, self-rectifying switching behavior in RRAM devices is proposed based on molybdenum disulfide nanocomposites decorated with palladium on SiO_2/Si substrates. The integration of Pd and MoS_2 at the nanoscale effectively mitigates leakage currents decreasing from cross-talk in the RRAM array, eliminating the need for a separate selector device. The successful demonstration of the expected RRAM switching behavior follows the application of a Pd nanoparticle coating. The fabricated Pd-MoS_2 synaptic device showed a high current ratio for forward/reverse current higher than 60 at a low resistance state and observed a memory on/off ratio of 10^3 performing stable resistance switching behavior.

Keywords: resistive random-access memory; molybdenum disulfide; palladium; self-rectifying; current ratio

1. Introduction

Emerging resistive random-access memory (RRAM) is gaining prominence in the field of non-volatile memory technology due to its excellent properties, such as fast operating voltage, low power consumption, scalability, and compatibility with CMOS. Neuromorphic synaptic RRAM devices offer the capability to store and retrieve data by altering their resistance states through the application of voltage pulses. This mechanism enables the realization of compact and energy-efficient memory solutions for various applications, including data storage & computing, artificial intelligence, and Internet of Things devices. However, RRAM devices face challenges in cross-bar array architectures due to leakage currents caused by interference between nearby cells. To alleviate cross-talk in memristive RRAM, a new concept of operational and structural solutions has been developed. Conventional synapse-based RRAM has been adopted in 1-transistor and 1-resister structure or 1-selector and 1-resister structure in which each RRAM cell is integrated with a nonlinear circuit device known as a selector device [1,2]. these approaches have disadvantages including larger cell sizes, increased operating voltages, and complex fabrication processes. As an alternative, research has been conducted to develop memory cells with self-rectifying properties to suppress leakage current interference in RRAM cells [3,4].

As shown in Figure 1, various materials have been explored for the application of self-rectifying RRAM, including nanomaterials, carbon-based materials [6,7], metal oxides [8], and transition metal dichalcogenides (TMDs), as electrodes and channel layers in various memory applications. Meanwhile, nanoparticles and nanosheets demonstrate the possibility of being used in memory device platforms and sensor applications through synthesis technology. Recently, nanocomposite materials have garnered interest in the fabrication of flexible RRAM devices due to their ability to

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form nanomaterials uniformly at room temperature [9]. The fabrication process of nanocomposites-based devices provides insights into low-power operation and resistance-switching characteristics. Metal oxide-based memristive devices possess intrinsic and favorable properties for switching behavior. Active layer deposition of metal oxides such as TiO_2 [10], ZnO, ZrO_2, HfO_2 [11–13], SnO_2, and Al_2O_3 [14], among others, is compatible with CMOS materials, making them suitable candidates for developing high-performance resistive switching memory and electronic synaptic devices.

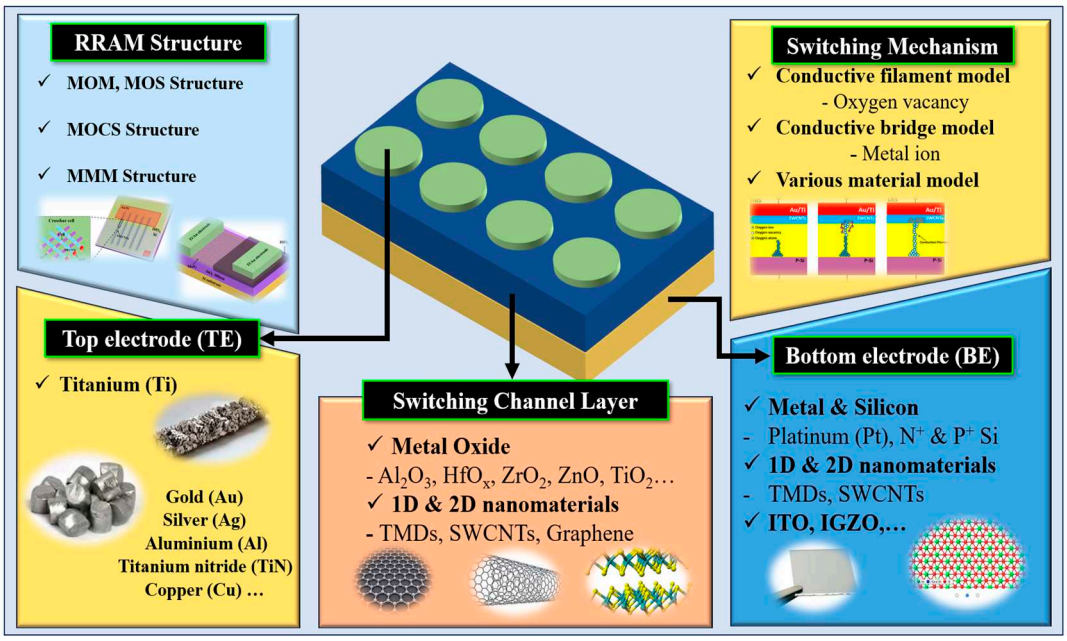

Figure 1. Illustration of various materials for RRAM device applications.

In this study, we propose a novel approach to achieve self-rectifying switching behavior in RRAM devices by applying Pd-decorated molybdenum disulfide (MoS_2) nanocomposites on SiO_2/Si substrates. The integration of Pd and MoS_2 at the nanoscale not only enhances the switching behavior of the device but also resolves the issue of leakage current caused by cross-talk in RRAM arrays. This advancement holds the potential for efficient operation in high-density memory cells without the need for additional selector devices.

2. Nanomaterials for Switching Layer

Memristive switching layers using carbon-based nanomaterials such as graphene, carbon nanotubes (CNTs), and multi-walled carbon nanotubes have been reported. On the other hand, CNTs can be categorized into metallic or semiconducting based on chirality and diameter, which affects the electrical and physical properties. Among the CNTs deposition methods, the synthesis of semiconducting CNTs is very difficult in dip-coating [15]. A semiconducting bandgap is required to represent RRAM self-rectifying diode characteristics as a switching channel layer. Consequently, two-dimensional (2D)-TMDs nanostructured materials are structurally like graphene materials but have adjustable bandgap [16]. The junction between the channel layer and the electrode facilitates the formation of a Schottky barrier, imparting diode characteristics. 2D-TMDs provide promising opportunities to optimize deposition thickness and leverage unique electrical and physical properties to enhance the performance of RRAM devices. Well-known 2D layered materials such as tungsten disulfide, molybdenum diselenide, and MoS_2 have attracted interest as suitable materials for RRAM channel layers [17]. MoS_2 has good characteristics as a channel layer due to its amazing flexibility, transparency, and good electron mobility compared to other materials. Various deposition methods were applied to satisfy the MoS_2 nanosheet with high quality. Many studies have attempted physical vapor deposition or chemical vapor deposition (CVD) technologies to grow thin MoS_2 layers [18,19]. MoS_2 has a special interest in RRAM applications for self-rectifying switching behavior, a

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phenomenon in which the direction of current flow is essentially controlled by the device structure. These switching behavior mechanisms eliminate the need for external diodes or selectors, simplifying device structures and reducing power consumption. Meanwhile, nanoparticles and nanosheets are showing the possibility of being used in emerging memory devices and intelligent memristors through synthesis technology.

3. Experimental Details

3.1. Fabrication Process

The memristor based on Pd-MoS_2 nanocomposites was fabricated as shown in Figure 2a. Initially, a sequence of cleaning steps was performed using acetone, isopropyl alcohol, and deionized water to remove organic solvents present on the p-type silicon substrate. After drying with N_2 gas, SiO_2 of 300 nm was formed on the p-type substrate by dry oxidation. For the synthesis of the MoS_2 switching layer, a CVD method was applied by introducing MoO_3 power (18mg) and S powder (120mg) into a furnace. During the growth of MoS_2, the argon (Ar)-gas flow rate, central heating zone temperature, and upstream S zone temperature were set at 25 SCCM, 750 °C, and 180 °C, respectively. Figure 2b illustrates the nanostructures of monolayer MoS_2 (≈ 0.72 nm) and multilayer MoS_2 (≈ 1.44 nm). Subsequently, a multilayer MoS_2 film was fabricated on the SiO_2. Figure 2c shows the deposition rate of the DC sputter equipment. Following photo-lithography pattering, Pd nanoparticles were mixed with MoS_2 nanosheets to form the switching channel layer. Pd, titanium (Ti), and gold (Au) were fabricated using 99.99% pure targets. DC sputter deposition conditions were kept constant with an Ar-gas flow rate, DC power, chamber working pressure, and substrate temperature set at 30 SCCM, 100 W, 1.4×10^{-3} Torr, and a range of 0 to 60 °C, respectively. To apply the top electrode (TE) and bottom electrode (BE) as two-terminal electrodes, Ti/Au were deposited with thicknesses of 10 nm/40 nm to complete the fabrication of the RRAM device.

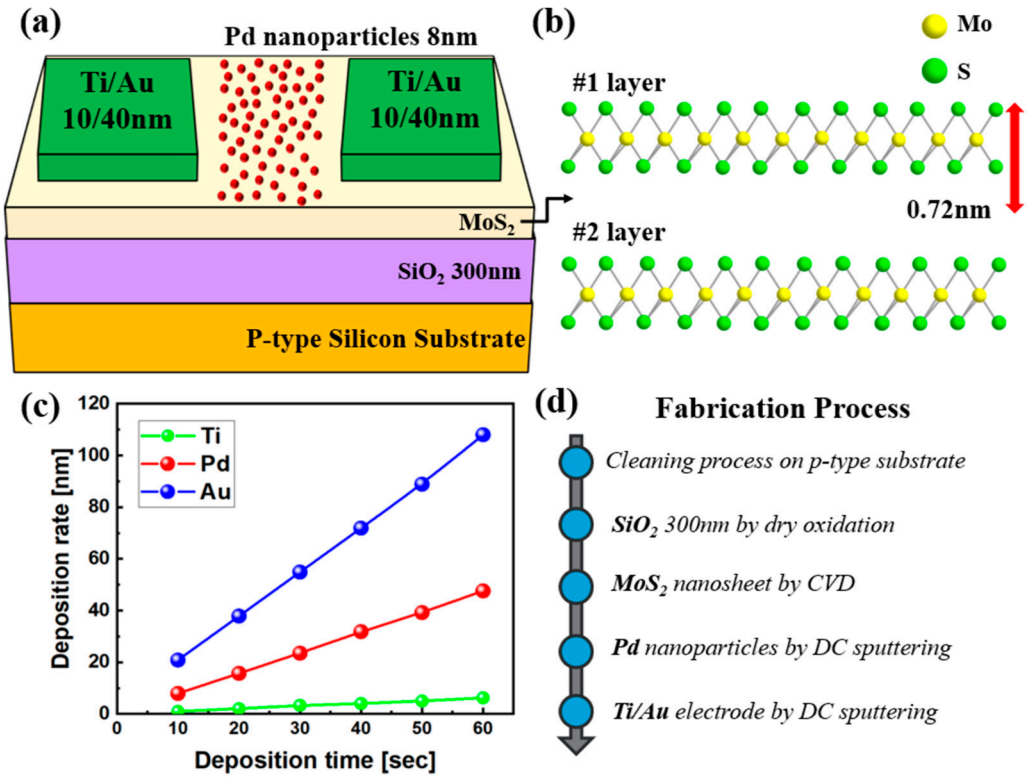

Figure 2. (**a**) The schematic of Pd-MoS_2 RRAM device; (**b**) The structure of monolayer or multilayer MoS_2 lattice layer; (**c**) Deposition rates of various metals (Ti, Pd, and Au) by DC sputter; (**d**) Fabrication process flow chart of the proposed RRAM architecture.

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3.2. Raman Spectroscopy

Raman data spectroscopy precisely analyzes the exact number of layers, structural properties, and energy of vibration modes, which provides important insights into nanomaterials [20]. In Raman data measurements, Figure 3a,b focus on the crucial peaks associated with two vibrational modes (E_{2g} and A_{1g}) of MoS_2. The E_{2g} peak of MoS_2 is significantly influenced by its crystalline structure, particle size, and thickness during growth. Additionally, the A_{1g} peak vibration is related to the crystalline structure and thickness of MoS_2, serving as an indicator of material quality. Figure 3c describes the Raman spectrum, an important indicator for understanding the physical properties and structure of monolayer & multilayer MoS_2 on SiO_2/Si substrate. For monolayer MoS_2, the E_{2g} and A_{1g} peaks were observed at 382 cm^{-1} and 402 cm^{-1}, respectively. In contrast, for multilayer MoS_2, these peaks were appeared at 380 cm^{-1} and 407 cm^{-1}, respectively. The E_{2g} peak (in-plane vibrational mode) involves parallel vibrations of Mo and S atoms within MoS_2. Also, the A_{1g} peak (out-of-plane vibrational mode) encompasses the vertical vibrations of S atoms [21]. The distance between the two peaks acts as an indicator that directly represents the number of layers of MoS_2. It has been confirmed that the distance between the peaks increases due to high-intensity vibrations as the number of layers increases.

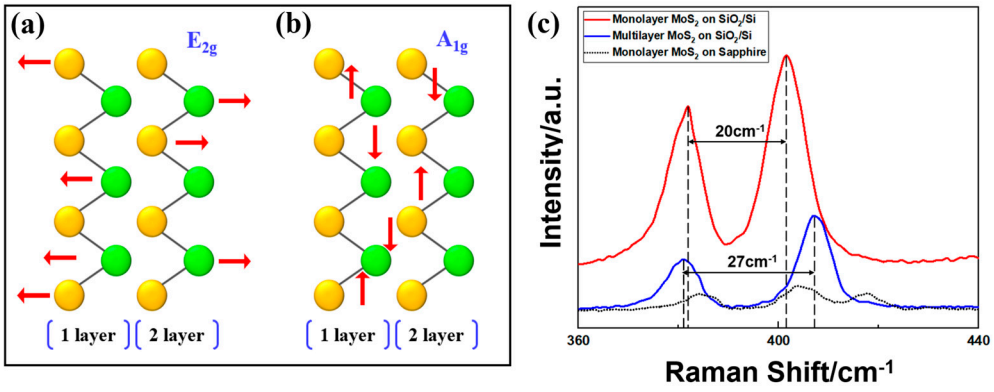

Figure 3. (**a**) E_{2g} band in-plane vibration of MoS_2; (**b**) A_{1g} band out-of-plane vibration of MoS_2; (**c**) Raman spectrum of monolayer MoS_2 and multilayer MoS_2 on the SiO_2/Si.

3.3. Photoluminescence Mapping

Photoluminescence (PL) spectroscopy is applied to determine the material's electronic states, structural characteristics, and bandgap based on the energy of emitted photons. In Figure 4a, PL signals were observed at room temperature using a 532nm laser. For monolayer MoS_2 samples, it can be observed that the PL intensity exhibits a lower peak compared to multilayer MoS_2. Through PL Mapping, MoS_2 synthesized by CVD techniques exhibits high-quality crystalline growth. Planck's constant (6.62×10^{-34} J·s), the speed of light (2.99×10^{8} m/s), and wavelength are denoted as h, c, and λ, respectively, and equation (1) is used to calculate the energy of emitted photons.

$$E = \frac{h \times c}{\lambda} = \frac{1240}{\lambda} \ (eV) \quad (1)$$

Figure 4a shows that the PL peak of monolayer MoS_2 appears at 660 nm, while that of multilayer MoS_2 is located at 995 nm. Applying the conversion relationship between wavelength and photon energy, Figure 4b reveals that the bandgap of monolayer MoS_2 is extracted as 1.87 eV, while that of multilayer MoS_2 is observed to be 1.24 eV. Consequently, this aligns with the bandgap range typically known through research [22]. The intensity of the PL peak represents the efficiency of the light emission process occurring in MoS_2 [23].

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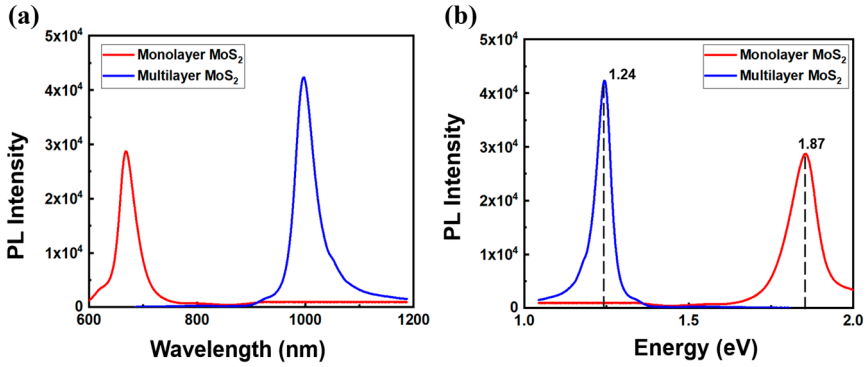

Figure 4. Scanning PL spectrum of monolayer MoS_2 and multilayer MoS_2; (**a**) wavelength; (**b**) Energy bandgap of the emitted photon.

4. Results and Discussions

The resistive switching (RS) model within RRAM devices has typically been applied by the application of two main theoretical mechanisms. Specifically, the electrochemical metallization (ECM) model is known for the formation of conductive bridges by metal ions within the channel, while the valence change mechanism (VCM) model regulates the conductive filaments (CFs) through the creation and recombination of oxygen vacancies induced by an electric field. Recently, new concept models have been proposed to control the current paths by generating ions or vacancies by various channel materials or nanomaterials applied to RRAM cells [24,25].

4.1. Resistive Switching Mechanisms

The RS mechanism for Pd coated multilayer MoS_2 RRAM device is illustrated in Figure 5. An electrical RS operation (electronic by TE & electronic by Pd) has been conceived to form the S vacancies (V_s) filaments in the current paths [26]. Figure 5a shows the initial high resistance state (HRS) with low concentrations of V_s distributed in the switching layer. When a forward voltage bias is applied to the TE, the switching layer collapses and negatively charged S ions are accumulated under the TE. By the SET process, the TiS_x layer is formed by reacting with Ti as shown in Figure 5b [27]. Additionally, S ions, which are far from TE, form V_s filaments due to an electrical field caught in Pd nanoparticles. When a conductive filament connects the TE and BE, the RRAM cells cause a low resistance state (LRS). The migration of S ions in the active channel layer occurs as follows. S ions that are far from TE are not subject to the electronic by TE effect. However, S ions are formed by the electric field effect of Pd nanoparticles [28]. When the TE and BE are connected by the CFs, the RRAM devices cause the LRS. When a negative voltage bias is applied to the TE, S ions migrate into the MoS_2 layer. As a result, the TiS_x layer decreases in size, and the CFs rupture, causing a transition to an HRS (RESET process).

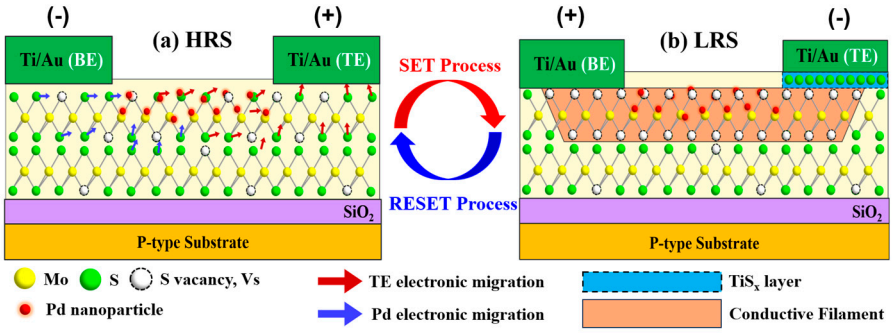

Figure 5. RS behavior of the Pd decorated multilayer MoS_2 RRAM device. (**a**) HRS (initial state); (**b**) LRS (after the SET process). The red and blue lines arrows show the S ion migration direction (electronic by TE & electronic by Pd).

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4.2. I-V Measurement

The fabricated Pd-MoS_2 nanocomposites RRAM were measured by a vacuum probe station and semiconductor parameter analyzer (HP4156A). Bias was applied to the TE with the BE grounded throughout the measurement process. Compliance current was set to a value of 20 μA to suppress overcurrent through the device. Figure 6a displays the measured current-voltage (I-V) characteristics of the RRAM device consisting of an ideal switching layer with multilayer MoS_2 (= 2 layers) and Pd nanoparticles (= 8 nm). Asymmetrical bipolar switching behavior was observed due to the Schottky barrier at the interface of multilayer MoS_2 and the electrode. The Schottky contact at the MoS_2/Ti interface prevented reverse current and allowed forward current to flow. In both the forward and reverse LRS, the rectifying current ratio (> 6 × 10) was assessed by comparing the forward current ($I_{forward}$) of 0.612 μA at a forward voltage of +2V with the reverse current ($I_{reverse}$) of 0.012 μA at a reverse voltage of -2V. Selector-integrated RRAM controlled leakage current and exhibited self-rectifying operation. The RRAM with Pd decorated MoS_2 channel structure demonstrated a bipolar switching with continuous and stable RS behavior (V_{SET} = +4.75 V, V_{RESET} = -4.1 V), as shown in Figure 6b. When extracting SET and RESET currents, I_{SET} and I_{RESET} were found to be less than 1 μA, indicating excellent memory performance, such as low-power operation, a high memory window on/off ratio (≈ 10^3), and nanoscale device fabrication. Furthermore, it appears that the issue of leakage current due to cross-talk in RRAM array cells has been addressed, and high-density memory array stacking is feasible. Table 1 summarizes the comparison of device stack structure, nanocomposites-based MoS_2, on/off ratio, and other parameters for MoS_2 switching layer RRAM.

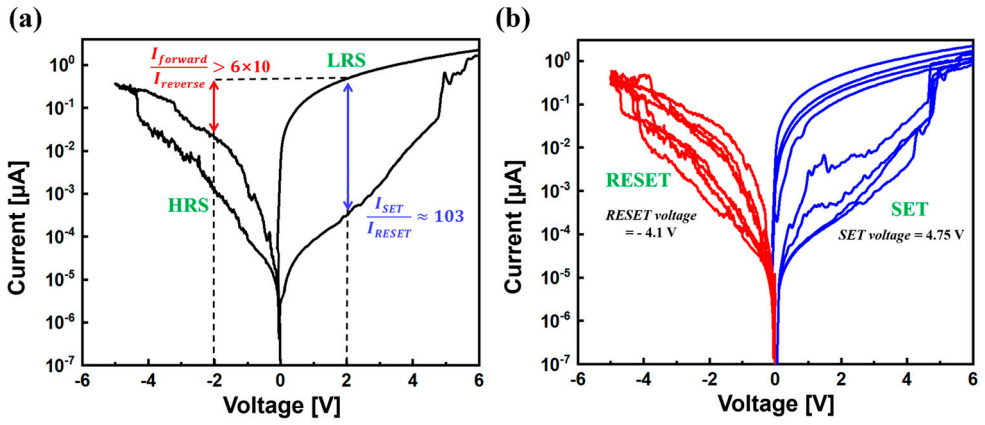

Figure 6. I-V characteristics of Pd-MoS_2 RRAM. (**a**) Self-rectifying RS operation. Rectifying current ratio was observed $I_{forward}$ (@ V = +2 V) and $I_{reverse}$ (@ V = -2 V). Memory window (≈ 10^3) was extracted; (**b**) I-V characteristics of Pd-MoS_2 RRAM for repeated voltage (-6V to 6V) sweeps.

Table 1. This is a table. Tables should be placed in the main text near to the first time they are cited.

TE & BE	Switching layer	On/Off ratio	Rectifying ratio	Ref
ITO & ITO	HfO_x/Pd-MoS_2	≈ 10^2	-	[3]
Au & Au	MoS_2	≈ 10^5	-	[17]
Au/Ti & Au/Ti	MoS_2	≈ 10^1	-	[26]
Ti & Pt	MoS_2	≈ 10^2	-	[27]
Ag & Ag	MoS_2/MoO_x	≈ 10^6	-	[29]
Au & TiN	HfO_x/MoS_2/TiO_x	≈ 10^6	-	[30]
Au/Ti & Au/Ti	Pd-MoS_2	≈ 10^3	> 6 × 10	This work.

5. Conclusions

This research work demonstrates a memristive RRAM based on Pd decorated multilayer MoS_2 nanocomposites solution. By optimizing Pd nanoparticles deposition (DC sputter) and MoS_2

nanosheets synthesis (CVD), we contributed to the electrical migration of V_s and TiS_x formation in the switching layer. MoS_2/Ti contact forms sufficient Schottky barriers to perform nonlinear I-V switching characteristics. Pd-MoS_2 RRAM, which consists of self-integration without a selector device, derives a high memory window ($\approx 10^3$) and the rectifying current ratio ($> 6 \times 10$) of asymmetric LRS. Nanocomposites-based RRAM should discuss leakage current by cross-talk in nanoscale cell fabrication and high-density 3D stack arrays. Finally, the application of a 2D nanomaterial memristor platform presents a direction for emerging memory devices and intelligent memristor fields.

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