Review

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Band Selective Notch Frequency Technology of EMI Noise Spectrum in DC-DC Switching Converters

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Posted Date: 21 March 2025

doi: 10.20944/preprints202503.1526.v1

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Review

Band Selective Notch Frequency Technology of EMI Noise Spectrum in DC-DC Switching Converters

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Abstract: This review presents the band selective frequency technology of Electromagnetic Interference (EMI) noise spectrum spread in the DC-DC switching converter for communication devices. This technology generates notch characteristic spectrum bands with a low noise level in the received frequency band spectrum. It detects the received frequency and generates a notch band there using a switching pulse control technology. First, we introduce the conventional spread spectrum technology. By modulating the clock frequency, EMI noise is dispersed to avoid concentrating at specific frequency bands. There are both analog modulation techniques and digital modulation methods. Next, we explain the main technology of this review, the notch band generation technology. This technique involves modulating the phase or pulse width of clock to produce notch band characteristics in the EMI noise spectrum. Then we present its simulation results, theoretical analysis, and implementation results. Finally, we demonstrate a technique that tunes the notch band frequency to the received signal one automatically.

Keywords: switching converter; Electro-Magnetic Interference (EMI); noise spectrum spread; clock pulse coding; frequency notch characteristics

1. Introduction

Nowadays, switching power supply circuits are widely used in many electronic devices, thanks to their advantages of high efficiency, continuously variable output voltage, small size and light weight. Also, the communication circuit has been enhanced for improved performance and high-density packaging. However, since the switching power supply circuit is driven by a high-frequency clock, it generates some amounts of switching noises called EMI noises, and their reduction is very important.

In this review paper, first we explain the fundamental DC-DC switching converters employing the Pulse Width Modulation (PWM) control. They cause EMI noises at the clock and harmonics frequencies, and for their reduction, the clock modulation is often utilized by shaking its phase or frequency. This technology spreads the noise power to other frequencies, though it makes the bottom level rise-up.

Next, we review our band-selective EMI spread spectrum technique, which realizes both reduction of the spectrum line noise and generation of the low noise spectrum band like the notch filter at the receive frequency of communication devices.

2. Fundamental DC-DC Switching Converters [1–8]

There are three fundamental DC-DC switching converters: buck, boost and buck-boost types. They are composed of power and control stages, and their configurations are almost the same among three types. The power stage has a switch, an inductor, a diode, and an output capacitor. However,

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its construction differs among them; the differences are distinguished by their positions. The control stage of each converter is quite similar, consisting of a comparator, a D-type Flip-Flop (DFF), and a reference voltage. Their voltage conversion ratio (Vo/Vi) and polarity of Vo vary , where Vi represents the input voltage and Vo does the output voltage: $0 < Vo < Vi$ for the buck converter, $0 < Vi < Vo$ for the boost converter, and $0 < -Vo \gtrless Vi$ for the buck-boost converter.

2.1. Buck Converter with PWM Control

Figure 1 shows the configuration of the buck converter. The red/blue broken line represents the current flow when the PWM pulse is high/low, respectively. The power stage is composed of a switch (SW), an inductor (L), a diode (Di), and an output capacitor (Co). The control stage is composed of an amplifier (AMP), a comparator (CMP), a D-type Flip-Flop (DFF), and a sawtooth generator.

In the power stage, SW is regulated by the PWM signal. In case the PWM signal is high, SW turns ON, and the input current from the power supply flows through SW to L (as shown by the red broken line in Figure 1). During this period, the input current increases, flowing into Co and R_L, resulting in an increase in Vo (Figure 2) and raising the magnetic energy in L. Conversely, when the PWM level is low, SW turns OFF, and the energy stored in L causes the current to flow through Di (as indicated by the blue dotted line in Figure 2). Then, Vo decreases and the duty ratio (D) of the PWM signal increases.

In the control stage, the AMP amplifies the voltage error of Vo and the reference voltage (Vref). This amplified error voltage is then compared with the sawtooth signal (SAW) and the PWM signal is generated. The DFF receives this data synchronously with the internal clock (CK) to provide the SAW pulse so that the SAW signal is generated by the sawtooth generator. Vo varies based on D, and Vo is related to D as shown by:

$$Vo = D \cdot Vi \quad (1)$$

Vo is less than Vi due to $0 < D < 1$.

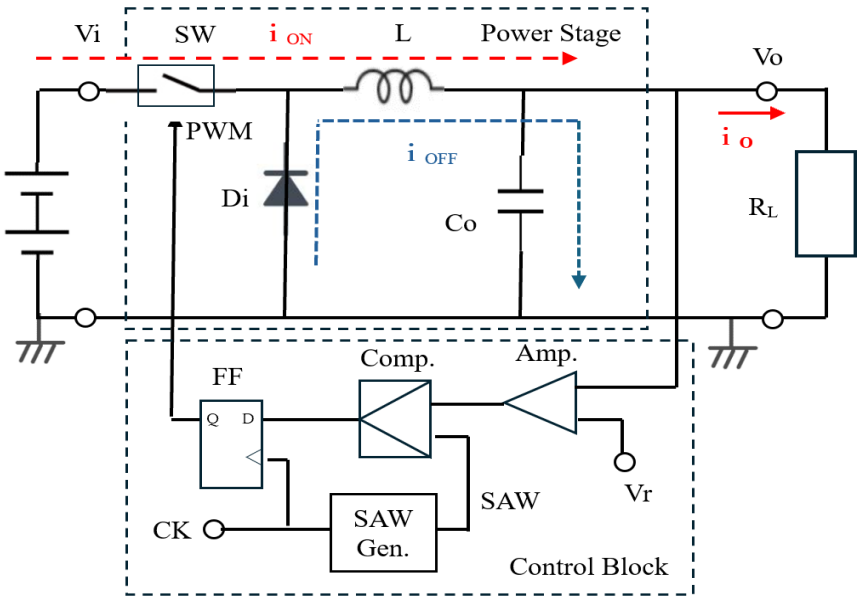

Figure 1. Configuration of the buck converter.

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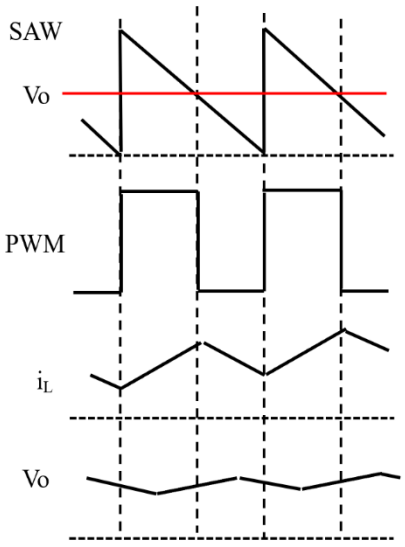

Figure 2. Waveforms of the buck converter.

2.2. Boost Converter

Figure 3 shows the configuration of the boost converter. When SW is ON, the input current flows through L, and it does not flow to Co or R_L (Figure 3), and then L charges the magnetic energy. When SW is OFF, the current to flow from L to Co and R_L through Di. As a result, the current into Co is intermittently interrupted, leading to some output voltage ripple. Vo is expressed by

$$Vo = 1/(1 - D) \cdot Vi \quad (2)$$

Notice $1 < 1/(1\text{-}D)$ and $Vo > Vi$.

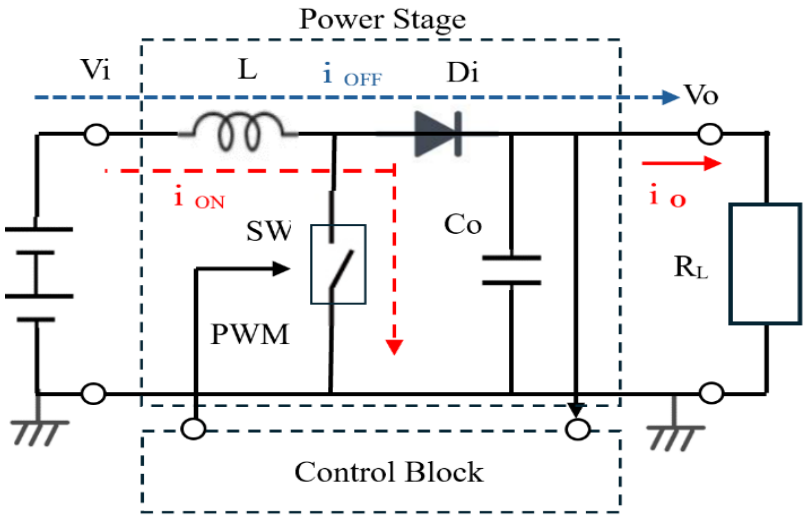

Figure 3. Configuration of the boost converter.

2.3. Buck-Boost Converter

The buck-boost converter produces a negative voltage output. Figure 4 illustrates its configuration, and it operates as follows:

・In case SW is ON, the input current flows through SW and L.

・In case SW is OFF, the inductor current flows into Co in a inverse direction, as shown by the blue dotted line in Figure 4. As a result, the polarity of Vo becomes negative. Vo can be expressed by Eq. (3), and the absolute value of Vo varies widely over or less than Vi.

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$$Vo = -D/(1-D) \cdot Vi \quad (3)$$

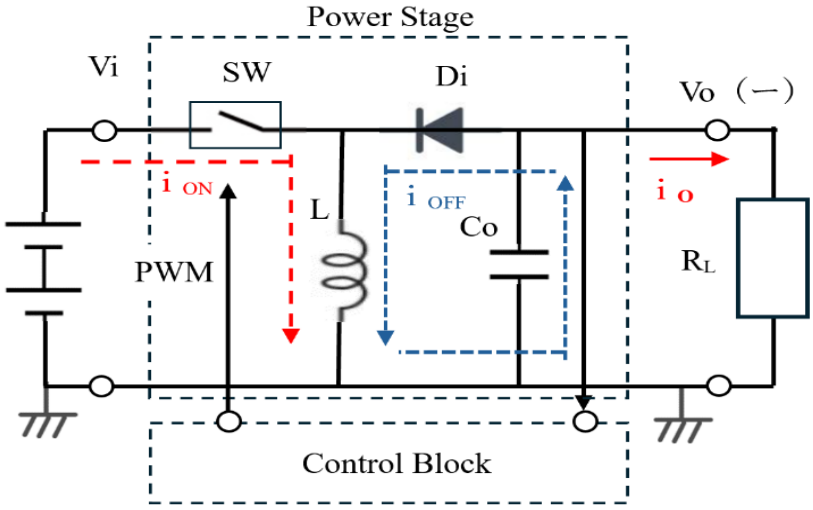

Figure 4. Configuration of the buck-boost converter.

3. Conventional Method of EMI Reduction with Suppressing Diffusion [9–24]

This section reviews some spread spectrum technology for EMI reduction with diffusion suppression of power supply and switching noises. Basic spread spectrum technologies for clock noise involve modification of the clock with frequency, phase and pulse width. The following will illustrate the one with the coding of the clock using both analog and digital methods.

3.1. Frequency Modulation with Analog Spread Spectrum Clock Generator

(A) Configuration and operation

It is recognized that the clock frequency or phase modulation in switching converters spreads the power spectrum of the EMI noise from the PWM signal and decreases its peak level at the clock and harmonics frequencies. Figure 5 shows the conventional clock frequency modulator and Figure 6 shows its associated signals. There, the voltage-controlled oscillator (VCO) is incorporated for the modulation of the frequency or phase of the SAW signal (Figure 6).

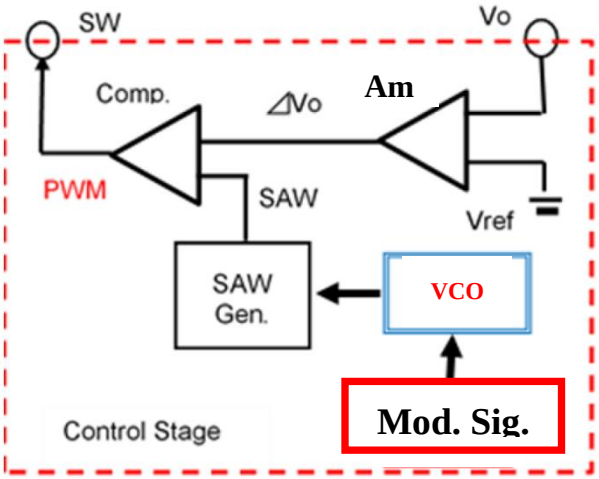

Figure 5. Frequency modulator in control stage.

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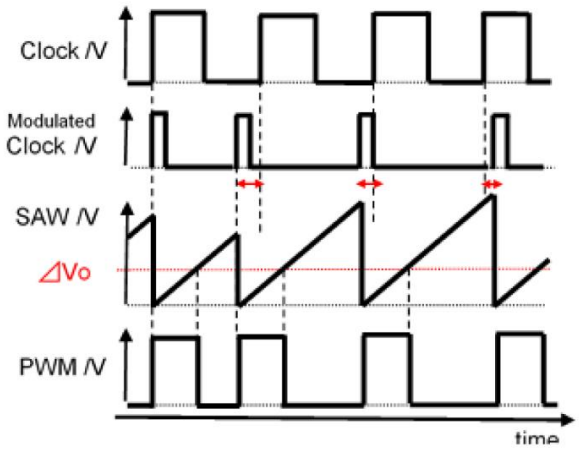
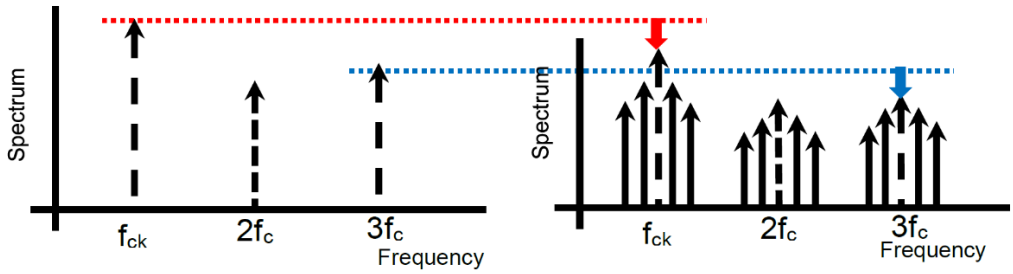


Figure 6. Signals for frequency modulation.

Figure 7a illustrates the spectrum of the PWM signal without clock modulation, whereas Figure 7b illustrates the one with modulation by two frequencies. The clock noise power spectrum is spread around the clock and harmonics frequencies. Several line spectra, indicated by the solid arrows, are discretely spread (marked by the dashed arrows); there the peak power levels are reduced.



(**a**) Spectrum without modulation (**b**) Spectrum with modulation.

Figure 7. Spread spectrum of PWM pulse [24] @JTSS.

(B) Simulation results

Figure 8 illustrates the spectrum of the PWM pulse without clock modulation. At the clock frequency of 0.5 MHz, a line spectrum reaching 3.5 V is observed, along with many harmonics. For the clock noise reduction, its modulation is utilized by shaking its phase or frequency (Figure 5). Figure 9 displays the spectrum with modulation. Since the power at the clock and harmonics frequencies spread to other bands, their peak levels become lower, though the bottom level becomes higher.

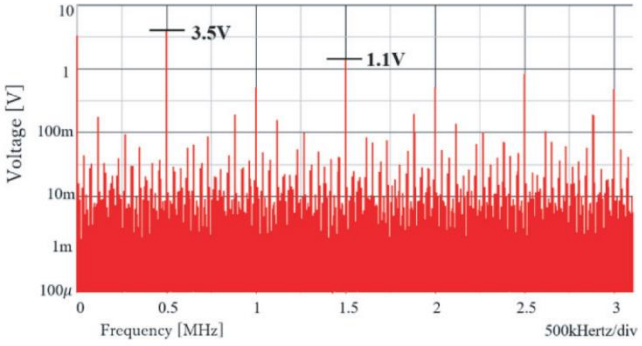


Figure 8. PWM spectrum without clock modulation.

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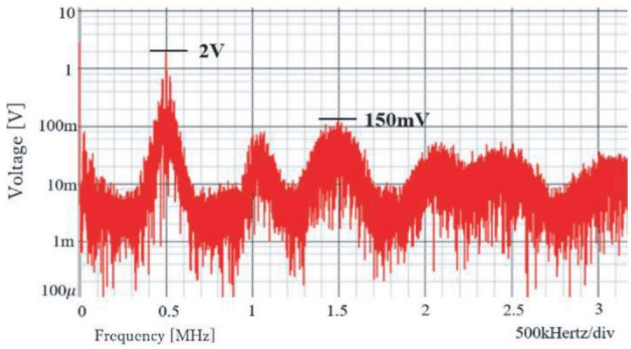


Figure 9. PWM spectrum with modulation.

3.2. Basic Digital Frequency Modulation with LFSR

(A) Configuration and generated pseudo analog signal

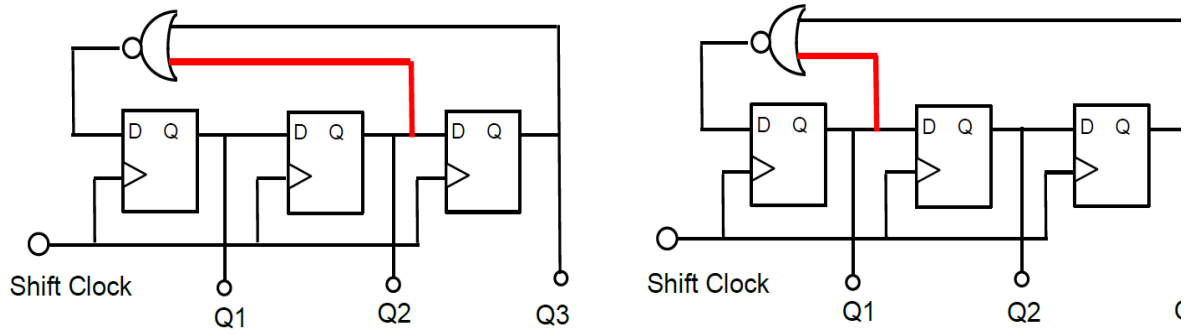
Pseudo-analog noise generation using a Phase Locked Loop (PLL) clock generator for modulation is reviewed.

Figure 10 illustrates the 3-bit Linear Feedback Shift Registers (LFSRs) or M-sequence circuits. Based on G3_1(x) in Eq. (4), the outputs of the 3rd and 2nd bits are connected to the inputs of the Exclusive NOR (EX-NOR) gate, and its output is provided to the first DFF. The n-bit LFSR generates K (=2^n -1) levels, where n is the order of the primitive polynomial. For n=3, K is 7 and there are two primitive polynomials G3_1(x) in Eq. (4) and G3_2(x) in Eq. (5).

Figure 11 illustrates the analog output levels obtained from (Q3, Q2, Q1) by the LFSR in Figure 10. There are periodic patterns with 7 levels: 0-1-3-6-5-2-4 or 0-1-2-5-3-6-4. These are transformed into a smooth signal as pseudo-analog noise. This pseudo analog noise is introduced into the PLL, and then, its output is frequency-modulated (Figure 12). Also, the PLL does not lock to the input noise due to its sluggish step response characteristics (Figure 13).

$G3\_1(x) = x^3 + x^2 + 1$ (4)

$G3\_2(x) = x^3 + x + 1$ (5)



(**a**) Based on G3_1(x). (**b**) Based on G3_2(x).

Figure 10. 3-bit LFSRs for two primitive polynomials [24] @JTSS.

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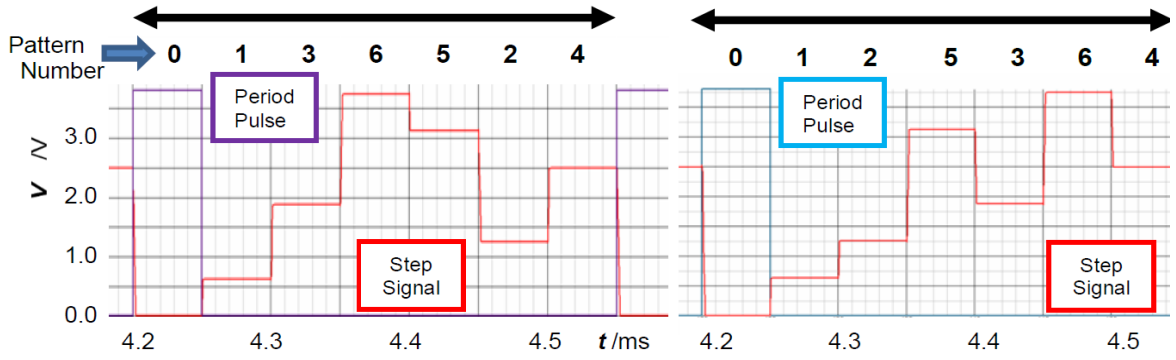

(**a**) Based on G3_1(x). (**b**) Based on G3_2(x).

Figure 11. Waveforms of output levels with LFSRs [24] @JTSS.

(B) Simulation of clock modulation with pseudo analog noise

The clock generator with modulation by the pseudo analog noise is illustrated in Figure 12. The generated pulse train by the LFSR in Figure 10 is converted to the analog signal by the DAC and smoothed by the LPF, and it is supplied to the PLL. Figure 13 shows its simulated characteristics of the damped vibrated signal when the input signal is changed with some steps.

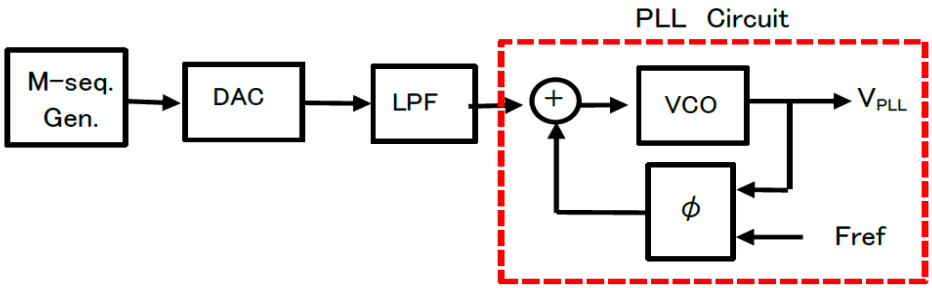

Figure 12. Configuration of the clock generator with analog modulation [24] @JTSS.

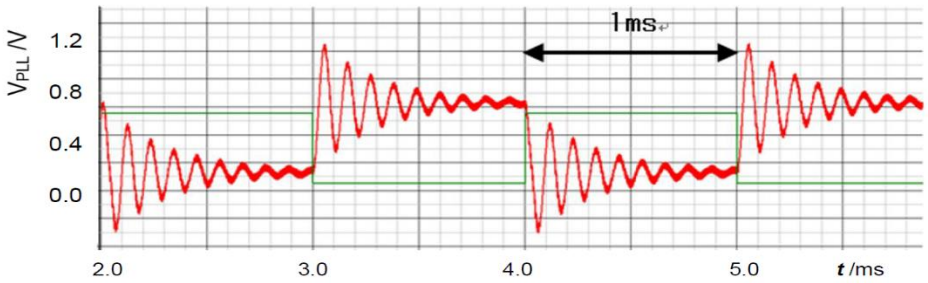

Figure 13. Step response of the PLL [24] @JTSS.

Figure 14 displays the pseudo analog noise (Vn: periodic), the VCO input signal (Vcont: non-periodic) and the output voltage ripple (⊿Vo: non-periodic) when an LFSR based on G3_1(x) is used. The clock frequency is 400 kHz, while the shift clock of the LFSR in Figure 10 is 10 kHz. Then the periodic frequency of Vn is 1.43 kHz, and ⊿Vo is about 10mVpp. Table 1 shows the simulation parameters, and SIMPLIS is used as simulator.

Figure 15 displays the simulated spectra of the PWM signal (red) and the conducted noise (green). Figure 15a displays the spectra without the pseudo-analog noise (Np), whereas Figure 15b includes the ones with Np. The peak level at the clock frequency is reduced from 3.0V to 0.55V, and that at the 3rd harmonic is from 1.0V to 0.1V, while that of the conductive noise is from 350mV to 70mV.

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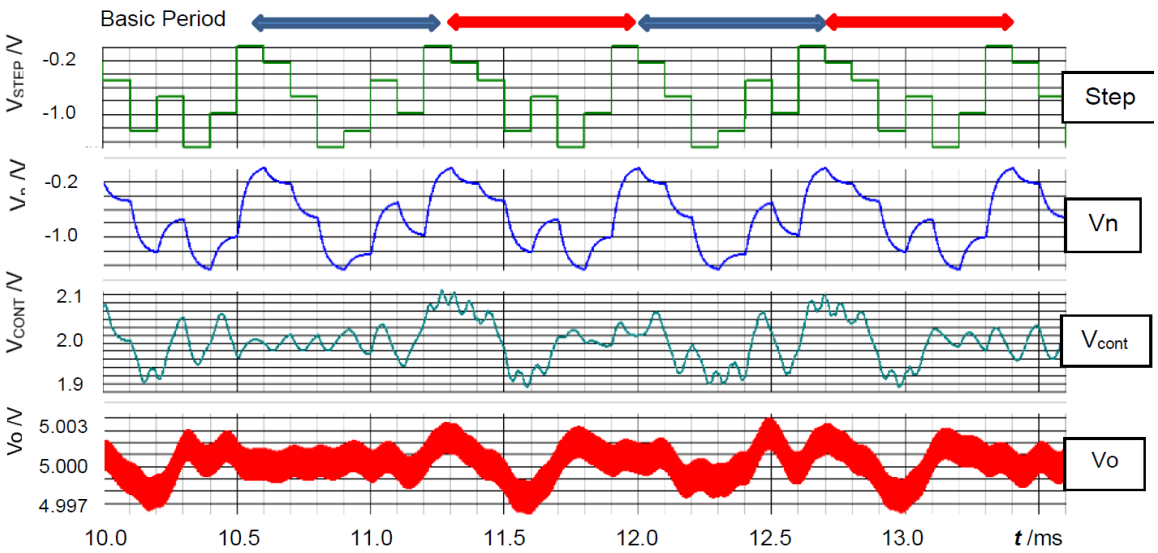
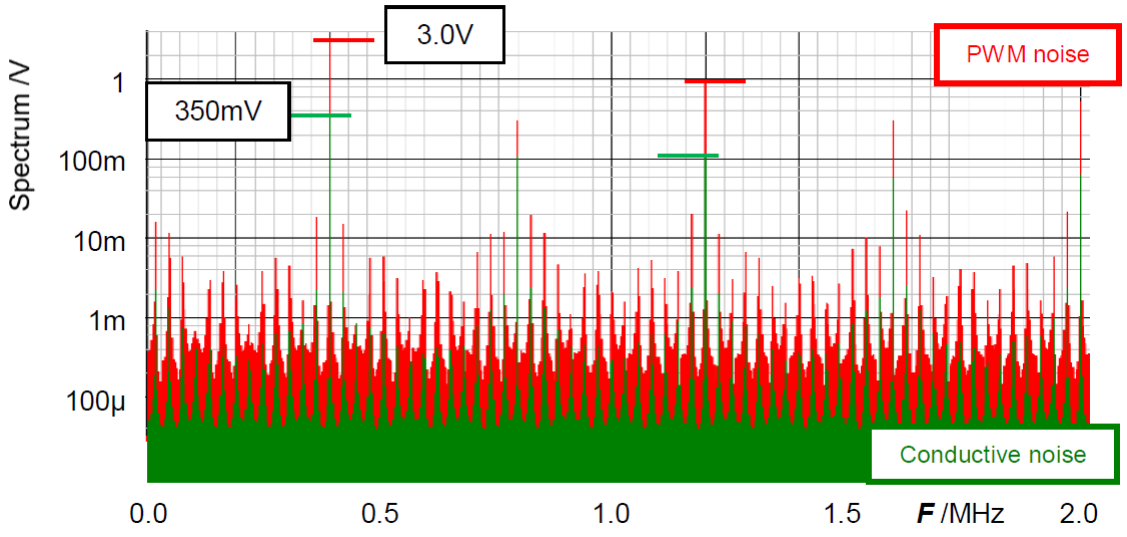
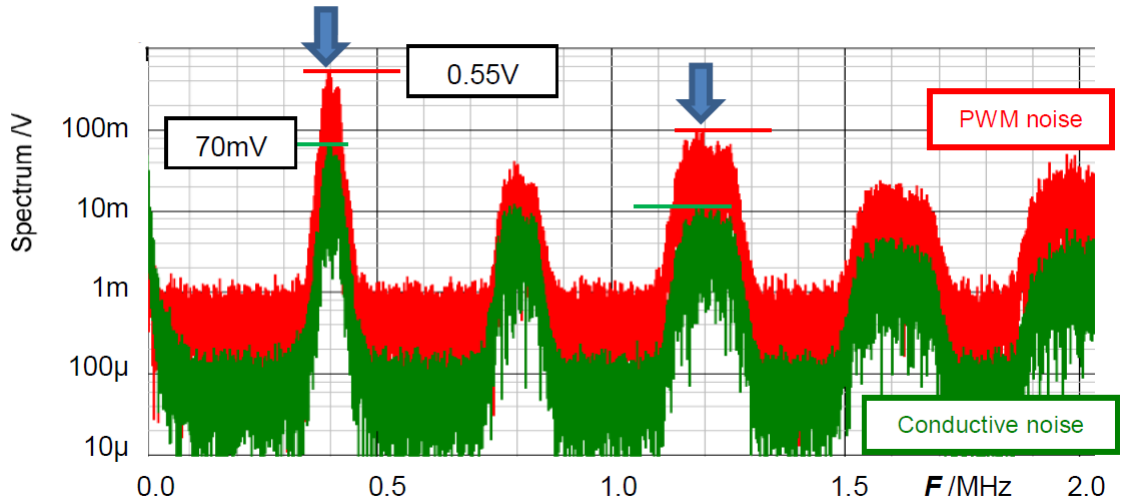


Figure 14. Signals associated with PLL circuit [24] @JTSS.



(**a**) Spectrum without analog noise.



(**b**) Spectrum with analog noise.

Figure 15. Spectrum of PWM and conductive noises [24] @JTSS.

Table 1. Simulation parameters.

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Parameter	Value
Vin	10.0 [V]
Vo	5.0 [V]
Io	0.5 [A]
L	5.0 [μH]
Co	470 [μF]
Fck	400 [kHz]

3.3. Analog Noise Generators using Bit Operation

(A) Expansion of analog pattern length using bit-inverse

We explain an analog noise generator using bit-exchange for an LFSR. The longer the period of the analog noise, the lower the peak level at the specific frequency, resulting in a broader sideband spectrum. The 3-bit system produces 8 analog levels, and the number of permutations of the pattern levels is ${}_7P_7$ = 5,040. Thus, a larger number of the bits increases the number of permutations. For instance, inversing some of the bits from the LFSR output produces other pattern levels.

Additional patterns from the combination of these pattern levels are included. Eqs. (6)- (13) illustrate the results of the bit-inversed level streams of Eqs. (4) (5). Usage of these streams extends the analog noise period to 8 times that of the original. The pattern length using the bit-inverse results in T1 =8・2・7=16・To, where To is the original pattern length of 7.

【Based on G3_1(x)】 : 【Based on G3_2(x)】

1) Q1Q2Q3： 0-1-3-6-5-2-4- ： 0-1-2-5-3-6-4- (6)

2) Q1Q2Q3： 1-0-2-7-4-3-5- ： 1-0-3-4-2-7-3- (7)

3) Q1Q2Q3： 2-3-1-4-7-0-6- ： 2-3-0-7-1-4-6- (8)

4) Q1Q2Q3： 3-2-0-5-6-1-7- ： 3-2-1-6-0-5-7- (9)

5) Q1Q2Q3： 4-5-7-2-1-6-0- ： 4-5-6-1-7-2-0- (10)

6) Q1Q2Q3： 5-4-6-3-0-7-1- ： 5-4-7-0-6-3-1- (11)

7) Q1Q2Q3： 6-7-5-0-3-4-2- ： 6-7-4-3-5-0-2- (12)

8) Q1Q2Q3： 7-6-4-1-2-5-3- ： 7-6-5-2-4-1-3- (13)

(B) Simulation results of pattern generator with bit-inverse

Figure 16 illustrates the simulation circuit of the LFSR (M-sequence circuit) with bit-inverse based on G3_1(x). The bit-inverse uses three EX-NOR gates, in conjunction with a 3-bit binary counter, that is triggered once within a period of the LFSR counter. In Figure 16, the binary counter increments when all bits of the LFSR counter are zero, and CK is triggered when all the outputs of the binary counter are zero. The periodic length of the 3-bit DAC input (B3, B2, B1) extends to 8 times of To (Figures 16 and 17).

Figure 18 displays the output voltage ripple (⊿Vo) of the converter using pseudo analog noise, while Figure 19 illustrates the spectrum of the PWM signal and the conductive noise using bit-inverse. The ripple voltage is 8.5 mVpp. The peak level at the clock frequency is reduced from 550 mV to 500 mV, and the level of the conductive noise is from 70 mV to 60 mV, compared to Figure 15b.

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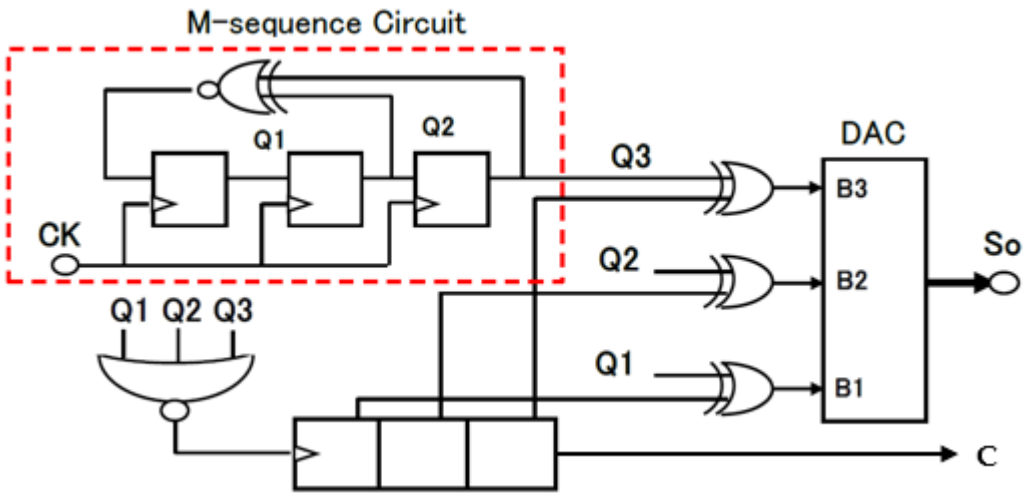

Figure 16. Pattern generator using bit-inverse [24] @JTSS.

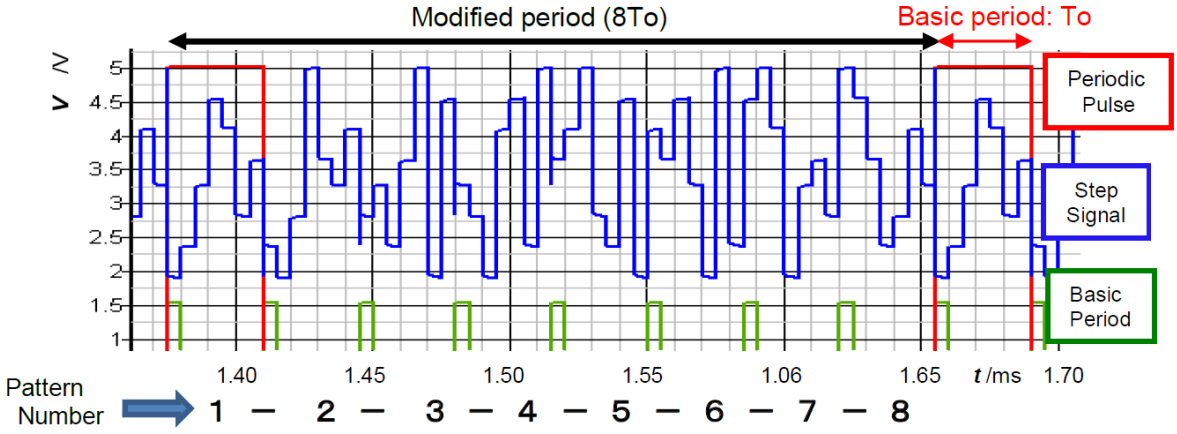

Figure 17. Expanded pattern length using bit-inverse [24] @JTSS.

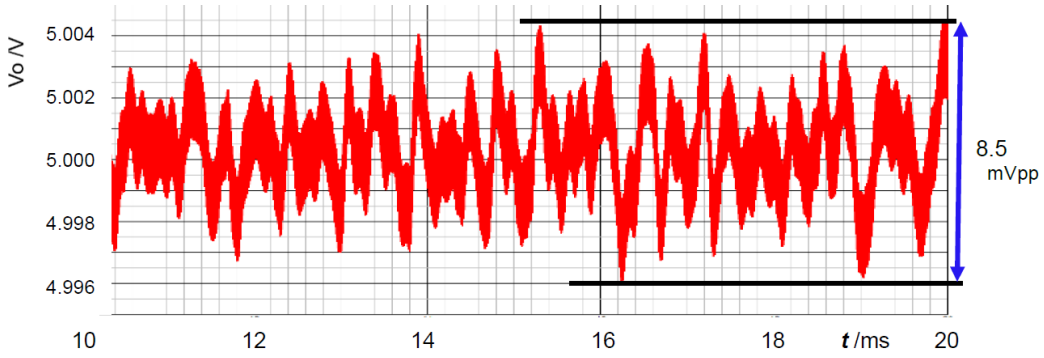

Figure 18. Output ripple of the buck converter using bit-inverse [24] @JTSS.

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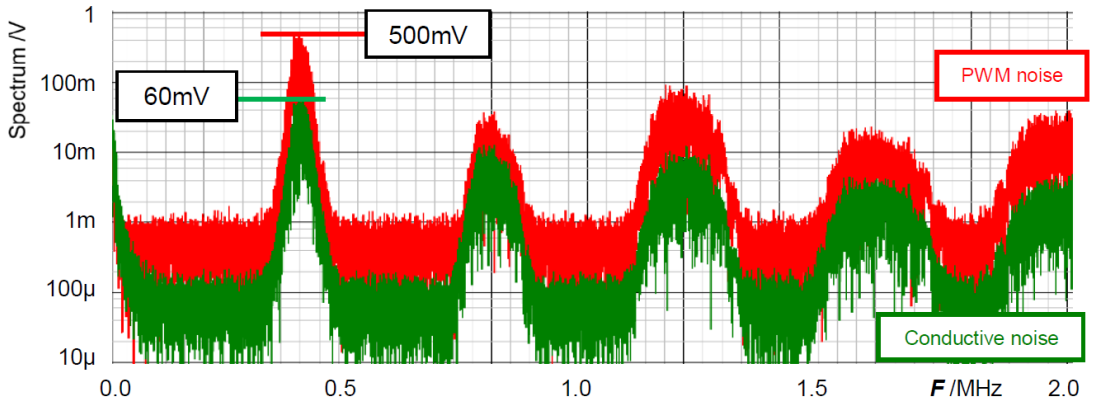

Figure 19. Spectrum of the buck converter output using bit-inverse [24] @JTSS.

3.4. Pattern Generator Using Bit-Inverse and Bit-Exchange and Simulation Results

(A) Expansion of analog pattern length using bit-inverse and bit-exchange

The bit-exchange technique for expansion of the analog noise period is introduced. There are no identical bit streams compared to Eqs. (6)-(13). The new pattern length becomes 6 times the one with only bit-inverse (T2 = 6・T1 =96・To).

【Based on G3_1(x)】 : 【Based on G3_2(x)】

1) Q1Q2Q3 : 0-1-3-6-5-2-4- : 0-1-2-5-3-6-4- [basic] (6)

2) Q1Q3Q2 : 0-1-5-6-3-4-2- : 0-1-3-5-2-4-6- (14)

3) Q2Q1Q3 : 0-2-3-5-6-1-4- : 0-6-2-3-5-1-4- (15)

4) Q2Q3Q1 : 0-4-5-3-6-1-2- : 0-4-3-2-5-1-6- (16)

5) Q3Q1Q2 : 0-2-6-5-3-4-1- : 0-6-5-3-2-4-1- (17)

6) Q3Q2Q1 : 0-4-6-3-5-2-1- : 0-4-5-2-3-6-1- (18)

(B) Simulation results of pattern generator using bit-inverse and bit-exchange

Figure 20 illustrates the configuration of the LFSR using bit-inverse and bit-exchange. The bit-inverse circuit is shown in Figure 16 and the bit-exchange circuit is composed of a multiplexer array. At the 3-bit DAC output, the number of the analog steps is 48 times of the original pattern one and Figure 21 illustrates its output of the expanded bit-pattern. Figure 22 illustrates its simulated spectra. The peak level of the PWM pulse noise is reduced from 500 mV to 400 mV (-17.5 dB), while the conductive noise remains 60 mV, compared to Figure 19.

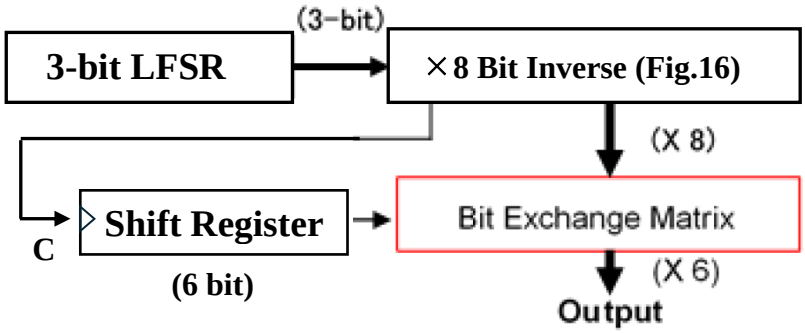

Figure 20. Pattern generator using bit-inverse and bit-exchange [24] @JTSS.

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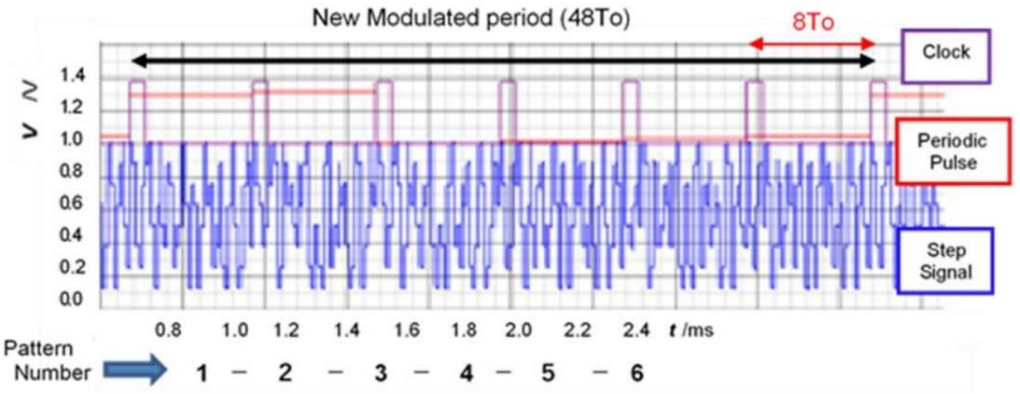

Figure 21. Expanded pattern length with bit-inverse and bit-exchange [24] @JTSS.

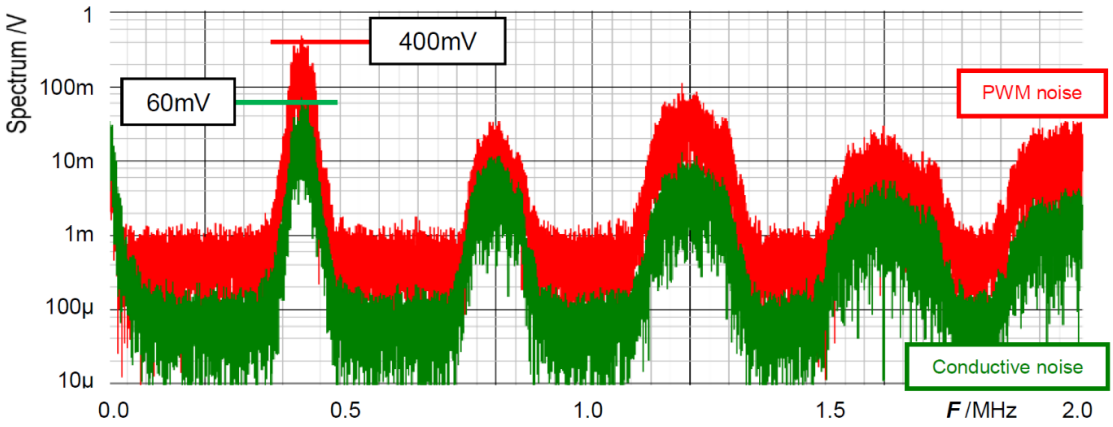

Figure 22. Spectrum with bit-inverse and bit-exchange [24] @JTSS.

3.5. Expansion of Number of Pseudo Analog Noise Generator Bits

(A) Expansion of number of bits

We found that it is not the number of bits for the LFSR that reduces EMI noise, but rather the ratio of the variation in pattern levels of the LFSR. There are two 4th-order primitive polynomials and the bit level series are given in Eqs. (27), (28), while the number of the pattern variations is To=2 ^{4} −1=15.

[4th-order] $G4\_1(y)=y^4+y^3+$ (19)

$G4\_2(y)=y^4+y+1$ (20)

[Pattern] G4_1：0-1-3-7-14-13-11-6-12-9-2-5-10-4-8- (21)

G4_2：0-1-2-5-10-4-9-3-6-13-11-7-14-12-8- (22)

(B) Simulation results with 4th-order primitive polynomials

Figure 23 illustrates the output step pattern from the 4-bit LFSR and the output of the LPF following the 4-bit DAC with the bit-inversed versions of Eqs. (19) and (20). The step pattern consists of non-periodic pulses, because the condition of the initial bit patterns in the LFSR varies based on the previous ones. Figure 24 illustrates the spectrum of the PWM pulse. The peak level is 600 mV, which matches the one with 3rd-order primitive polynomials.

There is little difference in EMI reduction of the 3-bit and 4-bit LFSRs with bit-inverse operation. Therefore, only the 3-bit LFSR is sufficient, and we see that fine frequency changes in modulation are not necessary.

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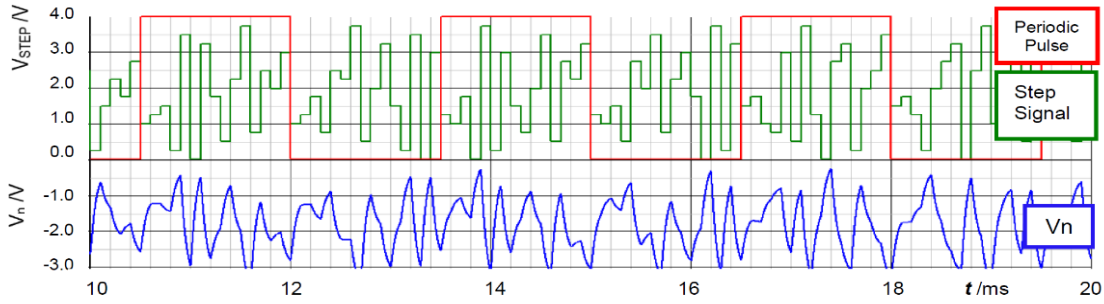

Figure 23. Signals of 4-bit LFSR with bit-inverse [24] @JTSS.

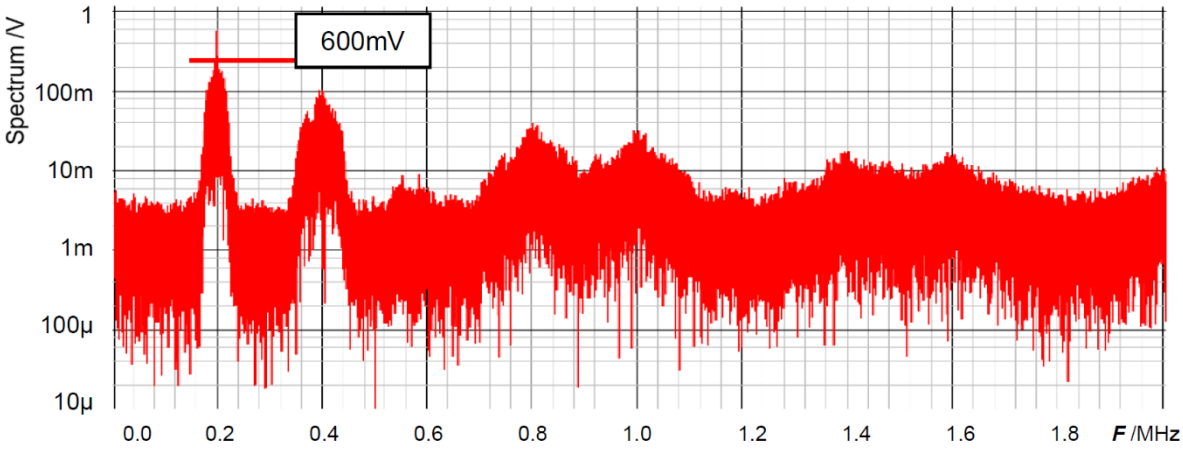

Figure 24. Spectrum of PWM pulse using 4-bit LFSR with bit-inverse [24] @JTSS.

4. Notch Band Select with Pulse Coding Control [25–28]

This section reviews our EMI noise spread spectrum techniques with notch band select using pulse coding methods: Pulse Width Coding (PWC), Pulse Cycle Coding (PCC), Pulse Width and Phase Coding (PWPC). The notches appear at frequencies determined by empirical equations. We demonstrate the relationships of the notch frequencies and the coded pulses in simulation. Also, their analytical formulae are shown.

4.1. Pulse Width Coding (PWC) Control

(A) Basic pulse coding control

In the pulse coding control method, the switch is regulated by the Pulse Coded Drive (PCD) signal, that is selected from two coded PWM pulses (Figure 25). Pulse 1 and Pulse 2 are generated using various coding methods with parameters of pulse width, phase and their composite, and then, one is selected by SEL.

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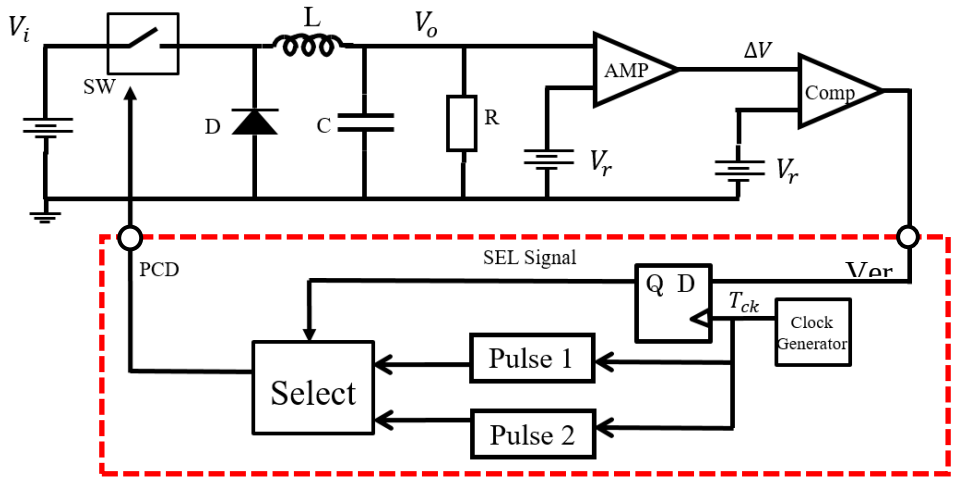

Figure 25. Switching converter with basic pulse coding control [25] @IEEE.

(B) Pulse Width Coding (PWC) control

The PWC method discretely modulates the feedback pulse width. Figure 26 illustrates the PWC control circuit, and there SEL is generated from the error voltage (Verr). Figure 27 illustrates SEL, V_H, V_L, and PWC pulse (W_H, W_L). When SEL is high, the multiplexer selects V_H, and the comparison with SAW generates W_H. When SEL is low, it selects V_L, and the comparison with SAW generates W_L. The output voltage is stably controlled by satisfying the following:

$$D_L < D_o (= V_o / V_i) < D_H \quad (23)$$

Here, $D_L = W_L / T_{ck}$ and $D_H = W_H / T_{ck}$ in Figure 27.

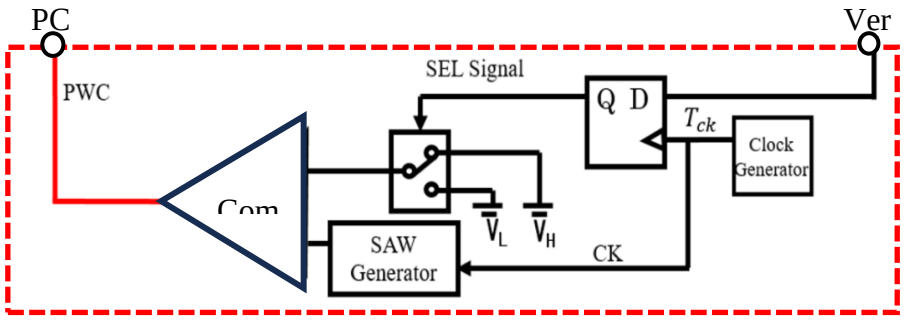

Figure 26. PWC control circuit.

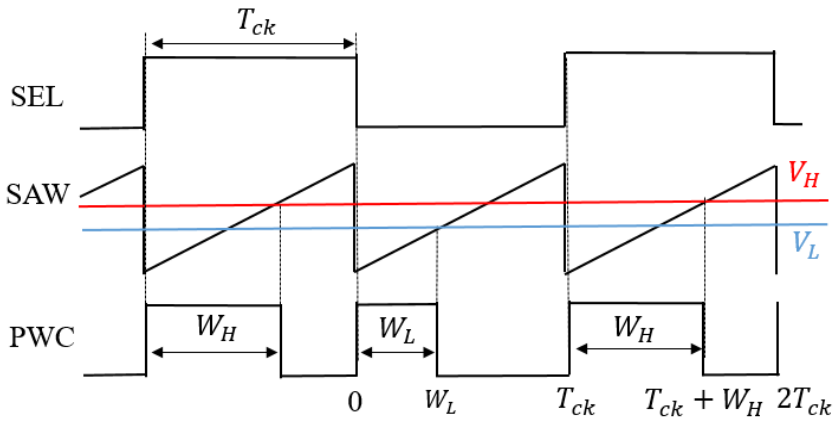

Figure 27. Signal waveforms for PWC control.

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In the PWC control, the analog output voltage error is converted to a digital signal and it modulates pulses. The converter output voltage is stabilized by appropriately switching these pulses. As a result, the noise spectrum is spread, and its notch is generated. Simulation shows the notch frequency (F_n) is given as follows:

$F_n = N / (W_H - W_L)$ (24)

Hereafter, N is a positive integer throughout this paper. We observe that F_n is determined by the difference of W_H and W_L and it is independent of the clock frequency. By adjusting W_H and W_L, F_n can be set arbitrarily.

(C) Simulation Results of PWC Control

The pulse coded control regulates the converter output voltage using only two pulses, but without a saw-tooth signal. The clock frequency is set to exceed 500 kHz to ensure precise control of the output voltage, and other parameters are in Table 2.

Table 2. Parameters of PWC control simulation.

V_i	V_o	I_o	L
12V	5V	0.52A	200μH
C	T_{ck}	W_H	W_L
470μF	2.0μs	1.6μs	0.3μs

The SAW peak voltage is set to 12V, V_H to 9.6V and V_L to 1.8V. Comparisons of V_H and V_L with the SAW under T_{ck} = 2μs results in W_H of 1.6μs and W_L of 0.3μs respectively. Figure 28 illustrates SEL and PWM signals, while Figure 29 displays the PWC signal the spectrum. The up-arrows indicate the clock, its double, and its triple frequencies. A notch is observed at F_n(= 770 kHz), corresponding to the theoretical frequency from Eq. (24). Another notch is generated at 1.54 MHz, which corresponds to $2F_n$. However, this notch is not very prominent due to the high-frequency noises from the clock. Comparing the peak level at the clock frequency in Figure 8 with that in Figure 29, it is suppressed from 3.5 V to 1.1 V. Also, notches are produced.

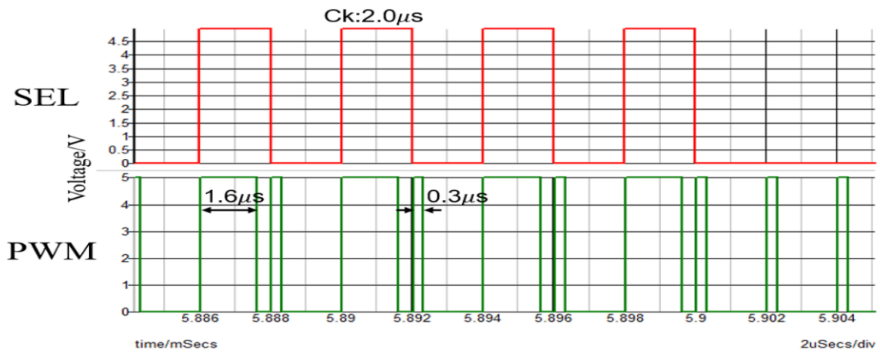

Figure 28. Signals of PWC control.

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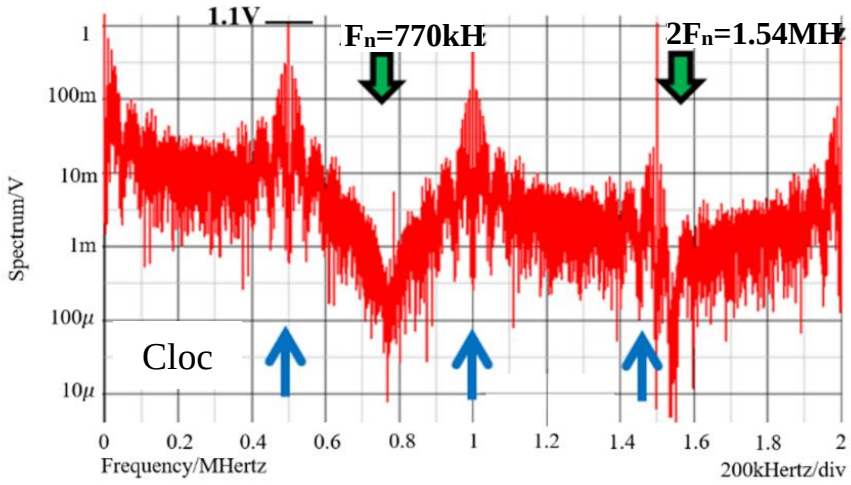

Figure 29. Spread spectrum of PCD signal with PWC control.

4.2. Pulse Phase Coding (PPC) Control

Pulse Phase Coding (PPC) control is realized with a delay circuit and a multiplexer (Figure 30). However, it does not alter D, and then it is used with the PWC system. Parameters are used for the notch frequency based on the empirical formula (Eq. (24)). Let τ represent the delay of pulse coding, with the longer delay τ_H and the shorter one τ_L (Figure 31). The notch characteristics are also obtained using the PCC method. In case of a pulse train with a clock cycle of T_o, the period $T(k)$ of the k -th pulse is given by:

$$T(k) = T_o + \{\tau(k) - \tau(k-1)\} \quad (25)$$

We see that in the PPC method, the notch is dependent on also the previous pulse. Therefore, notches are unlikely produced because the coding cycle T(k) has 2^2 patterns. To address this, the following two periodic patterns can be utilized if alternate high/low coding is applied to the phase coding:

$$T_H = T + \{\tau_H - \tau_L\}, \quad T_L = T - \{\tau_H - \tau_L\} \quad (26)$$

We obtain Eq. (27) from Eqs. (24), (26) as follows:

$$F_{np} = N /[2 (\tau_H - \tau_L)] \quad (27)$$

We see from Eq. (27) that the notch characteristics are determined by twice the difference in the pulse phases.

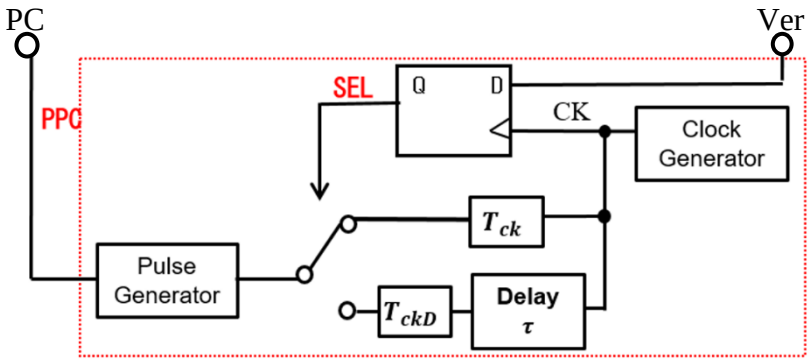

Figure 30. PPC control circuit.

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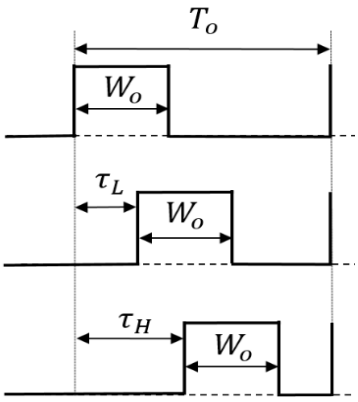

Figure 31. Signals of PPC control.

4.3. Pulse Cycle Coding (PCC) Control

(A) PCC control circuit

In Figure 32, the duties of the two coded pulses differ as described by Eq. (26). Consequently, the duty cycle changes by altering the pulse period (Figure 33). Figure 34 shows an example of two pulses using the PCC method. There W_o =0.4μs, T_s=0.5μs and T_L=2.0μs. Consequently, D_H=0.8 and D_L=0.2. The notch frequency F_{nc} in the spectrum of the PCD signal is given by

$$F_{nc} = N / (T_L - T_S) \quad (28)$$

Figure 32 shows the generator of these coded pulses. Pulses with different periods are generated from the pulse generation counter based on SEL (Figure 33). Here, T_L and T_s are defined as the pulse periods which are produced based on the SEL high and low states. By utilizing a differential circuit, a periodically modulated clock signal is generated. The generated saw-tooth is compared with V_r and the PCC pulse is produced. Figure 34 shows signal waveforms associated with the pulse coding in the PCC system. The clock cycle varies depending on SEL, and the PCC signal synchronized with that cycle is the output.

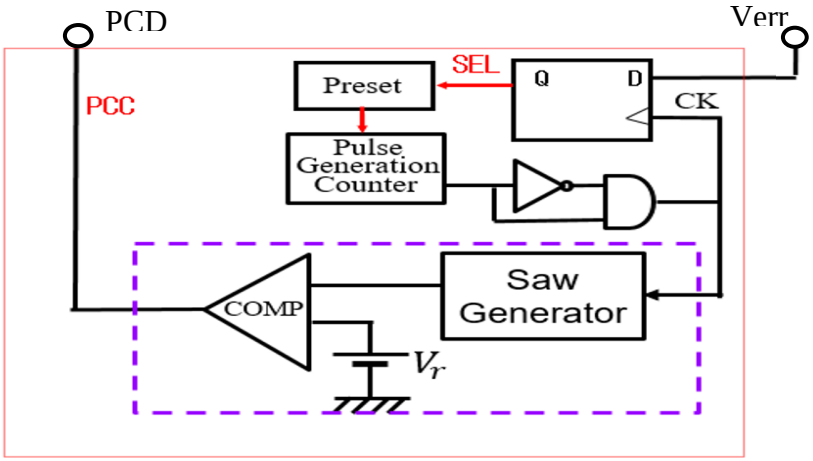

Figure 32. PCC control circuit.

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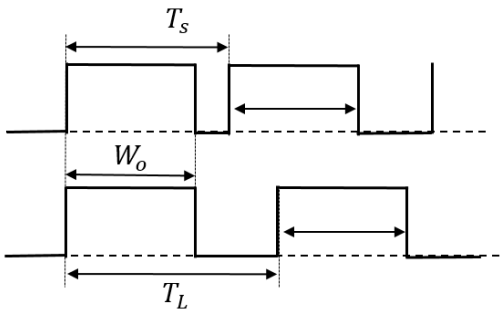

Figure 33. PCD pulse of PCC control.

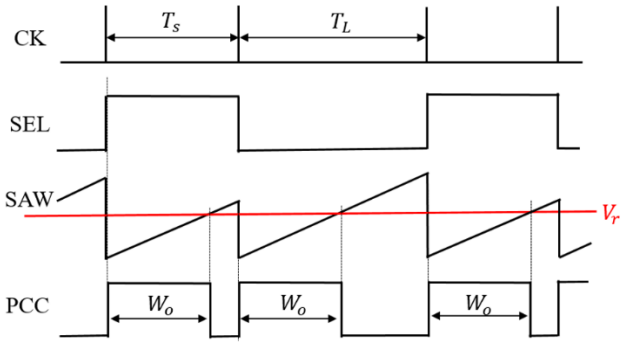

Figure 34. Main waveforms of PCC control.

(B) Simulation Result with the PCC Control

Figure 35 illustrates main signals, and the pulse lengths of the PCC signal vary based on SEL. Figure 36 presents the simulated spectrum of the PCD signal with the PCC control. There the pulse conditions are T_L=600 ns and T_s=220 ns, resulting in a notch frequency of F_{nc} = 2.6 MHz, as calculated from Eq. (28). However, in Figure 36, notches appear around F_{nc} though they are not clearly visible. There are many line spectra because spread spectrum technique is not utilized. The frequency position of notch spectrum can be altered by the coded pulse frequencies or the switching converter parameters. Table 3 shows the simulation parameters.

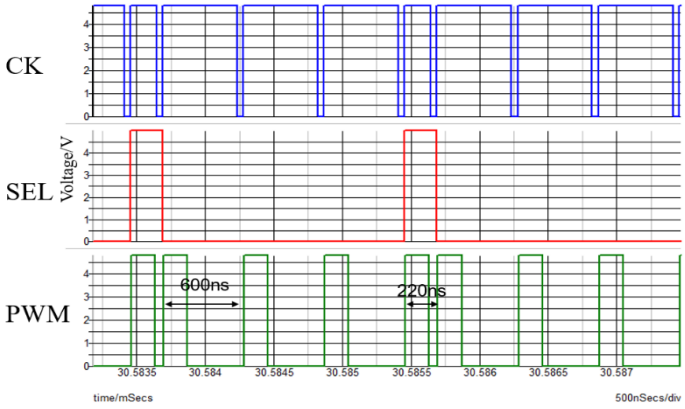

Figure 35. Simulated signals of PCC method.

Table 3. Parameters of PCC control circuit.

V_i	V_o	I_o	L
10V	3V	0.5A	100μH
C	W_o	T_L	T_s
470μF	170ns	600ns	220ns

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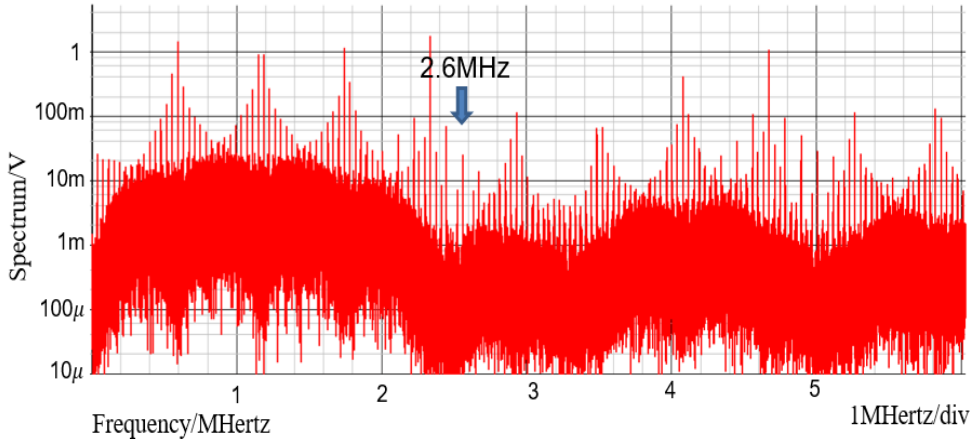

Figure 36. Spread spectrum of PCD signal with PCC control (without spread spectrum).

4.4. Pulse Width and Phase Coding (PWPC) Control

(A) PWPC Method

The PWPC method is realized by incorporating a PPC circuit followed by the SAW generator for PWC (Figure 37). There the frequency for a large notch is designed using Eqs. (27) and (28). Figure 38 illustrates the SEL and PWPC signals. When SEL is high, W_H is selected, and when SEL is low, the shifted W_L is selected. It is observed that the notch by the PWPC method is deeper compared to the PWC method.

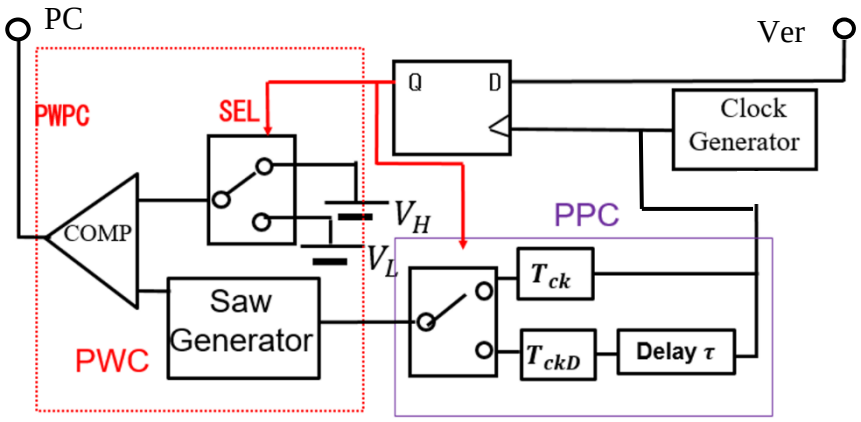

Figure 37. PWPC control circuit.

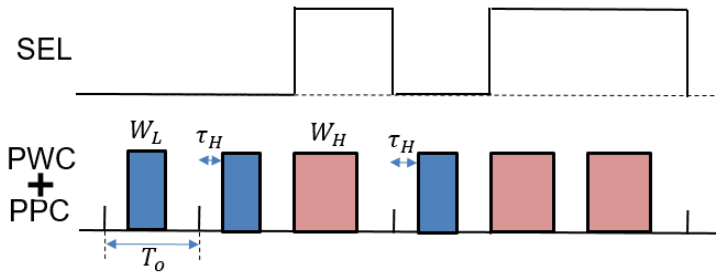

Figure 38. Signals of PWPC control.

(B) Simulation Results with PWPC Control

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In simulation, we set T_o=500 ns, W_H=320 ns, W_L=160 ns, τ_H=80 ns, τ_L=0 ns to produce a large notch at 6.25 MHz. Figure 39 illustrates the simulated spectrum of the PWPC signal. The noise level at the notch frequency is less than -20 dB relative to the average level.

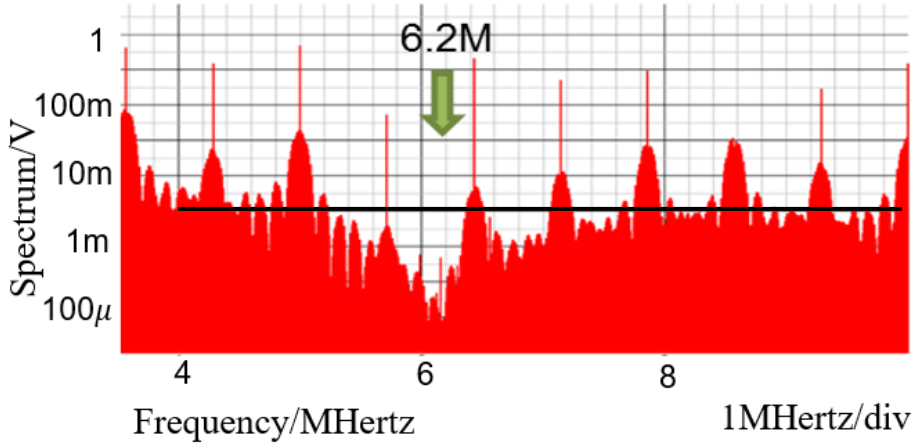

Figure 39. Spread spectrum of PCD signal with PWPC control.

4.5. Derivation of Notch Frequency Using Fourier Transform

Now we analyze various pulse coding methods and derive the formulae for their notch characteristics. We break down the analysis into four steps:

1) Define the signal of the pulse coding method.

2) Determine its Fourier transform.

3) Take its absolute value to obtain their spectrum characteristics.

4) Derive its zero point.

(A) Analysis of PWC Control

First, we analyze the PWC control. One period of the PWC signal is defined as T_{ck}, which has two different pulse widths: W_L and W_H (Figure 40). The zero frequency of the PWC control spectrum is obtained as Eqs. (29), (30), (31), using Fourier transform on the pair of coding pulses.

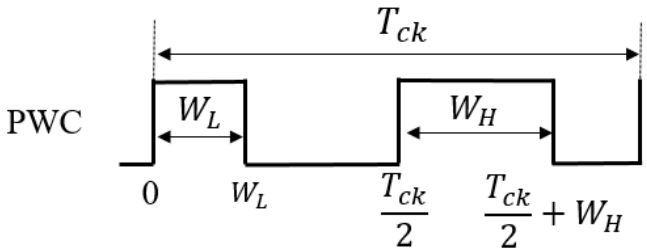

Figure 40. One-period two-pulse train of PWC signal.

$$
\begin{aligned}
F(\omega) &= \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt \\
&= \int_{0}^{W_L} e^{-j\omega t} dt + \int_{\frac{T_{ck}}{2}}^{\frac{T_{ck}}{2}+W_H} e^{-j\omega t} dt \\
&= \frac{1}{\omega}[\sin(\omega W_L) - \sin(\omega W_H) + j\cos(\omega W_L) - j\cos(\omega W_H)]
\end{aligned}
\tag{29}
$$

Then

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$$\omega^2 F^2(\omega) = [\sin(\omega W_L) - \sin(\omega W_H) + j\cos(\omega W_L) - j\cos(\omega W_H)]^2$$

$$\omega^2 \left|F(\omega)\right|^2 = 4\sin^2\left(\frac{\omega W_H - \omega W_L}{2}\right) \tag{30}$$

Now we have the following:

$$\begin{aligned} \left|F(\omega)\right| &= \frac{1}{\omega} 2\sin\frac{\omega W_H - \omega W_L}{2} \\ &= (W_H - W_L)\frac{\sin\frac{\omega(W_H - W_L)}{2}}{\frac{\omega(W_H - W_L)}{2}} \\ &= (W_H - W_L)\sin c\left\{\frac{\omega}{2}(W_H - W_L)\right\} \end{aligned} \tag{31}$$

We see that the PWC spectrum is expressed by a *sinc* function, which depends on the difference in pulse widths. The frequency at the zero point is obtained as follows:

$$F_{notch} = \frac{N}{(W_H - W_L)} \tag{32}$$

Eq. (32) shows that the notch characteristics correspond to the zero of the *sinc* function. Notice that the notch frequency is determined by the difference in pulse widths, and it is independent of the clock frequency.

Next, calculate the spectrum characteristics of the eight rows of PWC pulses in Figure 41. Assume that the entire eight trains of pulses have a period T_{ck}, and the Fourier transform yields Eq. (33).

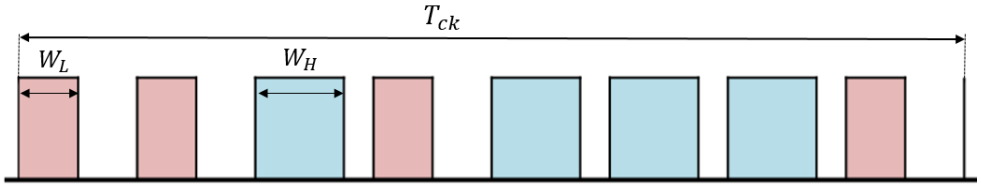

Figure 41. One-period eight-pulse train of PWC signal.

$$\begin{aligned} F(\omega) = -\frac{1}{j\omega}\{&\cos(\omega W_H) - j\sin(\omega W_H) + \cos(\omega W_H + \frac{\pi}{4}) - j\sin(\omega W_H + \frac{\pi}{4}) - \cos(\omega W_L) + j\sin(\omega W_L) \\ &- \cos(\omega W_L + \frac{\pi}{4}) + j\sin(\omega W_L + \frac{\pi}{4})\} \end{aligned} \tag{33}$$

$$\begin{aligned} \left|F(\omega)\right| &= (W_H - W_L)\sin c\left\{\frac{\omega}{2}(W_H - W_L)\right\} \cdot \sqrt{\left\{6 + 4\cos\left(\frac{\pi}{4}\right) + 4\cos\left(\frac{\pi}{2}\right) + 4\cos\left(\frac{3\pi}{4}\right)\right\}} \\ &= \sqrt{14} \cdot (W_H - W_L)\sin c\left\{\frac{\omega}{2}(W_H - W_L)\right\} \end{aligned} \tag{34}$$

The calculated result of the notch frequency based on Eq. (33) is the same as that of Eq. (32).

The notch characteristics depend solely on the difference of pulse widths, regardless of the arrangement and number of pulses. The frequency at the zero point is obtained by:

$$F_{notch} = \frac{N}{(W_H - W_L)}$$

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(35)

Figure 42 illustrates a comparison between the *sinc* function and the spectrum of the PWC waveform with W_H=3μs, W_L=7μs, f_{notch}=250 kHz. The envelopes of the spectrum in simulation match the theoretical result (Eq. (35)).

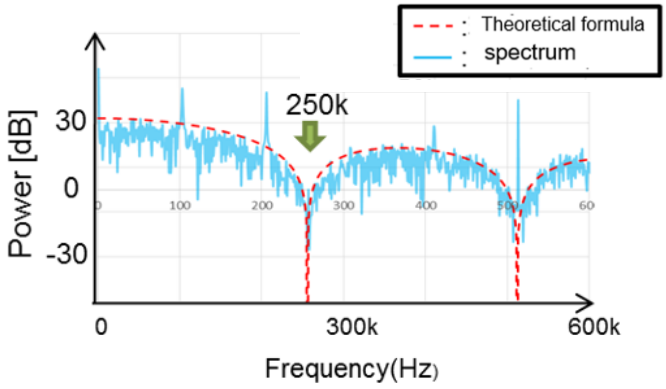

Figure 42. Comparison of theory and simulation.

(B) Analysis of PPC and PCC controls

We analyze the Pulse Position Coding (PPC) method. As illustrated in Figure 43, we define the PPC signal in one period as T_{ck}, which consists of two different phase pulse coding signals (τ_H and τ_L). The frequency characteristics of the PPC control are obtained by Fourier transform on the pair of coding pulses (Eq. (36)).

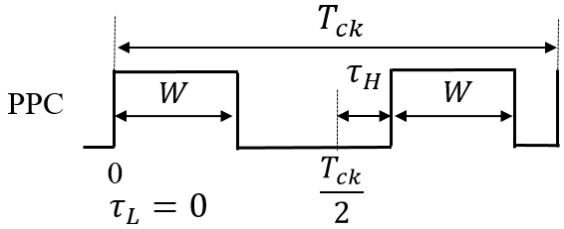

Figure 43. One-period two-pulse trains of PPC signal.

$$
\begin{aligned}
F_p(\omega) &= \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \\
&= \int_{\tau_L}^{\tau_L+W} e^{-j\omega t}dt + \int_{\frac{T_{ck}}{2}+\tau_H}^{\frac{T_{ck}}{2}+\tau_H+W} e^{-j\omega t}dt \\
&= \frac{1}{\omega}\{j\cos(\omega(\tau_L-\tau_H)) + \sin(\omega(\tau_L-\tau_H)) - j\cos(\omega(\tau_L-\tau_H-W)) \\
&\quad -\sin(\omega(\tau_L-\tau_H-W)) - j\cos(\omega(\tau_H-\tau_L)) - \sin(\omega(\tau_H-\tau_L) + j\cos(\omega(\tau_H-\tau_L-W)) + \sin(\omega(\tau_L-\tau_H-W))\}
\end{aligned}
\tag{36}
$$

By taking the absolute value, Eq. (37) is derived, which shows the frequency at the zero point as Eq. (38):

$$
\begin{aligned}
&|F_p(\omega)| = 2|\tau_H-\tau_L|\left|\sin c\left\{2|\tau_H-\tau_L|\frac{\omega}{2}\right\}\right|\left|\sin(W\frac{\omega}{2})\right| \\
&F_{notch1} = \frac{N}{2|\tau_H-\tau_L|}, F_{notch1} = \frac{N}{W}
\end{aligned}
\tag{37}
$$

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(38)

According to Eqs. (37) and (38), the PPC method relies on two *sinc* functions, each exhibiting distinct notch characteristics. This method relies on the coding phase and the pulse width. Here, Eq. (38) represents the theoretical equation of the PPC method when alternating coding is employed.

Next, we analyze the PCC method. We define the PCC signal in one period as T_{ck}, which consists of two different cycle coding signals: T_L and T_S (Figure 44). The theoretical frequency of the PCC control is obtained as Eq. (39), by Fourier transform on the pair of coding pulses.

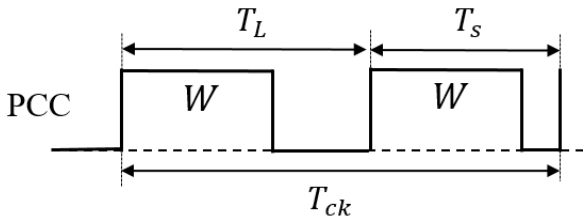

Figure 44. One-period two-pulse train of PCC signal.

$$
\begin{aligned}
F_c(\omega) &= \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \\
&= \int_0^{T_L-W} e^{-j\omega t}dt + \int_{T_L}^{T_S-W} e^{-j\omega t}dt \\
&= \frac{1}{\omega}\{j\cos(\omega T_S) + \sin(\omega T_S) - j\cos(\omega(T_S - W)) \\
&\qquad -\sin(\omega(T_S - W)) - j\cos(\omega T_L) - \sin(\omega T_L) + j\cos(\omega(T_L - W)) + \sin(\omega(T_L - W))\}
\end{aligned}
\tag{39}
$$

$$
\left|F_c(\omega)\right| = 2\left|T_L - T_S\right|\left|\sin c\left\{\left(T_L - T_S\right)\frac{\omega}{2}\right\}\right|\left|\sin(W\frac{\omega}{2})\right| \quad \therefore \tag{40}
$$

This equation shows that the notch characteristic depends on both the coding period and the pulse width, as in the PPC method.

(C) Analysis of PWPC method

Next, we analyze the Pulse Width and Phase Coding (PWPC) method, which encodes both the pulse width and phase. We define the PWPC signal in one period as T_{ck}, which represents two coding signals (Figure 45). The frequency characteristics of the PWPC control are derived as Eqs. (41) and (42).

$$
\begin{aligned}
F_{wc}(\omega) &= \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \\
&= \int_{\tau_L}^{\tau_L+W_L} e^{-j\omega t}dt + \int_{\frac{T_{ck}}{4}+\tau_H}^{\frac{T_{ck}}{4}+\tau_H+W_L} e^{-j\omega t}dt + \int_{\frac{T_{ck}}{2}+\tau_L}^{\frac{T_{ck}}{2}+W_H} e^{-j\omega t}dt + \int_{\frac{3T_{ck}}{4}+\tau_H}^{\frac{3T_{ck}}{4}+\tau_H+W_H} e^{-j\omega t}dt
\end{aligned}
\tag{41}
$$

$$
\left|F_{wc}(\omega)\right| = 2\left|\tau_H - \tau_L\right|\left|\sin c\left\{2\left|\tau_H - \tau_L\right|\frac{\omega}{2}\right\}\right| \cdot \left|\sin\{(W_H - W_L)\frac{\omega}{2}\}\right| \tag{42}
$$

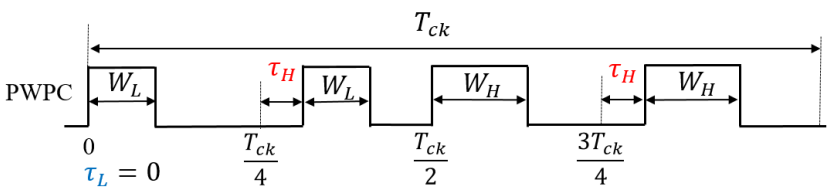

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Figure 45. One-period four-pulse-train of PWPC signal.

In the PWPC, a *sinc* function with the pulse width and phase is used for representation, and two notch characteristics are generated. Further, if the notch characteristics are set to overlap with $2|\tau_H - \tau_L| = |W_H - W_L|$, they become as follows:

$$|F_{wc}(\omega)| = \frac{\sin^2(\frac{\omega}{2}(W_H - W_L))}{\frac{\omega}{2}} \tag{43}$$

Figure 46 provides a comparison of the notch characteristics in Eqs. (43) and (31). The notch around the zero point at 250 kHz in Eq. (43) is broader than in Eq. (38). The composite coding method increases both the notch width and depth compared to the PWC or PPC method.

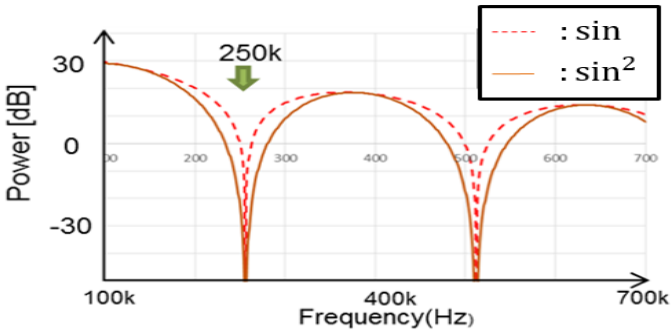

Figure 46. Comparison of notch characteristics with PWC and PWPC methods.

5. Automatic Notch Generation [19–25]

This section describes the generation method of W_H and W_L for automatic notch generation in PWC control and PWPC control.

5.1. Automatic Notch Generation Using PWC Control

(A) Design of Relationship Among $\boldsymbol{F_n}$, $\boldsymbol{F_{ck}}$ and $\boldsymbol{T_{in}}$

Our design is the generation of the notch frequency F_n so that it lies between F_{ck} and $2F_{ck}$ and it matches the received signal frequency (Figure 47). F_{in} is provided to match the receiving frequency and the relationship among F_{in}, F_n and F_{ck} is given by Eq. (44). Here, P is a positive integer. Then, the relationship of T_{in} $(=1/F_{in})$ and $T_{ck}(=1/F_{ck})$ is given by Eq. (45).

$$F_{in} = (P+0.5) \times F_{ck} \tag{44}$$

$$T_{ck} = (P+0.5) \times T_{in} \tag{45}$$

We see from Eq. (44) that in case of P=1, F_n is set between F_{ck1} and $2F_{ck1}$, and it is equal to F_{in1}. In the case of P=2, F_n is produced between $2F_{ck2}$ and $3F_{ck2}$, and $F_n = F_{in2}$ (Figure 47).

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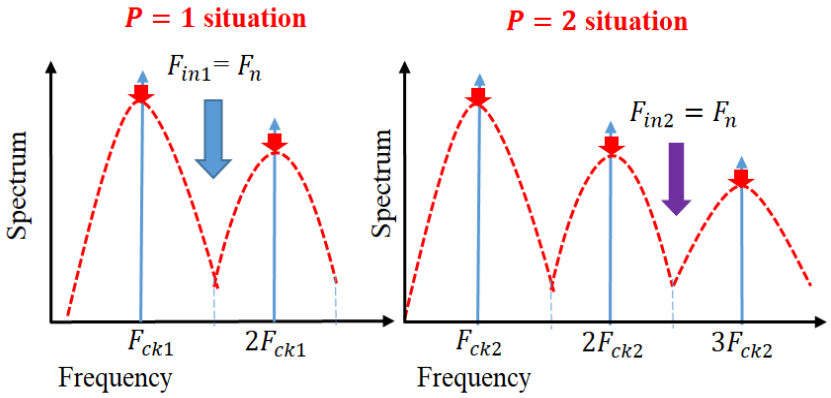

Figure 47. Positions of F_n [27] @IEICE.

Conversely, the duty ratio D of the PWC signal is represented by Eqs. (46), (47), (48). Further, the original clock signal in Figure 48 represents the PWC signal that is not encoded, with a pulse width of T_o. It also corresponds to Eq. (46), where D_o is set to 0.5. Pulse-H and pulse-L are generated based on T_o (Figure 48), and this corresponds to Eq. (47). Here, T_p represents the difference of W_H and T_o , or of T_o and W_L. T_n $(= 1/F_n)$ is determined by the difference of W_H and W_L. Also, W_H, W_L, and T_o must satisfy the relationship given in Eq. (48) to ensure a stable output voltage, V_o. Here, 2 $T_p = T_n$, and it is the difference of W_H and W_L.

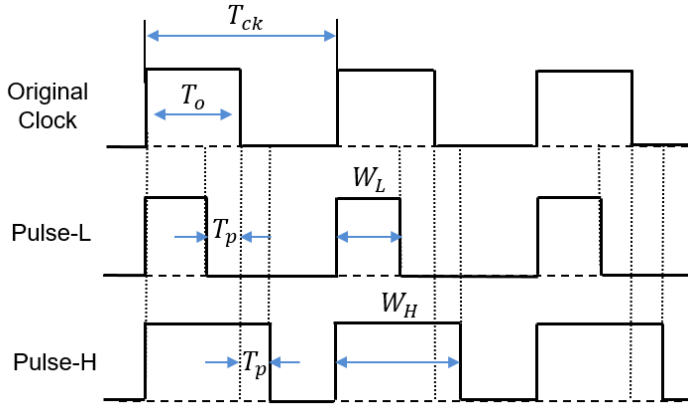

Figure 48. Timing of Pulse-H and Pulse-L [26] @IEEE.

$$T_o = D_o \times T_{ck} = \frac{V_o}{V_i} \times T_{ck} = 0.5T_{ck} \quad (46)$$

$$W_H = T_o + T_p,\ W_L = T_o - T_p \quad (47)$$

$$T_n = W_H - W_L = 2 \times T_p \quad (48)$$

(B) Automatic Notch Generation from Clock

T_{ck} is generated by T_{in} as shown in Eq. (45). For P=1, the notch frequency is produced between F_{ck} and $2F_{ck}$ from T_{in} (See Figure 47). T_{ck} is shown in Eq. (49), which can be realized with a shifter and an adder. Figure 49a,b show the automatic PWC pulse coding circuit based on Eqs. (46), (47), (48) for $D_o = 0.5$, where $W_H = 0.5T_{ck} + 0.5T_{in}$ and $W_L = 0.5T_{ck} - 0.5T_{in}$. Figure 49a shows the whole block diagram, while Figure 49b shows the detailed block diagram of Pulse-H, Pulse-L generation from N_H, N_L and N_{tclk}. Then, in the case of P=N, F_n is produced between NF_{ck} and $(N+1)F_{ck}$ with T_{ck} as shown in Eq. (50).

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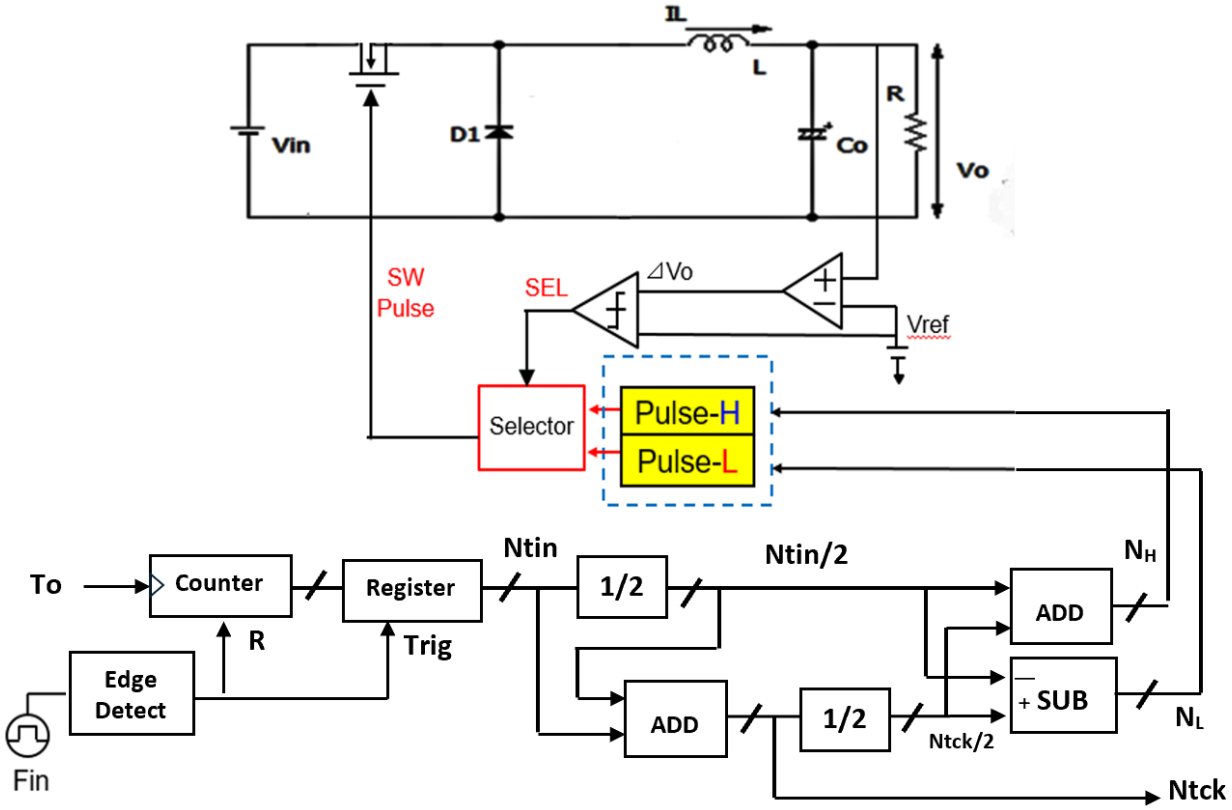
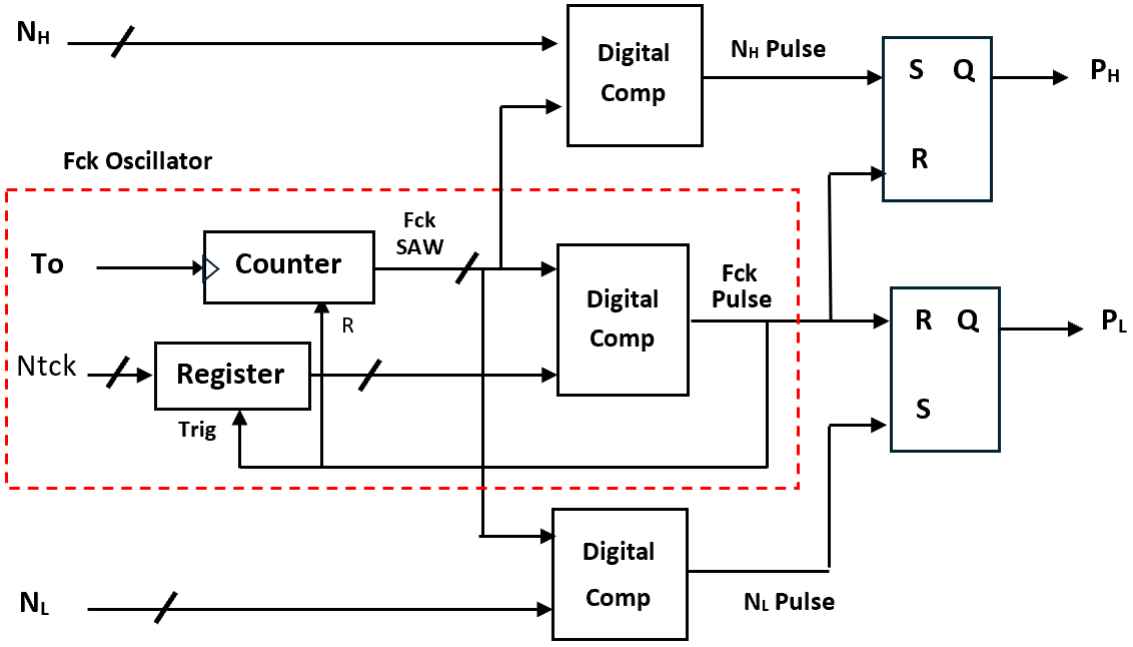
$$T_{ck} = (1+0.5) \times T_{in} \Rightarrow T_{ck} = 1.5T_{in} \tag{49}$$

$$T_{ck} = (N+0.5) \times T_{in} \tag{50}$$



(a) Pulse coding circuit of automatic PWC method.



(b) Coding pulse generator with Fck oscillator.

Figure 49. Pulse coding circuit of automatic PWC method for $P = 1$ [26] @IEEE.

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Figure 50 illustrates the automatic PWC method for P=N. For instance, in case N=2, F_{in} is set to 1.25 MHz, F_{ck} is 500kHz and F_n appears at 1.25 MHz, which falls between 2 F_{ck} and 3 F_{ck}.

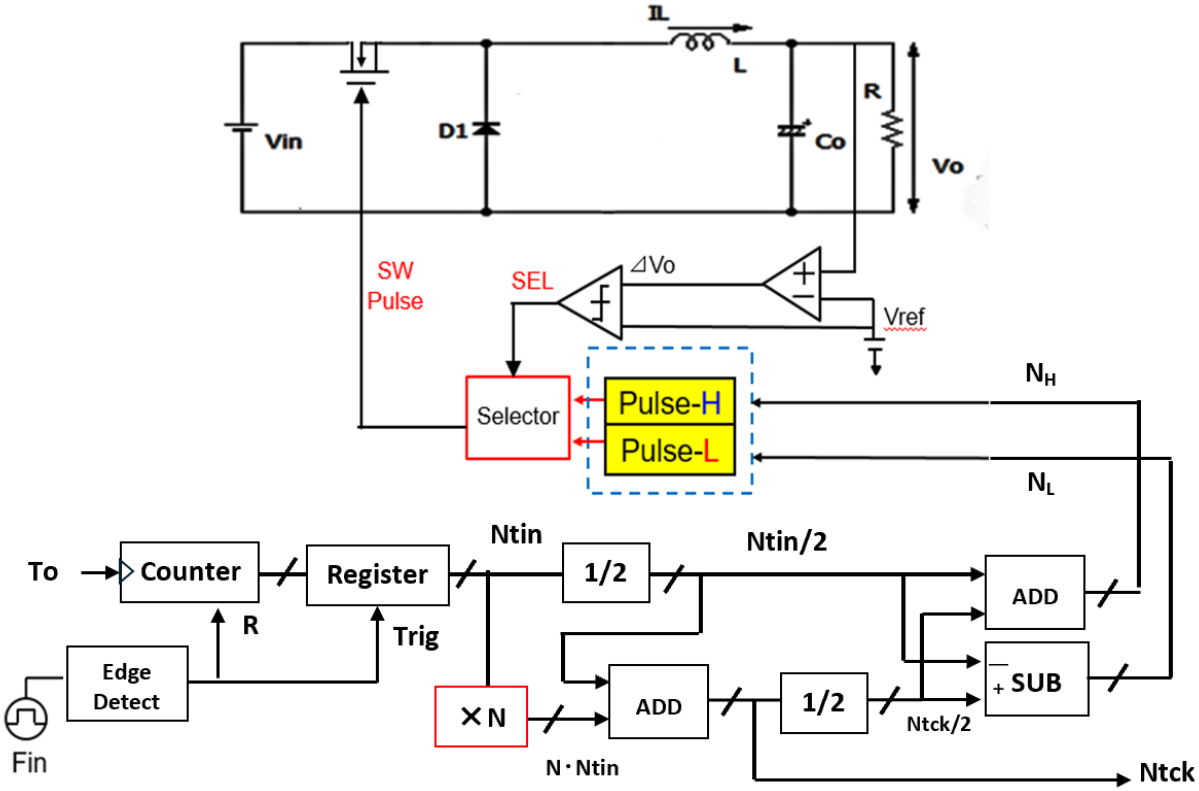

Figure 50. Pulse coding circuit of automatic PWC method for $P = N$.

(C) Simulation Results with Automatic Notch Generation

Digital circuit is used for coding pulse notch generation for $P = 1$ (Figure 49). Figure 51 displays the waveforms of pulse-H and pulse-L for F_{in} = 750 kHz. The saw-tooth period T_{ck} is automatically set to $2\mu s$. By comparing V_L and V_H, pulse-L and pulse-H with $W_L = 0.34\mu s$ and $W_H = 1.67\mu s$ are generated automatically. According to Eq. (23), F_n is 750 kHz, and the spectrum of the PWM signal is shown in Figure 52. The notch is at 750 kHz, which corresponds to F_{in}, and there the bottom level is 1mV. However, there is the line spectrum at F_{in} (= 500 kHz) with an amplitude of 900mV, and multiple harmonics spectra present. Thus, frequency modulation is considered for spectrum spread in the coding pulse notch generator.

The frequency modulation of F_{ck} is used for EMI reduction as described in Section 3.1, and the spectrum of the PWM signal is displayed in Figure 53. The notch is clearly observed at 750 kHz (= F_{in}). The bottom level of the notch frequency is 1mV, while the spectrum at F_{ck} (=500 kHz) is 20mV. Notice that another notch appears also at $4F_{in}$ in simulation. In principle, a 3MHz frequency is equal to $6F_{ck}$(= $4F_{in}$). Since the clock and the input signal overlap, the notch is not expected to appear at $4F_{in}$. The theoretical reason for the notch cause at $4F_{in}$ remains unknown and will be addressed in future work.

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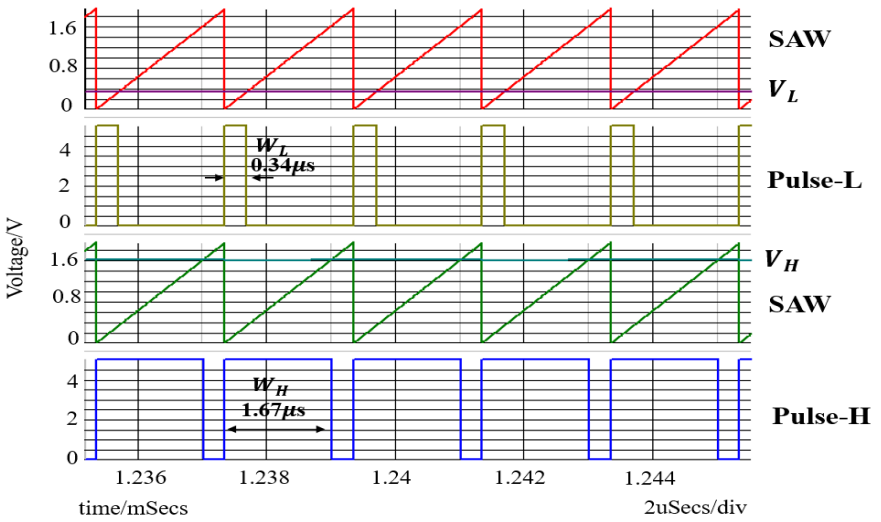

Figure 51. Simulated waveforms for $P = 1$.

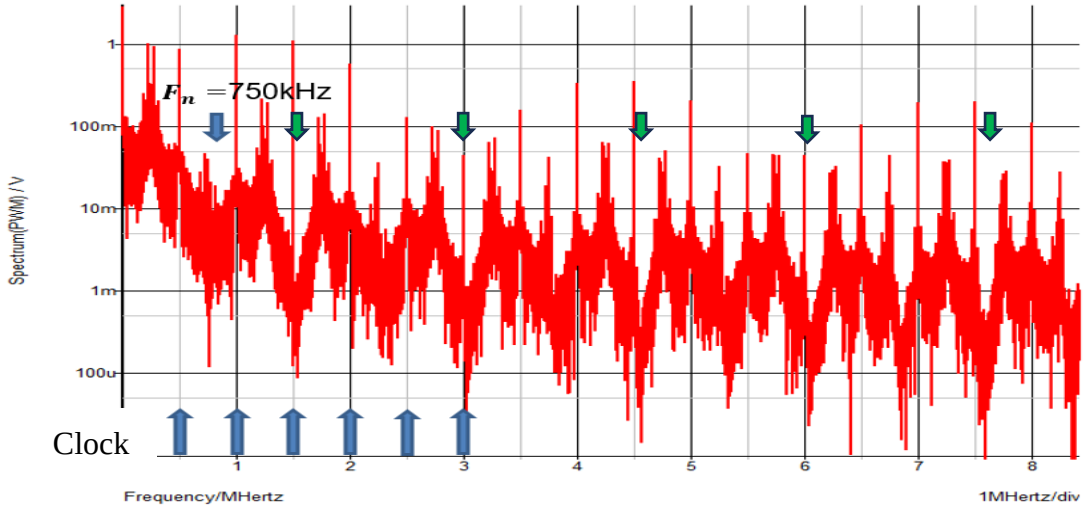

Figure 52. Simulated spectrum of PWM signal without spread spectrum (P=1).

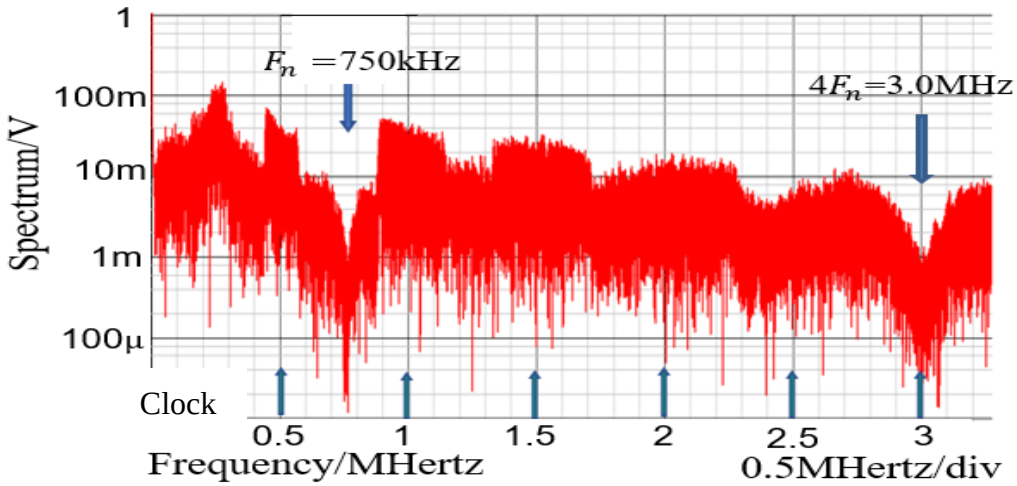

Figure 53. Simulated spectrum with spread spectrum for $P = 1$.

Next, we discuss the case for P=2. Figure 54 displays the simulated waveforms of pulse-H and pulse-L for F_{in} =1,250 kHz, and we observe $W_H = 1.39\mu s$ and $W_L = 0.6\mu s$. The expected F_n is 1,250

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kHz based on Eq. (24). The spectrum of the PWM signal is displayed in Figure 55. The notch is observed at 1,270 kHz, which is equal to F_{in} and falls between 2 F_{ck} and 3 F_{ck} .

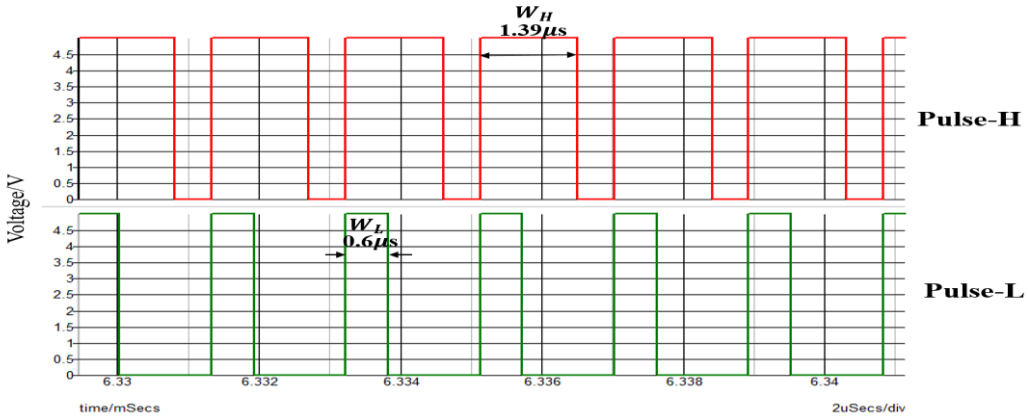

Figure 54. Simulated waveforms for $P = 2$.

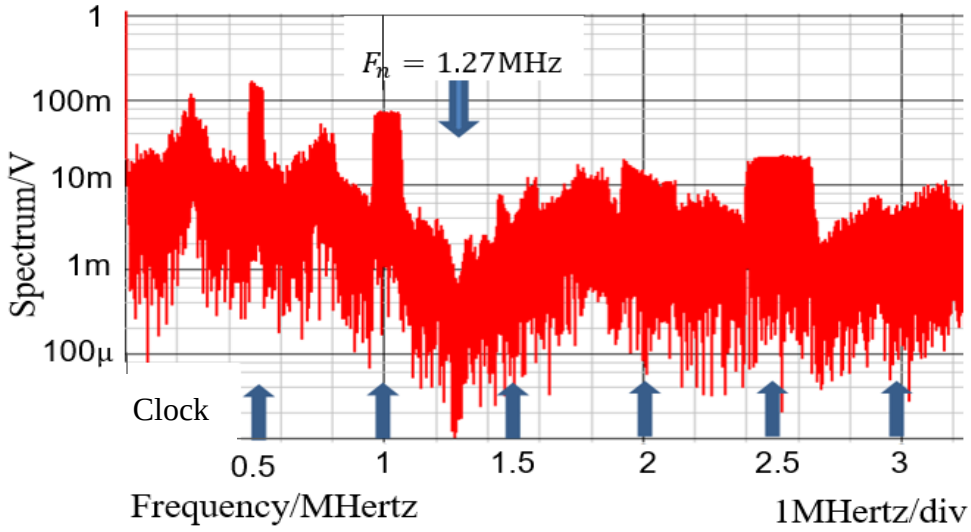

Figure 55. Simulated spectrum with spread spectrum for $P = 2$.

Then, we consider the case for P=3. Figure 56 displays the simulated waveforms of pulse-H and pulse-L for F_{in} =1,750 kHz. Also, $W_H = 1.29\mu s$ and $W_L = 0.72\mu s$. Based on Eq. (24), F_n is 1750 kHz. The spectrum of the PWM signal is displayed in Figure 57. The notch is observed at 1,750 kHz, which corresponds to F_{in} and lies between 3 F_{ck} and 4 F_{ck}.

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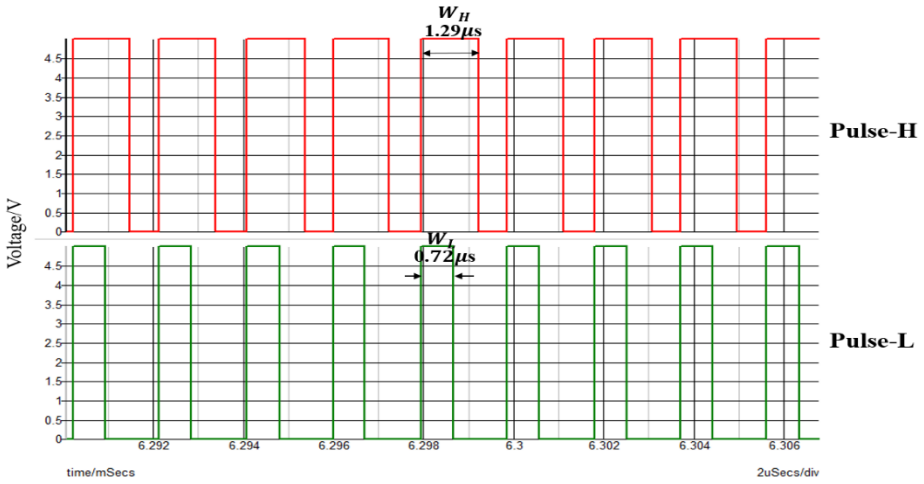

Figure 56. Simulated waveforms for $P = 3$.

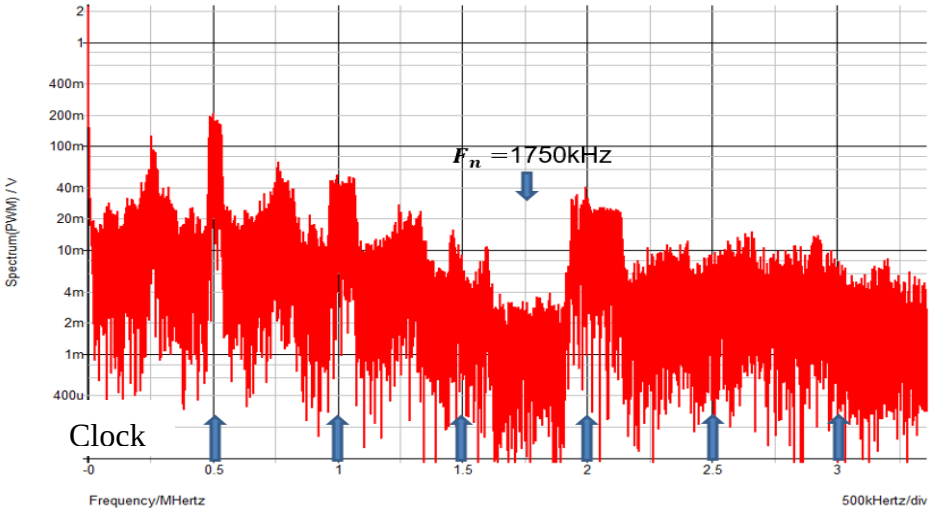

Figure 57. Simulated spectrum with spread spectrum for $P = 3$.

(D) Automatic Setting of Notch Frequency from Input Frequency

Here, we discuss the automatic adjustment of F_{in} changes from channel 1 to channel 2 in the radio receiver (Figure 58). We set $D = 0.5$, $P = 1$, and F_{in} of channel 1 to 750 kHz. Then the output of the automatic PWC controller produces a notch at 750 kHz. In case F_{in} changes to 1,250 kHz, the corresponding F_{ck}, W_H and W_L also change, and the notch is automatically produced at 1,250 kHz. Simulated spectra are shown in Figures 59 and 60, as F_{in} changes from F_{n1} = 750 kHz to F_{n2}= 1,250 kHz. The notches are observed at 750 kHz and 1,250 kHz, which correspond to F_{in}.

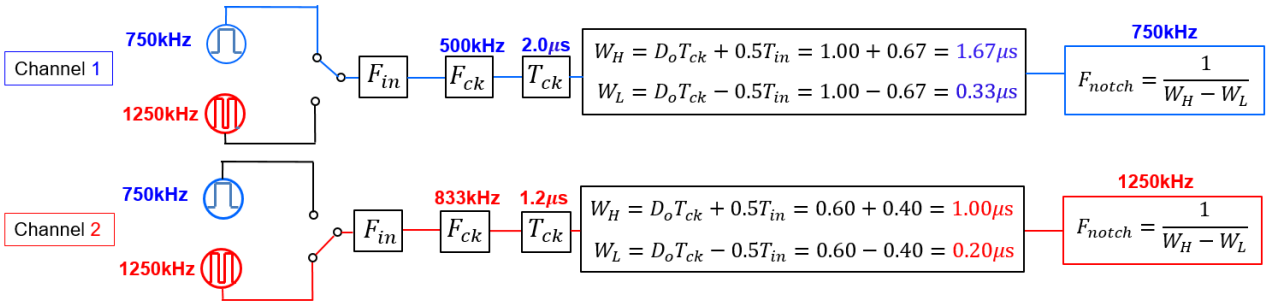

Figure 58. Block diagram of change from channel 1 to channel 2.

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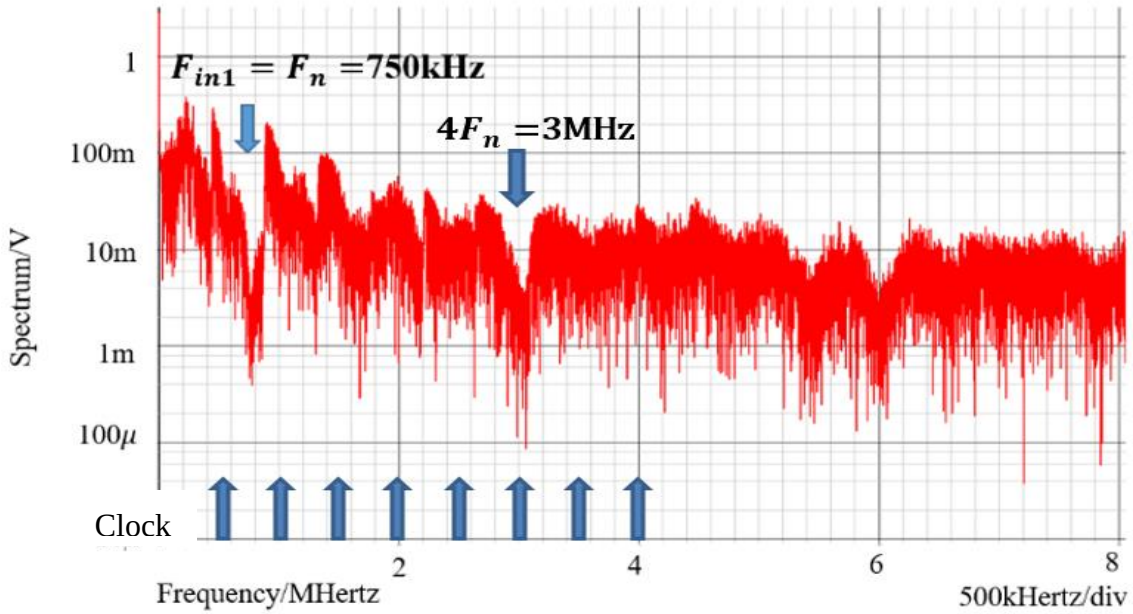

Figure 59. Simulated spectrum for $F_{in1} = 750$ kHz.

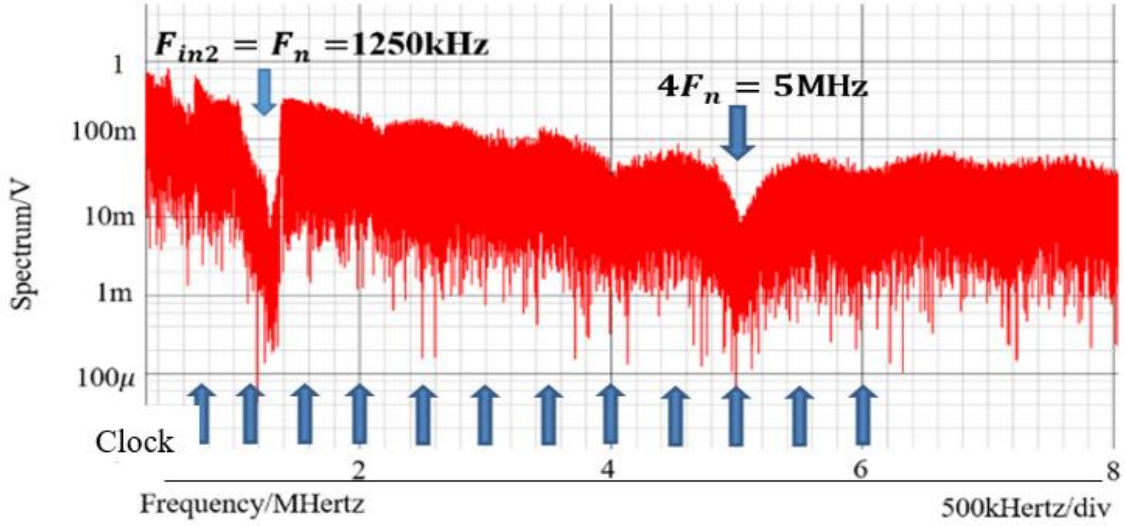

Figure 60. Simulated spectrum for $F_{in2} = 1{,}250$ kHz.

5.2. Automatic Notch Generation with PWPC Control

This subsection describes the automatic generation of Pulse-H, Pulse-L, and Pulse-LD for the PWPC control.

(A) Automatic Generation Method o PWPC Control

In the PWPC method, F_n is given by Eqs. (24) and (27), and Figure 61 illustrates the PWPC configuration. There the automatic PWC controller generates N_H and N_L. Comparison of N_H with the saw-tooth waveform produces Pulse-H, while comparison of N_L with the delayed saw-tooth produces Pulse-L_D. Figure 62 shows their waveforms, where the phase shift τ is equal to 0.5 T_{in} and Eq. (24) is equal to Eq. (27) for the steep notch.

The relationship of F_{ck} and F_n is given in Eq. (44). For P = 1, the followings are derived from Eq. (47). Here P_{LD} is the timing of the rear end of P_L.

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$$W_H = T_o + T_p = D \cdot T_{ck} + 0.5T_{in} \qquad W_L = T_o - T_p = D \cdot T_{ck} - 0.5T_{in}$$
$$P_{LD} = \tau + T_o - T_p = \tau + D \cdot T_{ck} - 0.5T_{in} \tag{51}$$

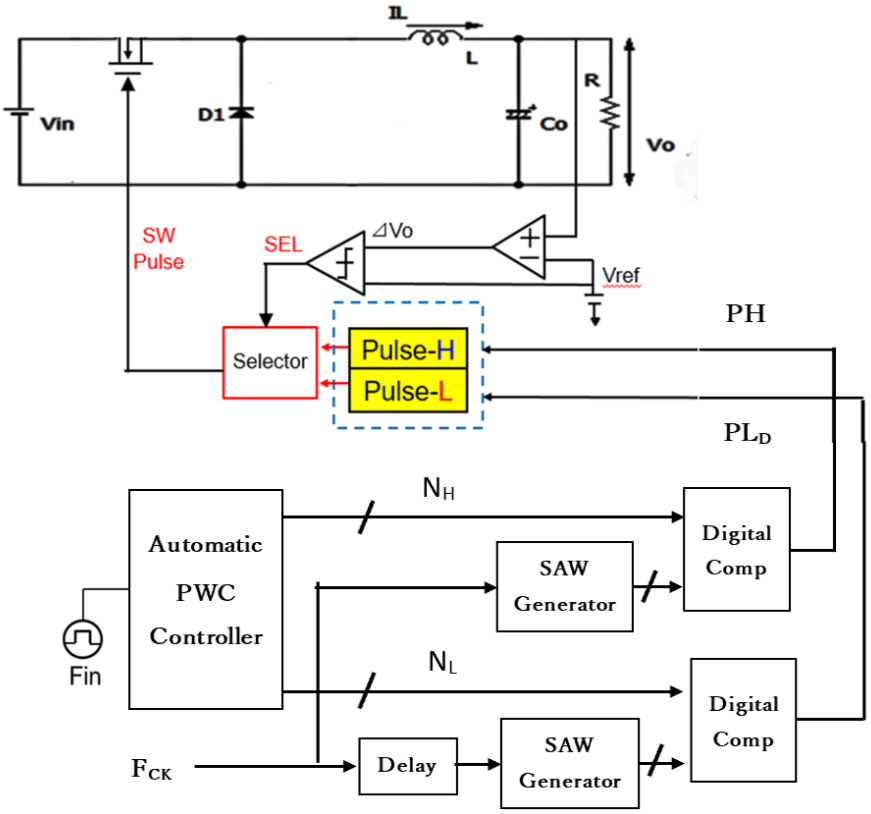

Figure 61. Pulse coding circuit of the PWPC method.

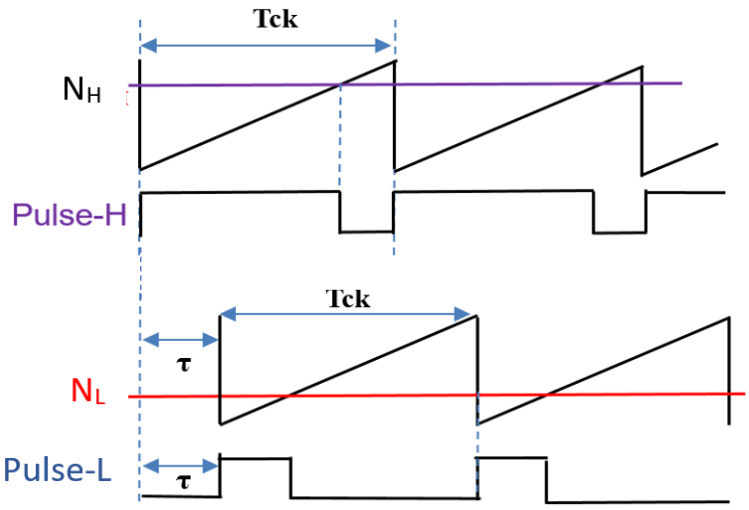

Figure 62. Signals of PWPC control.

(B) Simulation Results of Automatic Notch Generation with PWPC Control

Figure 63 presents the saw-tooth signals, and the primary signals are highlighted in Figure 61. The coding pulses P_H, P_L and P_{LD} are generated by comparing V_H and V_L with the sawtooth and the delayed sawtooth signals.

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There, V_{in} is 10V, and V_o is 5V. When F_{in} is set to 750 kHz and for P=1, F_{ck} is set to 500 kHz. To set F_n to F_{in}= 750 kHz, W_H=1.67μs,W_L = 0.33μs, and τ=0.67μs are used based on Eq. (51).

Simulation shows that with W_H=1.67μs, W_L=0.33μs, and τ=0.67μs, F_n is 750 kHz (= F_{in}) (Figures 64 and 65). A significant notch appears at 3.0 MHz (=4 F_n). Also, two notches are produced at higher frequencies.

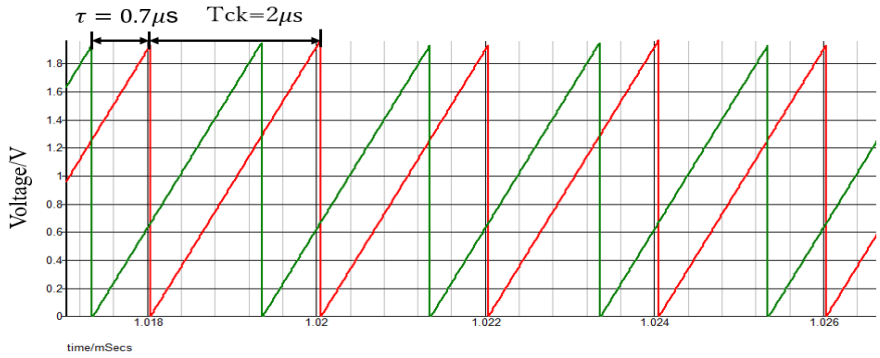

Figure 63. Saw-tooth signals with period T_{ck} and delay τ.

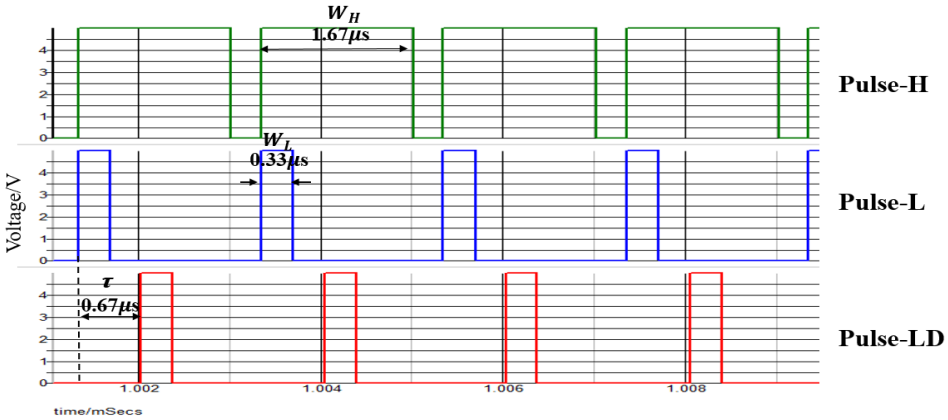

Figure 64. Signals in PWPC circuit.

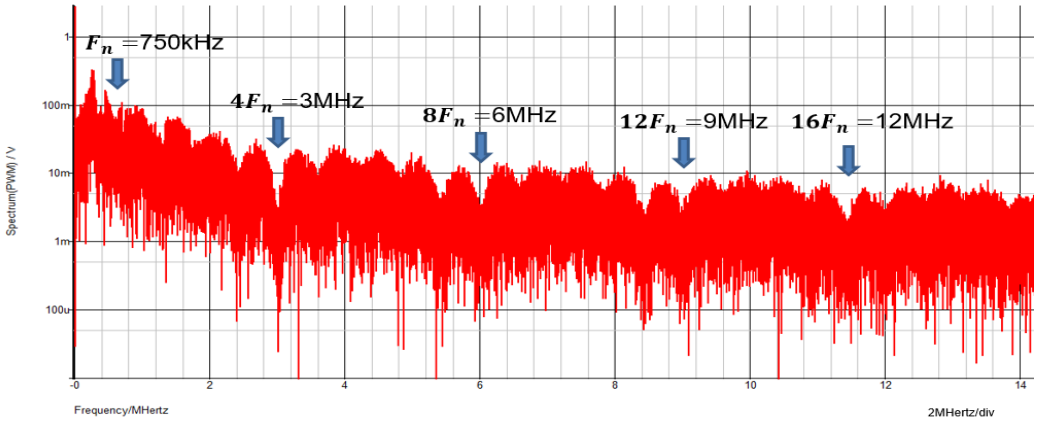

Figure 65. Simulated spectrum with spread spectrum using PWPC method.

5.3. Duty Ratio Generation in Automatic Notch Generation

This subsection discusses a method to automatically detect and set *D* for V_i and V_o change.

(A) Analysis of Relationship Between Voltage Conversion Ratio and PWM Duty Ratio

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In the automatic PWC control, F_{in} alone can generate F_{ck} as well as W_H and W_L using Eqs. (52), (53) based on Eqs. (45), (47), (48). Also see Figure 50. When $D_H = D_L = D_P$ (D_P: shift value of D), Tin is set to (2/3)Tck for P = 1 based on Eq. (45).

$$W_H = (D + D_H)T_{ck} = DT_{ck} + \frac{T_{in}}{2} = (D + \frac{1}{3})T_{ck} \tag{52}$$

$$W_L = (D - D_L)T_{ck} = DT_{ck} - \frac{T_{in}}{2} = (D - \frac{1}{3})T_{ck} \tag{53}$$

When D varies, the duty cycle of SEL, D_s is affected, which influences ΔV_o, and the resulting duty ratio D' is represented by Eq. (54). During the circuit design, the V_o/V_i ratio is fixed, meaning D, D_H and D_L are set. Even if F_{in} is changed, D_H and D_L are still produced automatically by the circuit. However, when V_o is changed, D also is changed, which differs from the designed D.

For instance, for $T_{in} = 0.67\mu s$ and $T_{ck} = 1\mu s$, we set $D=V_o/V_i=5V/10V$=0.5. That is, for $W_H = 0.83$ and $W_L = 0.17$ based on Eqs. (52) and (53), and D_s=0.5, the waveform of W_H and W_L remains balanced. However, when Dvaries, W_H changes to 0.86 and W_L changes to 0.20. In the designed circuit, when D_s remains at 0.5, W_H is increased while W_L is decreased.

In Eq. (54), ΔD represents the variation of D, and the change rate is defined as x=$\Delta D/D$. Then, the changed W_H' and D_H', along with W_L' and D_L', are given by Eqs. (55) to (58).

$$D' = D + \Delta D = D + D\frac{\Delta D}{D} = D(1 + x) \tag{54}$$

$$W_H' = (D + \Delta D + D_H)T_{ck} \tag{55}$$

$$D_H' = D_H - \Delta D \Rightarrow D(1 - x) \tag{56}$$

$$W_L' = (D + \Delta D - D_L)T_{ck} \tag{57}$$

$$D_L' = D_L + \Delta D \Rightarrow D(1 + x) \tag{58}$$

Before D varies, D_s=0.5 and $D_H : D_L = 1:1$. This means that the select signal keeps W_H and W_L balanced. After D varies, $D_H' : D_L'$ can be given by Eq. (59). The average voltage of the SEL signal, V_{SEL} is given by Eq. (60), and V_{SEL} is influenced by ΔD_o. Consequently, when V_{SEL} changes, ΔV_o increases.

$$D_H' : D_L' = (1 - x) : (1 + x) \tag{59}$$

$$V_{SEL} = \frac{V_{cc}}{(1 - x) + (1 + x)} = \frac{V_{cc}(1 - x)}{2} = \frac{V_{cc}(1 - \frac{\Delta D}{D})}{2} \tag{60}$$

It is inferred that when the duty ratio shifts from D to D', D_H changes to D_H' while D_L changes to D_L'. Consequently, the select signal for W_H and W_L is no longer balanced. It influences V_{SEL}, shifting it from $V_{cc}/2$ to V_{cc} (1−$\Delta D/D$)/2. Consequently, the output voltage also increases.

(B) Simulation Results of Duty Ratio Change

According to Section 5.2, when V_i is varied while keeping W_H and W_L fixed, the duty cycle of SEL changes significantly. This causes significant variations in I_L and ΔV_o. In simulation, $V_{ref} = V_o$ =5.0V and V_i are altered to 10V and 15V. Correspondingly, D changes to 0.5 and 0.33. Figure 66 displays the select signal waveforms. It is observed that for D = 0.5, the waveforms of W_H and W_L remain balanced. For D = 0.33, the waveform of the select signal becomes unbalanced, and the output of W_L exceeds that of W_H. Figure 67 illustrates ΔV_o as D varies. Any change in D affects ΔV_o.

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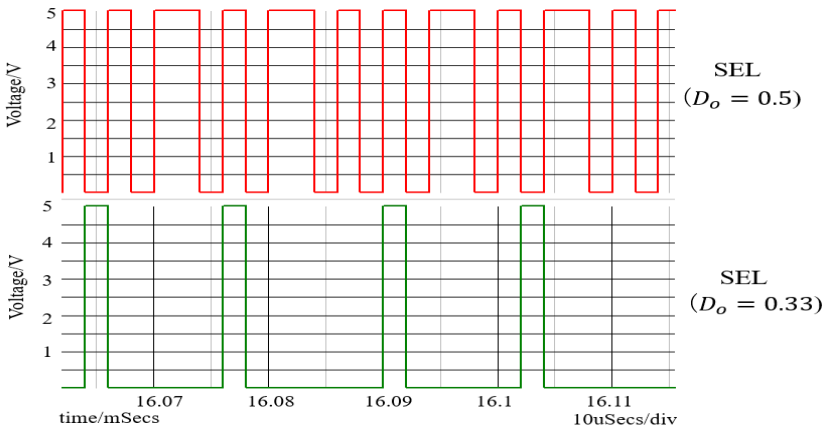

Figure 66. Waveforms of SEL [27] @IEICE.

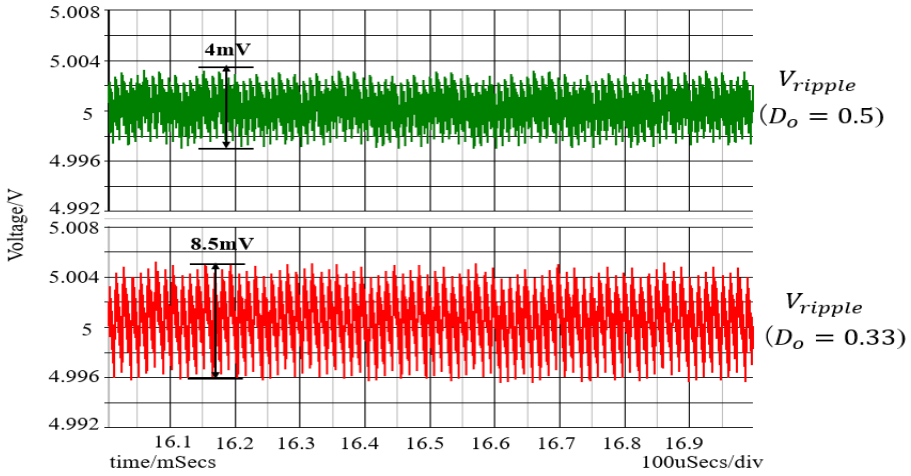

Figure 67. Output voltage ripples [26] @IEEE.

(C) Automatic Detection of PWM Duty

Based on D and Eqs. (52), (53), W_H and W_L are generated (Figure 49). When V_i varies, D also varies according to the ratio D=Vo/Vi. The number of W_H and W_L pulses are automatically adjusted based on D. Detection method of the SAW peak voltage produced by T_{ck} and Vi is considered. Under this condition, the peak voltage is proportional to D.

Figure 68 illustrates the automatic D detection circuit. There, the SAW signal is generated by a current source, with the frequency of the SAW designated as F_{ck}. A voltage follower serves as the peak hold circuit, and the peak voltage V_{peak} is compared with V_i by an error amplifier and an error voltage is generated. Usage of a voltage-controlled current source converts the error voltage into an error current, which is then fed-back to the SAW generator. In this process, the SAW peak voltage is automatically detected, which is equal to V_i . Then, the comparator produces the D detection signal by comparing the SAW signal with V_{ref}, which is equal to V_o.

Figure 69 shows signal waveforms of the D detection circuit. For $V_i = 12V$, the SAW peak voltage is 12V. By comparing the SAW with V_{ref}, the sampled data corresponds to D_1. For V_i = 10V, the SAW peak voltage automatically changes to 10V. By comparing the SAW and V_{ref}, the sampled data becomes D_2.

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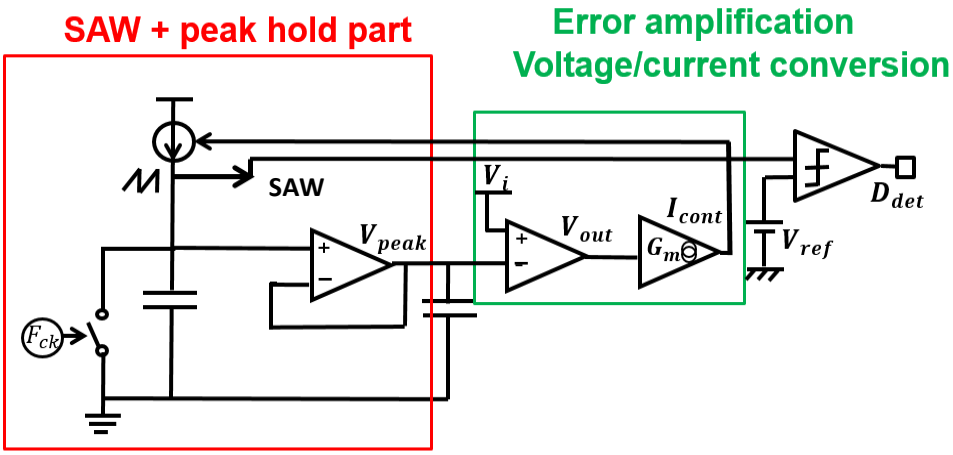

Figure 68. Automatic D detection circuit [26] @IEEE.

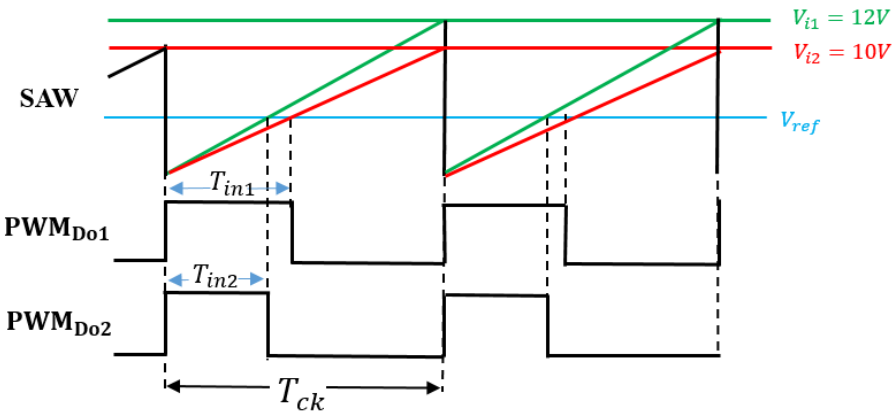

Figure 69. Signals of D detection circuit [26] @IEEE.

We have developed automatic notch frequency generator using this method. There, D is automatically detected in response to V_i change, for the notch creation at the input frequency. The simulation results are shown in Figure 70, with the same parameters as those in Section 5.1, except for V_i, which is 15V this time. Additionally, the clock is not modulated, and D can be automatically detected as 0.33. The simulation results show that the notch is at 750 kHz (= F_{in}).

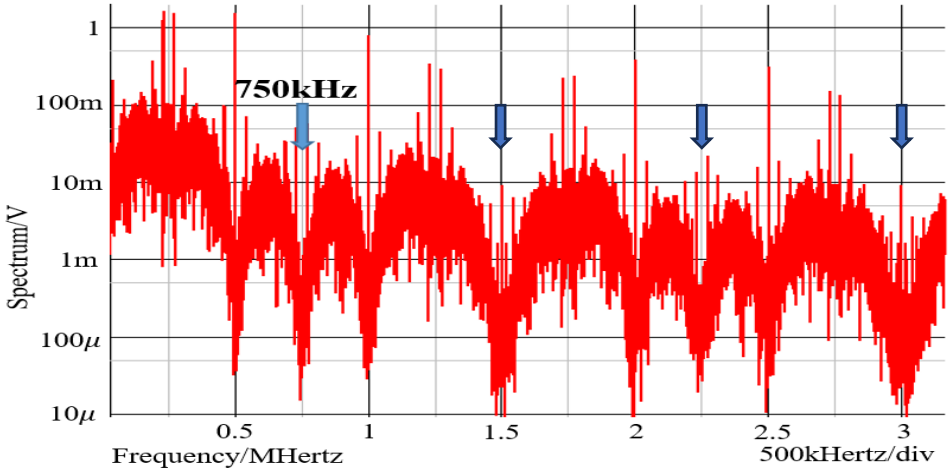

Figure 70. Simulated spectrum with automatic generation without spread spectrum.

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The SEL signal is illustrated in Figure 71. In comparison to Figure 66, under the condition of D=0.33, the waveform of W_H and W_L remains balanced. The output voltage ripple is displayed in Figure 72, that is decreased from 8.5 mV to 1.1 mV, compared with Figure 67.

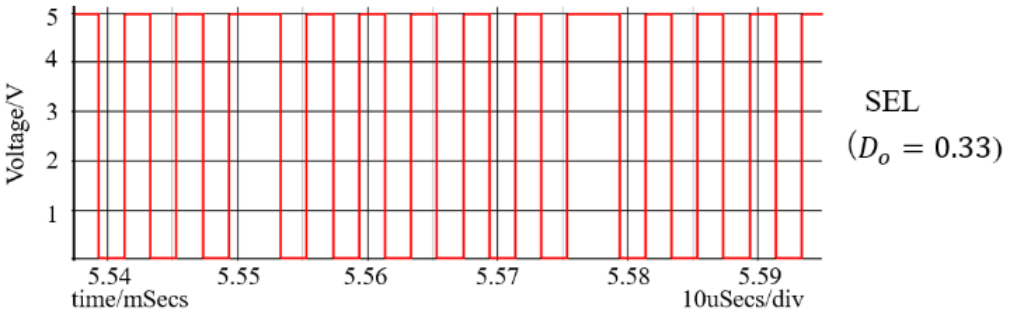

Figure 71. SEL for automatic notch generation.

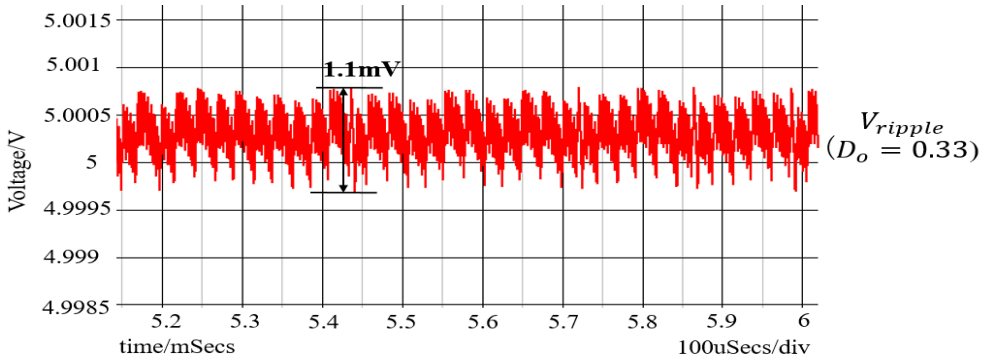

Figure 72. Output voltage ripple in automatic notch generation.

The above discussion says that for setting D ($0.33 < D < 0.67$) in automatic notch generation with the PWC control and the D automatic detection method, D is detected based on the change in V_i. This results in a notch being produced at F_{in}, while reducing ΔV_o.

6. Implementation of PWC Controlled Converter with Notch Generation

6.1. Experiment of Converter with Notch Generation

We have verified the notch frequency using the PWC control with the prototype circuit in Figure 73, with the parameters in Table 4. Figure 74 shows its implemented prototype on a PCB board.

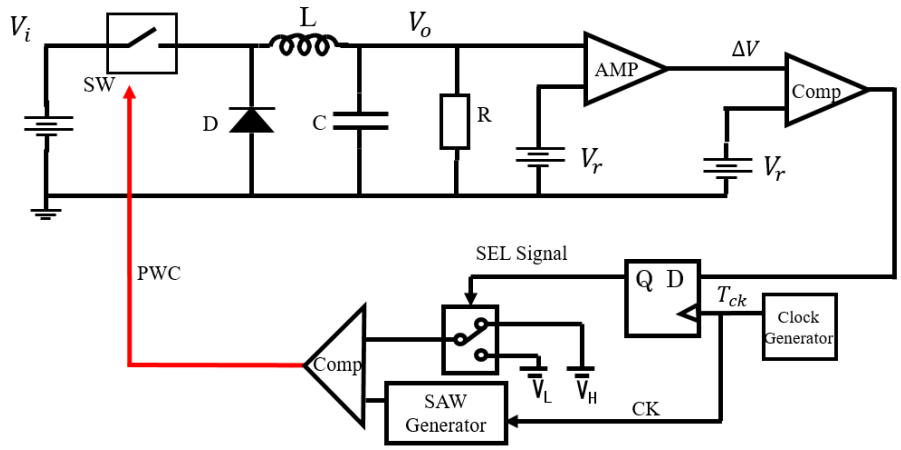

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Figure 73. Buck converter with PWC control.

Table 4. Parameter values of Figure 73.

V_i	V_o	I_o
12V	5V	0.2A
L	C	f_{clk}
100μH	47μF	500kHz

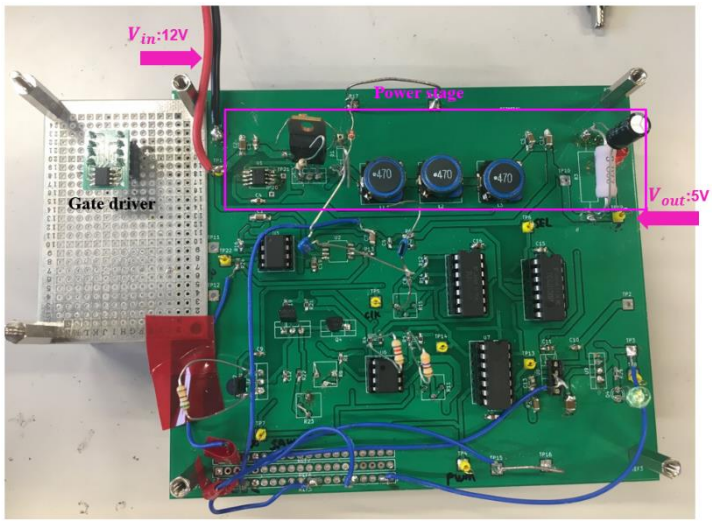

Figure 74. Prototype of PWC control buck converter.

Figure 75 shows measured waveforms of W_H and W_L. Additionally, we have analyzed the spectrum of the PWC control converter with $W_H = 1.0\mu s$ and $W_L = 0.4\mu s$ (Figure 76). The notches appear between F_{ck} and 2 F_{ck}, between 2 F_{ck} and 3 F_{ck}, and between 3 F_{ck} and 4 F_{ck}. By substituting the parameter values into Eq. (24), 1.66 MHz is obtained, which agrees with the measured result.

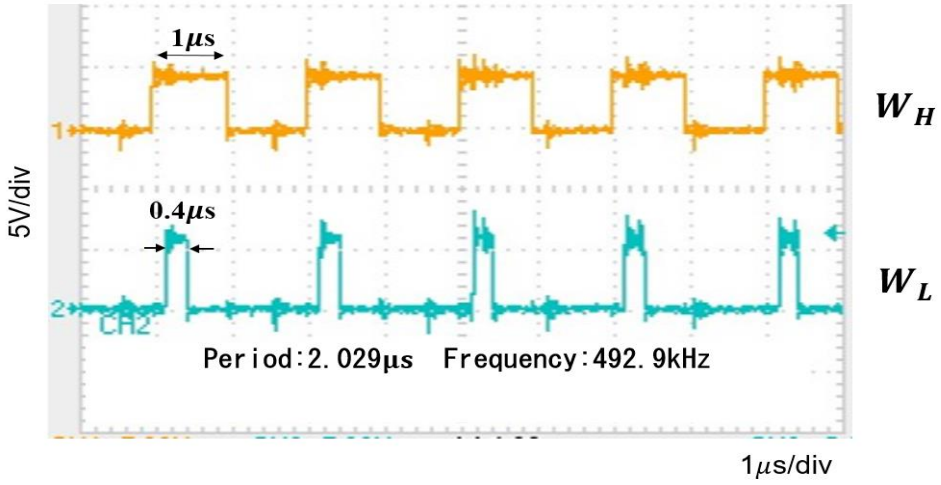

Figure 75. Measured waveforms of W_H and W_L in the PWC control converter.

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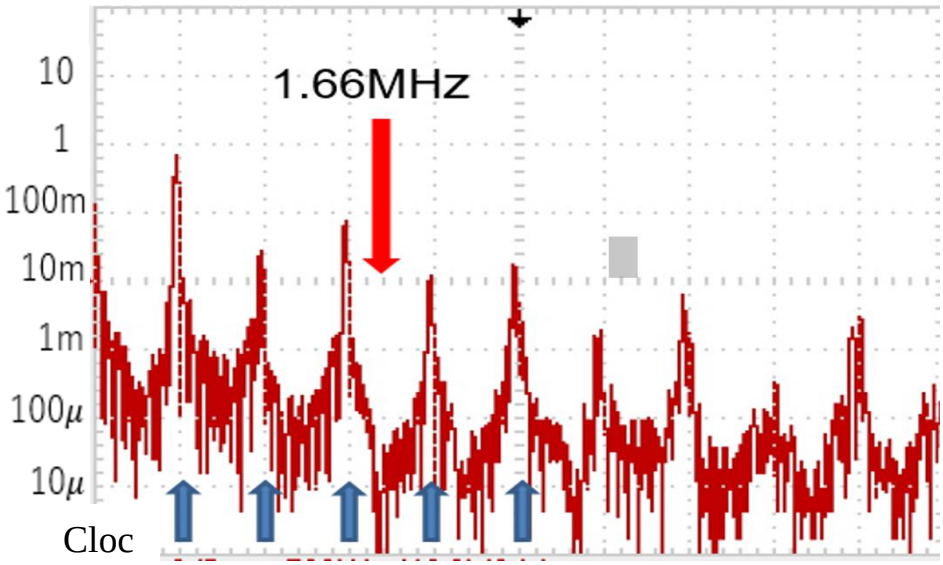

Figure 76. Measured spectrum of the PWC control converter.

6.2. Experiment of Automatic Notch Generation

Experiments examine the notch characteristics using the prototype circuit.

(A) Experiment Method of Automatic Notch Generation

In the automatic notch generation method, the control stage circuit corresponds to the one in Figure 49. We expect that by inputting F_{in} , the notch is automatically produced at F_{in}. We have $T_{ck} = 1.5T_{in}$. In 1.5 F_{in} frequency generation circuit (pink border), just the input a pulse with a period of T_{in} produces T_{ck}. The waveforms of T_{in}, T_{ck}, Q_2, and Q_R are illustrated in Figure 77. By comparing the saw-tooth waveform with T_{ck} to V_H and V_L, W_H and W_L are generated respectively.

Figure 78 shows the prototype with three red wires connecting the two boards. By inputting a pulse with a period of T_{in} using a pulse generator, a notch is produced automatically at the same frequency. Next, we evaluate the prototype circuit with the parameters in Table 5.

Table 5. Parameters of prototype.

V_i	V_o	I_o
10V	3.5V	0.16A
L	C	
141μH	570μF	

For the first example, we set P = 1 in Eq. (44), and a notch is produced between F_{ck} and 2 F_{ck}. We input F_{in}= 400 kHz, F_{ck} can be automatically about 267kHz ($T_{ck} = 3.7\mu s$) and $W_L = 0.7\mu s$ (Figure 79a). The PWM and SEL signals are shown in Figure 79b. Based on Eq. (24), the notch frequency is calculated as 435 kHz. From the experimental spectrum, the observed notch frequency is approximately 400 kHz, which closely matches the theoretical result by Eq. (24), and lies between F_{ck} and 2 F_{ck}.

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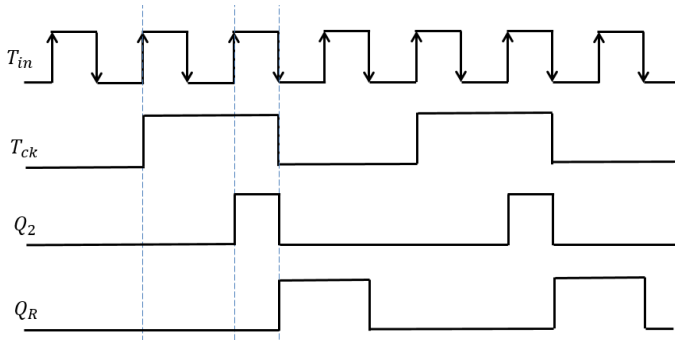

Figure 77. Signals when T_{in} produces T_{ck}.

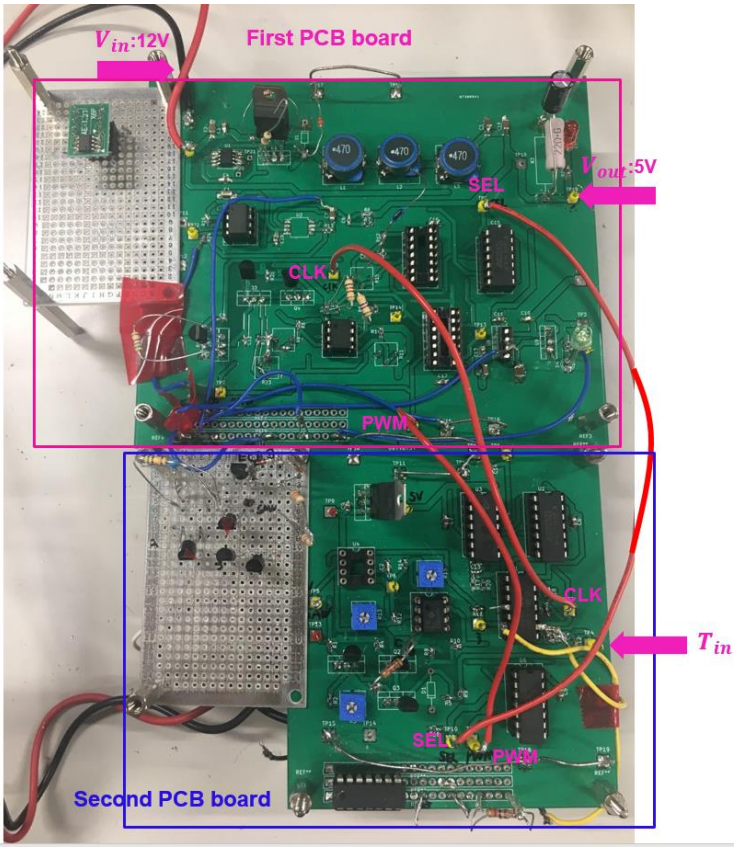

Figure 78. Prototype for automatic notch generation.

(B) Experimental Results of Automatic Notch Generation

When F_{in} is 400 kHz, F_{ck} is automatically set to 267 kHz (T_{ck} = 3.7 μs) for P=1. The pulse widths are automatically adjusted to W_H = 3.0 μs and W_L = 0.7 μs (Figure 79a). The PWM and SEL signals are illustrated in Figure 79b. F_n can be calculated as 435 kHz based on Eq. (30). The experiments show that the observed F_n is around 425 kHz (Figure 80), which matches the theoretical result in Eq. (30), and that this notch lies between F_{ck} and 2 F_{ck}.

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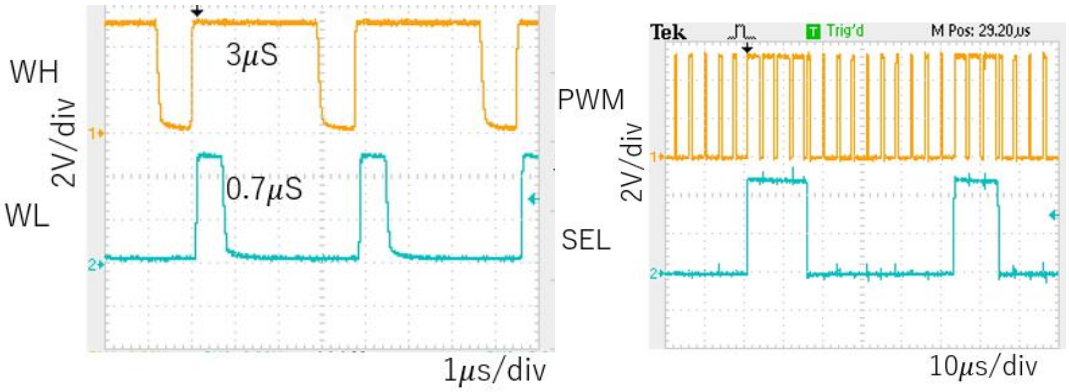


(**a**) Pulses of W_H and W_L (**b**) PWM and SEL signals

Figure 79. Measured waveforms ($F_{in} = 400kHz$).

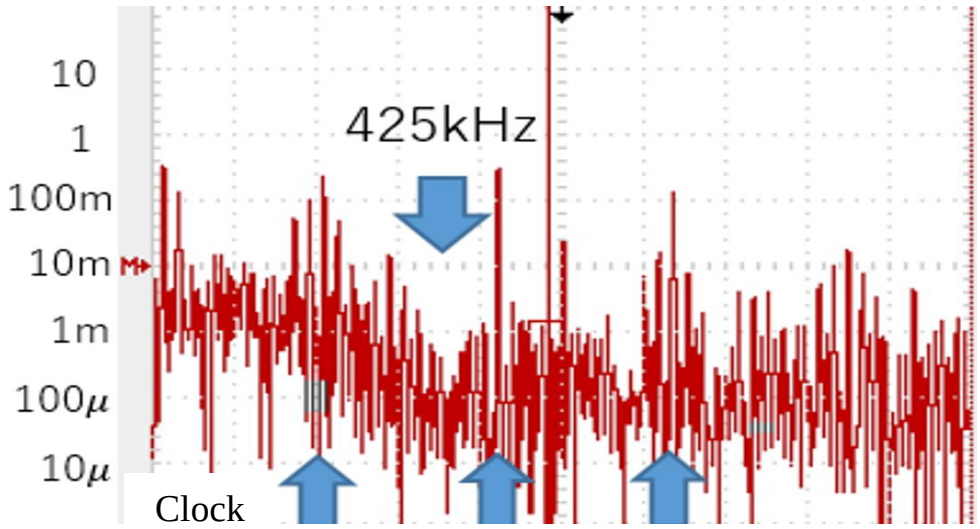
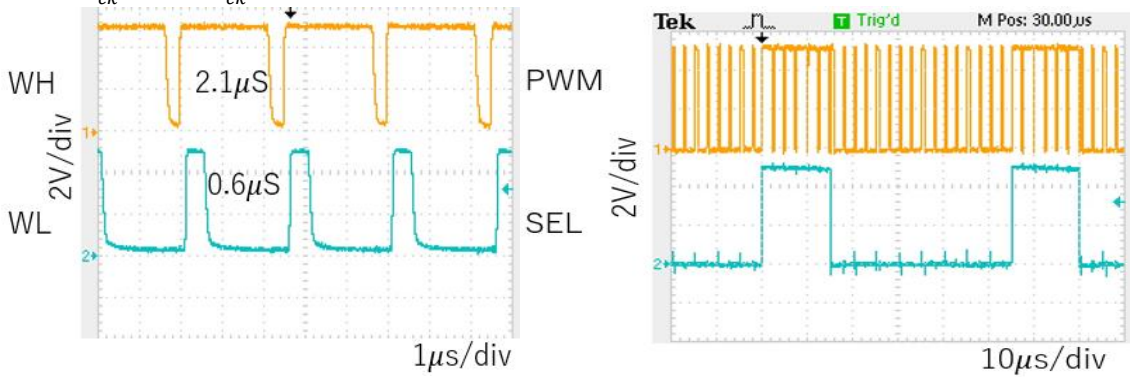


Figure 80. Measured spectrum of PWM signal ($F_{in} = 600kHz$).

For the second example, still P=1 is used. By changing F_{in} to 600 kHz, F_{ck} can be automatically adjusted to 400 kHz ($T_{ck} = 2.5\mu s$). Consequently, $W_H = 2.1\mu s$ and $W_L = 0.6\mu s$ (Figure 81a). The PWM and SEL signals are illustrated in Figure 81b. F_n is calculated as 666 kHz based on Eq. (24), and the experimental results show that the observed notch is at 666 kHz (Figure 82), which lies between F_{ck} and $2\,F_{ck}$.



(**a**) W_H and W_L pulses. (**b**) PWM and SEL signals

Figure 81. Measured waveforms ($F_{in} = 600kHz$).

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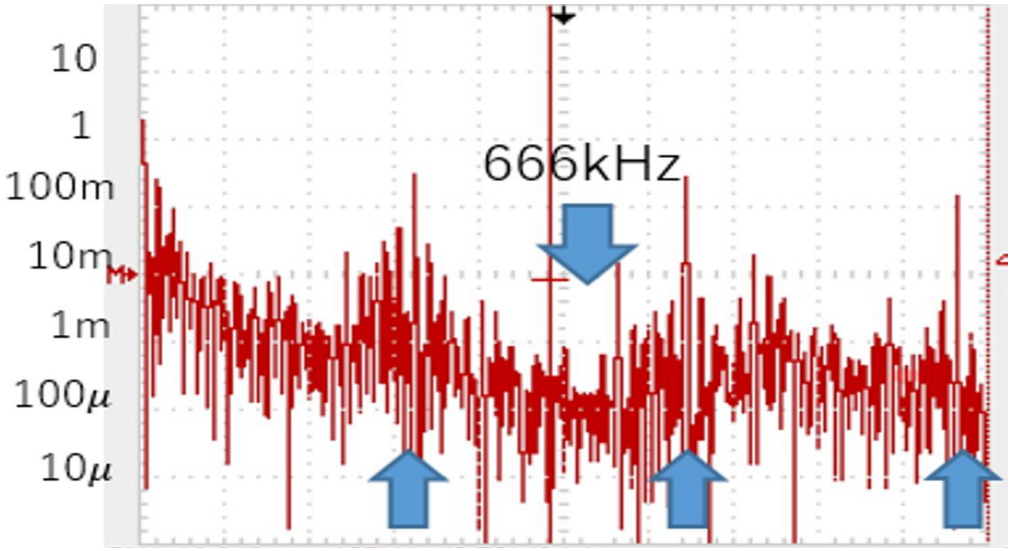

Figure 82. Measured spectrum of PWM signal ($F_{in} = 600kHz$).

7. Conclusion

This paper reviews technologies to realize the selectable band in the EMI noise spread spectrum of the DC-DC switching converter. The EMI noise is diffused from the switching signals caused by the clock, and then the noise spectrum spread techniques with the selectable notch band at the undesirable frequency such as the receiving radio signal band have been developed.

First, we review the configuration and operation of fundamental DC-DC switching converters of buck, boost and buck-boost types. They radiate some amount of EMI noise from the PWM signal with the line spectra at the frequencies of the clock and its harmonics.

Next, we introduce the conventional spread spectrum method that shakes the clock frequency and phase to reduce the line spectrum levels.

In addition to basic analog modulation methods, an analog noise generator using bit-inverse and bit-exchange in conjunction with an LFSR is explained. These spread spectrum techniques disperse noise power into unwanted frequencies. For example, in weak radio wave receivers, the dispersion of noise into the reception frequency band is undesirable.

Then we review the Pulse Coding Driving (PCD) control method, which significantly reduces the noise level at the selected frequency band. Instead of controlling the output voltage with the PWM signal, it controls the output voltage using two different pulse counts such as Pulse Width Coding (PWC) method, Pulse Phase Coding (PPC) method, Pulse Width and Phase Coding method. Also, the theoretical derivation of the notch frequencies is shown. The PCD control can be used in conjunction with the PWM control.

Further, a PCD control method that automatically tracks changes in the receiving frequency and the input voltage is introduced. The receiving frequency is often switched in the radio receiver and the input frequency fluctuates. There, the notch band characteristics need to automatically switch to another reception band. We explain a method to detect the received frequency and automatically switch the clock frequency to the proper one, as well as a method so that for the input voltage change, the PCD control automatically sets two types of pulse counts, while the conventional method automatically controls the duty of the PWM signal.

Finally, we review a PWC control method for automatic notch generation, with the notch characteristics of two types of PCD pulses and their spectra. There the PCD pulses and the switching of notch frequencies are changed when the reception frequency is switched.

The expansion to the FM and higher frequency bands for the notch and the application to single-inductor multi-output converters [29–32] are anticipated to be future challenges.

 doi:10.20944/preprints202503.1526.v1

Acknowledgments: All members and research collaborators in our laboratory who contributed to the research described in this paper are acknowledged.

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