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Article

A New Simulation Method to Assess Temperature and Radiation Effects on SiC Resonant-Converter Reliability

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Abstract

Silicon carbide (SiC) power converters are increasingly used in automotive, renewable energy, and industrial applications. While reliability assessments are typically performed at either the device or system level, an integrative approach that simultaneously evaluates both levels remains underexplored. This article presents a novel system-level simulation method with two strategies to evaluate the reliability of power devices and a resonant converter under varying temperatures and total ionizing doses (TIDs). Temperature sensitive electrical parameters (TSEPs), such as on-state resistance (R_{ON}) and threshold voltage shift (ΔV_{TH}), are calibrated and analyzed using a B1505A curve tracer. These parameters are incorporated into the system-level simulation of a 300 W resonant converter with a boosting cell. Both Silicon (Si) and SiC-based power resonant converters are assessed for power application in space engineering and harsh environments. Additionally, gate oxide degradation and ΔV_{TH} -related issues are discussed based on the simulation results. The thermal-strategy results indicate that SiC MOSFETs maintain more stable conduction loss at elevated temperatures, exhibiting higher reliability due to their high thermal conductivity. Conversely, increased TIDs result in a negative shift in conduction losses across all SiC devices under the radiation strategy, affecting the long-term reliability of the power converter.

Keywords: reliability; on-state resistance; threshold voltage shift; gate oxide degradation; total ionizing dose; silicon carbide devices; temperature-sensitive electrical parameters (TSEPs); total ionizing doses (TIDs)

1. Introduction

Wide bandgap (WBG) devices are extensively used in power electronics, particularly in automotive and renewable-energy applications. Over the past decade, DC-DC power converters have gained significant attention due to their expanding role across sectors ranging from aerospace to renewable energy. In renewable energy systems, especially grid-tied photovoltaic applications galvanically isolated, unidirectional LLC resonant converters have become common and the focus of numerous studies [1]. Efforts in low-voltage power converters have concentrated on improving key characteristics such as reliability, wide input and load ranges, low electromagnetic interference (EMI), and high efficiency. According to Parvez, Mohammad, *et al.* [2], isolated resonant converters can be broadly classified into three types: resonant-boost converters, hybrid resonant converters, and resonant single-ended primary-inductor converters (SEPIC). Resonant-boost converters are commonly employed in solar-energy systems to accommodate fluctuations in solar input. Recent advancements have introduced hybrid resonant converters with improved rectifier cells, offering a broad input-voltage range and California Energy Commission (CEC) efficiencies exceeding 96% [3–7]. These topologies are designed

to minimize component counts in rectifier tanks and extend the regulation range, as shown in Figure 1. For example, a resonant-boost converter with a simplified boosting rectifier cell has been proposed [7]. While this design reduces voltage stress on the resonant capacitor by clamping it at the output-voltage level, it does not fully accommodate variations in input voltage and output power. Although this topology has a limited input-voltage regulation range due to high step-up ratios and load currents [8], it remains valuable for studying the switching performance and reliability of modern power devices.

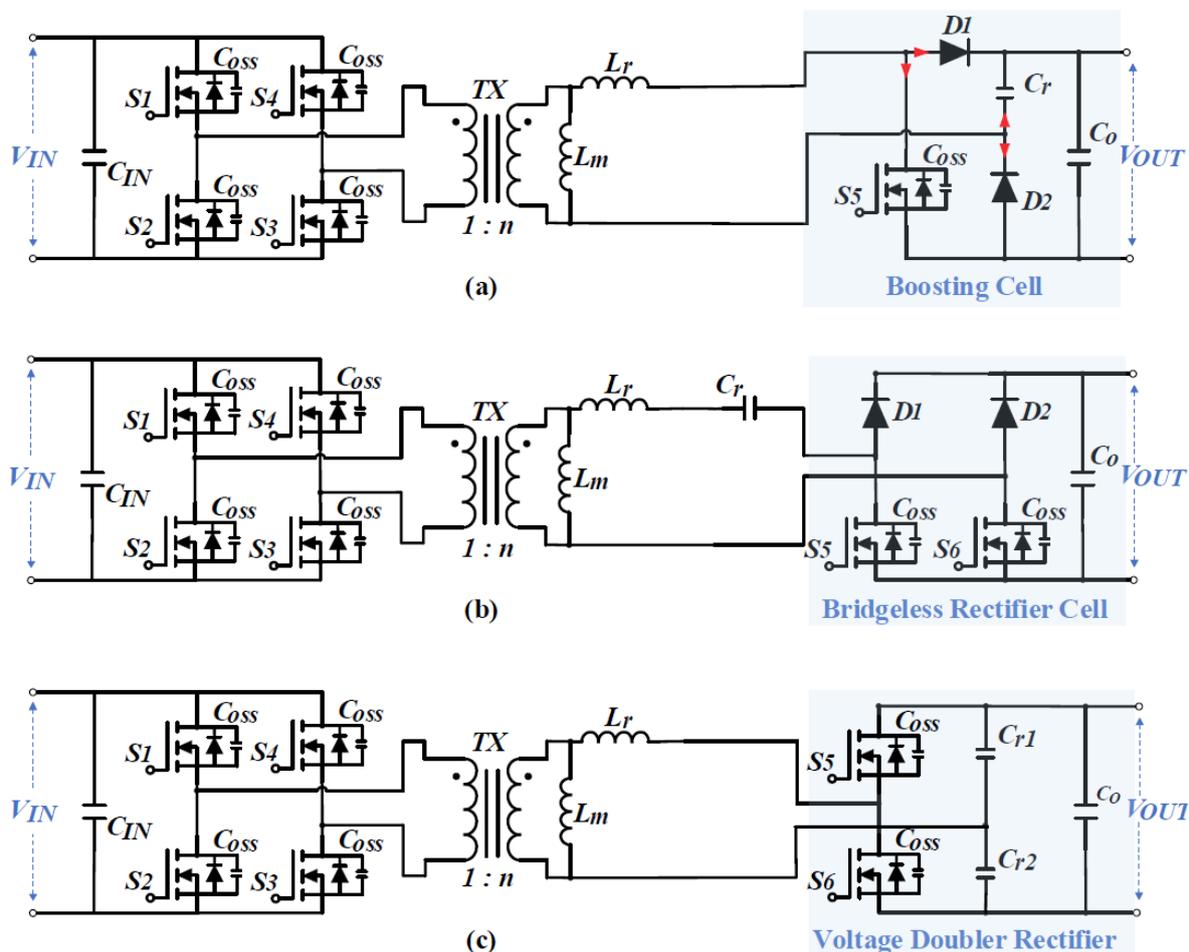


Figure 1. Three types of resonant converters with a boost rectifier cell: (a) boosting rectifier cell with only one switch and two diodes [7] (b) bridgeless rectifier cell with two switches and two diodes [4] (c) voltage doubler with two switches [5].

Recently, SiC power devices degradation has been extensively discussed at the device level under harsh environments such as high temperature and radiation [10–12,24]. However, the reliability of power converters, especially under high radiation doses, remains underexplored. Existing reliability assessments for power converters mostly rely on experimental testing, which is costly and case-specific. Thus, the development of system-level evaluation frameworks that explicitly incorporate device degradation is needed. Although several simulation-based SiC DC-DC converters have been designed and evaluated using PSIM manufacturer simulation tool [13–15,23]. While these studies analyze power losses and overall efficiency, they lack in-depth analysis of device reliability and do not fully leverage the simulation tool's capabilities. For system-level simulation of power converters, physics-based models often suffer from convergence issues and long runtime [17–19], whereas simplified models in simulation tools such as PSIM or PLECS sacrifice accuracy. To achieve both computational efficiency and degradation-aware modeling, a methodology that explicitly incorporates degradation effects in SiC power MOSFETs is required.

In this study, a novel simulation framework to model thermal and radiation induced degradation and quantify its impact on power converter efficiency. This approach facilitates extensive research without being constrained by datasheet limitation. Also, these two strategies offer a convenient approach for researchers and application engineers to evaluate the reliability of power converters under harsh environment conditions before conducting experiments. For comparison, both Si and SiC-based resonant converters with a boost cell are evaluated in PSIM. In addition, the results show that SiC-based converters are more reliable than their Si-based counterparts in harsh environments.

2. New Proposed Simulation Methodology

2.1. PSIM Thermal Model

Dynamic simulation in complex converter topologies remains a challenge for achieving a balance between accuracy, convergence reliability and simulation speed [20]. For new design topologies, the ideal models are first employed to verify the feasibility of the topology and its control scheme. Additionally, the thermal model can be employed to estimate switching losses and conduction losses in power devices. In PSIM, dedicated thermal models idealize switching transitions and evaluate losses using lookup tables. The parameters for the look-up table used in this work are shown in Table 1. The calculations in the PSIM simulation can account various conditions, such as the conducted voltage and current across the switch, junction temperature and gate drive voltage, and physic parameters such as parasitic capacitance and R_{ON} . It provides a good correlation with actual power losses while significantly reducing the computational time compared to the SPICE model. Although the present thermal model does not account for device degradation, degradation-aware device models can be incorporated in the future to enable system-level performance analysis. From both reliability and lifetime perspectives [21,22], this integration offers clear benefits. It enables more predictive loss and stress estimation and reduces reliance on costly long-duration experiments.

Table 1. Critical parameters in PSIM thermal model.

Part number	C3M0015065K	C3M012090D	FDMS86200
Material	SiC	SiC	Si
R_{ON} (m Ω)	15	120	15
V_{DS} (V)	650	900	150
V_{TH} (V)	2.3	2.1	2.5
Q_g (nC)	188	21	33
Q_{rr} (nC)	432	127	113
C_{iss} (pF)	5011	414	2041

In PSIM, the calculation of conduction losses (P_{cond}) and on/off switching losses ($P_{sw,on/off}$) is given by [23]:

$$P_{cond} = I_{RMS}^2 R_{ON} \quad (1)$$

$$P_{sw,on/off} = E_{on/off} f_{sw} \quad (2)$$

where, I_{RMS} is the root-mean-square value of the conducted current (obtained from the switching waveform), and R_{ON} which depends on the junction temperature T_j . R_{ON} can be expressed as:

$$R_{ON} = R_{ON, Norm} [1 + K_T (T_j - 25^\circ\text{C})] \quad (3)$$

where $R_{ON, Norm}$ is the normalized on-state resistance at 25°C (from the data-sheet's normalized R_{ON} versus temperature curve) and K_T is the corresponding temperature coefficient. However, in the thermal strategy, K_T is not applied in the simulation, because the actual R_{ON} is obtained directly using a curve tracer. The junction temperature is fixed at 25°C, so the measured R_{ON} and V_{TH} from [Figure 5](#) can be used in the thermal model without calculating K_T , providing a flexible and practical solution for system evaluation.

2.2. A New Simulation Method

A newly proposed simulation method to assess the efficiency and reliability of DC-DC resonant converter includes two strategies: (a) Thermal Simulation and (b) Radiation Simulation, illustrated in Figure 2. Both simulations utilize the PSIM simulation tool and its thermal model. In this paper, SiC-based resonant converter is evaluated under a wide-range temperature and radiation doses conditions. The conventional simulation approach employs a thermal model to estimate the switching and conduction losses for each device in the system. This model is based on datasheet characteristics, which can limit the exploration and evaluation of device performance in system-level analysis, especially for scenarios such as a resonant converter operating at high temperatures exceeding 175 °C.

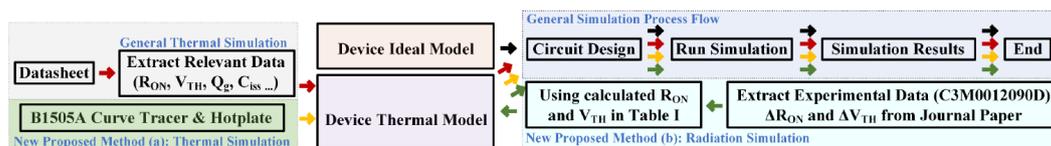


Figure 2. Proposed simulation methodology with two strategies: thermal simulation and radiation simulation.

To analyze the performance and degradation of SiC devices in a resonant tank, a simulation method is illustrated in Figure 2. This method includes two key strategies:

1. **Thermal Strategy:** This involves calibrating the power device using the B1505A curve tracer, with the device placed on a hot plate for high-temperature testing. The resulting characteristics, typically not provided in the datasheet, are then applied in thermal simulation using a system-level simulation tool.
2. **Radiation Strategy:** This utilizes relevant data, specifically the changes in ΔR_{ON} and ΔV_{TH} , from the article [24] on the commercial SiC power device (C3M0012090D) under investigation. The R_{ON} and V_{TH} values calculated at various total ionizing doses (TIDs), as shown in Table 2, are then integrated into the PSIM thermal model.

Table 2. Calculated R_{ON} and V_{TH} .

TID (dose/krad)	ΔR_{ON} (m Ω)	11.1		R_{ON} (m Ω)	V_{TH} (V)
		ΔV_{TH} (V)			
100	-2.01	-0.24		117.99	1.86
200	-2.21	-0.33		117.79	1.77
300	-4.52	-0.56		115.48	1.54
400	-6.02	-0.71		113.98	1.39
500	-7.44	-0.99		112.56	1.11

Thus, both thermal and radiation strategies offer valuable benefits for researchers engaged in extensive studies. While this work focuses on analyzing only the R_{ON} and V_{TH} parameters at the device level, other parameters listed in Table 1 can also be modified and examined. This approach enables device-level degradation insights to be extended to system-level analysis. Although current system-level simulators are limited and power loss remains the principal observable of converter after device degradation, the framework developed here is readily extensible. The present method cannot yet resolve degradation effects at the control-waveform level. In the future, degradation-aware device models could relate device degradation to system-level dynamics, for example by accounting for BTI (Bias Temperature Instability)-induced shifts in the gate plateau that delay rising and falling edges, and threshold voltage variation that affects the voltage slew rate [25–27]. In subsequent studies, false turn-on events could become observable under high slew-rate and crosstalk conditions, especially in the presence of both aging-induced and radiation-induced threshold shifts.

2.3. Device Calibration

This study examines two commercial devices, a Si MOSFET (FDMS86200) and a SiC MOSFET (C3M0015065K), each with a typical R_{ON} of 15 m Ω . Table 1 summarizes the key device parameters, and Figure 3 compares their dynamic performance and figure of merit (FOM). To address potential discrepancies between datasheet transfer characteristics and actual device behavior, the B1505A curve tracer was used for precise measurement of R_{ON} and V_{TH} . The combination of an extended printed circuit board (PCB) and hot plate to control the junction temperature is illustrated in Figure 4. During testing, the device under test (DUT) was placed on a hot plate for 15 minutes to allow the junction temperature to stabilize at the target level. Also, other quasi-static parameters can be characterized as a function of temperature using the same set-up, enabling quantitative assessment of temperature-accelerated degradation.

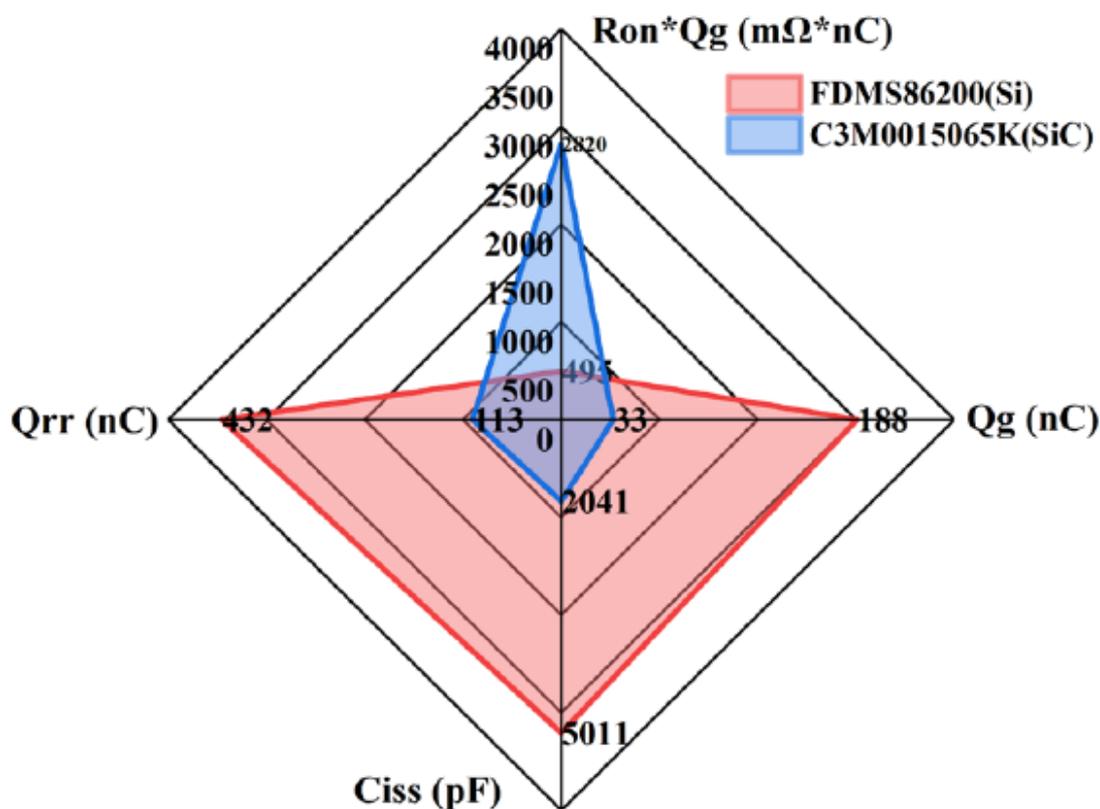


Figure 3. Proposed simulation methodology with two strategies: thermal simulation and radiation simulation.

The methodology for extracting R_{ON} and V_{TH} , as described in [28], was applied at different temperatures in this work with the results shown in Figure 5. The SiC MOSFET exhibited less variation in R_{ON} compared to the Si MOSFETs, which can be attributed to the thermal conductivity of the SiC. In fact, it is worth noting that the radiation strategy also employs the B1505A for device calibration prior to irradiation [24]. Moreover, a measurement setup similar to the temperature-accelerated degradation calibration can be used to characterize total ionizing dose (TID) effects, enabling assessment of both static and dynamic degradation [29].

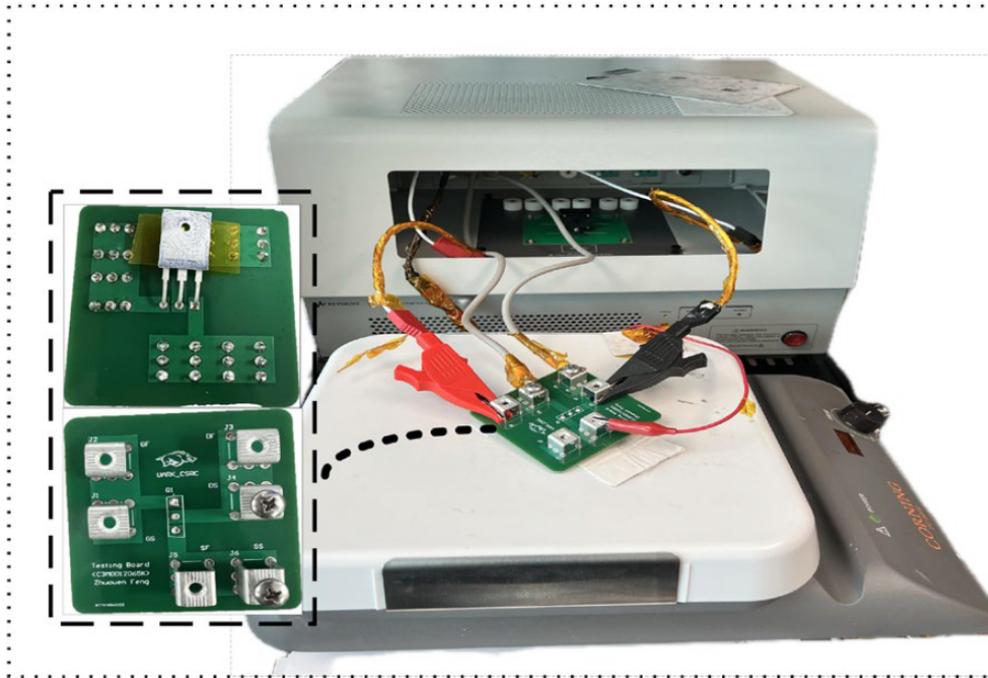


Figure 4. Proposed simulation methodology with two strategies: thermal simulation and radiation simulation.

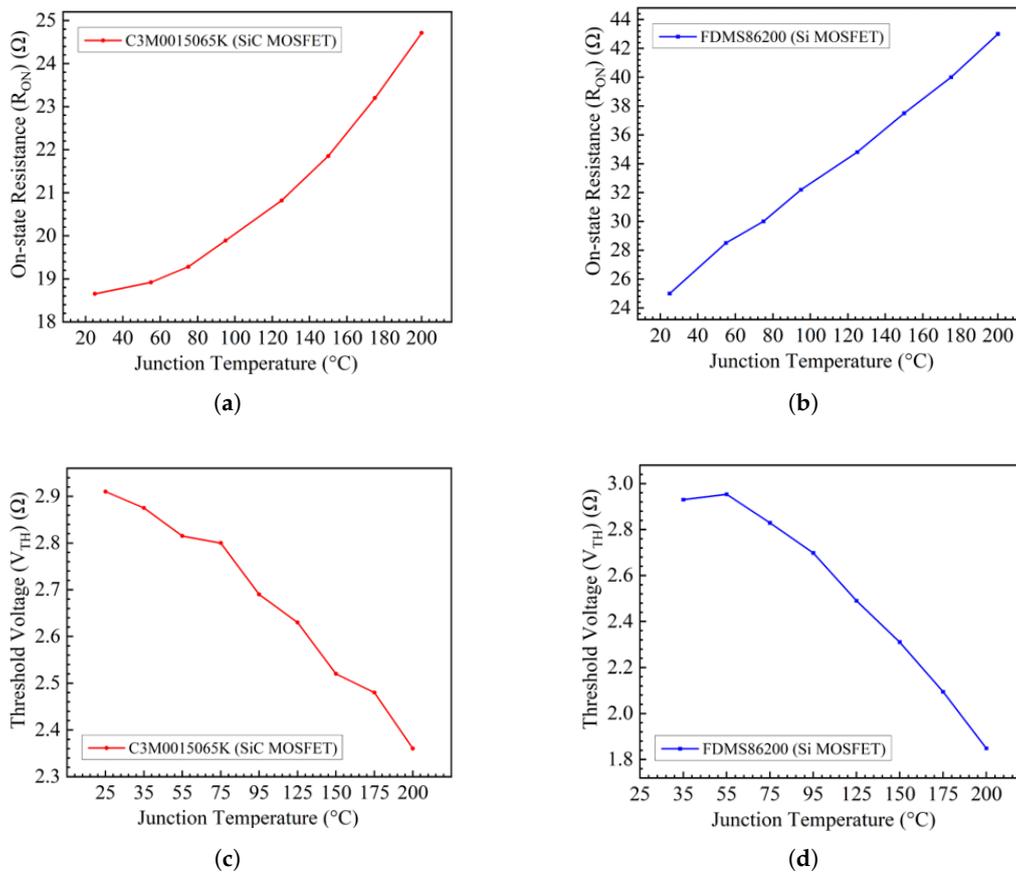


Figure 5. (a) SiC MOSFET (C3M0015065K) junction temperature vs. R_{ON} ; (b) Si MOSFET (FDMS86200) junction temperature vs. R_{ON} ; (c) SiC MOSFET (C3M0015065K) junction temperature vs. V_{TH} ; (d) Si MOSFET (FDMS86200) junction temperature vs. V_{TH} .

2.4. Radiation Simulation

In radiation strategy, experimental data is extracted and calculated from [24] due to the lack of a radiation source. This approach provides valuable insights for application engineers to analyze device performance in harsh environments, which is discussed in detail below.

2.4.1. Physical Mechanism of SiC MOSFET Degradation

As previously mentioned, the R_{ON} of SiC MOSFETs mainly depends on channel resistance, which is influenced by mobility and V_{TH} . When a SiC MOSFET is exposed to gamma radiation, electron-hole pairs are generated in the gate oxide. Due to their high mobility, electrons are more likely to escape from the gate oxide, while holes become trapped within the gate oxide, leading to an accumulation of negative charges at the SiO_2/SiC interface. Thus, the accumulation of oxide trap charges following irradiation leads to greater inversion in the NMOS channel and a negative shift in threshold voltage. The mechanism of threshold voltage degradation in SiC MOSFETs is illustrated in Figure 6.

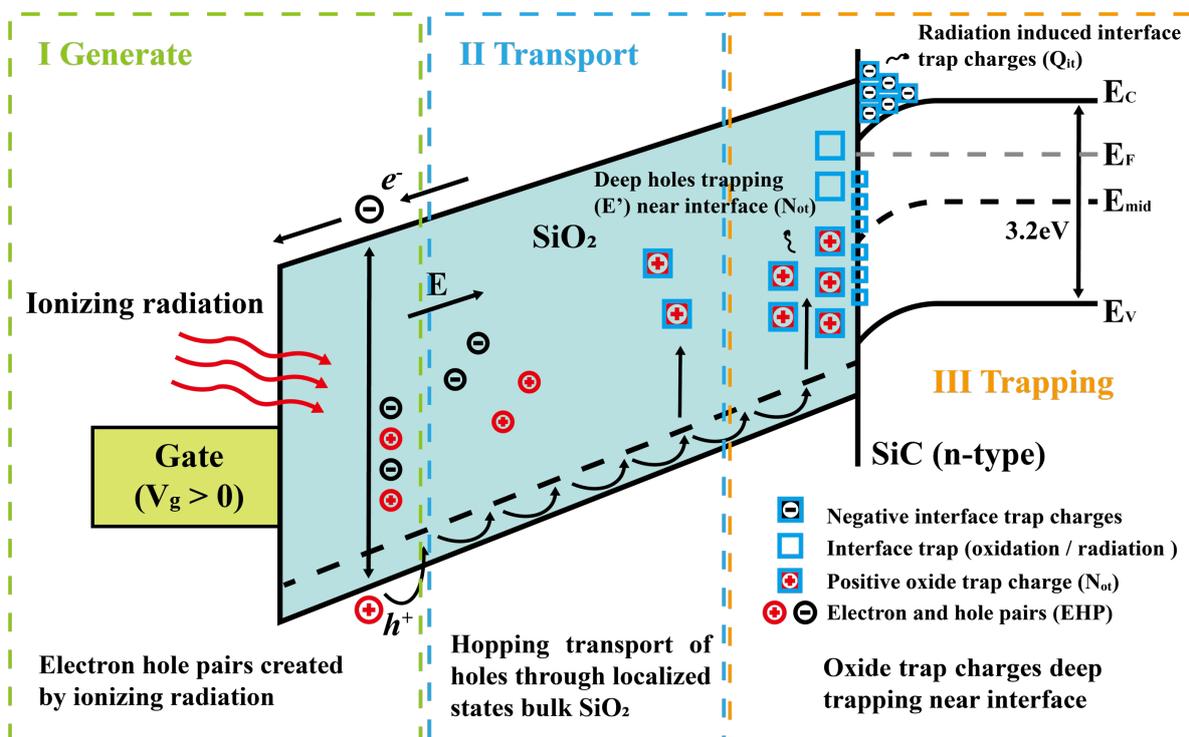


Figure 6. Energy Band Diagram of Radiation-Induced Charge Dynamics in the SiO_2/SiC System under positive gate bias.

To describe the TID irradiation-induced degradation of V_{TH} , a model derived by [24] can be applied:

$$\Delta V_{TH} = -\frac{qN_h T_{ox}^2 f(t)}{\epsilon_{ox}} \times f(E) \times Dose \quad (4)$$

where q is the elementary charge, N_h is the number of generated electron-hole pairs, T_{ox} is the gate oxide thickness, $f(t)$ is the fraction of positive oxide trap charges, ϵ_{ox} is the dielectric constant of oxide, $f(E)$ is the hole yield as a function of electric field and $Dose$ is the total ionizing dose in rads.

Under different bias conditions, the trapping effect results in varying degradation behavior due to the electric field. When the MOSFET is on, it operates under gate bias condition; when off, it operates under drain bias. Under gate bias, a high positive electric field is applied in the gate oxide above the channel region, while under drain bias, a comparatively lower negative electric field is present above the near-channel region. As a result, SiC MOSFETs exhibit greater sensitivity to gate bias during γ -ray irradiation, particularly in terms of changes in V_{TH} and R_{ON} . In the simulation, SiC MOSFETs

(C3M012090D) are used in [24]. The extracted ΔR_{ON} and ΔV_{TH} under gate bias, as shown in Table 2, are applied in the simulation.

In Equation (4), ΔV_{TH} is proportional to the TIDs, the electric field in the gate oxide, and the oxide thickness. Given that the oxide layer in SiC MOSFETs is typically thicker than 45 nm, electrons have sufficient space to accelerate under the electric field, gaining more than 8.9 eV of energy. This energy allows them to collide with SiO₂ lattice atoms, generating electron–hole pairs [30]. Due to the oxide thickness, V_{TH} variation in planar SiC MOSFET is significantly smaller than in trench SiC MOSFETs at higher dose levels [31,32]. However, limited research compares planar gate and split-gate MOSFETs under high radiation doses. Based on Equation (4), it can be inferred that the V_{TH} variation in split-gate MOSFETs might be significantly smaller than that in planar MOSFETs, as the electric field in the gate oxide is much lower in split-gate designs.

2.4.2. Threshold Voltage Shift Induced by Oxide Traps

The V_{TH} of SiC MOSFETs can be affected by radiation-induced oxide traps. The sensitivity of V_{TH} depends on TIDs, and the electric field generated by trapped hole. In the experiment [24], a negative shift of V_{TH} and R_{ON} was observed under γ -ray irradiation. For worst-case assessment, the V_{TH} shift caused by radiation-induced trapped charges should be evaluated together with the V_{TH} shift induced by high-temperature gate bias (HTGB) under negative gate bias [33].

When HTGB and TIDs are simultaneously applied, Zhang et al. [34] observed a substantial shift in V_{TH} . Therefore, although the R_{ON} decreases under TIDs, the overall power consumption of power devices in harsh environment (with both high temperature and high radiation doses) increases, potentially reducing the efficiency of power applications. Unfortunately, limited research addressed the performance of power devices in application level under harsh environments, including online R_{ON} measurements. Consequently, by experimentally characterizing parameter drifts under concurrent BTI and TID and integrating the extracted models into the proposed framework, the system-level impact on efficiency can be evaluated by using the proposed method.

3. Isolated Series Resonant Converter

In this paper, a galvanically isolated series resonant converter (SRC) topology is selected and designed. A brief introduction to the resonant converter is provided below.

3.1. Resonant Boost Converter Topology

The converter features a front-end full bridge and a boosting cell, connected through a galvanically isolated transformer [7]. It offers significant advantages including reduced stress on the resonant capacitor, which regulates the output voltage, as well as a lower component count compared to the topologies in Figure 1. The proposed converter can operate in four distinct modes, all based on discontinuous resonant current with a quality factor of less than one, irrespective of load conditions. The pure-SRC mode is employed solely in the simulation. The prototype developed for this study has a power rating of 300 W and achieves an output voltage of 355 V.

As a wide-input-range DC–DC resonant converter, this type is particularly suited for solar applications, especially in space solar applications. Therefore, it is essential to evaluate the performance of the converter in harsh environments, such as high temperature and high radiation doses. In this paper, two strategies are proposed and implemented to simulate the power losses of the converter under these extreme conditions.

3.2. Zero Voltage Switching

To minimize turn-on switching losses, zero-voltage switching (ZVS) has been implemented in this topology. As a result, turn-on switching loss is negligible, and the turn-off loss is determined by the fall time. The turn-off voltage slew rate of the device is influenced by the gate-drive circuit design.

In the front-end full bridge, the transformer's magnetizing inductance (L_m) serves as the current source during dead time. Thus, the magnetizing inductance should be designed such that the mag-

netizing current can fully charge and discharge the parasitic output capacitance of S1–S4, facilitating ZVS [7]. Figure 7 shows the drain–source voltage (V_{DS}) and drain current of S1 over one period, clearly demonstrating ZVS in this design. However, it is important that the magnetizing inductance of the transformer be designed according to the following criterion:

$$L_m \leq \frac{n^2 T_{DT}}{8 f_{sw} C_{OSS}}, \quad (5)$$

where n is the transformer turns ratio, T_{DT} is the dead time in the primary-side gate signals, f_{sw} is the switching frequency of the power devices, and C_{OSS} is the parasitic output capacitance of the front-end full-bridge switches.

When designing a resonant converter, it is crucial to account for the switch parasitic. In addition to the output capacitance, parameters such as gate charge and the dynamic characteristics of the body diode must align with the circuit design. The proposed strategy provides an effective approach for analyzing how these device parameters interact with the circuit, thereby ensuring optimal performance.

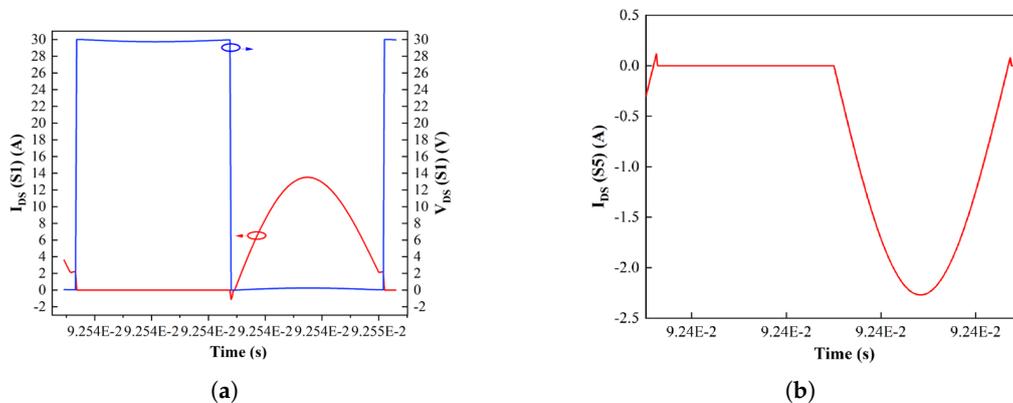


Figure 7. (a) V_{DS} (green) and I_D (red) of S1 showing the implementation of ZVS during dead time; (b) drain current I_D of S5 showing the implementation of ZCS during dead time.

4. Simulation Results and Reliability Analysis

4.1. Temperature-Sensitive Electrical Parameters (TSEPs)

Due to their excellent material characteristics, SiC MOSFETs can operate at extremely high temperatures and are suitable for harsh-environment applications. Various TSEPs of SiC MOSFETs, such as on-state resistance (R_{ON}) and threshold voltage (V_{TH}), should be analyzed.

4.1.1. On-State Resistance (R_{ON})

Gate-oxide degradation and total R_{ON} are critical aging indicators for SiC MOSFETs. In both typical planar MOSFET and trench MOSFET shown in Figure 1, the total R_{ON} is obtained by summing the individual resistances of each layer and region, which can be represented as:

$$R_{ON} = R_{CH} + R_{JFET} + R_A + R_D + R_{N^+} + R_{SUB} + R_{CS} + R_{CD}. \quad (6)$$

Here, R_{CH} is the channel resistance, R_{N^+} is the source region resistance, R_{JFET} is the resistance of the JFET region (Junction Field-Effect Transistor), and R_A , R_D , and R_{SUB} represent the accumulation resistance, the resistance of the drift region, and the N^+ substrate resistance, respectively. R_{CS} is the source contact resistance, while R_{CD} is the drain contact resistance. However, the dominant contributors to R_{ON} is different between Si MOSFETs and SiC MOSFETs (1.2 kV planar MOSFET). In Si MOSFETs, R_{JFET} and R_D are the primary contributors due to lower breakdown electric-field strength and thicker drift layer. In contrast, R_{CH} is a major contributor to R_{ON} in SiC MOSFETs because of lower inversion carrier mobility at the SiO_2/SiC interface [35,36]. Therefore, excluding the R_{CH} , the

rest of the resistances can be defined as the residual resistance (R_S). The total R_{ON} is the sum of the R_{CH} and R_S , where the contribution of channel resistance R_{CH} is given by [37]:

$$R_{CH} = \frac{L_{CH} P}{\mu_{inv} C_{OX} (V_G - V_{TH})}, \quad (7)$$

where L_{CH} is the channel length, P is the pitch of the MOSFET elementary cell, μ_{inv} is the electron mobility in the inversion layer, C_{OX} is the specific gate-oxide capacitance, V_G is the applied gate voltage, and V_{TH} is the threshold voltage.

In [38], it is noted that R_{JFET} and R_D exhibit a positive temperature coefficient (PTC), while R_{CH} displays a negative temperature coefficient (NTC). As previously discussed, R_{CH} is the primary contributor to R_{ON} in SiC MOSFETs. Thus, the temperature sensitivity of R_{CH} in SiC MOSFETs is less significant than in Si MOSFETs as illustrated in Figure 5. The normalized R_{ON} of the SiC MOSFET shows smaller change than that of the Si MOSFET as the junction temperature increases. Although R_{CH} has an NTC characteristic, the total R_{ON} still increases with rising junction temperature due to R_S , which exhibits a PTC [36,42]. As a result, the overall R_{ON} of SiC MOSFET remains PTC. Nevertheless, the stability of R_{ON} in SiC MOSFETs is superior to that of Si MOSFETs under varying temperatures. At a high temperature up to 375 °C, R_{CH} no longer dominates R_{ON} ; instead, R_D and R_{JFET} in R_S become more influential as the temperature increases [40].

4.1.2. Threshold Voltage (V_{TH})

As discussed in Section II, V_{TH} is a radiation-sensitive parameter that tends to shift negatively during gamma-ray radiation. However, it is also sensitive to temperature changes. The threshold voltage of the SiC MOSFET can be expressed as follows [40]:

$$V_{TH} = V_{FB} + 2\Psi_B + \frac{1}{C_{OX}} \left(\sqrt{2\varepsilon_s q N_A (2\Psi_B)} + q \int_{E_i}^{E_i + \Psi_B} D_{it}(E) dE \right) \quad (8)$$

where ε_s is the dielectric constant of SiC, q is the electronic charge, N_A is the doping concentration of the P-base region, V_{FB} is the flat-band voltage, Ψ_B is the Fermi potential from the substrate, and D_{it} is the interface state density. Notably, the commercial devices chosen from CREE have shown improvements in the SiO₂/SiC interface [41]. With the reduction of near-interface traps (NITs), the stability of V_{TH} performs well under high temperatures. The rate of variation of V_{TH} with temperature can be expressed as follows [42]:

$$\frac{dV_{TH}}{dT} = \frac{d\Phi_{ms}}{dT} + \frac{d\Psi_B}{dT} \left(2 + \frac{1}{C_{OX}} \sqrt{\frac{\varepsilon_s q N_A}{\Psi_B}} \right) + \frac{q}{C_{OX}} \frac{dN_{it}}{dT} \quad (9)$$

where T is temperature, Φ_{ms} is the work function difference between the metal and the semiconductor at the gate and substrate, and N_{it} is the number of traps between the neutral level and the conduction band. The temperature dependence of V_{TH} is determined by the Ψ_B , Φ_{ms} and N_{it} . Specifically, Ψ_B decreases with increasing temperature due to the rise of intrinsic carrier concentration. Additionally, N_{it} also decreases with temperature as the Fermi level energy (E_f) shifts toward the mid-gap, which reduces the occupancy of electrons in the interface traps. In general, the V_{TH} of SiC MOSFETs shows a negative shift characteristic as the temperature increases.

4.2. Thermal Simulation Results

It is important to note that the switching loss for each MOSFET is only an estimate. In the simulation, both the external turn-on and turn-off resistances are set to 1 Ω , with other parameters shown in Table II, which correspond to the switching loss in PSIM thermal model as discussed in Section II.

In the thermal strategy, the conduction losses of power devices in the front-end full bridge are primarily analyzed to compare the power consumption stability between Si and SiC MOSFETs, which can affect the power converter reliability. As shown in Figure 8, the change in total power conduction

losses for SiC MOSFETs is less pronounced than for Si MOSFETs as temperature increases. At a 40.8% load ($R_{load} = 1 \text{ k}\Omega$), the variation in R_{ON} for SiC MOSFETs is only 26%, compared to a significantly higher 67.7% for Si MOSFETs. Similarly, at an 81% load ($R_{load} = 500 \Omega$), the variation in R_{ON} for SiC MOSFETs is just 21%, while for Si MOSFETs, it remains significantly higher at 67%.

In summary, the power loss stability of the Si-based resonant converter is lower than that of the SiC-based resonant converter, primarily due to the superior R_{ON} stability of SiC under high temperatures. However, it is important to emphasize that the switching performance discussed is only an estimate and depends on the gate driver design. As previously noted, the switch's fall time significantly affects switching performance, especially when achieving ZVS. SiC devices, with their high dv/dt and di/dt characteristics, enable faster turn-on and turn-off speeds compared to Si devices. The key consideration is the tradeoff involving overshoot. In low input voltage scenarios, the overshoot voltage remains below the breakdown voltage, reducing potential risks. Therefore, SiC MOSFETs in today's technology are more adaptable to harsh environments, even in low-power applications.

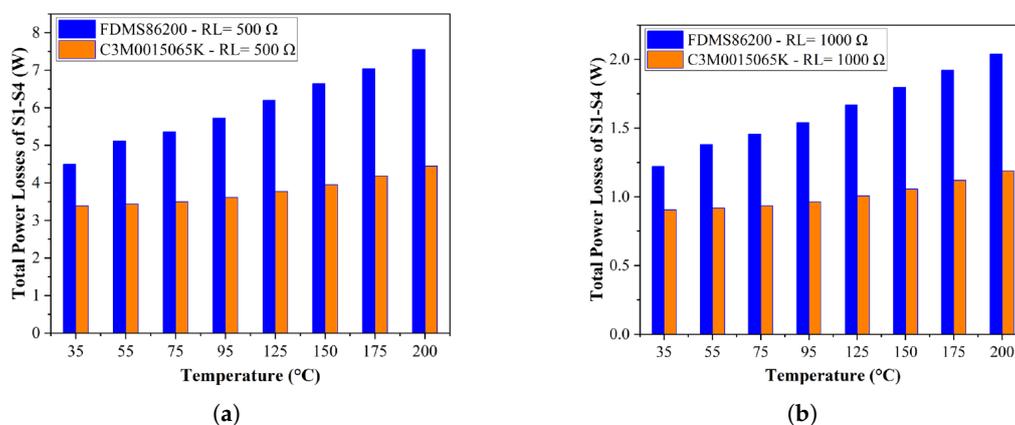


Figure 8. (a) Power conduction losses of Si (blue) and SiC (orange) MOSFETs (S1-S4) under different temperatures ($R_{load} = 500 \Omega$); (b) Power conduction losses of Si (blue) and SiC (orange) MOSFETs (S1-S4) under different temperatures ($R_{load} = 1000 \Omega$).

4.3. Radiation Simulation Results and Analysis

The radiation simulation results shown in Figure 9 indicate that SiC MOSFETs experience a decrease in R_{ON} as the TID increases from 0 to 500 krad, with a 5.24% reduction noted at a load resistance of 500 Ω . While this reduction in R_{ON} may initially appear beneficial due to the resulting lower power conduction losses, the threshold voltage shift observed under gamma-ray irradiation raises more significant concerns regarding long-term reliability. A negative shift in V_{TH} implies that the MOSFET can turn on more easily, which increases the risk of unintended switching in the presence of noise, ultimately compromising circuit performance and reliability. Furthermore, as the load decreases (e.g., at 1000 Ω), the overall power conduction losses continue to decrease further, but the impact on V_{TH} remains considerable. The accumulation of trapped charges in the gate oxide causes a more permanent degradation of V_{TH} , potentially leading to device failure after prolonged operation under radiation. While the decrease in R_{ON} contributes to lower conduction losses, this trade-off compromises long-term device reliability. In addition, the negative shift in V_{TH} increases the device's sensitivity to environmental noise, which poses a significant risk in space applications where long-term reliability is critical.

The combined effects of radiation exposure, high temperature, and prolonged operation must be analyzed in system-level design. A simulation-based method can aid in predicting potential issues that may arise in real experiments. For instance, the permanent degradation of V_{TH} and the alterations in R_{ON} could lead to catastrophic device failure, resulting in simulation that fails to accurately replicate real-life conditions.

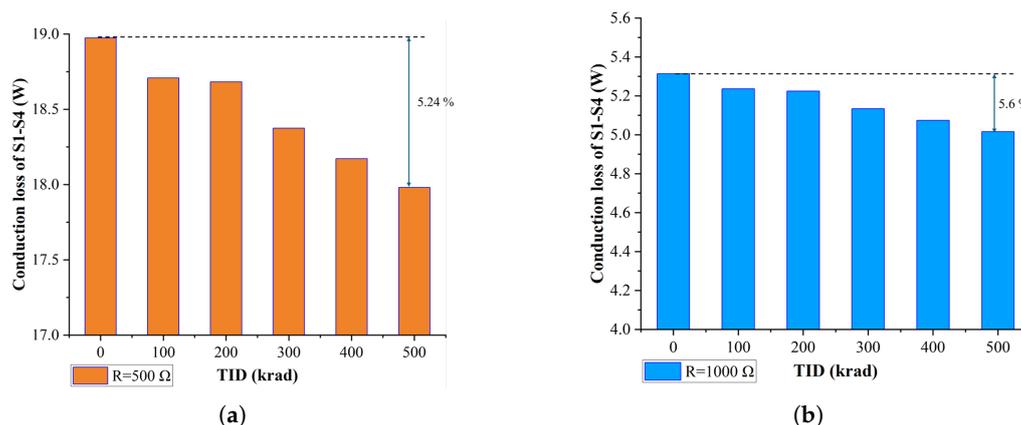


Figure 9. (a) Power conduction losses of SiC MOSFETs (S1-S4) under different TIDs ($R_{load} = 500 \Omega$); (b) Power conduction losses of SiC MOSFETs (S1-S4) under different TIDs ($R_{load} = 1000 \Omega$).

5. Conclusions

This paper proposes a simulation methodology that integrates thermal and radiation strategies within the PSIM thermal-modeling framework. In the thermal strategy, device calibration is performed using a B1505A curve tracer to correct deviations between datasheet and measured transfer characteristics. Simulation results indicate that the SiC-based resonant converter exhibits greater power-loss stability than its Si-based counterpart at elevated temperatures. In the radiation strategy, experimental data are used to simulate power losses in the resonant converter under total-ionizing-doses (TIDs) condition. Gate-oxide degradation and threshold-voltage instability are observed under high gamma irradiation. Although conduction losses may decrease under certain load conditions, increasing TID still induces permanent threshold voltage shift, degrading device reliability and system-level performance of the converter.

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