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Atomic Layer Deposition Grown Zinc-Oxide based MIS-Type Schottky Barrier Diode

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Abstract: We report on the fabrication and electrical characteristics of zinc-oxide (ZnO) based metal-insulator-semiconductor (MIS) type Schottky barrier diodes (SBHs). ZnO thin layer on the p-type silicon substrate was fabricated by atomic layer deposition (ALD). The structure and surface properties of the thin film were characterized by X-ray diffraction (XRD), atomic force microscope (AFM) and secondary ion mass spectrometer (SIMS). The current-voltage (I-V) characteristics of Al/*ALD-grown* ZnO/p-Si diodes were measured under dark at room temperature. The electrical parameters such as ideality factor (n), series resistance (R_s) and barrier height (ϕ_b) of the diodes were analyzed using standard thermionic emission (TE) theory, Norde and Cheung method. The barrier height value obtained from I-V and Cheung method was found to be 0.73 eV and 0.76 eV, respectively. The interface state density (Dit) of the diodes was determined from the I-V characteristics. The nonideal behavior of measured parameters suggested the presence of interface states. The obtained results showed that the prepared diode can be used for NIR Schottky photodetector applications.

Key words: Atomic Layer Deposition, ZnO, ideality factor, series resistance, Schottky photodetector

1. Introduction

Zinc oxide (ZnO), which has excellent electronic and optoelectronic properties such as high dielectric constant, high thermal stability, large saturation velocity, wide band gap (3.37eV) and high exciton binding energy (60 MeV), is one of the most used materials. Zinc oxide is an n-type semiconductor and a transparent conductive oxide [1]. Because of these excellent properties, Zinc oxide is used applications such as solar cells, biosensors, gas sensors, optoelectronic devices, transducers [2-5], liquid crystals display, light emitting diodes [6], visible light and UV photo-detectors [7, 8]. ZnO layers have been grown by using different deposition techniques such as sol-gel, spin coating method [9], reactive evaporation [10], chemical vapor deposition (CVD) [11], magnetron sputtering [12], and atomic layer deposition (ALD) [13]. In the recent years, there has remarkable interest to deposit ZnO thin

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films using atomic layer deposition. ALD is the special type of chemical vapor deposition technique which is based on sequential self-limiting surface reactions. Compared to other CVD technique, precursors are introduced to the surface at separate cycles. During each cycle, saturation of the precursor on the surface occurs and this results in a self-limiting growth [14]. This technique can produce suitable surfaces with high precision at the atomic scale and control sensitive film thickness. For this reason, it is a production technique that provides great advantages in thin film technology [15]. The ALD method allows high-quality thin films to be produced at low temperatures because the precursors of the gas phase can be held on the surface without going out to very high temperatures [16]. In ALD technique, the reactions reach saturation after forming a single atomic layer. This provides accurate, precise and easy thickness control and homogeneous coating. The film thickness depends only on the number of reaction cycles. In this way, it is possible to conformal coat even the most challenging geometric shaped surfaces. ALD is a perfect method for depositing thin films with 3D structures. The ALD technique has high performance in the 3D aspect in high/ aspect ratio [17]. ALD is very compatible substrate surface. ALD has many features such as reproducibility, good film density, low-temperature growth, uses very reactive precursors [18-20]. *ALD-grown* ZnO is shown a great potential for various nano-electronic device applications such as dynamic random access memory (DRAM), high-k gate dielectrics for CMOS, multilayer capacitors, organic light emitting diode (OLED layers), optical filters, integrated optics, transparent conductive oxide (TCOS) layer used thin film solar cells and photo-detectors, photonic crystals, atomic force microscope tips, nanotubes, nano-rods and nano-dots [18-22].

In this study, ZnO layer was deposited on *p-type* Si by using the ALD technique to prepare high-quality Al/*ALD- grown* ZnO/p-Si Schottky diodes. The MIS type diode was analyzed by using XRD, AFM, and SIMS. The current-voltage (I-V) characteristics were measured under dark and at room temperature. The ideality factor (n), series resistance (R_s), barrier height (ϕ_b) of the prepared diodes were analyzed by using standard thermionic emission (TE) theory, Norde's function and Cheung methods.

2. Experimental

In this work, we used *p-type* Si (100) wafer which had 380 µm thickness and 1-10 Ωcm resistivity as the substrates. Before processing the wafer, Radio Corporation of America (RCA) cleaning procedures were applied for removing organic residues from *p-type* Si wafer [23]. In order to form an ohmic contact, Al (99.999%) metal was deposited on the unpolished back surface of the wafer with a thickness of 124 nm by using sputtering systems at 500˚C under 4.7 x 10^{-6} Torr pressure condition. After the wafer was annealed at 500˚C for 10 min to dope aluminum into the back surface of the wafer, again, the back surface of the wafer was coated by Al with a thickness of 124 nm at room temperature for completing ohmic contact. ZnO was deposited on the polished *p-type* Si (100) wafer by using ALD (Okyay Nanotech) at a low substrate temperature of 170 °C. ZnO deposition was performed for 125 cycles to achieve a layer thickness of 16 nm at a growth rate of 1.29 Å/cycle. Diethylzinc ($Zn(C_2H_5)_2$ (DEZ)) and H_2O were used as precursor materials of ZnO. Nitrogen (%99.999) was used as a

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carrier and cleaning gas with a flow rate of 7 sscm to separate precursor cycles. System pressure is 2.72 x10^{-1} Torr, circle inner temperature is 170 ˚C and precursive temperatures is 150 ˚C. One ZnO ALD cycle consists of 100 ms DEZ pulse, 20 s N_2 purge, 15 ms H_2O pulse and 10 s N_2 purge, respectively. Later, the high purity (~ 99.999%) of 128 nm thick Al dots by using the mask with the shape of circular dots of 1.5 mm in diameter to rectify contacts were deposited the ZnO layer at room temperature by using the sputtering technique at 7.06x10^{-6} Torr. The schematic representation of the obtained Al/*ALD-grown* ZnO/p-Si Schottky barrier diode is seen in Fig.1.

3. Results and Discussion

3.1 Surface morphology and depth profile

The surface structure of the ZnO films was clarified by using a high performance atomic force microscope (AFM) (Nano Magnetics Instruments Ltd., Oxford, UK) by dynamic mode scanning at room temperature (RT). The scanning speed was set at 1 μm/s, and the area of 3 × 3 μm^2 was scanned. Fig.2 shows AFM images and the surface morphology of the grown ZnO films on the *p-type* Si substrate. It can be easily seen from the three-dimensional (3D) and two-dimensional (2D) AFM images with 3 × 3 μm^2 scan area of the sample shown in Fig. 2 that its surface is quite homogeneous at the nano-scale with a roughness of 3.17 nm and no particular defects can be observed.

The depth profile of the ZnO film on the Si substrate was carried out by using Hiden Analytical SIMS Workstation with Cs+ ion for sputtering having 5 keV energy and 30 nA beam current. To prevent faulty signals, the depth profile was recorded in MCs+ cluster mode, scanning for atomic masses 129, 160 and 197 for OCs, SiCs, and ZnCs, respectively. Secondary Ion Mass Spectrometer (SIMS) measurement was performed under a vacuum of 10^{-8} Torr. A stylus type profilometer (Veeco, Dektak 150) was used to measure the depth of the crater which has 100 μm^2 area obtained by the Cs ion gun etching of the sample.

Fig. 3 shows the depth profile of the grown ZnO film on the *p-type* Si substrate. It was clearly seen that the distribution of the both Zn and O was uniform throughout the depth of the achieved film. In addition, the thickness of the ZnO layer was about 15-20 nm which is the same target thickness of the growth procedure. The constant stoichiometry of the film was observed from SIMS results with the help of the signals of the MCs+ detected sensitively.

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3.2 Electrical properties of Al/ ALD-grown ZnO /p-Si Schottky barrier

Firstly, the electrical characteristics of Al/ *ALD-grown* ZnO/p-Si Schottky barrier diodes have been examined by using the standard thermionic emission (TE) theory. According to the TE theory, relation between forward bias voltage (*V>3kT/q*) and current through a Schottky diode is given [24].

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \quad (2)$$

where I_0 is saturation current which obtained from the straight line intercept of the lnI-V plot at V=0. A^* is determined as the Richardson constant (32 A/cm^{2}K^2 for *p-type* Si). q, k, and T are the electron charge, the Boltzmann's constant, the temperature in Kelvin, respectively. A, ϕ_b, V are described as the diode area, the effective barrier height, the applied voltage, respectively.

The values of ideality factor (*n*) were obtained from the slope of the semi-logarithmic I-V plots for the linear region by using Eq.(3) [24].

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

ϕ_b can be derived from Eq. (4) as are given by

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

Fig. 4 shows that the measured I-V and lnI-V characteristics of the three diodes (D1, D2, and D3) on Al/ALD-grown ZnO/p-Si Schottky diodes at room temperature, respectively. The values of ϕ_b were calculated from the intercepts of the forward bias lnI-V plot at room temperature.

It is thus easy to understand in Fig. 4, the I-V characteristics of Al/*ALD-grown* ZnO/p-Si structure show perfect rectifying behavior although low leakage. The reason of rising to the curvature at high currents in the semi-logarithmic ln(I)-V characteristics is that the current curve in the forward bias region becomes dominated by series resistance from contact wires

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or bulk resistance of MIS structures. Therefore, the values of series resistance were calculated by using Norde's and Cheung methods.

In this study, we used the modified Norde's function method suggested by Norde to determine the value of series resistance and barrier height. According to this method, the applied voltage is greater than 3kT/q like TE theory. In case of ideal Schottky barrier diode with n=1, Norde's function F(V) can be described by the following equation [25].

$$F(V,I) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{5}$$

I(V) is current taken from I-V curve. The minimum value $F(V_0)$ is obtained from F(V) vs V plot. The barrier height of Schottky diode is defined as

$$\phi_b = F(\mathrm{Vo}) + \frac{\mathrm{Vo}}{2} - \frac{kT}{q} \tag{6}$$

where V_0 is corresponding applied voltage. F(V)-V plots of the Al/ *ALD-grown* ZnO/p-Si structure is shown in Fig.5. The values of series resistance (R_s) can be calculated by using the formula.

$$\mathrm{Rs} = \frac{kT}{qI} \tag{7}$$

By using Eq (6) and (7), the obtained series resistance and barrier height values of D1, D2 and D3 diodes were given in Table 1.

Rs is significant in the linear region that is the downward curvature of the forward bias I-V characteristics, however, the other two parameters that are n and ϕ_b, are significant in both the non-linear and linear regions of I-V characteristics. The values of n, ϕ_b, and Rs were calculated by using a method that developed by S.K. Cheung and N.W Cheung [26]. According to this method, *n*, ϕ_b. R_s and H(I) can be written as

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \tag{8}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{9}$$

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$$H(I) = n\phi_b + IR_s \tag{10}$$

The barrier height (ϕ_b) was obtained from the linear region in the forward bias I–V characteristics. In Fig. 6, experimental dV/dlnI vs I and H(I) vs I plots are presented for typically three diodes on Al/*ALD-grown* ZnO/p-Si Schottky structure at room temperature, respectively.

The plot of dV/d(ln I) vs I is linear having the slope of R_s and nkT/q y-axis interception point, because of Eq. (8) gives a straight line towards the bottom left curvature region in the forward bias I-V characteristics. R_s value is obtained from the slope of the dV/d(ln I) vs I curve and n is obtained from the cut-point of the curve. In Eq. (10), R_s from the slope of the H(I) vs I curve and ϕ_b from the cut-off point of the curve are obtained using the n value found in Eq. (8). As seen in Table 1, n, ϕ_b and R_s values are calculated for typically D1, D2, and D3 diodes.

For the typically three diodes (D1, D2, and D3) on Al/ *ALD-grown* ZnO/ p-Si structure, the values of n, Φ_b and R_s expressing the electrical properties are given in the Table 1. According to the standard method, the values of n are in accordance with those of Cheung method. The Φ_b values for all three methods are in agreement each other. As it is expected, the R_s values obtained by using Norde method that is considered to be ideal (n = 1), are higher than the obtained values by using both standard and Cheung methods. The values of ϕ_b obtained from lnI-V plots, Norde's function and Cheung method are different from each other by comparing their results. These differences may be due to the extraction from the different region of the I-V plot. The values of R_s calculated from Norde's method is higher than those of calculated another method. While Norde's model is executed for the all forward bias region of I-V plots, Cheung's model is executed for a nonlinear high-voltage region of the forward bias of I-V plots [27].

Downward curvature of the forward bias I–V characteristics may be due to the fact that effect of interface states. The density distribution profile of the interface state (D_{it}) in equilibrium with semiconductor can high-performance by using the forward bias I-V curves. In case of the presence of interfacial insulator layer and interface states, the voltage-dependent of the barrier height is determined as

$$\frac{d\phi_e}{dV} = \Gamma = 1 - \frac{1}{n(V)} \tag{11}$$

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where ϕ_e, Γ are the effective of barrier height, the voltage coefficient of the effective of barrier height, respectively. The voltage-dependent of ϕ_e is described by

$$\phi_e = \phi_B + \left(1 - \frac{1}{n(V)}\right)V \tag{12}$$

According to Card and Rhoderick [28, 29], D_{it} versus E_{ss}-E_v for p-type semiconductor barrier diode can be given as

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qD_{it}(V)\right] \tag{13}$$

$$n(V) = \frac{q}{kT}\left(V_i \ln\left(\frac{I_i}{I_0}\right)\right) \tag{14}$$

$$D_{it} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_i}{W_D}\right] \tag{15}$$

where δ=16 nm is the thickness of the interfacial insulator. $\varepsilon_s = 11.8\,\varepsilon_0$ and $\varepsilon_i = 8.65\,\varepsilon_0$ are the permittivity of the semiconductor and the interfacial insulator, respectively. W_D is the weight of depletion layer obtained from $1/C^2$-V plots at 1 MHz. I_0 is the saturation current which obtained from the straight line intercept of the lnI-V curves at V=0. The values of interface states as a function for D1, D2 and D3 diodes were calculated by using Eq. (13) and (14).

For p-type semiconductors, the energy of the E_{ss} with respect to the top of valence band at the surface of semiconductor is described by the following equation,

$$E_{SS} - E_V = q(\phi_e - V) \tag{16}$$

The obtained energy dependent distributions of interface states were given in Fig.7.

These values are suitable for a semiconductor as described in the literature. Fig.7 shows that interface states increase the middle of the forbidden energy band gap towards the top of valence band for typically three diodes in the same feature. The D_{it} versus Ess-Ev changes from 5×10^{12} to 1×10^{11} $eV^{-1}.cm^{-2}$ for D1, 4×10^{12} to 1.4×10^{11} $eV^{-1}.cm^{-2}$ for D2, 3×10^{12} to 1.2×10^{10} $eV^{-1}.cm^{-2}$ for D3 diode.

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Conclusion

The electrical characteristics of the fabricated Al/*ALD-grown* ZnO/p-Si Schottky barrier diodes have been investigated with help of standard thermionic emission (TE) theory, Norde's function and Cheung method. The I-V characteristics of the diodes were measured under dark and at room temperature. For three diodes, the ideality factor and barrier height values were obtained from standard thermionic emission (TE) method, 1.44 and 0.73 eV for D1 diode, 1.75 and 0.73 for D2 diode and 1.64 and 0.72 for D3 diode, respectively. The barrier height determined from Cheung method was found to be 0.76 eV. Moreover, the barrier height obtained from Norde's function that was limited to the highly idealized case of n = 1 exactly match those of Standard method. In addition, the measured densities of interface states in this study are sufficient level for the performance of the device. As results, the fabricated diode can be used for NIR Schottky photodetector applications.

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FIGURE CAPTIONS

Figure 1. Schematic representational cross-sectional views of Al/*ALD-grown* ZnO/p-Si Schottky diode.

Figure 2. (a) 2D (b), (c) 3D of the AFM surface morphology of Al/*ALD-grown* ZnO/n-Si Schottky diode on the 3×3 μm^2 scan area.

Figure 3. SIMS depth profile of the ZnO film on p-type Si.

Figure 4. Semi-logarithmic I-V characteristics of the Al/ *ALD-grown* ZnO/p-Si Schottky diodes.

Figure 5. Norde plot of F(V,I) for Al/ *ALD-grown* ZnO/p-Si diodes.

Figure 6. The dV/d(ln I) vs. I and H(I) vs I characteristics of Al/ *ALD-grown* ZnO/p-Si diodes.

Figure 7. The D_{it} vs. Ess-Ev of Al/*ALD-grown* ZnO/p-Si structure.

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TABLES CAPTIONS

Table 1. Electrical parameters from calculated I–V measurements of Al/ *ALD-grown* ZnO/p-Si diodes.

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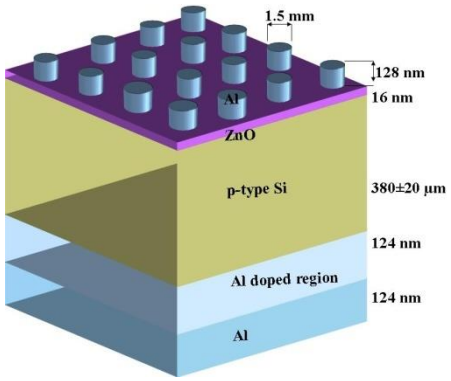

Figure 1

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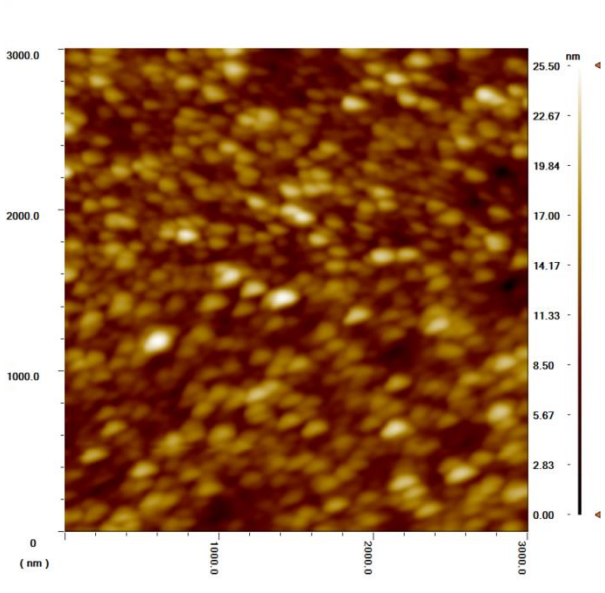
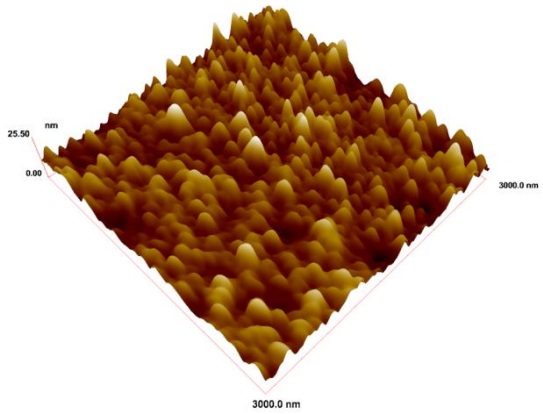
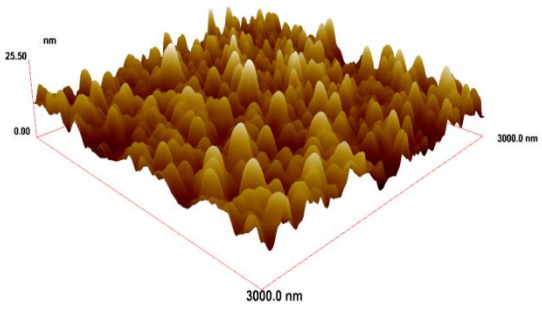


a)





b) c)

Figure 2

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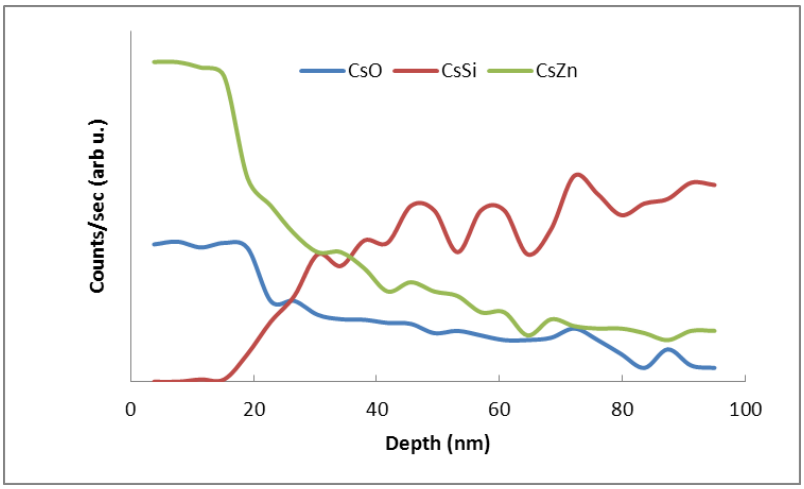

Figure 3

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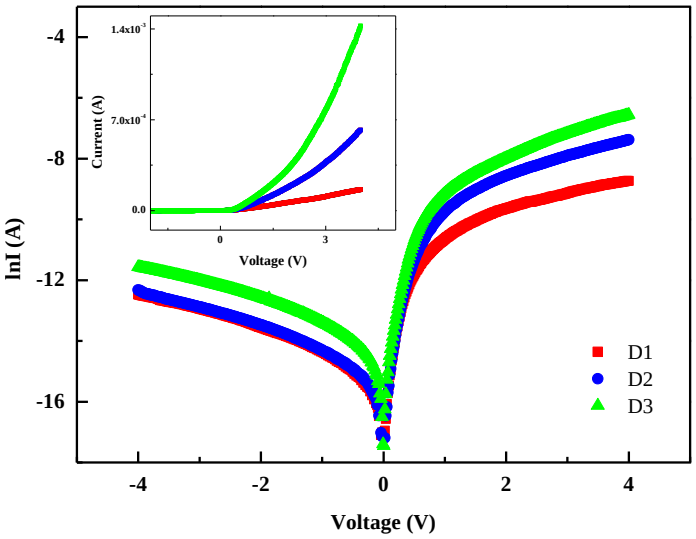

Figure 4

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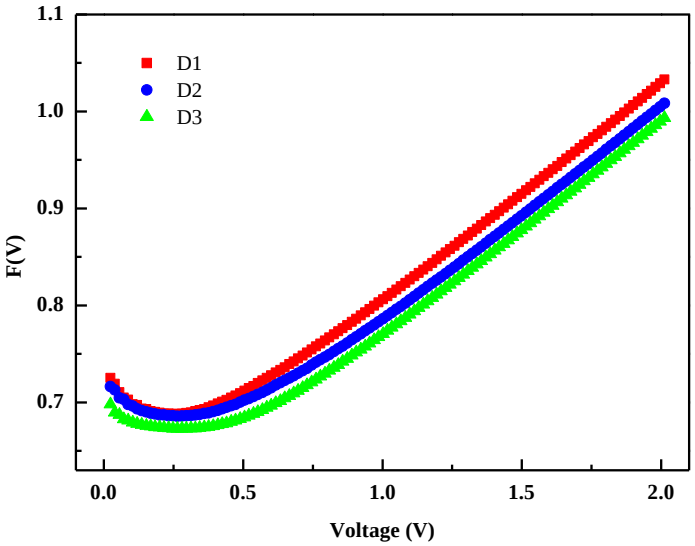

Figure 5

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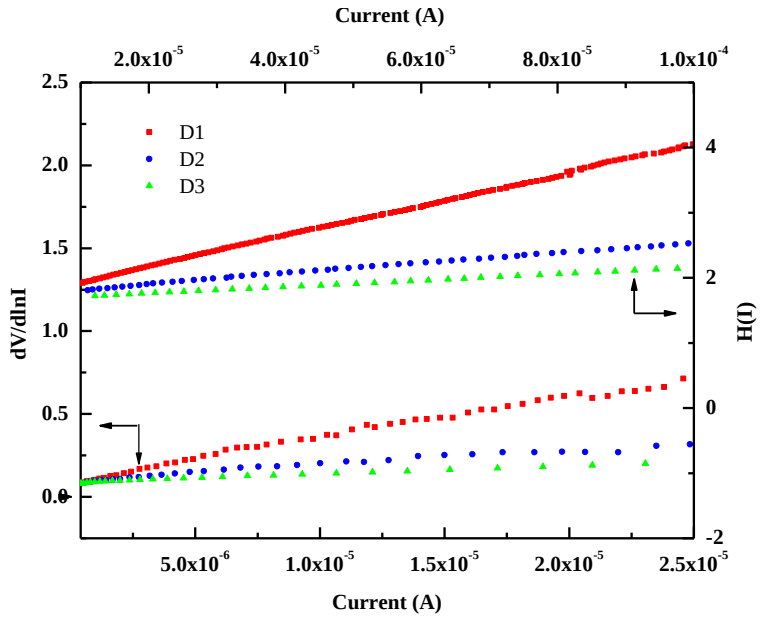

Figure 6

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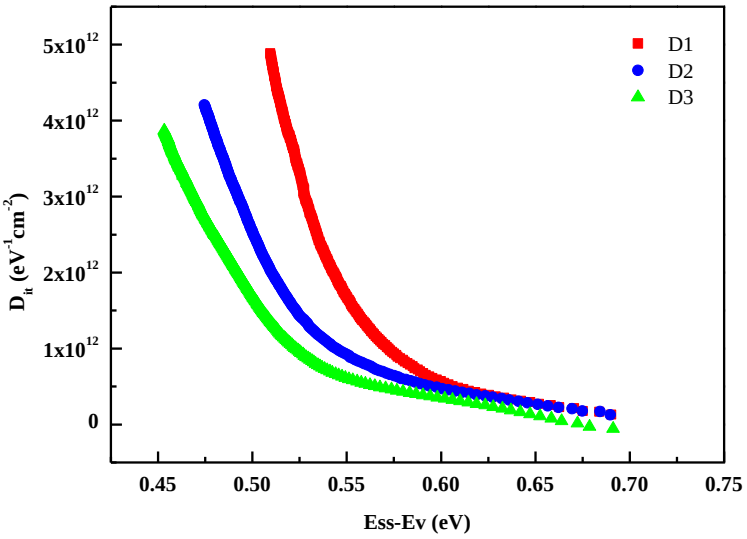

Figure 7

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Table 1

Methods		**Diodes**								
		D1			**D2**			**D3**		
		n	**Φ_b (eV)**	**R_s (kΩ)**	**n**	**Φ_b (eV)**	**R_s (kΩ)**	**n**	**Φ_b (eV)**	**R_s (kΩ)**
Standard		1.44	0.73	-	1.75	0.73	-	1.64	0.72	-
Norde		-	0.73	174	-	0.73	170	-	0.71	111
Cheung	**dV/dlnI vs I**	2.85	-	32.93	2.54	-	34.80	2.58	-	5.58
	H(I) vs I	-	0.72	21.56	-	0.81	7.01	-	0.77	4.5