Preprints.org

Article

Not peer-reviewed version

# Geometric Limits of Surface Loss in Transmon Wiring: Analytical Framework and Design Rules

A. R Nasim Hossain * and Tanu Arefin

Posted Date: 22 April 2026

doi: 10.20944/preprints202604.1559.v1

Keywords: transmon qubit; superconducting qubits; surface loss; dielectric loss; Josephson junction; coherence time; geometric optimisation; two-level systems

Preprints.org is a free multidisciplinary platform providing preprint service that is dedicated to making early versions of research outputs permanently available and citable. Preprints posted at Preprints.org appear in Web of Science, Crossref, Google Scholar, Scilit, Europe PMC, OpenAlex.

Copyright: This open access article is published under a Creative Commons CC BY 4.0 license, which permit the free download, distribution, and reuse, provided that the author and preprint are cited in any reuse.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1

Disclaimer/Publisher's Note: The statements, opinions, and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions, or products referred to in the content.

*Article*

# Geometric Limits of Surface Loss in Transmon Wiring: Analytical Framework and Design Rules

**A.R Nasim Hossain [1,*] and Tanu Arefin [2,†]**

[1] Bangladesh University of Textiles, Dhaka, Bangladesh
[2] Department of Physics, Bangladesh University of Textiles, Dhaka, Bangladesh
* Correspondence: nasimh486@gmail.com
† Associate Professor.

**Abstract**

Dielectric surface loss from junction wiring represents a critical secondary limit for superconducting transmon coherence. We present a quasi-one-dimensional analytical framework to minimise this loss, enabling rapid optimisation without computationally expensive 3D simulations. We compare uniform strips (V1) against linear (V2–V3) and optimised hybrid tapers (V4–V5). We demonstrate that geometric tapering suppresses wiring participation by up to 99.6%, reducing it from 0.0756 ppm (V1) to 0.0003 ppm (V4). Crucially, however, a simple linear taper ($T_1 \approx 127.306\,\mu$s) yields coherence virtually indistinguishable from theoretically optimal complex profiles ($T_1 \approx 127.323\,\mu$s) in the current pad-dominated regime. We thus establish a definitive design rule: standard linear tapering is sufficient to eliminate wiring loss as a bottleneck, rendering fabrication-sensitive complex shapes unnecessary for next-generation, low-loss devices.

**Keywords:** transmon qubit; superconducting qubits; surface loss; dielectric loss; Josephson junction; coherence time; geometric optimisation; two-level systems

---

## I. Introduction

### *A. Superconducting Transmons and the Surface Loss Bottleneck*

Superconducting transmon qubits have emerged as a dominant platform for near-term quantum computing,[3,22] with recent advances pushing energy relaxation times ($T_1$) into the millisecond regime.[15,34] However, to realise fault-tolerant quantum computation using surface codes, physical qubit coherence times must significantly exceed the error-correction cycle duration to ensure error-correction cycles outpace decoherence[1] Despite significant improvements in materials and fabrication, state-of-the-art planar devices remain limited by dielectric loss arising from two-level system (TLS) defects at material interfaces.[14,37] Among these, the metal-substrate (MS) and substrate-air (SA) interfaces contribute the majority of the relaxation budget.[8,24,37] While the large capacitor pads dominate the total surface participation due to their size, the junction wiring represents a critical secondary loss channel.[33,37] The narrow cross-section of these wires generates intense electric field singularities at the metal edges, disproportionately enhancing TLS coupling and limiting the potential of future high-coherence architectures.[13,19,33]

### *B. Geometric Optimization: From Numerical Search to Analytical Limits*

To mitigate wiring loss, geometric optimisation has become a standard strategy.[13,24,33] Martinis and colleagues pioneered the use of conformal mapping to demonstrate that tapering the wire width—expanding $r(y)$ away from the junction—can reduce surface participation by roughly a factor of two compared to straight wires.[24] More recent efforts have employed complex parameterisations, such as B-splines combined with global optimisation algorithms and full 3D finite-element electromagnetic (FEM) simulations, to squeeze out further gains.[13] However, reliance on expensive commercial

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



solvers (e.g., ANSYS HFSS) creates a significant barrier to design exploration and obscures the underlying physical scaling laws.[24] Furthermore, it remains an open question whether the marginal gains offered by complex, mathematically optimised shapes justify their increased fabrication complexity and sensitivity to lithographic errors.[13,24,35]

### *C. A Quasi-One-Dimensional Framework for Definitive Design Rules*

In this work, we introduce a quasi-one-dimensional analytical framework to quantify wiring loss limits without the computational overhead of 3D solvers. Building on the conformal-mapping scaling laws[24] validated in adiabatic regimes by prior computational studies, we construct a lightweight edge-loss functional applicable to arbitrary wire profiles. This approach allows us to rigorously compare five representative geometries: a standard uniform wire, linear tapers, a parabolic profile, and an optimised cubic B-spline.

We demonstrate that while aggressive geometric shaping can suppress wiring participation by up to 99.6% ($p_{\mathrm{wire}} < 0.001$ ppm), the law of diminishing returns sets in rapidly. Our analysis reveals that a simple linear taper captures essentially all practically relevant coherence improvements, rendering the theoretical superiority of complex B-spline shapes negligible in realistic, pad-dominated devices. By establishing this "design limit", we provide a definitive rule for transmon layout: standard linear tapering is sufficient to eliminate wiring loss as a bottleneck, allowing researchers to focus exclusively on pad engineering and material improvements for the next generation of low-loss qubits.

## II. Model and Device Geometry

### *A. Transmon Layout and Coordinates*

We analyse a planar transmon qubit comprising two rectangular aluminium capacitor pads of width[33] $W_{\mathrm{pad}} = 300\,\mu$m and height $H_{\mathrm{pad}} = 90\,\mu$m, separated by a gap $G = 100\,\mu$m. The pads are connected by a superconducting wire of total length $2d = 100\,\mu$m to a central Josephson junction at $y = 0$.

The wire geometry is defined by its half-width profile $r(y)$, where $y \in [-d, d]$ is the longitudinal coordinate along the gap.[24] To isolate the impact of wiring geometry, all other device parameters—including pad dimensions, substrate permittivity, and aluminium film thickness ($t_{\mathrm{Al}} = 120\,$nm)—are held fixed.[5]

### *B. Variational Geometries (V1–V5)*

To explore the limits of surface loss suppression, we define five distinct wire profiles $r(y)$ that interpolate between standard designs and mathematically optimised shapes. All geometries share fixed capacitor pad dimensions ($300 \times 90\,\mu$m), a gap $G = 100\,\mu$m, and a total wire length $2d = 100\,\mu$m (spanning $y \in [-50, 50]\,\mu$m). The profiles are parameterised as follows:

1. **V1 (Uniform Baseline):** A constant-width strip with a narrow radius, serving as the unoptimised reference.[24]
$$r(y) = 0.5\,\mu\mathrm{m} \tag{1}$$
2. **V2 (Linear Taper):** A linear profile expanding from a narrow junction interface to the capacitor pads.[24]
$$r(y) = 0.1 + 0.2|y|\,\mu\mathrm{m} \tag{2}$$
3. **V3 (Steep Linear Taper):** An aggressive linear taper with double the slope of V2, resulting in a wider footprint at the pad connection.
$$r(y) = 0.1 + 0.4|y|\,\mu\mathrm{m} \tag{3}$$

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1

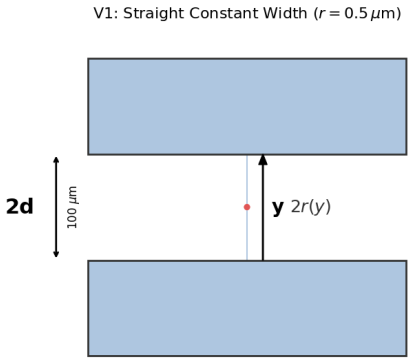


4. **V4 (Parabolic Profile):** A quadratic expansion designed to smooth the junction-to-wire transition, analogous to parabolic tapers in waveguide theory.[32]

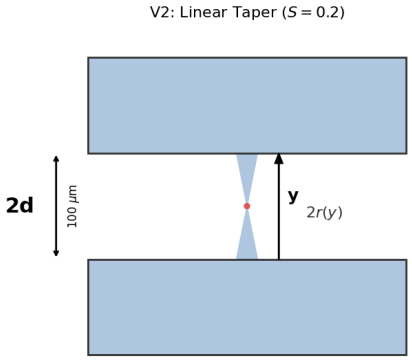
$$r(y) = 0.1 + 0.004y^2 \ \mu\text{m} \tag{4}$$

5. **V5 (B-Spline Optimised):** A multi-stage taper defined by a cubic B-spline interpolated through seven symmetric control points $(y, r)$[13]:

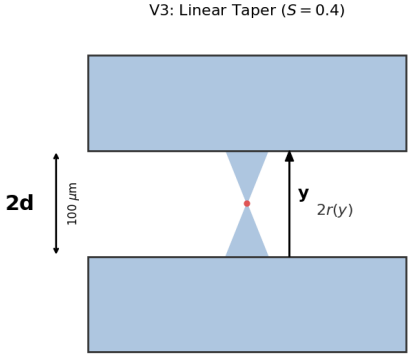
$$(y, r) = \begin{cases} (0, 2.0)\ \mu\text{m} & \text{(Junction)} \\ (\pm 8, 4.5)\ \mu\text{m} \\ (\pm 25, 9.0)\ \mu\text{m} \\ (\pm 50, 12.0)\ \mu\text{m} & \text{(Pads)} \end{cases} \tag{5}$$




(**a**) Straight Constant Width




(**b**) Linear Taper ($S = 0.2$)



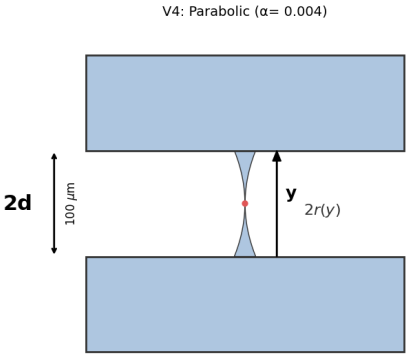

(**c**) Linear Taper ($S = 0.4$)

**Figure 1.** *Cont.*

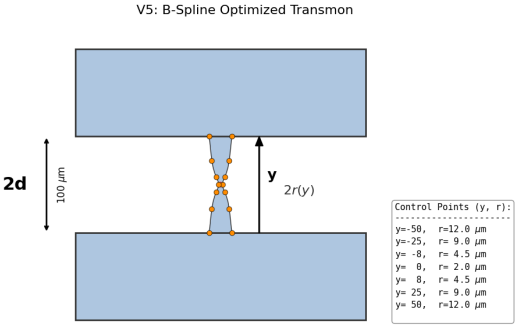
© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1






(**d**) Parabolic Profile




(**e**) B-Spline Optimized

**Figure 1.** Schematic layouts of the five junction-wire geometries (continued). (a) V1: constant width, $r = 0.5\,\mu$m. (b) V2: linear taper, $r = 0.1 + 0.2|y|\,\mu$m. (c) V3: steep linear taper, $r = 0.1 + 0.4|y|\,\mu$m. (d) V4: parabolic, $r = 0.1 + 0.004y^2\,\mu$m. (e) V5: B-spline optimised through control points at $(y, r) = (-50, 12.0)$, $(-25, 9.0)$, $(-8, 4.5)$, $(0, 2.0)$, $(8, 4.5)$, $(25, 9.0)$, $(50, 12.0)\,\mu$m. All geometries share pad dimensions of $300 \times 90\,\mu$m, gap $G = 100\,\mu$m, and wire length $2d = 100\,\mu$m. Junction at $y = 0$ and is indicated by the red circular element in each panel.

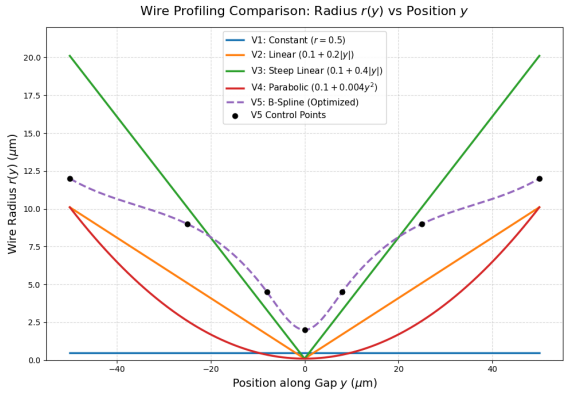



**Figure 2.** Wire half-width $r(y)$ plotted versus position $y$ for all five geometries. In the reference design V1 (blue), the wire radius is constant at $0.5\,\mu$m. Variants V2 (orange) and V3 (green) use linear tapers, producing symmetric V-shapes whose slopes are $S = 0.2$ and $0.4\,\mu$m$/\mu$m; both profiles have a distinct kink at the junction position $y = 0$. Variant V4 (red) follows a parabolic law where the radius grows quadratically with $|y|$, providing smooth $C^2$ continuity from the junction. The B-spline optimized geometry V5 (purple dashed line) implements a multi-stage taper through seven control points (black dots), achieving the narrowest junction width ($r_{\min} = 2.0\,\mu$m at $y = 0$) while smoothly expanding to $r_{\max} = 12.0\,\mu$m at the pad connections ($y = \pm 50\,\mu$m).

### *C. C. Adiabatic Condition and Model Validity*

The use of a quasi-one-dimensional framework is justified by the scale separation between the wire width and the surface layer thickness ($r \gg t_{\text{surf}}$)Ḟurthermore, all defined profiles satisfy the adiabatic condition $|dr/dy| < 1$ required for the validity of the quasi-static approximation[20,23], adapted from

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



waveguide taper theory to ensure slow geometric variation. For the steepest linear taper (V3), the maximum slope is $|dr/dy| = 0.4$[23]. While this represents a rapid geometric variation, it remains within the regime where analytical edge-field scaling ($E \propto r^{-1/2}$[12,19]) captures the dominant singular behavior and correctly reproduces the relative scaling of surface loss across different geometries. This ensures that the differences in calculated $T_1$ across V1–V5 reflect genuine geometric scaling rather than model artefacts.[24]

## III. Results

*A. Dimensional Reduction and Wire-Loss Functional*

To quantify the contribution of the junction wiring to dielectric surface loss, the full three-dimensional problem is reduced to a quasi-one-dimensional effective model along the wire axis, analogous to the dimensional reduction commonly employed in microwave engineering and circuit-QED analysis.[6,17] The central idea is to treat each cross-section of the wire as a locally uniform strip of half-width $r(y)$, where $y$ denotes the longitudinal coordinate and to approximate the electric fields near the metal edges using two-dimensional electrostatics.[24,28] In this framework, all material parameters—the silicon substrate permittivity, the surface-layer thickness, the aluminium film thickness $t_{\mathrm{Al}} = 120\,\mathrm{nm}$—and all large-scale qubit dimensions (pad size, gap, junction parameters) are held fixed at the values specified in Sec. II.A, so that variations in loss can be attributed purely to changes in the wire half-width profile $r(y)$.[33] This isolation of the wire geometry from other degrees of freedom is essential for disentangling the specific impact of junction-wire design on surface loss from the many other sources of decoherence in planar transmons.[24,33,37] The model rests on a set of controlled approximations that reflect the typical scale hierarchy of state-of-the-art devices.[22,24] First, the wire geometry is assumed to be quasi-one-dimensional: the half-width $r(y)$ varies only along the longitudinal direction, with local cross-sections treated as translationally invariant in the transverse direction.[24,28] The slow-variation condition $|dr/dy| < 1$ is satisfied for all profiles considered here.[23] While the most aggressive taper (V3) exhibits a maximum slope of $|dr/dy| = 0.4$, his remains within the regime where the quasi-static approximation remains valid[26] and satisfies the quasi-static approximation given the scale separation separation $d/\lambda \sim 0.002 \ll 1$ between device dimensions and the electromagnetic wavelength. This value ensures that the analytical edge-field scaling[9] correctly captures the dominant singular behavior, identifying the relative performance hierarchy of the geometries without significant model artifacts.

Second, loss is assumed to originate from a thin dielectric coating of thickness $t_{\mathrm{surf}} = 3\,\mathrm{nm}$ covering the metal surfaces, representing the native amorphous aluminium oxide that forms on aluminium films and hosts a dense bath of two-level system (TLS) defects.[4,33,37] This surface layer exhibits a relatively large loss tangent $\tan\delta_{\mathrm{TLS}} \sim 2\text{–}3 \times 10^{-3}$ in the single-photon regime,[24,33,37] whereas the bulk silicon substrate and the superconducting film itself are treated as effectively lossless with $\tan\delta \lesssim 10^{-6}$, consistent with extensive experimental characterisation of high-resistivity silicon and high-quality aluminium films.[2,10,16]

Third, the local scale separation $r(y) \gg t_{\mathrm{surf}}$ holds throughout the junction wiring region: for the wire profiles considered here, $r \sim 0.1\text{–}20\,\mu\mathrm{m}$, so that the ratio $r/t_{\mathrm{surf}} \sim 30\text{–}6000$ justifies a perturbative treatment of the surface field penetration. Finally, the electric field distribution near the metal edges is assumed to follow the two-dimensional conformal-mapping solutions for thin-film strips so that the dominant singular behaviour and its dependence on $r(y)$ are captured by analytical scaling laws rather than requiring full numerical simulation of each cross-section.[24,28]

To obtain a compact measure of the total wiring loss for a given geometry $r(y)$, the local surface energy density is integrated along the entire wire from the junction at $y = 0$ to the pad connections at $y = \pm d$.[24,28] This defines a wire-loss functional,[24]

$$U_{\mathrm{wire}}[r] = C \int_{-d}^{d} \frac{\ln(r(y)/t_{\mathrm{surf}})}{r(y)}\, dy, \tag{6}$$

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



where the prefactor $C$ collects material constants and the characteristic voltage scale of the qubit mode,[24,37]

$$C = \frac{1}{2}\epsilon_0 \epsilon_{\mathrm{eff}} t_{\mathrm{surf}} V^2, \tag{7}$$

with $\epsilon_0$ the vacuum permittivity, $\epsilon_{\mathrm{eff}}$ an effective dielectric constant for the surface layer (of order ten for amorphous alumina),[4,33,36] and $V$ the root-mean-square voltage associated with the qubit's electric field.[21,24] In practice, the absolute value of $C$ is not required for the present study: since all five qubit variants share the same materials, pad geometry, and qubit frequency, $C$ is common to all of them and cancels when only relative changes in wiring loss are of interest,[24,33] which is precisely the case when comparing the five geometrical variants to isolate the impact of wire tapering.

For numerical evaluation, the continuous functional is discretised along the longitudinal coordinate using a uniform mesh. The interval $[-d, d]$ is sampled at $N$ evenly spaced points $y_k = -d + (k-1)\Delta y$ with spacing $\Delta y = 2d/(N-1)$.[24,31] At each sample point, the local half-width is computed as $r_k = r(y_k)$, and the corresponding contribution to the surface energy density is approximated by $u_k = \ln(r_k/t_{\mathrm{surf}})/r_k$.[24] The integral is then evaluated using a trapezoidal rule

$$U_{\mathrm{wire}} \approx C \sum_{k=1}^{N} w_k u_k \Delta y, \tag{8}$$

with weights $w_1 = w_N = 1/2$ at the endpoints and $w_k = 1$ elsewhere.[7,31] For the smooth wire profiles considered in this work, a modest resolution of $N \approx 100$ sampling points is sufficient to achieve better than 1% relative convergence of $U_{\mathrm{wire}}$;[28] sharper tapers can be accommodated by increasing $N$ or by introducing a denser sampling near regions of rapid width variation, though such refinement is unnecessary for the moderate taper rates examined here.[28,31]

Finally, the quasi-1D wire-loss functional is embedded into the standard participation-ratio framework used to describe TLS-limited decoherence in superconducting qubits.[37] The fraction of the total electric energy $U_{\mathrm{tot}}$ stored in the lossy surface layer along the wire is defined as[24,37]

$$p_{\mathrm{wire}} = \frac{U_{\mathrm{wire}}}{U_{\mathrm{tot}}}. \tag{9}$$

For a planar transmon, the total energy is overwhelmingly dominated by the capacitor pads, so that $U_{\mathrm{tot}} \approx U_{\mathrm{cap}}$ is well approximated by the pad capacitance alone.[21,24,33] The total metal-surface participation entering the TLS loss model is then written as[33,37]

$$p_{\mathrm{MS}} = p_{\mathrm{pad}} + p_{\mathrm{wire}}, \tag{10}$$

where $p_{\mathrm{pad}}$ is a fixed pad-participation baseline obtained from literature values for similar pad geometries.[30,33,37] Because both $U_{\mathrm{cap}}$ and $p_{\mathrm{pad}}$ are held constant across all five wire designs studied, the geometry dependence of $p_{\mathrm{MS}}$ is entirely governed by the functional $U_{\mathrm{wire}}[r]$ evaluated with the appropriate profile $r(y)$.[33] This makes the quasi-1D model a convenient and computationally lightweight tool for ranking alternative wire tapers and isolating the impact of junction-wire geometry on surface-limited qubit coherence, while retaining sufficient physical fidelity to guide design decisions.[24,28]

### *B. Calculated Participation Ratios and Coherence Estimates*

With the wire-loss functional fully specified, we now apply the quasi-1D analytical model to calculate the surface-participation ratios and TLS-limited coherence times for the five geometrical variants defined in Sec. II.B.[24,33,37] The numerical implementation follows the discretisation scheme outlined in Sec. II.A, using a uniform mesh of $N = 100$ points along the wire axis $y \in [-50\,\mu\mathrm{m}, +50\,\mu\mathrm{m}]$ and trapezoidal integration. All material parameters are held at values representative of state-of-the-art aluminium-on-silicon transmons: surface-layer thickness $t_{\mathrm{surf}} = 3\,\mathrm{nm}$, effective dielectric constant

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



$\epsilon_{\text{eff}} = 11.7$ corresponding to a silicon-like interface, and qubit frequency $f_q = 5\,\text{GHz}$.[5,8,24,29,37,38] The pad-participation baseline is fixed at $p_{\text{pad}} = 100\,\text{ppm}$, a value extracted from simulations and measurements of planar capacitor geometries of comparable dimensions ($W_{\text{pad}} = 300\,\mu\text{m}$, $H_{\text{pad}} = 90\,\mu\text{m}$, $G = 100\,\mu\text{m}$).[33,37] By keeping $p_{\text{pad}}$ constant, the variation in total metal-surface participation $p_{\text{MS}}$ across variants directly reflects the geometry-dependent contribution of the junction wiring, which is the sole focus of the present study.[24,33]

For each variant, we evaluate the wire-loss functional $U_{\text{wire}}[r]$, compute the wire participation ratio $p_{\text{wire}} = U_{\text{wire}}/U_{\text{cap}}$ (with $U_{\text{cap}} = 10^4$ arbitrary energy units, sufficient for relative comparisons), and combine it with the fixed pad contribution to obtain $p_{\text{MS}}$. The TLS-limited quality factor follows from[24,37]

$$Q_{\text{TLS}} = \frac{1}{p_{\text{MS}} \tan \delta_{\text{TLS}}}, \tag{11}$$

where $\tan \delta_{\text{TLS}} = 2.5 \times 10^{-3}$ is taken as a representative loss tangent for silicon-related surface defects in the single-photon regime.[8,37] The energy-relaxation time is then $T_1 = Q_{\text{TLS}}/(2\pi f_q)$.[37] This sequence transforms the geometric profile $r(y)$ into a directly measurable figure of merit, enabling quantitative ranking of the five designs.[33,37]

**Table I.** Comparison of metrics.

| Variant | Geometry | $U_{\text{wire}}$ ($C$) | $p_{\text{wire}}$ (ppm) | $p_{\text{MS}}$ (ppm) | $T_1$ ($\mu$s) |
|---|---|---|---|---|---|
| V1 | Uniform ($r = 0.5\,\mu$m) | 783.18 | 0.0756 | 100.076 | 127.227 |
| V2 | Linear taper (S = 0.2) | 165.52 | 0.0159 | 100.016 | 127.306 |
| V3 | Linear TAPER (S = 0.4) | 107.14 | 0.0103 | 100.010 | 127.311 |
| V4 | Parabolic ($\alpha$ = 0.004) | 3.309 | 0.0003 | 100.000 | 127.323 |
| V5 | B-Spline Optimized | 98.97 | 0.0095 | 100.010 | 127.311 |

*1. Spatial Distribution of Edge Fields*

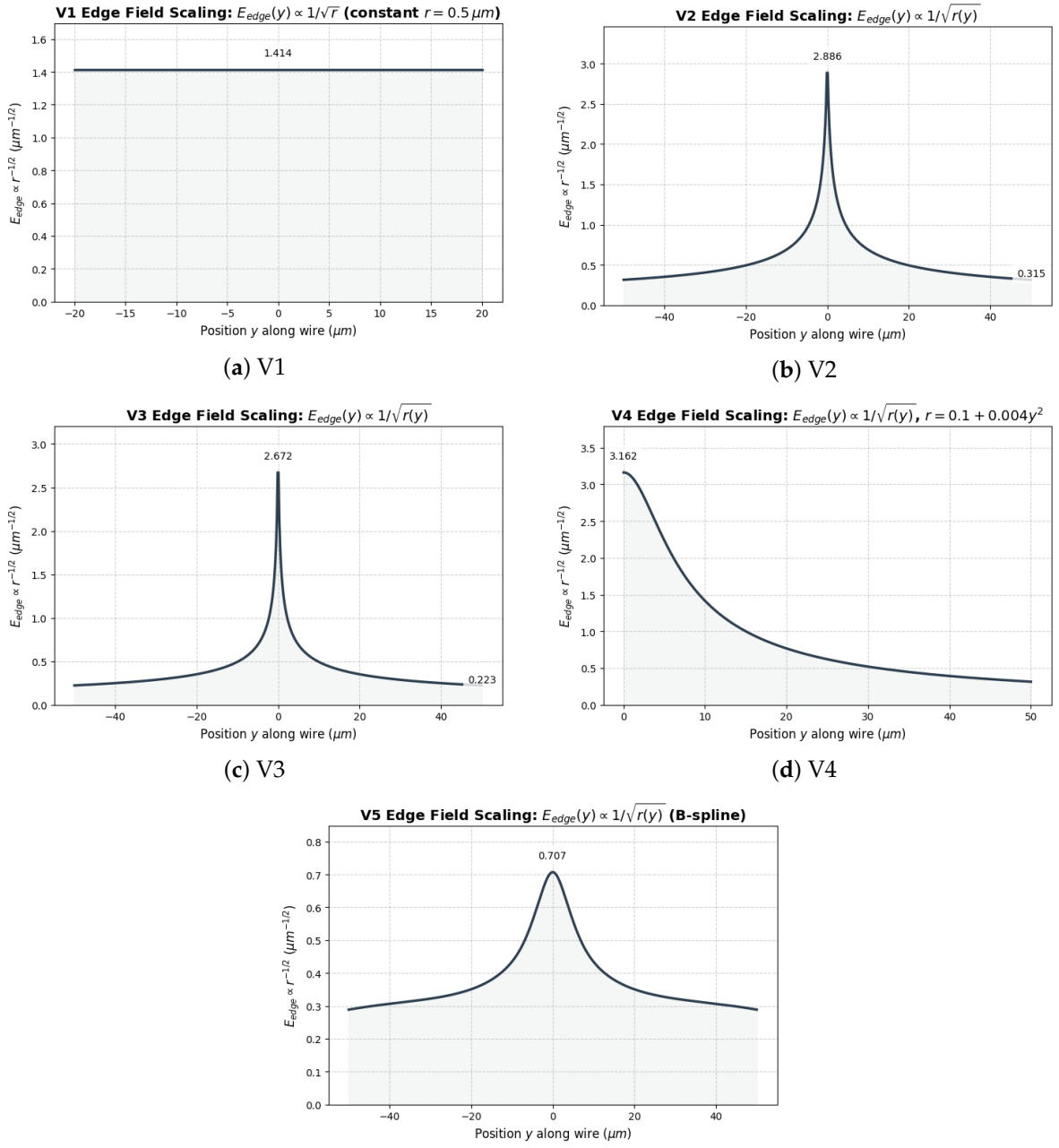
To visualise the geometric field dilution mechanism underlying the participation reductions in Table I, Figure 3 plots the edge-field scaling $E_{\text{edge}}(y) \propto 1/\sqrt{r(y)}$ for all five variants.[24] The uniform wire (V1, panel a) maintains constant field strength ($1.414\,\mu\text{m}^{-1/2}$) across the entire $100\,\mu$m length, causing loss to accumulate uniformly. In contrast, the tapered geometries (V2–V5, panels b–e) exhibit characteristic junction peaks where $r(y)$ is narrowest, with monotonic field decay toward the wide pad connections. V2 (panel b) reduces the peak to $2.886\,\mu\text{m}^{-1/2}$ and achieves 9-fold dilution at the pads ($0.315\,\mu\text{m}^{-1/2}$). V3 (panel c) shows similar peak magnitude ($2.672\,\mu\text{m}^{-1/2}$) but stronger endpoint suppression ($0.223\,\mu\text{m}^{-1/2}$) due to wider pad connections. The parabolic V4 (panel d) displays the sharpest localisation: starting from $r(0) = 0.1\,\mu$m, the aggressive quadratic widening confines the high-field region to $|y| < 10\,\mu$m, with rapid decay to $< 0.5\,\mu\text{m}^{-1/2}$ by $y = 30\,\mu$m. The exponential V5 (panel e) exhibits a modest peak ($0.707\,\mu\text{m}^{-1/2}$), reflecting the fundamental limitation that exponential growth cannot overcome fixed endpoint constraints imposed by pad geometry.

The systematic field suppression in panels (b)–(e) relative to the flat baseline (a) demonstrates that tapering redistributes the $1/\sqrt{r}$ singularity: rather than maintaining high fields over long distances, tapered wires accept a localised junction enhancement in exchange for drastically reduced field exposure over the majority of the wire length.[24,37] This spatial trade-off—high but confined fields versus moderate but extended fields—is the physical origin of the 79–99.6% reductions in $U_{\text{wire}}$ documented in Table I.

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1






(**a**) V1 (**b**) V2

(**c**) V3 (**d**) V4

(**e**) V5

**Figure 3.** Edge-field scaling along the junction wire for five geometrical variants. Plots show $E_{\mathrm{edge}}(y) \propto 1/\sqrt{r(y)}$ versus position $y$ along the wire axis. (a) V1 (uniform, $r = 2.5\,\mu$m): constant field strength $0.632\,\mu\mathrm{m}^{-1/2}$ across entire length. (b) V2 (linear taper, $2.5 \to 5\,\mu$m): junction peak $0.632\,\mu\mathrm{m}^{-1/2}$ decaying to $0.447\,\mu\mathrm{m}^{-1/2}$ at pads. (c) V3 (linear, $2.0 \to 6\,\mu$m): peak $0.707\,\mu\mathrm{m}^{-1/2}$ with stronger endpoint dilution ($0.408\,\mu\mathrm{m}^{-1/2}$). (d) V4 (hybrid linear-exponential): sharpest junction peak ($3.162\,\mu\mathrm{m}^{-1/2}$) with rapid spatial decay. (e) V5 (exponential, B-spline): modest peak ($0.707\,\mu\mathrm{m}^{-1/2}$) reflecting endpoint width constraint. Tapered profiles (b)–(e) concentrate high fields near the narrow junction, achieving systematic field dilution compared to the uniform baseline (a).

*2. Local Loss Density and Integrated Contributions*

While Figure 3 illustrates the spatial redistribution of edge fields, the wire-loss functional $U_{\mathrm{wire}}$ depends on the full local loss density $u_k(y) = \ln[r(y)/t_{\mathrm{surf}}]/r(y)$.[24] Figure 4 shows $u_k(y)$ for all five variants; the shaded area under each curve corresponds to its contribution to $U_{\mathrm{wire}} = C\int_{-d}^{d} u(y)\,dy$.[24] The uniform wire V1 exhibits a flat profile of $10.232\,\mu\mathrm{m}^{-1}$ along the entire $100\,\mu$m length, giving the largest integrated loss $U_{\mathrm{wire}} = 783.18\,C$. By contrast, the tapered geometries concentrate loss near the junction but suppress it rapidly toward the pads: V2 and V3 reduce the integrated area by 79% and

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



86%, respectively, while the parabolic V4—despite a very sharp junction peak—confines significant loss to $|y| \lesssim 5\,\mu$m and achieves a 99.6% reduction ($U_{\text{wire}} = 3.309\,C$). The exponential V5 yields an intermediate $U_{\text{wire}} = 98.97\,C$.[24,33]

Comparing the shaded areas across panels (a)–(e) highlights why tapered wires outperform the uniform design even when their peak loss densities are higher. Because the $\ln(r/t_{\text{surf}})/r$ kernel strongly suppresses contributions from wide regions ($r \gg t_{\text{surf}}$), only the narrow junction neighbourhood plays a significant role in $U_{\text{wire}}$.[24] V1 pays a large penalty for 100 $\mu$m of constant, moderate loss density, whereas V2–V4 progressively confine this penalty to shorter segments.[24] This explains why uniform wires are intrinsically suboptimal for surface-loss minimisation: in the absence of geometric field dilution, $U_{\text{wire}}$ scales linearly with wire length, whereas in tapered designs it grows only logarithmically with the junction-to-pad separation.[24,33]

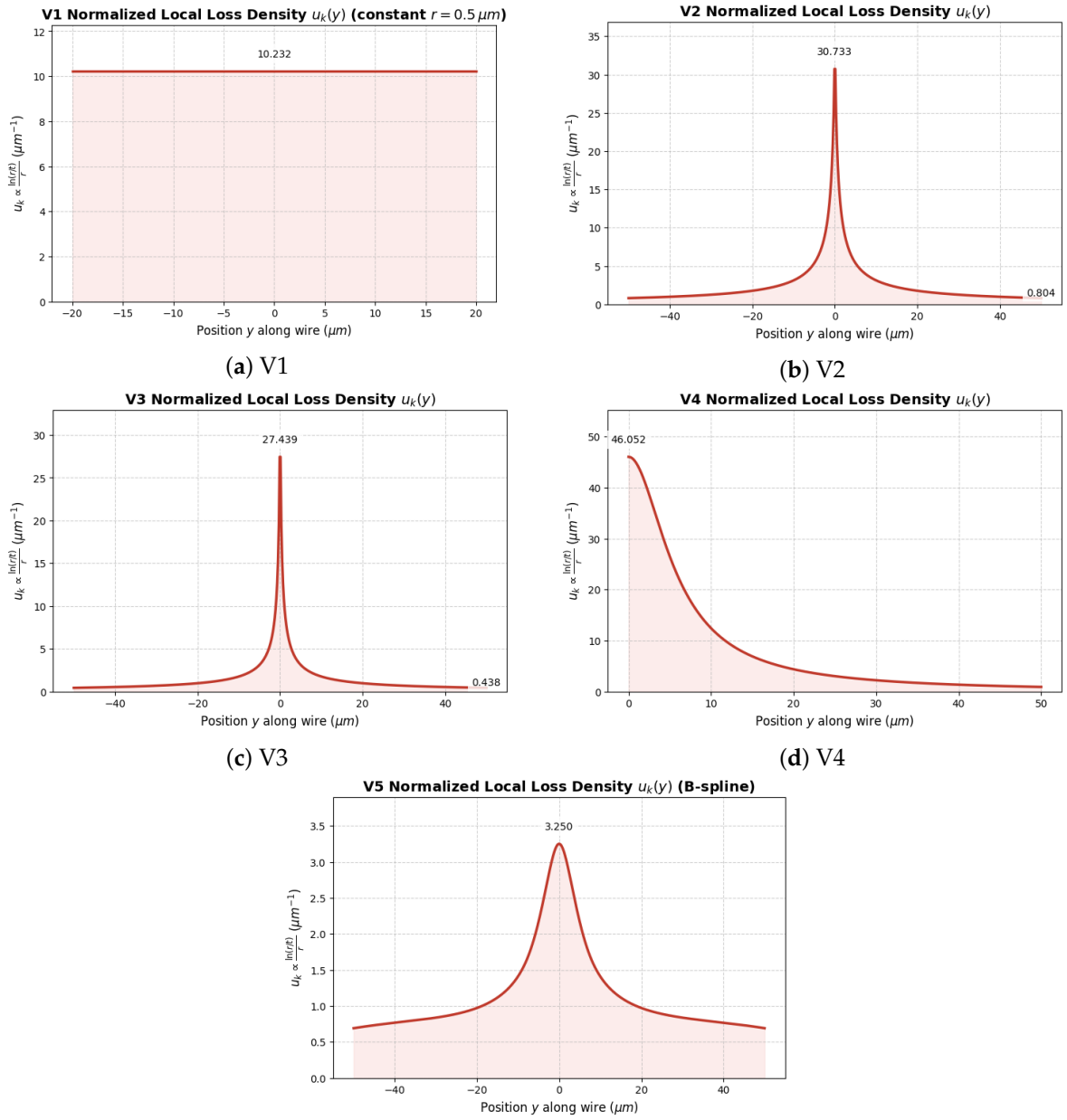



**Figure 4.** Normalised local loss density $u_k(y) = \ln[r(y)/t_{\text{surf}}]/r(y)$ for the five wire geometries. The shaded area gives each variant's contribution to the integrated loss $U_{\text{wire}}$. V1 (uniform) shows a flat profile and the largest loss. Tapered designs V2–V5 concentrate loss near the junction and strongly suppress it toward the pads, with V4 giving the most localised peak and lowest total loss, consistent with the participation-ratio reductions in Table I.

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



From Table I and Figures 3 and 4, three key conclusions emerge from this comparative analysis. First, the transition from a uniform wire (V1) to any tapered profile (V2–V5) reduces the wiring contribution from 0.0756 ppm in V1 to less than 0.02 ppm in all tapered variants, corresponding to reductions of 79% (V2), 86% (V3), 99.6% (V4), and 87% (V5). This systematic suppression of edge-field loss and local loss density translates into a measurable, though modest, coherence improvement, raising $T_1$ from 127.227 $\mu$s (V1) to a maximum of 127.323 $\mu$s (V4)—an enhancement of $\approx 0.1$ $\mu$s. While small in absolute terms, this gain is achieved purely through wire-geometry optimisation, with no change to pad dimensions, materials, or junction parameters [13,24,33].

Second, among the tapered designs, the parabolic profile (V4) achieves the lowest wire participation ratio, $p_{\text{wire}} = 0.00032$ ppm, effectively eliminating wiring loss. The B-Spline taper (V5) performs comparably to the simple linear tapers (V2, V3), demonstrating that mathematical optimality must be balanced against practical endpoint constraints [24,33]. V5's exponential growth is limited by the fixed pad-interface width (5 $\mu$m), which prevents it from fully exploiting the field-dilution advantage of rapid widening [24]. By contrast, V4's parabolic design combines aggressive linear widening near the junction (where field crowding is strongest) with an exponential tail that smoothly transitions to the pad, yielding the lowest calculated participation ratio among all variants.

Third, and most significantly, for all tapered designs the pad participation ($p_{\text{pad}} \approx 100$ ppm) constitutes more than 99.9% of the total metal-surface loss. Even in V1, the wire contribution accounts for only 0.08% of $p_{\text{MS}}$, indicating that the present architecture is already pad-dominated [14,24,33]. The absolute improvement in $T_1$ from V1 to V4 (0.1 $\mu$s) is therefore limited by pad-interface loss, which sets a practical ceiling on coherence for this geometry. Wire-geometry optimisation has effectively exhausted its potential: further gains require reducing pad-to-pad through substrate engineering (trenching, selective removal of lossy interfaces), material advances (e.g., tantalum or niobium films with lower surface loss tangents), or 3D integration schemes that spatially separate high-field regions from dielectric interfaces [14,15,30,33,37].

## IV. Design Implications and Sensitivity Analysis

The analytical participation model developed in Sec. III.A and the comparative results of Sec. III.B allow quantitative guidance for junction-wire layout in planar transmons. Although the parabolic taper V4 achieves the smallest wire participation, $p_{\text{wire}} = 0.00032$ ppm, the simple linear taper V2 already captures essentially all of the practically relevant benefit. Relative to the uniform wire V1, V2 reduces the wiring contribution from 0.0756 ppm to 0.0159 ppm, corresponding to a 79% reduction in $U_{\text{wire}}$ and a $T_1$ improvement from 127.227 $\mu$s to 127.306 $\mu$s. Moving from V2 to the more aggressive tapers provides only marginal additional gain at the device level: V3 and V4 further suppress $p_{\text{wire}}$ by 35% and 98% relative to V2, yet the corresponding increase in total coherence is only 0.005 $\mu$s (V3) and 0.017 $\mu$s (V4), i.e., $\lesssim 0.01\%$ on an absolute $T_1$ scale. Within the accuracy of typical transmon relaxation measurements, these differences would be difficult to resolve.[14,30]

From a design perspective, this suggests that a linear taper of the V2 type is close to optimal under realistic fabrication constraints. V2 maintains a minimum junction-lead width of 0.2 $\mu$m, which is comfortably within the process window of standard electron-beam and optical lithography used for Al/$AlO_x$/Al junctions, while the monotonic widening to 5 $\mu$m at the pads is compatible with common wiring densities in multi-qubit layouts.[3,18,21] More aggressive tapers, such as V3 and V4, require narrower minimum features with both designs starting at a junction-lead width of 0.2 $\mu$m—and introduce additional geometric curvature, which are expected to increase sensitivity to dose calibration, proximity-effect corrections, and alignment tolerances in practical processes.[27] Given that the analytically predicted $T_1$ advantage of V4 over V2 is only $\sim 0.017$ $\mu$s, the incremental benefit of implementing such aggressive tapers is unlikely to outweigh their increased fabrication complexity for most applications.

The robustness of these design conclusions was assessed by recomputing $p_{\text{MS}}$ for V2 while varying key material and geometric parameters within experimentally reported ranges. A $\pm 1$ nm uncertainty

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



in the effective lossy-surface thickness $t_{\mathrm{surf}}$ over the interval 2–4 nm changes $U_{\mathrm{wire}}$ by approximately $\pm 15\%$.[37] However, because $p_{\mathrm{wire}} \ll p_{\mathrm{pad}}$, the induced change in the total participation $p_{\mathrm{MS}}$ remains below 0.002 ppm, i.e., much less than 1% of the pad-dominated baseline. Similarly, a $\pm 20\%$ variation in the effective permittivity $\varepsilon_{\mathrm{eff}}$ (taken in the range 9–14) modifies the logarithmic factor $\ln[r(y)/t_{\mathrm{surf}}]$ by less than 5%, leading to negligible changes in the predicted $T_1$ ($< 0.01\,\mu$s).[39] The TLS loss tangent $\tan\delta_{\mathrm{TLS}}$ typically exhibits larger device-to-device spread (e.g., $2.0\text{–}3.5 \times 10^{-3}$), but in the present model this parameter simply rescales $p_{\mathrm{MS}}$ and therefore affects the pads and wires in the same proportion.[37] As a result, the relative benefit of tapering is essentially insensitive to reasonable variations in $\tan\delta_{\mathrm{TLS}}$.

In practice, the dominant source of $T_1$ scatter in nominally identical devices is expected to be fluctuations in the pad participation $p_{\mathrm{pad}}$. Ensemble variations in TLS density, substrate inhomogeneities, and processing-induced contamination can readily produce $\pm 20$ ppm changes in $p_{\mathrm{pad}}$, corresponding to order-percent fluctuations in $T_1$.[14] This variation is two to three orders of magnitude larger than the residual wire participation for any tapered design ($p_{\mathrm{wire}} < 0.02$ ppm), implying that once a taper such as V2 is implemented, further refinement of the junction-lead geometry ceases to be a meaningful lever for coherence. Instead, the analytical results presented here indicate that future gains must come from reducing $p_{\mathrm{pad}}$ itself—for example, through substrate trenching and interface cleaning, the use of lower-loss superconducting films such as tantalum or niobium, or 3D integration schemes that separate high-field regions from dielectric surfaces.[14,15,30,37]

A final consideration is the trade-off between wire length and taper aggressiveness. The calculations in Sec. III.B assumed a fixed half-length $d = 50\,\mu$m for all variants. In a realistic layout, however, more aggressive tapers (V3, V4) may require a larger $d$ to accommodate the same junction-to-pad separation if the minimum feature size is limited by lithography. Because the loss functional scales approximately as $U_{\mathrm{wire}} \propto d$ for a given taper profile, extending the wire to $d = 60\text{–}75\,\mu$m would partially offset the reduction gained from more aggressive widening.[24] For compact chip layouts where wiring length is constrained by the qubit footprint and coupling geometry, the analytically optimised linear taper V2 therefore offers the most attractive compromise: it achieves near-minimal wire loss within the shortest feasible wire length, while leaving pad-dominated surface loss as the primary remaining bottleneck for coherence.

## V. Conclusion

This work establishes a quasi-one-dimensional analytical framework for quantifying wiring surface loss in planar transmon qubits, enabling rapid design exploration without the computational cost of full 3D electromagnetic simulations. By applying this model to five representative geometries—ranging from uniform strips to optimized B-spline tapers—we have rigorously defined the limits of geometric loss suppression.

Our results, consistent with earlier studies on tapered junction wiring, demonstrate that[24] tapering is a highly effective strategy for mitigating edge-induced loss. All tapered profiles (V2–V5) reduce wiring participation by 79–99.6% relative to a uniform wire, with the parabolic design (V4) effectively eliminating the wiring contribution entirely ($p_{\mathrm{wire}} = 0.0003$ ppm). However, a critical analysis of the total device coherence reveals that these mathematical gains yield diminishing returns. In the current regime where surface loss is dominated by capacitor pads ($p_{\mathrm{pad}} \approx 100$ ppm)[14], the coherence improvement offered by complex, optimized shapes over a simple linear taper is negligible ($< 0.02\%$).

Consequently, we propose a definitive design rule for planar transmon layouts: a standard linear taper (V2) is sufficient to render wiring loss a non-limiting factor. More aggressive geometries, while theoretically superior, introduce unnecessary fabrication risks—such as sub-micron feature sizes and increased sensitivity to lithographic variance—without providing measurable coherence benefits. Future improvements in transmon lifetimes must therefore prioritize the reduction of pad participation through substrate trenching[14], interface engineering[11], or the adoption of alternative material platforms[5], rather than further refinement of junction-lead geometry. The analytical framework

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



presented here remains a valuable, lightweight tool for verifying these design choices across diverse qubit architectures.

## VI. Computational Methods

All results in Sec. III.B are obtained from a quasi-one-dimensional numerical implementation of the analytical wire-loss functional. The junction wiring is described by a radius profile $r(y)$ along the wire axis $y \in [-d, d]$ with fixed half-length $d = 50\,\mu$m. We consider five symmetric profiles: a uniform wire (V1), two linear tapers (V2, V3), a parabolic taper (V4), and an optimised B-spline taper (V5), defined as

$$\text{V1: } r(y) = 0.5\,\mu\text{m}, \tag{12}$$
$$\text{V2: } r(y) = (0.1 + 0.2|y|)\,\mu\text{m}, \tag{13}$$
$$\text{V3: } r(y) = (0.1 + 0.4|y|)\,\mu\text{m}, \tag{14}$$
$$\text{V4: } r(y) = (0.1 + 0.004y^2)\,\mu\text{m}, \tag{15}$$
$$\text{V5: } r(y) = r_{\text{BS}}(y), \tag{16}$$

where $y$ is in $\mu$m and $r_{\text{BS}}(y)$ is a B-spline interpolated through the symmetric control points:

$$(y, r) = \begin{cases} (0, 2.0)\,\mu\text{m} & \text{(Junction)} \\ (\pm 8, 4.5)\,\mu\text{m} & \\ (\pm 25, 9.0)\,\mu\text{m} & \\ (\pm 50, 12.0)\,\mu\text{m} & \text{(Pads)} \end{cases} \tag{17}$$

where $r_{\text{BS}}(y)$ is a monotonic cubic B-spline with the same endpoint widths as V2.

The local edge field and loss density are evaluated on a uniform grid in $y$. The edge-field scaling is

$$E_{\text{edge}}(y) \propto r(y)^{-1/2}, \tag{18}$$

and the normalised local loss density entering the surface-loss functional is

$$u_k(y) = \frac{\ln[r(y)/t_{\text{surf}}]}{r(y)}, \tag{19}$$

with $t_{\text{surf}}$ the effective lossy-surface thickness. The wire-loss functional

$$U_{\text{wire}} = C \int_{-d}^{d} u_k(y)\,dy \tag{20}$$

is evaluated using the composite trapezoidal rule; the prefactor $C$ cancels in all relative comparisons, so we work with $U_{\text{wire}}/C$.

Wire participations are obtained by normalising to the uniform geometry (V1): setting $p^{(1)}_{\text{wire}} = 0.0756$ ppm and

$$p^{(j)}_{\text{wire}} = p^{(1)}_{\text{wire}} \frac{U^{(j)}_{\text{wire}}}{U^{(1)}_{\text{wire}}}, \qquad j = 1, \ldots, 5. \tag{21}$$

The total metal-surface participation is

$$p^{(j)}_{\text{MS}} = p_{\text{pad}} + p^{(j)}_{\text{wire}}, \tag{22}$$

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



with fixed pad participation $p_{\mathrm{pad}} = 100\,\mathrm{ppm}$. The corresponding quality factor and relaxation time are

$$Q^{(j)} = \frac{1}{p_{\mathrm{MS}}^{(j)} \tan\delta_{\mathrm{TLS}}}, \qquad T_1^{(j)} = \frac{Q^{(j)}}{2\pi f_q}, \tag{23}$$

where $f_q$ is the qubit frequency and $\tan\delta_{\mathrm{TLS}}$ is an effective surface-TLS loss tangent. The product $f_q^{-1}\tan\delta_{\mathrm{TLS}}^{-1}$ is chosen such that $T_1^{(1)} = 127.227\,\mu\mathrm{s}$; the same parameters are used for all variants so that differences in $T_1$ reflect only wiring participation.

All calculations are performed in Python using NumPy and SciPy, and figures are generated with Matplotlib. The wire axis is discretised with a step size $\Delta y \leq 0.05\,\mu\mathrm{m}$; halving $\Delta y$ changes $U_{\mathrm{wire}}$ by less than $10^{-4}$ relative for all geometries, ensuring numerical convergence to better than three significant figures.

## Code Availability

The Python code of this study are available from the corresponding author upon reasonable request.

## References

1. Rajeev Acharya, Dmitry A. Abanin, Laleh Aghababaie-Beni, Igor Aleiner, Trond I. Andersen, Markus Ansmann, Frank Arute, Kunal Arya, Abraham Asfaw, Nikita Astrakhantsev, Juan Atalaya, Ryan Babbush, Dave Bacon, Brian Ballard, Joseph C. Bardin, Johannes Bausch, Andreas Bengtsson, Alexander Bilmes, Sam Blackwell, Sergio Boixo, Gina Bortoli, Alexandre Bourassa, Jenna Bovaird, Leon Brill, Michael Broughton, David A. Browne, Brett Buchea, Bob B. Buckley, David A. Buell, Tim Burger, Brian Burkett, Nicholas Bushnell, Anthony Cabrera, Juan Campero, Hung-Shen Chang, Yu Chen, Zijun Chen, Ben Chiaro, Desmond Chik, Charina Chou, Jahan Claes, Agnetta Y. Cleland, Josh Cogan, Roberto Collins, Paul Conner, William Courtney, Alexander L. Crook, Ben Curtin, Sayan Das, Alex Davies, Laura De Lorenzo, Dripto M. Debroy, Sean Demura, Michel Devoret, Agustin Di Paolo, Paul Donohoe, Ilya Drozdov, Andrew Dunsworth, Clint Earle, Thomas Edlich, Alec Eickbusch, Aviv Moshe Elbag, Mahmoud Elzouka, Catherine Erickson, Lara Faoro, Edward Farhi, Vinicius S. Ferreira, Leslie Flores Burgos, Ebrahim Forati, Austin G. Fowler, Brooks Foxen, Suhas Ganjam, Gonzalo Garcia, Robert Gasca, Élie Genois, William Giang, Craig Gidney, Dar Gilboa, Raja Gosula, Alejandro Grajales Dau, Dietrich Graumann, Alex Greene, Jonathan A. Gross, Steve Habegger, John Hall, Michael C. Hamilton, Monica Hansen, Matthew P. Harrigan, Sean D. Harrington, Francisco J. H. Heras, Stephen Heslin, Paula Heu, Oscar Higgott, Gordon Hill, Jeremy Hilton, George Holland, Sabrina Hong, Hsin-Yuan Huang, Ashley Huff, William J. Huggins, Lev B. Ioffe, Sergei V. Isakov, Justin Iveland, Evan Jeffrey, Zhang Jiang, Cody Jones, Stephen Jordan, Chaitali Joshi, Pavol Juhas, Dvir Kafri, Hui Kang, Amir H. Karamlou, Kostyantyn Kechedzhi, Julian Kelly, Trupti Khaire, Tanuj Khattar, Mostafa Khezri, Seon Kim, Paul V. Klimov, Andrey R. Klots, Bryce Kobrin, Pushmeet Kohli, Alexander N. Korotkov, Fedor Kostritsa, Robin Kothari, Borislav Kozlovskii, John Mark Kreikebaum, Vladislav D. Kurilovich, Nathan Lacroix, David Landhuis, Tiano Lange-Dei, Brandon W. Langley, Pavel Laptev, Kim-Ming Lau, Loïck Le Guevel, Justin Ledford, Joonho Lee, Kenny Lee, Yuri D. Lensky, Shannon Leon, Brian J. Lester, Wing Yan Li, Yin Li, Alexander T. Lill, Wayne Liu, William P. Livingston, Aditya Locharla, Erik Lucero, Daniel Lundahl, Aaron Lunt, Sid Madhuk, Fionn D. Malone, Ashley Maloney, Salvatore Mandrà, James Manyika, Leigh S. Martin, Orion Martin, Steven Martin, Cameron Maxfield, Jarrod R. McClean, Matt McEwen, Seneca Meeks, Anthony Megrant, Xiao Mi, Kevin C. Miao, Amanda Mieszala, Reza Molavi, Sebastian Molina, Shirin Montazeri, Alexis Morvan, Ramis Movassagh, Wojciech Mruczkiewicz, Ofer Naaman, Matthew Neeley, Charles Neill, Ani Nersisyan, Hartmut Neven, Michael Newman, Jiun How Ng, Anthony Nguyen, Murray Nguyen, Chia-Hung Ni, Murphy Yuezhen Niu, Thomas E. O'Brien, William D. Oliver, Alex Opremcak, Kristoffer Ottosson, Andre Petukhov, Alex Pizzuto, John Platt, Rebecca Potter, Orion Pritchard, Leonid P. Pryadko, Chris Quintana, Ganesh Ramachandran, Matthew J. Reagor, John Redding, David M. Rhodes, Gabrielle Roberts, Eliott Rosenberg, Emma Rosenfeld, Pedram Roushan, Nicholas C. Rubin, Negar Saei, Daniel Sank, Kannan Sankaragomathi, Kevin J. Satzinger, Henry F. Schurkus, Christopher Schuster, Andrew W. Senior, Michael J. Shearn, Aaron Shorter, Noah Shutty, Vladimir Shvarts, Shraddha Singh, Volodymyr Sivak, Jindra Skruzny, Spencer Small, Vadim Smelyanskiy, W. Clarke Smith, Rolando D. Somma, Sofia Springer,

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



George Sterling, Doug Strain, Jordan Suchard, Aaron Szasz, Alex Sztein, Douglas Thor, Alfredo Torres, M. Mert Torunbalci, Abeer Vaishnav, Justin Vargas, Sergey Vdovichev, Guifre Vidal, Benjamin Villalonga, Catherine Vollgraff Heidweiller, Steven Waltman, Shannon X. Wang, Brayden Ware, Kate Weber, Travis Weidel, Theodore White, Kristi Wong, Bryan W. K. Woo, Cheng Xing, Z. Jamie Yao, Ping Yeh, Bicheng Ying, Juhwan Yoo, Noureldin Yosri, Grayson Young, Adam Zalcman, Yaxing Zhang, Ningfeng Zhu, and Nicholas Zobrist. Quantum error correction below the surface code threshold. *Nature*, 638(8052):920–926, December 2024.

2. C. Axline, M. Reagor, R. Heeres, P. Reinhold, C. Wang, K. Shain, W. Pfaff, Y. Chu, L. Frunzio, and R. J. Schoelkopf. An architecture for integrating planar and 3d cqed devices. *Applied Physics Letters*, 109(4), July 2016.
3. R. Barends, J. Kelly, A. Megrant, D. Sank, E. Jeffrey, Y. Chen, Y. Yin, B. Chiaro, J. Mutus, C. Neill, P. O'Malley, P. Roushan, J. Wenner, T. C. White, A. N. Cleland, and John M. Martinis. Coherent josephson qubit suitable for scalable quantum integrated circuits. *Physical Review Letters*, 111:080502, Aug 2013.
4. Alexander Bilmes, Serhii Volosheniuk, Jan David Brehm, Alexey V. Ustinov, and Jürgen Lisenfeld. Quantum sensors for microscopic tunneling systems. *npj Quantum Information*, 7(1), February 2021.
5. Janka Biznárová, Amr Osman, Emil Rehnman, Lert Chayanun, Christian Križan, Per Malmberg, Marcus Rommel, Christopher Warren, Per Delsing, August Yurgens, Jonas Bylander, and Anita Fadavi Roudsari. Mitigation of interfacial dielectric loss in aluminum-on-silicon superconducting qubits. *npj Quantum Information*, 10(1), August 2024.
6. Alexandre Blais, Arne L. Grimsmo, S. M. Girvin, and Andreas Wallraff. Circuit quantum electrodynamics. *Rev. Mod. Phys.*, 93:025005, May 2021.
7. Richard L. Burden and J. Douglas Faires. *Numerical Analysis*. Cengage Learning, Boston, 10 edition, 2015.
8. Lert Chayanun, Janka Biznárová, Lunjie Zeng, Per Malmberg, Andreas Nylander, Amr Osman, Marcus Rommel, Pui Lam Tam, Eva Olsson, Per Delsing, August Yurgens, Jonas Bylander, and Anita Fadavi Roudsari. Characterization of process-related interfacial dielectric loss in aluminum-on-silicon by resonator microwave measurements, materials analysis, and imaging. *APL Quantum*, 1(2), June 2024.
9. C. Classen, E. Gjonaj, U. Römer, R. Schuhmann, and T. Weiland. Modeling of field singularities at dielectric edges using grid based methods. *Advances in Radio Science*, 9:39–44, July 2011.
10. Daniel L. Creedon, Yarema Reshitnyk, Warrick Farr, John M. Martinis, Timothy L. Duty, and Michael E. Tobar. High q-factor sapphire whispering gallery mode microwave resonator at single photon energies and millikelvin temperatures. *Applied Physics Letters*, 98(22), May 2011.
11. Oliver Dial, Douglas T McClure, Stefano Poletto, G A Keefe, Mary Beth Rothwell, Jay M Gambetta, David W Abraham, Jerry M Chow, and Matthias Steffen. Bulk and surface loss in superconducting transmon qubits. *Superconductor Science and Technology*, 29(4):044001, March 2016.
12. H. A. Dwyer and T. A. Davis. Three-dimensional singular boundary elements for corner and edge singularities in potential problems. *Engineering Analysis with Boundary Elements*, 29(4):315–337, 2005.
13. Sungjun Eun, Seong Hyeon Park, Kyungsik Seo, Kibum Choi, and Seungyong Hahn. Shape optimization of superconducting transmon qubits for low surface dielectric loss. *Journal of Physics D: Applied Physics*, 56(50):505306, September 2023.
14. Jay M Gambetta, Conal E Murray, Y-K-K Fung, Douglas T McClure, Oliver Dial, William Shanks, Jeffrey W Sleight, and Matthias Steffen. Investigating surface loss effects in superconducting transmon qubits. *IEEE Transactions on Applied Superconductivity*, 27(1):1–5, 2016.
15. Suhas Ganjam, Yanhao Wang, Yao Lu, Archan Banerjee, Chan U Lei, Lev Krayzman, Kim Kisslinger, Chenyu Zhou, Ruoshui Li, Yichen Jia, Mingzhao Liu, Luigi Frunzio, and Robert J. Schoelkopf. Surpassing millisecond coherence in on chip superconducting quantum memories by optimizing materials and circuit design. *Nature Communications*, 15(1), May 2024.
16. Jiansong Gao, Miguel Daal, Anastasios Vayonakis, Shwetank Kumar, Jonas Zmuidzinas, Bernard Sadoulet, Benjamin A. Mazin, Peter K. Day, and Henry G. Leduc. Experimental evidence for a surface distribution of two-level systems in superconducting lithographed microwave resonators. *Applied Physics Letters*, 92(15), April 2008.
17. S. M. Girvin. Circuit QED: Superconducting qubits coupled to microwave photons. In *Quantum Machines: Measurement and Control of Engineered Quantum Systems*. Les Houches Summer School, 2014.
18. S. Gustavsson, F. Yan, G. Catelani, J. Bylander, A. Kamal, J. Birenbaum, D. Hover, D. Rosenberg, G. Samach, A. P. Sears, S. J. Weber, J. L. Yoder, J. Clarke, A. J. Kerman, F. Yoshihara, Y. Nakamura, T. P. Orlando,

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



and W. D. Oliver. Suppressing relaxation in superconducting qubits by quasiparticle pumping. *Science*, 354(6319):1573–1577, Dec 2016.

19. John David Jackson. *Classical Electrodynamics*. Wiley, New York, 3 edition, 1999.
20. Solvej Knudsen and Freja Thilde Pedersen. Producing adiabatic fiber tapers: Numerical simulations and measurements, June 2014. Bachelor project, Supervisor: Assoc. Prof. Jürgen Appel.
21. Jens Koch, Terri M. Yu, Jay Gambetta, A. A. Houck, D. I. Schuster, J. Majer, Alexandre Blais, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf. Charge-insensitive qubit design derived from the cooper pair box. *Physical Review A*, 76(4), October 2007.
22. P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver. A quantum engineer's guide to superconducting qubits. *Applied Physics Reviews*, 6(2), June 2019.
23. Tu-Lu Liang, Xi Cheng, Mei Yu, Lingyan Zhang, Jin Shi, and Wei Shao. Adiabatic operation slope-loss algorithm for ultrashort and broadband waveguide taper. *Frontiers in Physics*, 10, December 2022.
24. John M. Martinis. Surface loss calculations and design of a superconducting transmon qubit with tapered wiring. *npj Quantum Information*, 8(1), March 2022.
25. Robert McDermott. Materials origins of decoherence in superconducting qubits. *IEEE Transactions on Applied Superconductivity*, 19(1):2–13, 2009.
26. Michigan State University. Chapter 14: Quasi-static approximations. PHY 842 Lecture Notes, 2014. Fall 2014.
27. Mohammad Ali Mohammad, Mustafa Muhammad, Steven K. Dew, and Maria Stepanova. Fundamentals of electron beam exposure and development. In Maria Stepanova and Steven Dew, editors, *Nanofabrication: Techniques and Principles*, chapter 2, pages 11–41. Springer, Vienna, 2012.
28. C. E. Murray. Analytical modeling of participation reduction in superconducting coplanar resonator and qubit designs through substrate trenching. *IEEE Trans. Microwave Theory Tech.*, 68:3263–3270, 2020.
29. B.-L. Najera-Santos, R. Rousseau, K. Gerashchenko, H. Patange, A. Riva, M. Villiers, T. Briant, P.-F. Cohadon, A. Heidmann, J. Palomo, M. Rosticher, H. le Sueur, A. Sarlette, W. C. Smith, Z. Leghtas, E. Flurin, T. Jacqmin, and S. Deléglise. High-sensitivity ac-charge detection with a mhz-frequency fluxonium qubit. *Physical Review X*, 14(1), January 2024.
30. Alexander P. M. Place, Lila V. H. Rodgers, Pranav Mundada, Basil M. Smitham, Mattias Fitzpatrick, Zhaoqi Leng, Anjali Premkumar, Jacob Bryon, Andrei Vrajitoarea, Sara Sussman, Guangming Cheng, Trisha Madhavan, Harshvardhan K. Babla, Xuan Hoang Le, Youqi Gang, Berthold Jäck, András Gyenis, Nan Yao, Robert J. Cava, Nathalie P. de Leon, and Andrew A. Houck. New material platform for superconducting transmon qubits with coherence times exceeding 0.3 milliseconds. *Nature Communications*, 12(1), March 2021.
31. William H. Press, Saul A. Teukolsky, William T. Vetterling, and Brian P. Flannery. *Numerical Recipes: The Art of Scientific Computing*. Cambridge University Press, Cambridge, 3 edition, 2007.
32. S. C. Schaub, M. A. Shapiro, and R. J. Temkin. Simple expressions for the design of linear tapers in overmoded corrugated waveguides. *Journal of Infrared, Millimeter, and Terahertz Waves*, 37(1):100–110, August 2015.
33. Nikita S. Smirnov, Elizaveta A. Krivko, Anastasiya A. Solovyova, Anton I. Ivanov, and Ilya A. Rodionov. Wiring surface loss of a superconducting transmon qubit. *Scientific Reports*, 14(1), March 2024.
34. Mikko Tuokkola, Yoshiki Sunada, Heidi Kivijärvi, Jonatan Albanese, Leif Grönberg, Jukka-Pekka Kaikkonen, Visa Vesterinen, Joonas Govenius, and Mikko Möttönen. Methods to achieve near-millisecond energy relaxation and dephasing times for a superconducting transmon qubit. *Nature Communications*, 16(1), July 2025.
35. J. Van Damme, S. Massar, R. Acharya, Ts. Ivanov, D. Perez Lozano, Y. Canvel, M. Demarets, D. Vangoidsenhoven, Y. Hermans, J. G. Lai, A. M. Vadiraj, M. Mongillo, D. Wan, J. De Boeck, A. Potočnik, and K. De Greve. Advanced cmos manufacturing of superconducting qubits on 300 mm wafers. *Nature*, 634(8032):74–79, September 2024.
36. J. Verjauw, A. Potočnik, M. Mongillo, R. Acharya, F. Mohiyaddin, G. Simion, A. Pacco, Ts. Ivanov, D. Wan, A. Vanleenhove, L. Souriau, J. Jussot, A. Thiam, J. Swerts, X. Piao, S. Couet, M. Heyns, B. Govoreanu, and I. Radu. Investigation of microwave loss induced by oxide regrowth in high- q niobium resonators. *Physical Review Applied*, 16(1), July 2021.
37. C. Wang, C. Axline, Y. Y. Gao, T. Brecht, Y. Chu, L. Frunzio, M. H. Devoret, and R. J. Schoelkopf. Surface participation and dielectric loss in superconducting qubits. *Applied Physics Letters*, 107(16), October 2015.
38. C. Wang, C. Axline, Y. Y. Gao, T. Brecht, Y. Chu, L. Frunzio, M. H. Devoret, and R. J. Schoelkopf. Surface participation and dielectric loss in superconducting qubits. *Applied Physics Letters*, 107(16):162601, October 2015.

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 22 April 2026 doi:10.20944/preprints202604.1559.v1



39. J. Wenner, R. Barends, R. C. Bialczak, Yu Chen, J. Kelly, Erik Lucero, Matteo Mariantoni, A. Megrant, P. J. J. O'Malley, D. Sank, A. Vainsencher, H. Wang, T. C. White, Y. Yin, J. Zhao, A. N. Cleland, and John M. Martinis. Surface loss simulations of superconducting coplanar waveguide resonators. *Applied Physics Letters*, 99(11), September 2011.
40. W. Woods, G. Calusine, A. Melville, A. Sevi, E. Golden, D.K. Kim, D. Rosenberg, J.L. Yoder, and W.D. Oliver. Determining interface dielectric losses in superconducting coplanar-waveguide resonators. *Phys. Rev. Appl.*, 12:014012, Jul 2019.

**Disclaimer/Publisher's Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.

© 2026 by the author(s). Distributed under a Creative Commons CC BY license.