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Posted Date: 17 May 2023

doi: 10.20944/preprints202305.1182.v1

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Low-Noise Amplifier and Neurostimulator in Submicron CMOS for Closed-Loop Deep-Brain Stimulation (CLDBS)

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Abstract: Deep-Brain Stimulation (DBS) is a a highly effective and safe medical treatment that improves the lives of patients with a wide range of neurological and psychiatric deceases, and has been consolidated as a first-line tool in the treatment of these conditionsin the last two decades. Closed Loop Deep-Brain Stimulation (CLDBS) pushes this tool further by automatically adjusting the stimulation parameters to the brain response in real time. In this context, this paper presents a Low-Noise Amplifier (LNA) and a Neurostimulator circuits fabricated in the low-power/low-voltage 65 nm CMOS process from the TSMC, which were designed targeting implantable applications. To achieve the best trade-off between input-referred noise and power consuption, metaheuristic algorithms were employed to determine and optimizes the dimentions of the LNA devices during the design phase. The measurement results showed that the LNA had a gain of 40.6 dB, a -3 dB bandwidth spanning over three decades from 10 Hz to 8.6 kHz, and a power consumption of 6.19 µW. Simulations results indicated an input-referred noise of 4.86 μV_{rms} for the LNA. The circuit of the Neurostimulator is a programmable Howland Current-Pump, whose measurements showed its ability to generate currents with arbitrary shapes ranging from between -325 µA to +318 µA. The simulations showed a quiescent power consumption of 0.13 µW with a zero neurostimulation current. The LNA and the Neurostimulator circuits are supplied with 1.2 V voltage and occupy a microdevice area of 145 µm × 311 µm and 88 µm × 89 µm, respectively, making them suitable for implantation in applications involving Closed Loop Deep-Brain Stimulation.

Keywords: CMOS; Closed Loop Deep-Brain Stimulation (CLDBS); Low-Noise Amplifier (LNA); neurostimulation; implantable devices

1. Introduction

Deep Brain Stimulation (DBS) is a surgical procedure that involves the implantation of a medical device called a neurostimulator (often called a brain pacemaker) that sends mild impulses to specific areas of the brain through implanted electrodes [1–3]. The electrical current used is very low in the range of µA and is injected into strategic points in the brain, which are mostly located deep within the brain tissue. This type of procedure involves inserting implantable tips, with electrodes rings at the ends, into specific points in the thalamus, subthalamic region, globus pallidus, among others. The electrodes are then connected to the neurostimulator itself by means of extension cables containing metallic wires [4]. The neurostimulator is a device with dimensions no larger than a matchbox and includes an attached battery to provide power and be able to operate [5–7].

The first current use of the DBS technique dates back to 1997, when authorization was granted by the American FDA (Food and Drug Administration) for the treatment of Parkinson's disease [8].

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Since then, and thanks to proven success, DBS has become first-line therapy option for relieving symptoms associated with neurological and movement disorders that are unresposible to other therapies [9], namely chronic pain [10,11], Parkinson's disease [12,13], tremor [14,15], dystonia [16,17], morbid obesity [18], Tourette's syndrome [19], essential tremor [20], and obsessive-compulsive disorder [21].

There are two paradigms for classifying DBS, namely open-loop DBS (also known as conventional DBS) and closed-loop DBS (also known as adaptive DBS or CLDBS) [22]. In the case of open-loop DBS, a neurologist manually adjusts the stimulation parameters every 3-12 months after implantation. On the other hand, in the case of closed-loop DBS, programming of stimulation parameters is performed automatically based on some measured biomarkers [22]. Biomarkers are acquired signals and they can have different natures, namely bioelectrical, psychological, biochemical, among others [22]. Biomarkers are essential indicators in closed-loop DBS because, based on the disease to be treated, they help to adaptively reconfigure the signals used in neurostimulation [22].

It is interesting to note that advances in the microelectronics are paving the way for the simultaneous acquisition of several types of biopotentials with the same microdevice resulting in the closed loop DBS. It was precisely this that motivated the development of the CMOS microdevice presented in this paper. Figure 1 illustrates the block diagram containing the acquisition, neurostimulator and control modules of a CMOS microdevice for application on CLDBS. The Low-Noise Amplifier (LNA) and the Neurostimulator modules presented in this paper are shown in yellow and green colors in the block diagram, respectively.

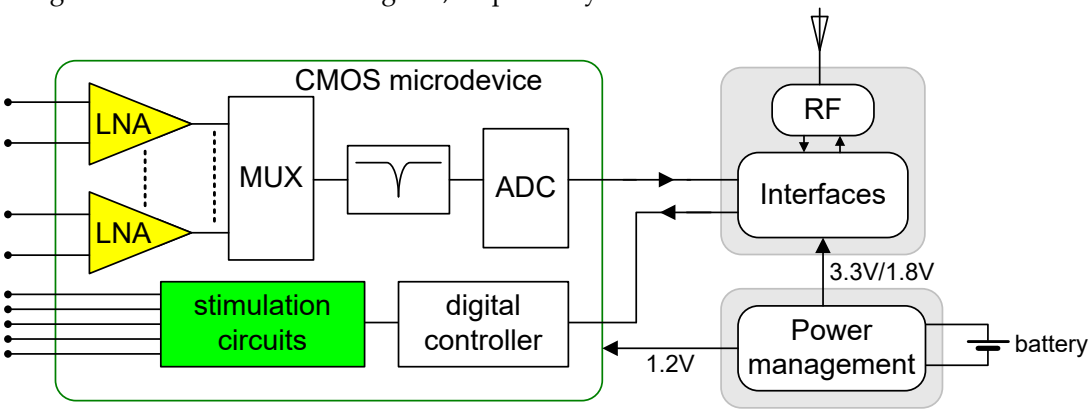

Figure 1. A block diagram of a CMOS microdevice containing the acquisition, neurostimulator and control modules for closed-loop DBS (CLDBS). The Low Noise Amplifier (LNA) and the Neurostimulator modules presented in this paper are filled with the yellow and green colors.

2. Design

The signals at the input of an LNA present a variety of challenges, such as low amplitudes, on the order of microvolts, low frequencies, very close to 0 Hz, or both. The amplifiers for neural recordings found in the literature typically exibit a mid-band gain of 40 dB, with bandwidths ranging from sub-Hz to a few kHz or even a few dozens of kHz [23–32].

Figure 2a shows the schematic of the LNA presented in this paper [32]. This amplifier is composed by an operational amplifier (OpAmp), two pairs of capacitors C_1 and C_2, and a pair of resistors R_2. The internal schematic of the OpAmp, in turn, is presented in Figure 2b. The OpAmp has a basic configuration with two stages and comprises six PMOS and four NMOS transistors. The PMOS transistors M_1 and M_2 form a differential pair, working as the input stage. The NMOS transistors M_3 and M_4 form an active pair load. The PMOS transistors M_5 and M_7 form the biasing circuit for the input and output stages, respectively. These two PMOS mirror the current I_{sd9} of M_9, multiplying it to form I_{sd5} and I_{sd7}. The NMOS M_6 forms a common source amplifier and provides additional gain to the input stage, thereby increasing the total gain of the OpAmp. The PMOS M_{8p}

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and the NMOS M_{8n} act as a resistance in series with the capacitor C_C, creating a dominant pole f_p and ensuring that the OpAmp is unconditional stable.

The calculation of the LNA gain requires the knowledge of the input and feedback impedances Z_1 and Z_2, respectively. These impedances are given by:

$$Z_1 = \frac{1}{sC_1} \tag{1}$$

$$Z_2 = \frac{1}{sC_2} // R_2 = \frac{R_2}{sR_2C_2 + 1} \tag{2}$$

The relation of the impedances Z_1 with (Z_1+Z_2), named feedback factor, is given by:

$$\frac{Z_1}{Z_1 + Z_2} = \frac{sR_2C_2 + 1}{sR_2(C_1 + C_2) + 1} = \beta \tag{3}$$

The gain of the LNA can be easily deduced if we consider V_{IM}= -V_{IP} = V_{in}/2 (Figure 2) Since the complete LNA forms a difference amplifier, the voltage V_{out} at the output of LNA, is given by:

$$V_{out} = -(\beta - 1) \times \frac{A(s)}{1 + \beta A(s)} \times V_{IM} + \frac{A(s)}{1 + \beta A(s)} \times V^+ \tag{4a}$$

$$V_{out} = -(\beta - 1) \times \frac{A(s)}{1 + \beta A(s)} \times V_{IM} + \frac{A(s)}{1 + \beta A(s)} \times \frac{Z_2}{Z_1 + Z_2} \times V_{IP} \tag{4b}$$

$$V_{out} = -(\beta - 1) \times \frac{A(s)}{1 + \beta A(s)} \times \frac{V_{in}}{2} - \frac{A(s)}{1 + \beta A(s)} \times \frac{Z_2}{Z_1 + Z_2} \times \frac{V_{in}}{2} \tag{4b}$$

where $A(s)$ is the transfer function of the OpAmp. Therefore, the gain of the LNA, i.e., the feedback gain, $A_f(s)$ is given by:

$$A_f(s) = \frac{V_{out}}{V_{in}} = -\frac{A(s)}{1 + \beta A(s)} \times \frac{Z_2}{Z_1 + Z_2} = -\frac{A(s)}{1 + \beta A(s)} \times \frac{sR_2C_1}{sR_2(C_1 + C_2) + 1} \tag{5}$$

Normally, $A(s)$ can be expressed with a single pole, or at least with a dominant pole close to the origin. However, additional poles must be considered if they exists and are located near the pass-band of the LNA. The one-pole appoximation is a useful and general model, employed here for deducing the feedback gain and to understanding the frequency behavior of the LNA. Taking the example of the existence of only one pole, the OpAmp transfer function $A(s)$ is given by:

$$A(s) = \frac{V_{out}}{V_{in}} = \frac{A_0}{s(\frac{1}{2\pi f_p}) + 1}, \; A_0 \gg 1 \tag{6}$$

Now, by substituting $A(s)$ into equation (5), a new expression for the LNA is found:

$$A_f(s) = -\frac{2\pi f_p A_0 R_2 C_1 s}{s^2 R_2(C_1 + C_2) + s[2\pi f_p R_2(A_0 C_2 + C_1 + C_2) + 1] + 2\pi f_p(A_0 + 1)} \tag{7}$$

It must be noted that the transfer function of the LNA has a zero at 0 Hz and two negative poles, which are called p_L = -1/(2πf_L) and p_H = -1/(2πf_H) (f_L and f_H are postive real numbers). If A_0 is such that $A_0 \gg 1$, then, $2\pi f_p A_0 \gg 1/(R_2C_2)$, i.e., the gain × bandwidth product (GBW) of the OpAmp is such that $GBW \gg 1/(R_2C_2)$, the expression for $A_f(s)$ can be approximated as:

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$$A_f(s) \approx -\frac{2\pi f_p A_0 R_2 C_1 s}{s^2 R_2 (C_1 + C_2) + s(2\pi f_p A_0 R_2 C_2) + 2\pi f_p A_0} \tag{8}$$

Additionaly, if the two poles p_L and p_H are well spaced between one to each other and assuming that $p_L << p_H$, then, the approximated values for f_L and f_H can be found as follows:

$$f_H \approx f_p A_0 \times \frac{C_2}{C_1 + C_2} = GBW \times \frac{C_2}{C_1 + C_2} \tag{9}$$

$$f_L \approx \frac{1}{2\pi R_2 C_2} \tag{10}$$

and relation (8) can be rewritten as:

$$A_f(s) \approx -\frac{ks}{(\frac{s}{2\pi f_L} + 1)(\frac{s}{2\pi f_H} + 1)} \approx -\frac{R_2 C_1 s}{\left(\frac{s}{2\pi f_p A_0 \times \frac{C_2}{C_1 + C_2}} + 1\right) \times (sR_2 C_2 + 1)} \tag{11}$$

For medium frequencies operation, i.e., $f_L << frequency << f_H$, the LNA gain is then:

$$A_f = \frac{C_1}{C_2} \tag{12}$$

which is in accordance with what is stated in literature [32].

The capacitances C_1 and C_2 are in the order of pF, therefore, the resistor R_2 must be in the order of TΩ, to ensure that the first pole $f_L=1/(2\pi R_2 C_2)$ of $A_f(s)$, equation (8), has a value near or lower than 1.0 Hz.

High-value resistors, like R_2, can not be implemented in a conventional form in an integrated circuit due to the large area they would occupy.

Pseudo-resistors are a widely recognized method for implementing high-value resistors, as described in references [33]. Figure 2a also illustrates the implementation of resistors R_2 with pseudo-resistors. Each of these pseudo-resistors employs a series of two PMOS transistors, as detailed in the zoomed section of the figure. It has been found that these pseudo-resistors can reach values in the order of TΩ and occupy an area many orders of magnitude smaller than that of a conventional resistor implementation. These implementations are called "pseudo" because they mimic the behavior of a real resistor when small voltages are applied at their terminals. The red dots at terminal A of the pseudo-resistors R_2 serve to show how these pseudo-resistors connect to the LNA.

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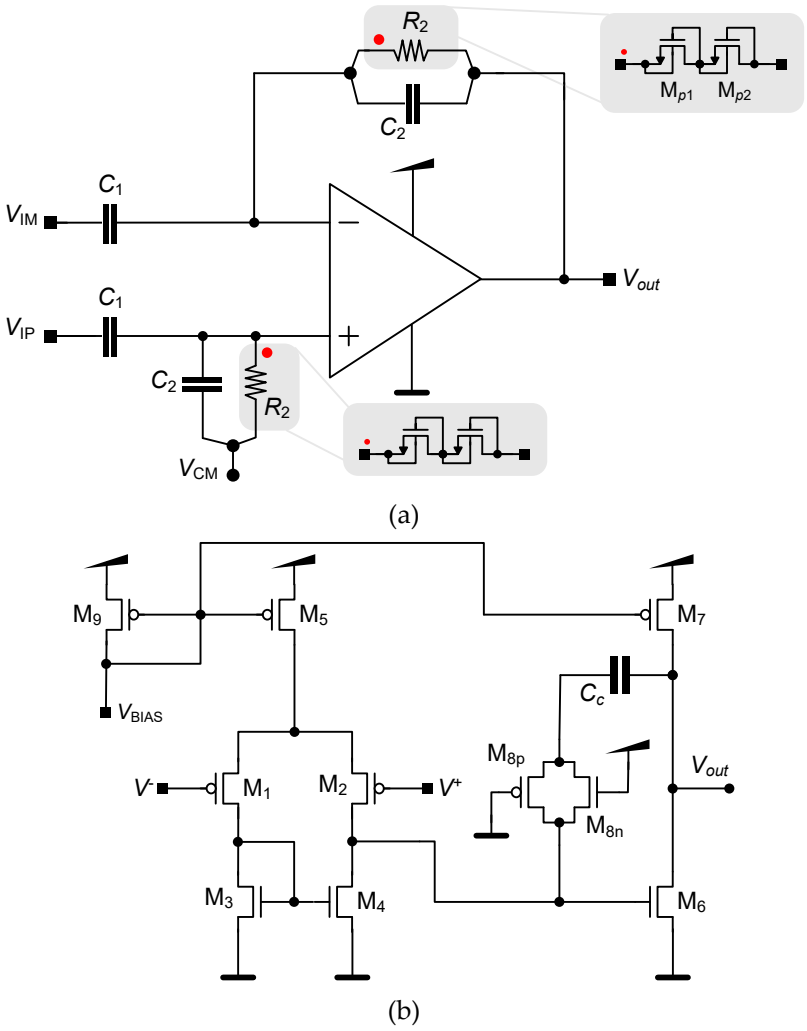
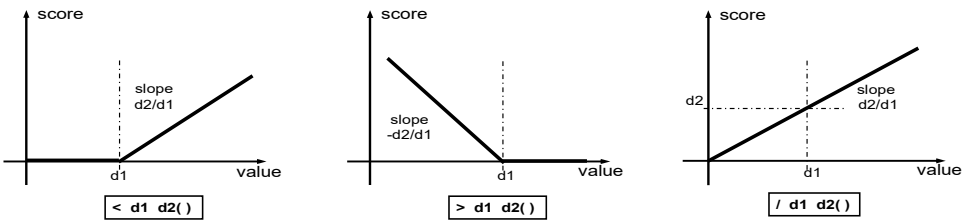


Figure 2. Schematics (**a**) of the Low-Noise Amplifier, and (**b**) of the OpAmp.

To achieve low noise and low power, even using an OpAmp with a simple configuration, the LNA design in this work was done through the use of metaheuristic algorithms, specifically particle swarm and simulated annealing [34,35]. To accomplish this task, a framework for transistor sizing and circuit optimization, based on metaheuristics, was applied. The framework requires for its operation a rating score for each design, obtained through electrical simulations. To acquire the design score, an aggregated objective function must be developed that generates a simulation file containing the circuit netlist, device sizes, and simulation commands. The function also triggers an electrical simulation, reads the results, and calculates the score. To carry out this calculation, the relevant circuit attributes are measured and predefined shaping functions. Figure 3, which reflect desired goals, are applied to the measured values. Finally, the fuction outputs are combined to build the score. Users can choose which shaping function to apply for each attribute result, enabling them to tailor the sizing and optimization to their specific needs. For example, if an attribute must be kept below a certain limit, the function **< d1 d2( )** can be used; if the attribute should be minimized, the function **/ d1 d2( )** is applied.



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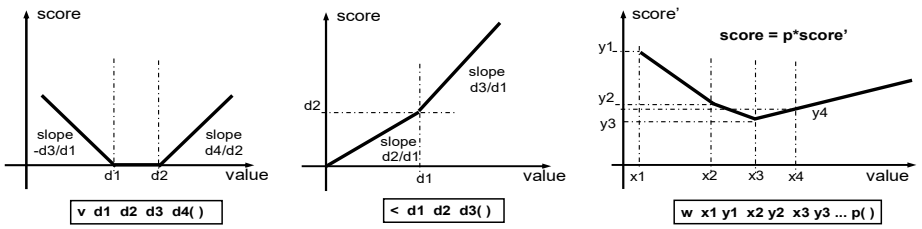

Figure 3. Shaping function examples (Output Score × Input Value).

Objective functions are tailored to specific classes of circuits, such as Voltage Reference Sources, OpAmps, Oscillators, Prescalesr, and neuronal LNAs. Once the objective function of a class is available, the framework will make possible the sizing/optimization of any circuit topology for which a SPICE like parameterized netlist, describing this particular topology, is provided. In Figure 4 is shown part of the parameterized SPICE netlist of the LNA (Figure 2 presents the circuit described in the netlist). For the netlist, X1, .., X12 are the circuit parameters that provide the device dimensions, and their values will be adjusted in the sizing/optimization process. The level of detail included in the netlist, such as the areas and perimeters of the transistor drain/source, parasitic elements, etc., as well as the knowledge embedded in it, such as the fact that dimensios of M5 and M7 shoud be related to avoid a systematic offset, directly affects the quality of the optimization.

```
M1 1 in 4 4 pch L='X1*1u' W='X5*1u' AD='X5*1u*Wpadrao/2' PD ='X5*1u Wpadrao'
+AS= 'X5*1u*Wpadrao/2' PS = 'X5*1u + Wpadrao'
M2 3 ip 4 4 pch L='X1*1u' W = 'X5*1u' AD='X5*1u*Wpadrao/2' PD='X5*1u + Wpadrao'
+AS = 'X5*1u*Wpadrao/2' PS = 'X5*1u + Wpadrao'
M3 1 1 vs vs nch L ='X2*1u' W='X6*1u' AD='X6*1u*Wpadrao/2' PD ='X6*1u + Wpadrao'
+M = 'nint(X12)'
M4 3 1 vs vs nch L='X2*1u' W= X6*1u' AD='X6*1u*Wpadrao/2' PD ='X6*1u + Wpadrao'
+M = 'nint(X12)'
M5 4 bias vd vd pch L='X3*1u' W='X7*1u' AD='X7*1u*Wpadrao/2' PD='X7*1u + Wpadrao'
+M = '2*nint(X12)*nint(X8)'
M6 out 3 vs vs nch L='X2*1u' W='X6*1u' AD ='X6*1u*Wpadrao/2' PD ='X6*1u
+Wpadrao'
M7 out bias vd vd pch L = 'X3*1u' W='X7*1u' AD='X7*1u*Wpadrao/2' PD='X7*1u + Wpadrao'
+M= 'nint(X8)'
*** compensation
M8n 3 vd 5 vs nch L ='X4*1u' W ='X9*1u' AD ='X9*1u*Wpadrao/2' PD = 'X9*1u + Wpadrao'
+As = 'X9*1u*Wpadrao/2' Ps ='X9*1u + Wpadrao'
M8p 3 vs 5 vd pch L = 'X4*1u' W = '2*X9*1u' AD = '2*X9*1u*Wpadrao' PD = '2*X9*1u
+Wpadrao' +AS = '2*X9*1u*Wpadrao' Ps = '2*X9*1u + Wpadrao'
Cc 5 out 'X10*1p'
** Bias
M9 bias bias vd vd pch L = 'X3*1u' W = 'X7*1u' AD = 'X7*1u*Wpadrao/2' PD = 'X7*1u
 +Wpadrao'
* external bias current
Ibb bias 0 DC '(10^X11)*1u'
```

Figure 1 Parameterized SPICE netlist for AmOp of Figure 2. X1, .. X12 are the wanted parameters of the sizing/optmization process.

The framework has already been employed for design of Reference Voltage Sources [36], OpAmps, LNAs, VCOs, Prescalers [37], etc. The metaheuristics available in it are genetic algorithms (GA), simulated annealing (SA), particle swarm (PSO), quatum QPSO (QPSO) among others.

In Figure 5 the operation flux of the framework is detailed. The sizing/optimization process starts with the selection of a circuit class for which an objective function is available. Next, a topology of the specified class is chosen, along with some parameter values (power supply, operation frequency),

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the goals of the sizing/optimization (power consuption, noise, gain, etc.), the shaping functions applied to each goal, and the search space (minimum and maximum allowed values for circuit parameters to be sized). Finally, a metaheuristic, along with execution conditions (initial solutions, stop condition, etc.) is selected, and the sizing/optimizing process begins. The process will continue until the stop condition is met, and the duration of the process can vary from a few minutes to several hours, depending on factors such as the size and operation of the circuit, the performed simulations, and the stop condition employed. In this work, the number of evaluated circuits was used as the stop condition.

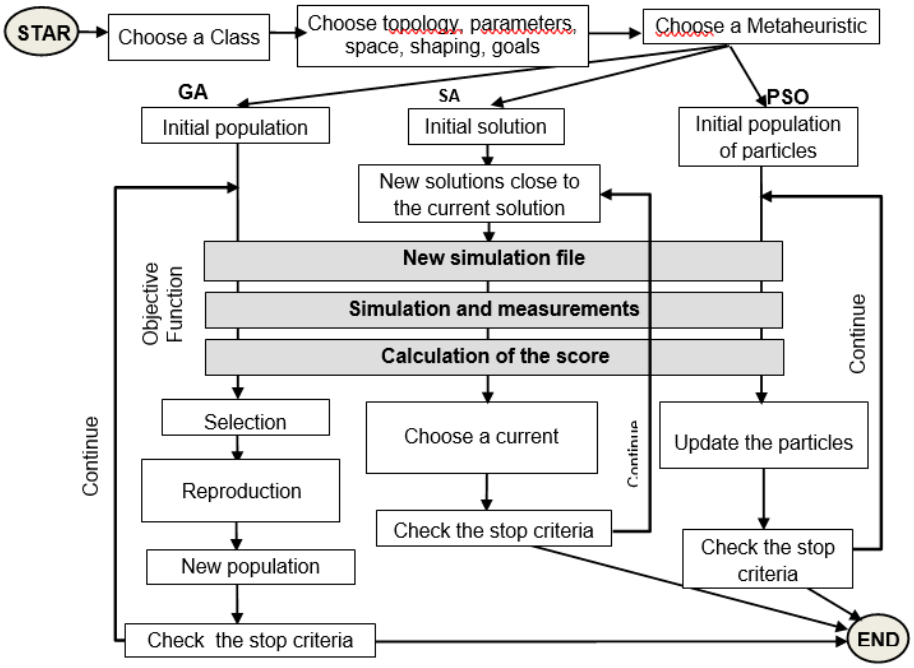

Figure 5. Sizing/optimization framework flowchart.

For the design of a circuit, one or more sizing/optimization processes were performed. When multiple processes are applied, they may or may not be independent. In the latter case, the results of the optimization are used as initial conditions for the next.

For the calculation of the design score in the neuronal LNA class, the following attributes are taken in consideration: the Differential gain, Common Mode gain, CMRR (Commum Mode Rejection Rate), PSRR (Power Supply Rajection Rate), common mode volatage range, slew rate, and phase margin of the AmpOp; the gain, power consuption, input noise, low and high cut off frequency, and area of the LNA. The evaluations of the area do not require simulations and are estimated based on the width and length of the transistors and of capacitors.

Table 1 presents the simulated characteristics of the final version of the sized/optmized LNA.

Table 1. LNA characteristics for the corner models (power supply equal to 1.2 V). The biasing of the circuit is achieved by connecting a bias resistor of 4.4 MΩ between the V_{BIAS} node (Figure 2b) and ground.

Characteristics	Value tt	Value ss	Value ff	Value sf	Value fs
OpAmp					
Differential gain [dB]	76.6	76.7	75.1	76.2	76.9
Common Mode Rejection Rate [dB] (CMRR)	72.8	71.1	70.4	74.7	70.9

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Power Supply Rejection Rate [dB] (PSRR)	71.7	69	74	72.8	70.4
Phase Margin [º]	48	40	37	41	42
Slew Rate [V/µs]	0.138	0.132	0.145	0.142	0.134
LNA					
Gain [dB]	40.43	40.66	40.1	40.19	40.78
Low cut off frequency (-3 dB) [Hz]	19	13.3	32.6	24.5	16.3
High cut off frequency (-3 dB) [kHz]	9.0	8.1	10.1	9.8	8.1
Power consumption [µW]	6.19	5.85	6.5	6.4	5.97
Input noise [μV_{rms}]	4.86	4.85	4.84	4.72	5.03

Note that during the design otimization, an input noise of 4.0 µVrms was initially specified. However, achieving this level of noise requires a significant amount of power consuption in the technology applied, due to various factors, including the large gate capacitance of the diferential pair transistors, M_1 and M_2. Technologies with larger minimum dimensions, like 180 nm technology, can be advantageously used in the design of low noise LNAs.

Several neural amplifiers aim for noise floors as low as 1-3 µVrms, which is significantly below the cortical recording noise [23,26]. For this reason, in our design, we increased the input noise while maintaining a low power consuption.

Table 2 lists the dimensions of the MOSFETs of the OpAmp and of the pseudo-resistors and the value of the capacitor C_c generated by the sizing/optimization algorithms. The listed Total (W/*L*) refers to the total value ratio and the other columns refere to the numer of paralel transistors and number of fingers applied. For example, the transistors M_1 and M_2 with Total $(W/L)_{1,2}$=(59 µm/0.52 µm) are composed of two parallel transistors, each with dimensions of (24.5 µm/0.52 µm) and, at the same time, containing ten fingers measuring (2.45 µm/0.52 µm). In another example, the transistor M_5 with Total $(W/L)_5$=(48 µm/2.22 µm) is composed by twenty four parallel transistors, each with dimensions of (2 µm/2.22 µm) containing only one finger for each of the twenty-four parallel transistors. The capacitor C_C was composed by 36 sub-capacitors of MIMcap type, which are connected in parallel and form a 6 × 6 array arrangement. Each sub-capacitor cell measures 10 µm × 10 µm.

Table 2. Dimensions of the MOSFETs that comprises the OpAmp and the pseudo-resistors, and the value of the capacitor C_c, obtained with the optimizer.

MOSFET	Total (*W*/*L*)	Multiplier (parallel MOSFETs)	Fingers/multiplier
M_1, M_2	59 µm/0.52 µm	2	10
M_3, M_4	25 µm/14.9 µm	2	1
M_5	48 µm/2.22 µm	24	1
M_6	12.5 µm/14.9 µm	1	1
M_7	12 µm/2.22 µm	6	1
M_{8n}	1.55 µm/12 µm	1	1
M_{8p}	3.1 µm/12 µm	1	1
M_9	2 µm/2.22 µm	1	1
Pseudo-resistors	12 µm/0.6 µm	1	1
Capacitor	**Total value**	**Type**	**Sub-capacitor size**	**Nr. of sub-capacitors**
C_c	7.5 pF	MIMcap	10 µm × 10 µm	36 (6 × 6 array)

2.2. Neurostimulator

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The neurostimulators must preferably provide current pulses with biphasic shape due to electrical safety reasons, such as avoiding the accumulation of charges at the interfaces between the electrodes and the ionic species within the neuronal tissue [39]. Figure 6a,b illustrate two examples of pulse shaping, where the durations (or stimulation times), frequency, amplitudes, and interpulses delay of the pulses can be settled according medical requirements. The mean value of the signals is zero on both examples in Figure 6a,b, thanks for the arbitrary pulse shaping. The neurostimulator presented in this paper can generate other types of pulses with arbitrary shapes, gradients, amplitudes and mean values.

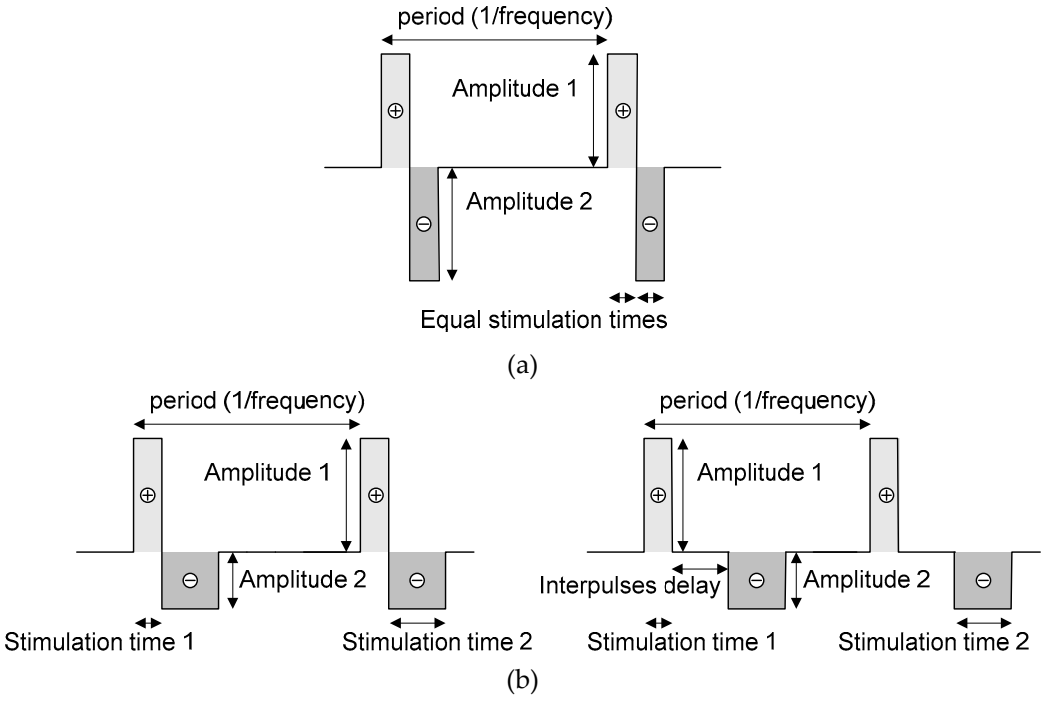

Figure 6. (a) Example of symmetric biphasic pulse shape without interpulses delay and mean value of zero, and (b) two examples of asymmetric biphasic pulse shape, with zero (on left) non-zero (on right) interpulses delay and also with mean value of zero.

To maintain electrical safety, as previously mentioned, the neurostimulator circuit was designed to offer the capability of generating current with a biphasic waveform, which can invert the direction of charge injection in the neuronal tissue. The phenomenon to nullify charge accumulation is called charge balance [39]. Traditionally, the inversion of the current direction requires a bridge with H-topology [40], with the disadvantage of requiring four transistors for current inversion, increasing the number of necessary components and the programming complexity. However, the biggest disadvantage of the H-topology is that it requires access to two different contact points on the electrodes, which are normally unipolar. For these reasons, the circuit responsible for injecting the current into the electrodes is based on the Howland Current-Pump [41]. This circuit is easy to integrate because it uses low resistance values, that is, below 20 kΩ.

Figure 7a shows the schematic of the Current-Pump that implements the neurostimulator, which is a Howland Current-Pump circuit. The neurostimulator is composed by an OpAmp and four resistors {R_1, R_2, R_3, R_4}, all fully implemented using the mask layers of the TSMC 65 nm CMOS process.

Figure 7b presents the schematic of the OpAmp used by the Current-Pump. The PMOS M_8 also works as resistance Rc in series with the capacitor C_c. The series combination of Rc/C_c is placed in parallel with the capacitor C_x to form a struture that ensures unconditional stability of the OpAmp.

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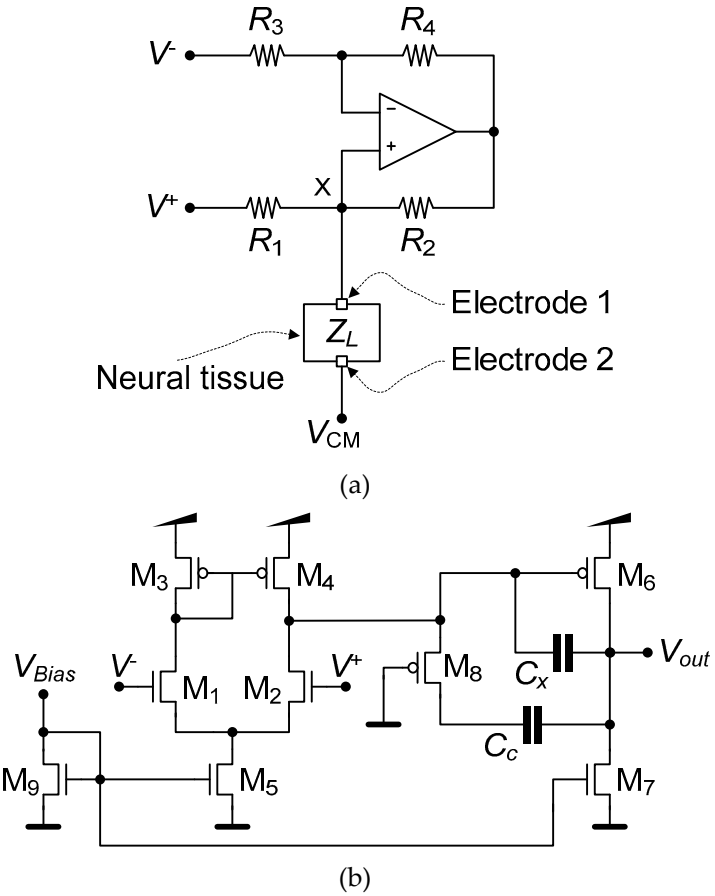

Figure 7. Schematics (a) of the Current-Pump that implements the neurostimulator, and (b) of the OpAmp used by the Current-Pump.

Table 3 lists the dimensions of the MOSFETs of the OpAmp and the internal capacitance *Cx* generated by the sizing/optimization algorithm. The relations (*W*/*L*) listed in the table follows the same logic of the relations in the Table 2. The same applies to the capacitors *Cc* and *Cx*.

Table 3. Dimensions of the MOSFETs that comprises the OpAmp, the value of the capacitor C_x, and the resistors used by the Howland Current-Pump.

MOSFET	**Total (*W*/*L*)**	**Multiplier (parallel MOSFETs)**	**Fingers/multiplier**
M_1, M_2	14.8 µm/0.24 µm	2	1
M_3, M_4	4.68 µm/0.18 µm	2	2
M_5	14.4 µm/0.36 µm	1	10
M_6	18.72 µm/0.18 µm	2	6
M_7	28.8 µm/0.36 µm	2	10
M_9	0.80 µm/0.36 µm	1	1
MOSFET	**Total (*W*/*L*)**	**Number of MOSFETs in series with common gate connections**	**Fingers/each series multiplier**
M_8	0.51 µm/7.2 µm	4	1
Capacitor	**Total value** **Type**	**Sub-capacitor size**	**Nr. of sub-capacitors**

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C_c	2.5 pF	MIMcap	10 µm × 10 µm	12 (4 × 3 parallel array)
C_x	417.2 fF	MIMcap	10 µm × 10 µm	2 (2 × 1 parallel array)
Resistor	**Total value**	**Type**	**Nr. of sub-resistors**	
R_1, R_2	≈3.52 kΩ	P^+ poly resistor without salicide (rppolyw0), $R_{\square}$≈690 Ω	Parallel of 2 series, each series composed by 2 subresistors of ≈3.52 kΩ	
R_3, R_4	≈24.61 kΩ		Parallel of 2 series, each series composed by 2 subresistors of ≈24.61 kΩ	

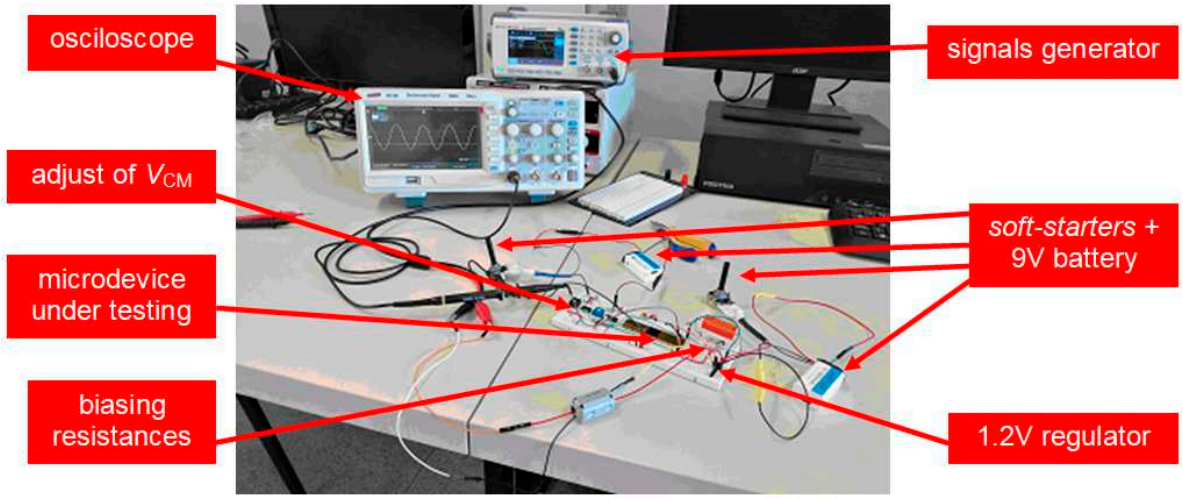
3. Experimental Results

3.1. LNA

Figure 8a illustrates a photograph of the laboratory setup used during the experimental tests. Figure 9b illustrates how the common-mode voltage V_{CM} is produced. The circuit to produce the V_{CM} voltage uses a commercial Operational Amplifier TL081 with a symmetrical voltage supply of ±9 V, which is powered by two 9V batteries to ensure low noise at the output. The voltage supply of 1.2 V for the CMOS microdevice is obtained with the AMS1117 voltage regulator. In addition, each battery is connected in series with two potentiometers working as soft starters to prevent potential high gradients of charge currents of the MOSFET parasitic capacitances, particularly those used in the inputs of the LNA. The gate areas of the MOSFETs in the inputs of the LNA present high values, such as 59 µm × 0.52 µm, and, in consequence, a high gate capacitance.

Figure 8c shows the measured gain for several common-mode voltages V_{CM} and input signals with amplitude of 2 mV_{pp}. Figure 8d also shows the measured gain for several common-mode voltages V_{CM} and input signals with amplitude of 10 mV_{pp}. In both sets of plots, the simulation results are also shown (solid blue) to allow comparisons.

Table 4 lists the measured common-mode voltage $V_{CM,out}$ at the output of LNA and its maximum gain G_{max} in terms of the input voltage V_{in} and the common-mode voltage V_{CM}.



(a)

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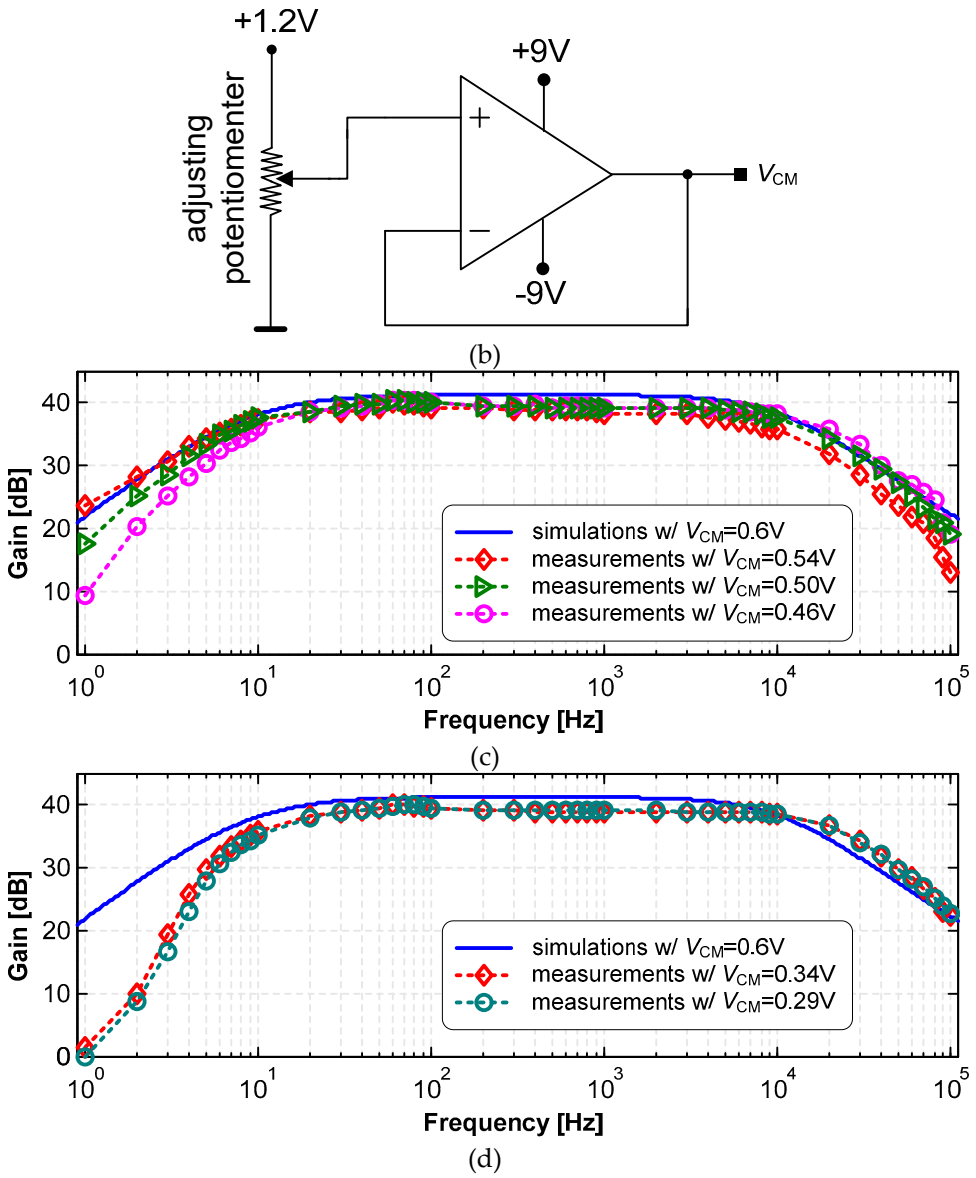

Figure 8. (a) Photograph of the experimental setup used to obtain the gain and bandwidth characteristics of the LNA. (b) The electronic circuit used to adjust the various common-mode voltages V_{CM} of the LNA. (c Plots of the measured gain with the input signals with an amplitude of $2mV_{pp}$ that was measured for several values of V_{CM}. (d) Plots of the measured gain with the input signals with an amplitude of $10mV_{pp}$ that was measured for several values of V_{CM}. Both sets of plots in (c) and (d) are compared with the simulations (line in solid blue).

Table 4. Measured common-mode voltage $V_{CM,out}$ and the maximum gain G_{max} at the output of LNA.

V_{in} [mV_{pp}]	V_{CM} [V]	$V_{CM,out}$ [V]	G_{max} [dB]
2	0.54	0.92	40.0
	0.50	0.6	40.6
	0.46	0.53	40.6
10	0.34	0.6	40.1
	0.29	0.63	40.2

The measurements, in general, agree well with the simulations. An increase in the common-mode voltage (V_{CM}), as depicted in Figure 8c, results in an improvement of the gain at low frequencies,

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but a corresponding degradation at high frequencies gains. On the other hand, the variations in V_{CM} within the range of [0.46, 0.54] V did not result in significantly different gains, thus demonstrating the robustness of this LNA with respect to V_{CM}, and amplifying the range of interest for acquiring neuronal signals with practically unchanged gain, resulting in a low potential for linear distortion of the signals during amplification.

The biasing voltage applied in the tests was V_{BIAS} = 0.68 mV, obtained using a bias resistence R_{BIAS} = 810 kΩ connected to the V_{bias} node, Figure 2b. This resulted in a biasing current I_{BIAS} = 770 nA, higher than the designed value. Even in such conditions, the LNA behavior is satisfactory, except by the total power consuption of 27.7 µW,

This LNA was also tested with a saline solution to emulate an *ex-vivo* situation and evaluate its performance in real *in-vivo* applications. Figure 9a illustrates a photograph of the experimental setup used in these measurements, while Figure 9b presents the measured gain for signals injected into the saline solution with an amplitude of 20 mV_{pp}. It should be noted that this was not the amplitude at the input of the amplifier, which was measured simultaneously with the amplitude at the output of LNA to calculate the LNA gain.

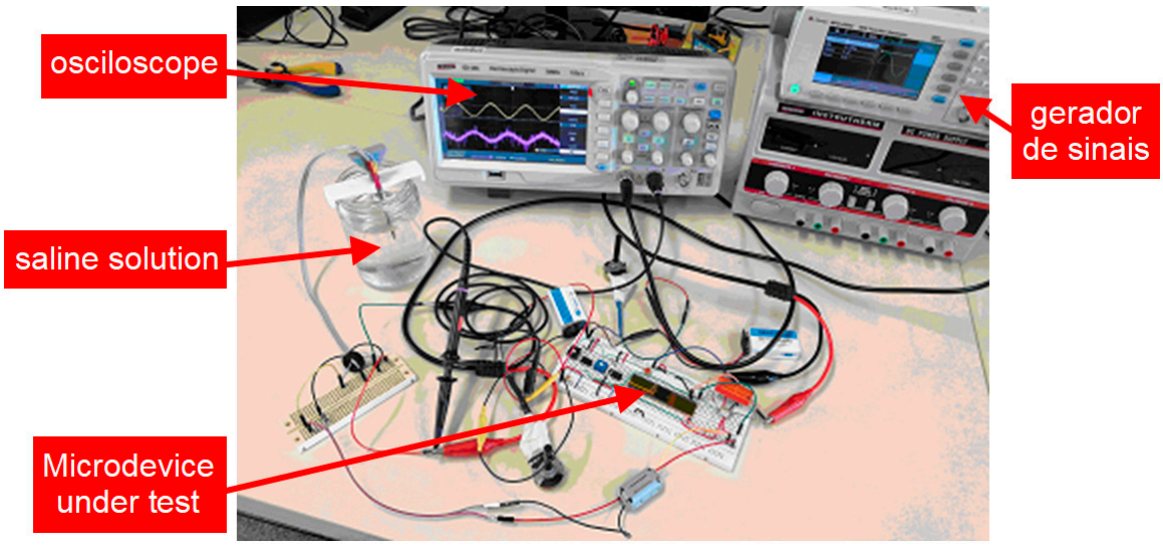
During the tests with saline solution, it was not possible to completely compensate for the effects of 60 Hz interference for input signals with frequencies less than 20 Hz. As a result, it was impossible to accurately characterize the LNA at these low frequencies. However, above 20 Hz, the gains, red points on the plot of measured gain, were easily and accurately measured. As seen in Figure 9b, the gain did not show any appreciable reduction in the frequency range between 20 Hz and 10 kHz. In fact, it is possible to observe that the gain remained high, with its maximum value of 40.1 dB at 30 Hz.

3.2. Neurostimualtor Circuit

The tests of this electronic module can be divided in static and dynamic tests. In static tests, the signals applied to the circuit do not change over time. On the other hand, in the dynamic tests, the different signals vary over time. The experimental setups used for both types of tests are essentially the same, except for the way in which the test signals were generated.

Figure 10a illustrates the schematic of the experimental setup for the static characterization of the neurostimulator circuit. This setup comprise a voltage follower, implemented with the operational amplifier TL084, to generate the common-mode voltage $V_{CM,electrode}$ applied in the reference terminal of the electrode. The implantable electrode is represented by the load resistor R_{LOAD}.

Although it is possible to apply a resistor between the gate of M_9 node and V_{dd}, Figure 7b, to bias the OpAmp, it is more convenient to apply a voltage V_{BIAS} directly to this node, since an external voltage can be easily ajusted, making the testing process simpler. A circuit similar to the one used to generate $V_{CM,electrode}$ was also used to generate and trim the bias voltage V_{BIAS}, which was settled to 315 mV.



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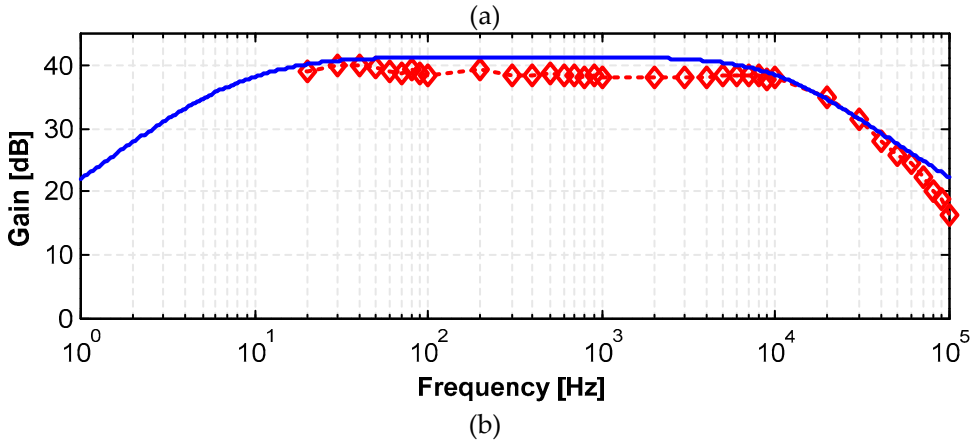

Figure 9. (a) Photograph of the experimental setup used in the characteristics of the LNA in saline solution. (b) Plot of the measured gain for signals injected into the solution with amplitude of 20mV$_{pp}$.

The circuits used for generating the common mode voltages are similar to the one presented in Figure 8b, where the V_{CM} adjustment was done manually. The manual adjustament is not a real problem in our setup because only a few common-mode voltages were needed. Specifically, the common-mode voltage V_{CM} in the reference electrode was set between 0 V and 1.2 V in coarse steps of 0.3 V.

Two breakout boards based on the MCP4725 digital-to-analogue converter (DAC) with an I²C interface were used to provide fine tuning adjustments to the inputs V^+ and V^- and, thus, precise adjustments of the currents injected into the load resistor R_{LOAD}. An Arduino board was selected to control the DACs.

Figure 10b shows a photograph of the experimental setup used in the static characterization of the Current-Pump. Figure 10c illustrates the currents for the various combinations of control and common mode voltages {V^+, V^-, $V_{CM,electrode}$} in "raw" form to allow a clear and immediate visualization of the wide and quasi-symmetrical range of currents that are possible to generate with this Current-Pump. In contrast, Figure 10d illustrates the currents parameterized in terms of the reference voltage of the electrode $V_{CM,electrode}$ and the inverting input voltage V^-. The output current was determined by the following expression:

$$I_{out} = \frac{V_{out} - V_{CM,electrode}}{R_{LOAD}} \quad (13)$$

where V_{out} is the output voltage of Current-Pump (node X in Figure 8a)

A load resistance of R_{LOAD} = 986.5 Ω was used for these tests. The output voltage V_{out} can range from 0 V to 1.2 V, therefore, the output current I_{out} can either be positive or negative, simply making the voltage of the reference electrode $V_{CM,electrode}$ either equal to 0 V or 1.2 V, respectively. As it is possible to observe in Figures 12c,d, other intermediate currents are possible to be generated. The inversion of current direction is mandatory in Deep Brain Stimulation applications.

The Current-Pump was able to generate stimulation currents from -325 µA to +318 µA. The path marked with the dashed yellow lines in Figure 12d illustrates how continuous current signals can be generated from -325 µA to +318 µA.

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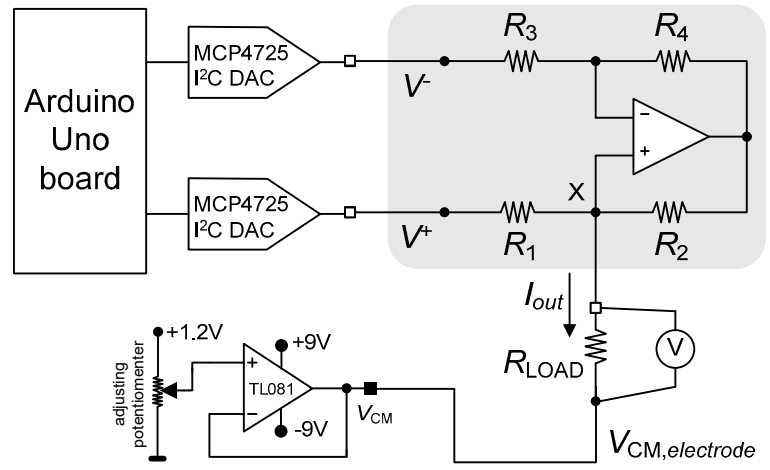

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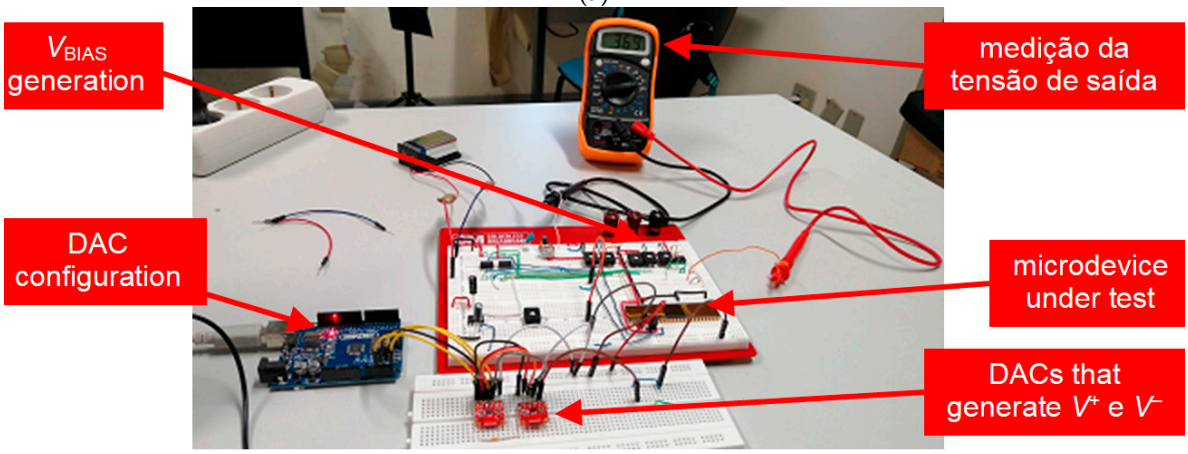

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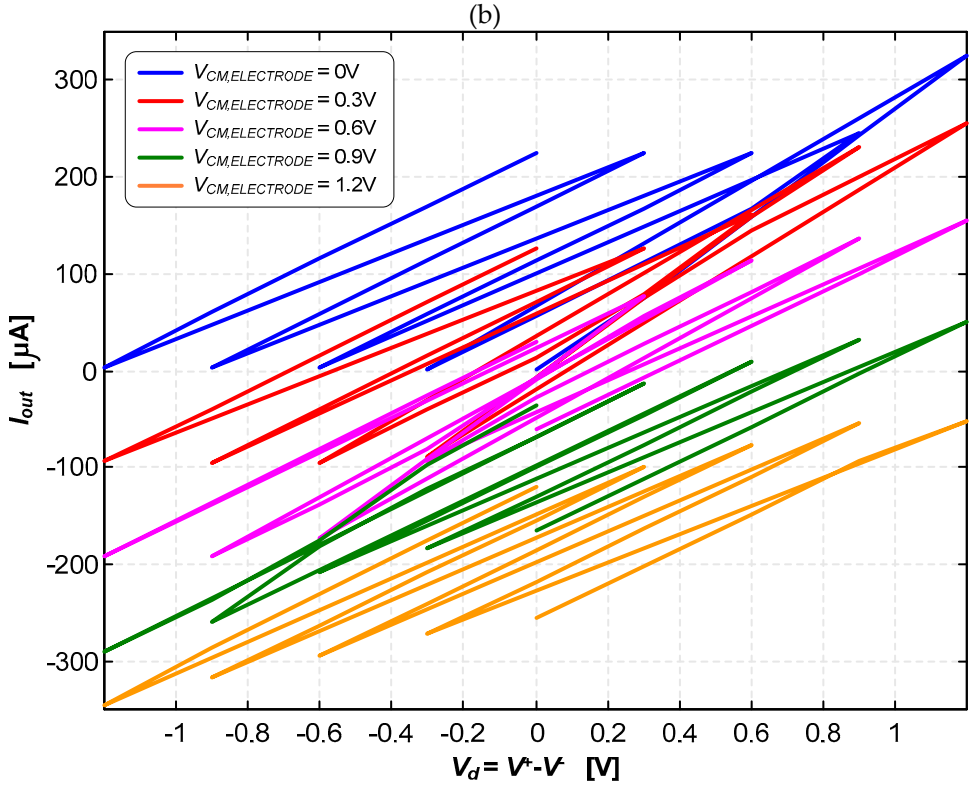

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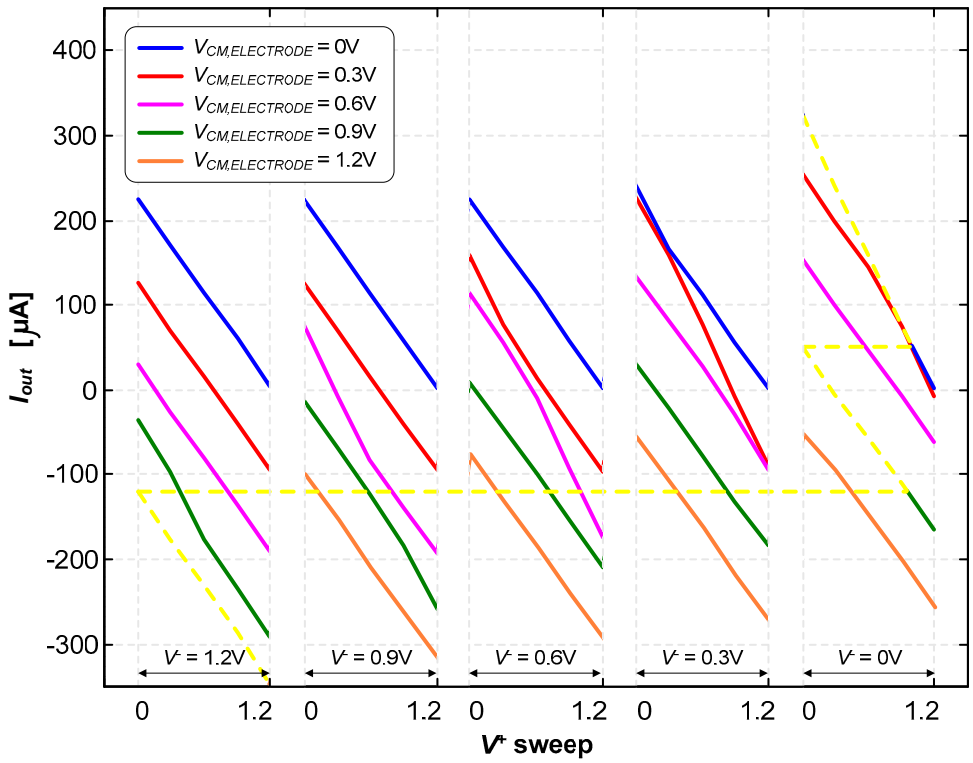

(d)

Figure 10. (a) Schematic of the experimental setup used on the static characterization of the neurostimulator circuit. (b) Photograph of the experimental setup used in the static characterization of the Current-Pump. (c) Stimulation currents for the various combinations of voltages $\{V^+,V^-,V_{CM,electrode}\}$ in "raw" form to allow a clear and immediate visualization of the wide and quasi-symmetrical range of currents. (d) Stimulation currents doubly parameterized in terms of the reference voltage of the electrode $V_{CM,electrode}$ and the inverting input V^-.

Figure 12a illustrates the schematic of the experimental setup for the dynamic characterization. Figure 12b shows the photograph of the experimental setup.

The frequency of the signal at V^- is ten times higher than the frequency of the signal applied at V^+. The amplitude of both signals varies between 0 V and 1.2 V. These settings result in a wave, product of the two input waves, with a sliced sine shape . In this setup, the reference voltage $V_{CM,electrode}$ of the electrode was manually adjusted between 0 V and 1.2 V.

Figure 12c shows the experimental results of the dynamic characterization. A set of sine waves with common-mode voltage of 0.6 V and different amplitudes were applied in the non-inverting input V^+ with V^- and $V_{CM,electrode}$ settled to one of the voltages {0, 0.6, 1.2} V. The voltage ΔV^+ in the plot is the difference between the maximum and the minimum values of the voltage V^+. The voltage ΔV^+ is equal to $2A^+$ for a non-inverting input V^+ of $V^+ = 0.6+A^+.\cos(2\pi ft)$. The amplitude ΔV^+ was swept from 0.2 V to 1.2 V in steps of 0.2 V. The non-inverting input V^+ voltage variation is rail-to-rail for $A^+ = 0.6$ V. Figure 12d shows the results for seven combinations of $\{V^-, V_{CM,electrode}\}$ in the set {0, 0.6, 1.2} V. Each combination defines the admissible range of the output current, whose plane domains are bounded above and below by two straight lines. The upper line occurs for $V^+ = 0.6+\Delta V^+$, while the bottom line occurs for $V^+ = 0.6-\Delta V^+$. It is possible to observe in Figure 12d the abillity to dynamically sweep the complete current limit, ranging from I_{max} = +375 µA to I_{min} = -218 µA, simply selecting the most suitable voltage combination of $\{V^+, V^-, V_{CM,electrode}\}$.

It is also possible to observe in Figure 12c that a limited set of voltage combination of $\{V^+, V^-, V_{CM,electrode}\}$ must be avoided, under the penalty of not being able to generate very specific values of electric current. These voltage combinations are associated with the "no-man's land" regions marked

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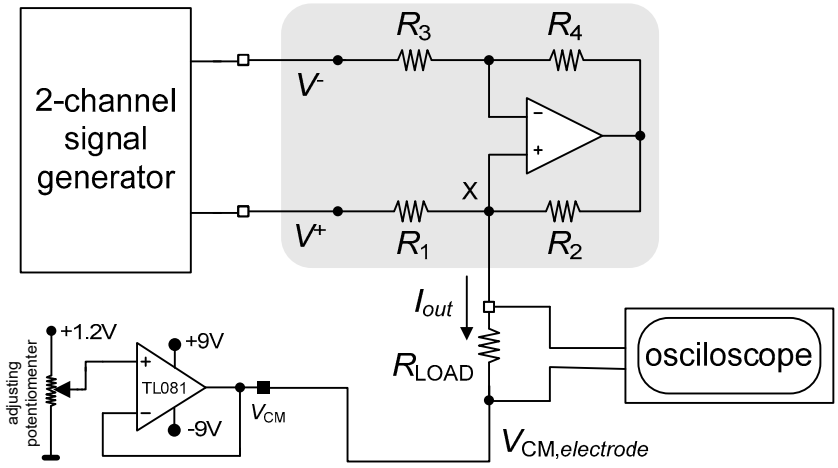
with gray shading. The "no-man's land" regions are the combinations that are not contained in the set of the seven plane domains for the different voltage combinations {V^+, V^-, $V_{CM,electrode}$}.

The measurements showed that these results are valid with all voltage combinations {V^+, V^-, $V_{CM,electrode}$} for a frequency up to f_{-3dB} = 1.5 MHz. This frequency is the one that narrows the current range I_{max}-I_{min} to -3 dB. For example, the measurements showed that I_{max} = +297 µA and I_{min} = +248.4 µA for V^+ = 0.6+0.1cos(2$\pi$$ft$) or ΔV^+ = 0.2 V with f<f_{-3dB}/10, and V^- = 0 V and $V_{CM,electrode}$ = 0 V. This results on ΔI_{out} = I_{max}-I_{min} = +49 µA. The measurements also showed ΔI_{out} = (+49)×(2)$^{-1/2}$×(10^{-6}) = +34.6 µA for f = f_{-3dB} = 1.5 MHz.



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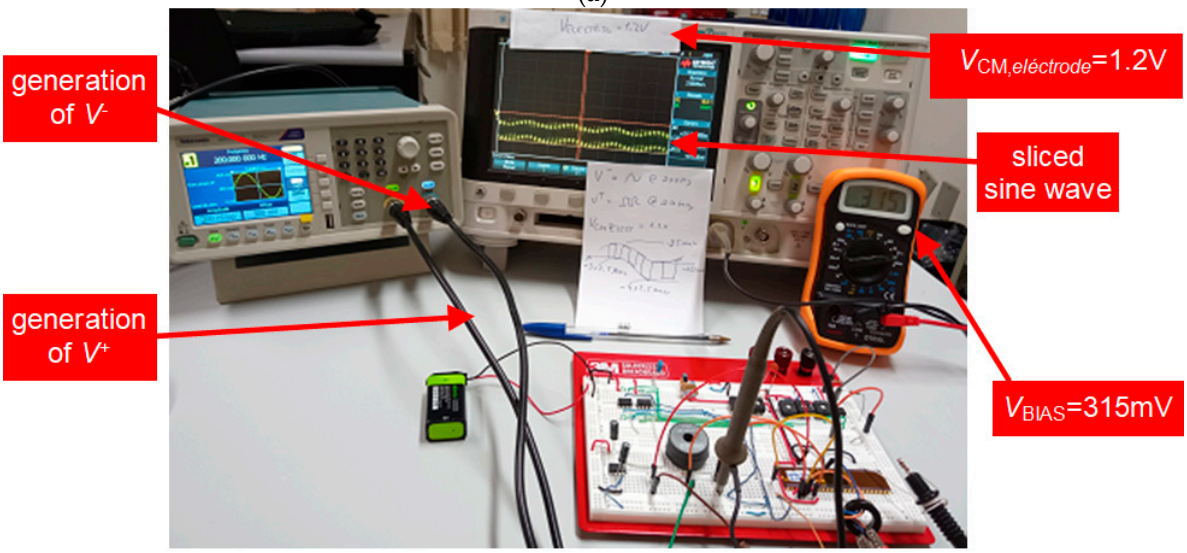

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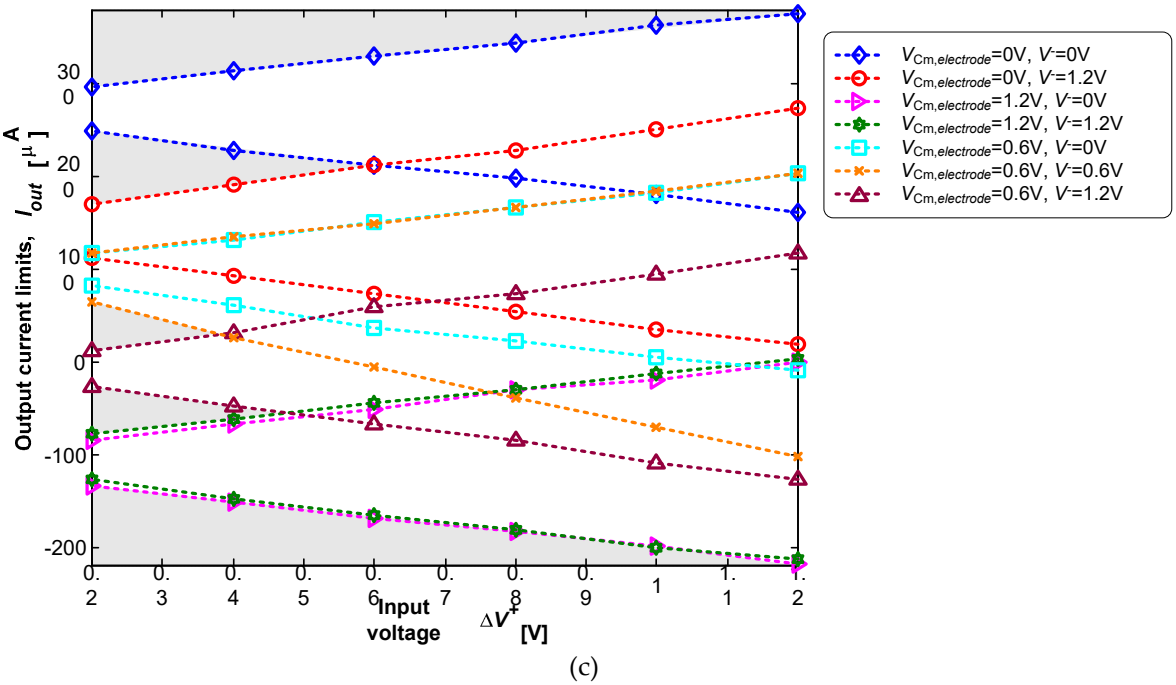

(c)

Figure 12. (a) Schematics of the experimental setup used on dynamic characterization of the neurostimulator circuit. (b) Photograph of the experimental setup used in the static characterization of the Current-Pump. (c) Dynamic characterization using sine waves with rail-to-rail amplitude.

4. Conclusions

This paper presented a low-noise amplifier (LNA) and a neurostimulator circuit, which were optimized for application on Closed-Loop Deep-Brain Stimulation (CLDBS). The LNA and neurostimulator were designed and fabricated in the CMOS 65 nm from TSMC. Table 5 compares this LNA with a few related key works found in the literature [12–32]. It was calculated the figure-of-merit (*FOM*) to better rank and compare this work with the others with respect to the internal noise-power consuption trade off. The noise efficiency factor (*NEF*) was introduced in 1987 by Steyaert et al. [38], and since then, it has been widely used. It is given by:

$$NEF = IRN \times \sqrt{\frac{2I_{total}}{\pi \times U_T \times (4kT) \times BW}} \tag{14}$$

where I_{total} is the total current absorbed by the amplifier stage (this current excludes the amount absorbed by the bias stage), U_T is the thermal voltage given by kT/q (≈ 26 mV at the room temperature of 300 K), k is the Boltzmann constant, T is the room temperature expressed in Kelvin, IRN [V_{rms}] is the total input-referred noise, and BW is the LNA bandwidth.

It must be noted that this FOM compares the noise-power trade-off with that of a single ideal bipolar transistor. The lowest the FOM, the better will be the LNA with relation to the global noise performance.

Two important observations must be made regarding the results presented in Table 5: the two circuits with the lowest NEF, [24,28], use a single-input CMOS inverter as the first gain stage. The invert has half the number of transistors compared to the inpu stage of an OpAmp, and therefore introduces approximately half the amount of power noise. Consequently, the NEF is reduced by $(2)^{½}$; implementations with technologies with higher minimum length, [29–32], have a better NEF.

The LNA presented in this work exhibits an NEF that is comparable to the best ones found in the literature. This result is partly due to the sizing/optimization process performed through the application of metaheuristics.

Table 6 compares the features of this neurostimulator circuit with few related key works found in the literature [42–48]. All works listed in Table 6 were implemented using CMOS components. The

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neurostimulator presented in this paper and the neurostimulator presented by Adams *et al* [46] are the only ones that simultaneously allows the generation of current signals with non-standard waveforms and are suitable for delayed feedback.

To conclude, Figure 12 shows a photograph of the fabricated CMOS microdevice, which occupies 1.8 mm × 1.8 mm of area. Moreover, this figure also makes an emphasis to the LNA and neurostimulator presented in this paper.

Table 5. Comparison of this LNA with the state-of-the art.

Ref.	CMOS process	Mid-Band Gain [dB]	Bandwidth [Hz]	Power Supply [V]	Power Consup. [µW]	Area [mm²]	IRN [μV_{rms}]	FOM [kHz/(μV_{rms}.µW)]
this work+	65nm	40.4	19 — 9k	1.2	6.19	0.046	4.86	4.34
[23]	40nm	25.7	200 — 5.0k	1.2	2.8	N/A	5.3	4.40
[24]	65nm	52.1	1.0 — 8.2k	1.0	2.8	0.042	4.13	2.93
[25]	65nm	46	1.0 — 10k	0.5	1.5	0.0039	6.5	4.34
[25]	65nm	30	300 — 10k	0.5	2.3	0.025	5.8	4.76
[27]	90nm	58.7	0.49 — 10.5k	1.0	2.85	0.137	3.04	1.93
[28]	0.13µm	40	0.05 — 10.5k	1.0	12.1	0.072	2.2	2.90
[29]	0.18µm	40	0.1 — 7.4k	1.0	3.44	0.012	4.27	3.07
[30]	0.18µm	40	0.05 — 7.5k	1.2	4.8	0.022	3.87	3.44
[31]	0.5µm	49.26 — 60.63	0.5 — 300 0.27—12.9k	3.3	4.12	0.0144	3.16	2.53
[32]	0.5µm	39.5	0.025 —7.2k	±2.5	80 µW	0.16	2.2	4.0

+ simulation results.

Table 6. Comparison of this neurostimulator with the state-of-the art.

Ref.	Current [µA]	Voltage [V]	Maximum pulse frequency/ Bandwidth [Hz]	Minimum pulse duration/ Bandwidth^{-1} [µs]	Charge balance	Active charge balancing method
This work	-325 to +318	1.2	1.5×10^6 (BW)	25	Active	Continuous (Howland Current-Pump)
[42]	20 to 2000	12	500	10	Active	Switched (H-bridge)
[43]	-200 to +200	3.6 (bat)	185	90	Active	Switched
[44]	0 to 200	3.2 (bat)	130	90	Passive	Switched
[45]	30 to 1000	3.7 (bat)	5000	10	Active	Switched
[46]	-375 to +250	10	5000	20	Active	Continuous (Howland Current-Pump)
[47]	20 to 2000	4.8 (bat)	300	40	Active	Switched (H-bridge)
[48]	10 to 500	3.1 (bat)	200	60	Passive	Switched

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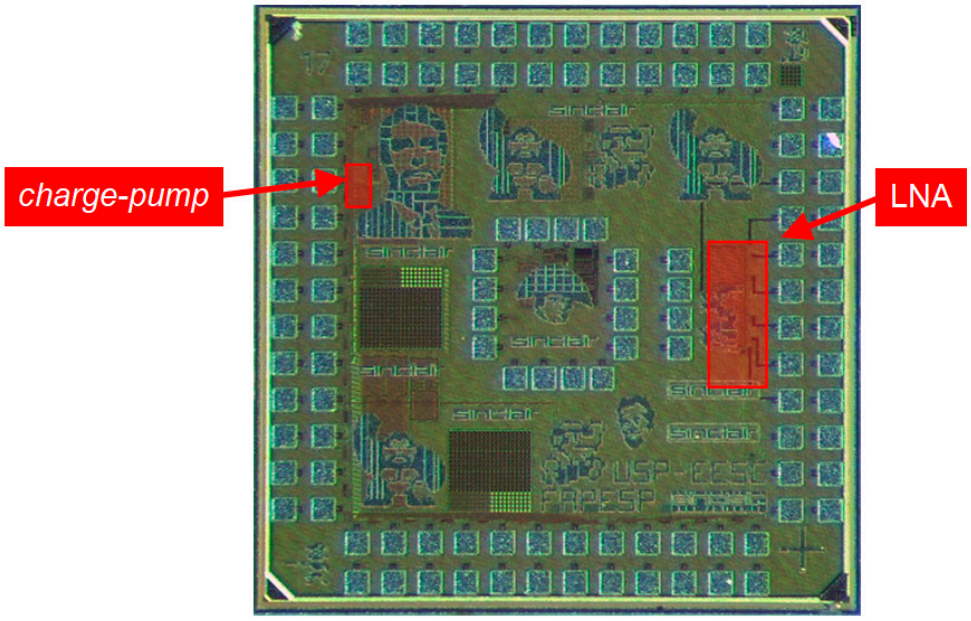

Figure 12. Photograph of the fabricated CMOS microdevice (1.8 mm × 1.8 mm), with emphasis to the LNA presented in this paper and to one of the ESD protections.

Author Contributions: Conceptualization, T.M.N., R.H.G., and J.P.C.; Methodology, T.M.N., R.H.G. and J.P.C.; Validation, T.M.N., G.A.J., M.L.M.A. and R.H.G.; Writing—original draft preparation, T.M.N., R.H.G., J.N. and J.P.C.; Supervision, E.T.F. and E.C.; Project administration, M.L., J.N., J.P.C. and M.A.R.; Funding acquisition, M.L., J.N., J.P.C. and M.A.R.

Funding: This work was partially supported by the FAPESP agency (Fundação de Amparo à Pesquisa do Estado de São Paulo) through the project with the reference 2019/05248-7. Professor João Paulo Carmo was support by a PQ scholarship with the reference CNPq 304312/2020-7.

Acknowledgments: Tiago Mateus Nordi was sponsored by Federal University of São Carlos (USFCar).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. B. S. Appleby, P. S. Duggan, A. Regenberg, and P. V. Rabins, "Psychiatric and Neuropsychiatric Adverse Events Associated With Deep Brain Stimulation: A Meta-analysis of Ten Years' Experience", Movement Disorders, Vol. 22, No. 12, pp. 1722 1728, 2007.
2. Sui, Y.; Tian, Y.; Ko, W.K.D.; Wang, Z.; Jia, F.; Horn, A.; de Ridder, D.; Choi, K.S.; Bari, A.A.; Wang, S.; et al. Deep brain stimulation initiative: Toward innovative technology, new disease indications, and approaches to current and future clinical challenges in neuromodulation therapy. Front. Neurol. 2021, 11, 59745.
3. Medtronic DBS Therapy for Parkinson's Disease, Medtronic Inc., Catalog UC201607188bEE. 2020. Available online: https://asiapac.medtronic.com/content/dam/medtronic-com/uk-en/patients/documents/parkinsons-disease/pd-brochure-uc201607188ee.pdf?bypassIM=truelead (accessed on 5 March 2022).
4. Hickey, P.; Stacy, M. Deep Brain Stimulation: A Paradigm Shifting Approach to Treat Parkinson's Disease. Front. Neurosci. 2016, 10, 173.
5. Vercise™ DVBS Leads: Directions for Use, Boston Scientific Corporation, Catalog 91172963-02 REV A 2017-02. 2017. Available online: https://www.bostonscientific.com/content/dam/Manuals/eu/current-rev-da/91172963-02_Vercise%E2%84%A2_DBS_Leads_DFU_multi-OUS_s.pdf (accessed on 1 Dec. 2021).
6. Hoang, K.B.; Cassar, I.R.; Grill, W.M.; Turner, D.A. Biomarkers and Stimulation Algorithms for Adaptive Brain Stimulation. Front. Neurosci. 2017, 11, 1–15.
7. Vercise™ Deep Brain Stimulator System. Available online: https://www.bostonscientific.com/en-IN/products/deep-brain-stimulation-systems/vercise-deep-brain-stimulation-system.html (accessed on 17th January 2023).
8. J. J. Fins, Chapter 9: Deep Brain Stimulation: Ethical Issues in Clinical Practice and Neurosurgical Research, pp. 81 91, Neuromodulation. Academic Press. 2009.

9. M. L. Kringelbach, N. Jenkinson, S. L. F. Owen, and T. Z. Aziz, "Translational principles of deep brain stimulation", Nature Reviews Neuroscience, Vol. 8, No. 8, pp. 623 635, 2007.
10. S. L. Owen, A. L. Green, J. F. Stein, and T. Z. Aziz, "Deep brain stimulation for the alleviation of poststroke neuropathic pain", Pain, Vol. 120, pp. 202 206, 2006.
11. S. Marchand, R. C. Kupers, M. C. Bushnell, and G. H. Duncan, "Analgesic and placebo effects of thalamic stimulation", Pain, Vol. 105, pp. 481 488, 2003.
12. R. G. Bittar, et al., "Deep brain stimulation for movement disorders and pain", Journal of Clinical Neuroscience, Vol. 12, pp. 457 463, 2005.
13. R. G. Cury, R. Galhardoni, E. T. Fonoff, S. P. Lloret, M. G. S. Ghilardi, E. R. Barbosa, M. J. Teixeira, and D. C. de Andrade, "Sensory abnormalities and pain in Parkinson disease and its modulation by treatment of motor symptoms", European Journal of Pain, Vol. 20, No. 2, pp. 151 165, 2016.
14. S. Rehncrona, et al., "Long-term efficacy of thalamic deep brain stimulation for tremor: double blind assessments", Movement Disorders, Vol. 18, pp. 163 170, 2003.
15. M. G. S. Ghilardi, M. Ibarra, E. J. L. Alho, P. R. Reis, W. O. L. Contreras, C. Hamani, and E. T. Fonoff, "Double-target DBS for essential tremor: 8-contact lead for cZI and Vim aligned in the same trajectory", Neurology, Vol. 90, No. 10, pp. 476 478, 2018.
16. E. T. Fonoff, M. G. S. Ghilardi, and R. G. Cury, Neurocirurgia funcional para o Clínico: Estimulação Cerebral Profunda em Doença de Parkinson, Distonia e Outros Distúrbios do movimento, pp. 53 67, Capítulo de livro, Condutas em Neurologia: 11ª edição. Ricardo Nitrini (Ed.). Manole Editora. 2016. *In Portuguese*.
17. M. Vidailhet, et al., "Bilateral deep-brain stimulation of the globus pallidus in primary generalized dystonia", The New England Journal of Medicine, Vol. 352, pp. 459 467, 2005.
18. R. Franco, E. T. Fonoff, P. Alvarenga, A. C. Lopes, E. C. Miguel, M. J. Teixeira, D. Damiani, and C. Hamani, "DBS for Obesity", Brain Sciences, Vol. 6, No. 3, pp. 1-23, 2016.
19. L. Almeida, D. Martinez Ramirez, P. J. Rossi, Z. Peng, A. Gunduz, and M. S. Okun, "Chasing tics in the human brain: development of open, scheduled and closed loop responsive approaches to deep brain stimulation for tourette syndrome", Journal of Clinical Neurology, Vol. 11, pp. 122 131, 2015.
20. J. A. Herron, M. C. Thompson, T. Brown, H. J. Chizeck, J. G. Ojemann, and A. L. Ko, "Chronic electrocorticography for sensing movement intention and closed-loop deep brain stimulation with wearable sensors in an essential tremor patient", Journal of Neurosurgery, Vol. 127, pp. 580 587, 2017.
21. Ron Gadot, Ricardo Najera, Samad Hiran, Adrish Anand, Eric Storch, Wayne K Goodman, Ben Shofty, and Sameer A Sheth, "Efficacy of deep brain stimulation for treatment-resistant obsessive-compulsive disorder: systematic review and meta-analysis", Journal of Neurology, Neurosurgery & Psychiatry, Vol. 93, pp. 1166–1173, 2022.
22. K. B. Hoang, I. R. Cassar, W. M. Grill, and D. A. Turner, "Biomarkers and Stimulation Algorithms for Adaptive Brain Stimulation", Frontiers in Neuroscience, Vol. 11, Article 564, pp. 1 15, 2017.
23. H. Chandrakumar and D. Marković, ''An 80-mVpp linear-input range, 1.6-G input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference,'' IEEE J. Solid-State Circuits, vol. 52, no. 11, pp. 1–18, Nov. 2017.
24. Ng, K.A.; Xu, Y.P. A multi-channel neural-recording amplifier system with 90 dB CMRR employing CMOS-inverter-based OTAs with CMFB through supply rails in 65 nm CMOS. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 Feb. 2015; pp. 1–3.
25. Biederman, W.; Yeager, D.J.; Narevsky, N.; Koralek, A.C.; Carmena, J.M.; Alon, E.; Rabaey, J.M. A Fully-Integrated, Miniaturized (0.125 mm2) 10.5 μW Wireless Neural Sensor. IEEE J. Solid-State Circuits 2013, 48, 960 970.
26. R. Muller, H.-P. Le, W. Li, P. Ledochowitsch, S. Gambini, T. Bjorninen, A. Koralek, J. M. Carmena, M. M. Maharbiz, E. Alon, and J. M. Rabaey, ''A minimally invasive 64-channel wireless μECoG implant,'' IEEE J. Solid-State Circuits, vol. 50, no. 1, pp. 344–359, Jan. 2015.
27. T. Yang and J. Holleman, ''An ultralow-power low-noise CMOS biopotential amplifier for neural recording,'' IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 62, no. 10, pp. 927–931, Oct. 2015.
28. Zhang, F.; Holleman, J.; Otis, B.P. Design of Ultra-Low Power Biopotential Amplifier for Biossignal Acquisition Application. IEEE Trans. Biomed. Circuits Syst. 2012, 6, 244–355.
29. Kim, H.-J.; Park, Y.; Eom, K.; Park, S.-Y. An Area- and Energy-Efficient 16-Channel, AC-Coupled Neural Recording Analog Frontend for High-Density Multichannel Neural Recordings. Electronics 2021, 10, 1972.
30. Kwak, J.Y.; Park, S.-Y. Compact Continuous Time Common-Mode Feedback Circuit for Low-Power, Area-Constrained Neural Recording Amplifiers. Electronics 2021, 10, 145.
31. Tasneem, N.T.; Mahbub, I. A 2.53 NEF 8-bit 10 kS/s 0.5 μm CMOS Neural Recording Read-Out Circuit with High Linearity for Neuromodulation Implants. Electronics 2021, 10, 590.

32. Harrison, R.R.; Charles, C. A low-power low-noise cmos for amplifier neural recording applications. IEEE J. Solid-State Circuits 2003, 38, 958–965.
33. H. Kassiri, K. Abdelhalim and R. Genov, "Low-distortion super-GOhm subthreshold-MOS resistors for CMOS neural amplifiers," 2013 IEEE Biomedical Circuits and Systems Conference (BioCAS), Rotterdam, Netherlands, 2013, pp. 270-273.
34. M. Clerc and J. Kennedy, "The particle swarm – explosion, stability, and convergence ia a multimensional complex space," Trans. Evolutionary Compution, vol. 6, no. 1, Feb. 2002.
35. T.O. Weber and W.A.M.V. Noije, "Design of analog circuits using simulated annealing/quenching with crossovers and particle swarm optimization," in Simulating Annealing – Advances, Apllications and Hybridizations, M.S.G. Tuzuki Ed., IntechOpen, 2012. pp 219-244.
36. E.I. Ishibe and J.N. Soares, "A CMOS bandgap reference circuit with a temperature coefficient adjustment block," in Proccedings of the 26th Symposium on Integrated Circuits and Systems Design (SBCCI), Sept. 2013, pp. 1-6.
37. J. Navarro and M. Luppe, "Performance Comparison of High-Speed Dual Modulus Prescalers Using Metaheuristic Sizing/Optimization," 2020 33rd Symposium on Integrated Circuits and Systems Design (SBCCI), Campinas, Brazil, 2020, pp. 1-6.
38. Steyaert, M.S.; Sansen, W.M. A micropower low-noise monolithic instrumentation amplifier for medical purposes. IEEE J. Solid-State Circuits 1987, 22, 1163–1168.
39. F. Kölbl, G. N'Kaoua, F. Naudet, F. Berthier, E. Faggiani, S. Renaud, A. Benazzouz, and N. Lewis, "An Embedded Deep Brain Stimulator for Biphasic Chronic Experiments in Freely Moving Rodents", IEEE Transactions on Biomedical Circuits and Systems, Vol. 10, No. 1, pp. 72-84, February 2016.
40. F. Kölbl, et al., "An Embedded Deep Brain Stimulator for Biphasic Chronic Experiments in Freely Moving Rodents", IEEE Trans. on Biomedical Circuits and Systems, Vol. 10, pp. 72-78, 2016.
41. AN-1515, A Comprehensive Study of the Howland Current Pump, 26 Apr 2013, Texas Instruments.
42. R. C. Pinnell, A. P. de Vasconcelos, J. C. Cassel, and U. G. Hofmann, "A miniaturized programmable deep-brain stimulator for group-housing and water maze use", Frontiers in Neuroscience, Vol. 12, 2018. #231. https://doi.org/10.3389/fnins.2018.00231.
43. S. G. Ewing, W. J. Lipski, A. A. Grace, and C. Winter, "An inexpensive charge-balanced rodent deep brain stimulation device a step-by-step guide to its procurement and construction", Journal of Neuroscience Methods. Vol. 219, No. 2, pp. 1-17, 2013. doi: 10.1016/j.jneumeth.2013.08.003.
44. A. Z. Kouzani, O. A. Abulseoud, S. J. Tye, M D. Kamal Hosain, and M. Berk, "A low power micro deep brain stimulation device for murine preclinical research", IEEE Journal of Translacional Engineering Health Medicine, Vol. 1, pp. 1-9, 2013. #1500109. doi: 10.1109/JTEHM.2013.2264093.
45. R. C. Pinnell, J. Dempster, and J. Pratt, "Miniature wireless recording and stimulation system for rodent behavioural testing", Journal of Neural Engineering, Vol. 12, No. 6, pp. 1-15, 2015. #066015. doi: 10.1088/1741-2560/12/6/066015.
46. S. D. Adams, K. E. Bennet, S. J. Tye, M. Berk, and A. Z. Kouzani, "Development of a miniature device for emerging deep brain stimulation paradigms", PLoS One, Vol. 14, No. 2, pp. 1-17, 2019. https://doi.org/10.1371/journal.pone.0212554.
47. H. Tibara, F. Naudeta, F. Kölblc, B. Ribota, E. Faggiania, G. N'Kaouac, S. Renaudc, N. Lewisc, and A. Benazzouza," In vivo validation of a new portable stimulator for chronic deep brain stimulation in freely moving rats", Journal of Neuroscience Methods, Vol. 333, pp. 1-9, March 2020. #108577.
48. F. Fluri, T. Mützel, M. K. Schuhmann, M. Krstić, H. Endres, and J. Volkmann, "Development of a head-mounted wireless microstimulator for deep brain stimulation in rats", Journal of Neuroscience Methods, Vol. 291, pp. 249-256, November 2017.