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Cascaded Three-Phase Multilevel Inverter with Minimal Components for Power System Applications

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Abstract: This paper proposes a new cascaded three-phase multilevel inverter based on a cascaded submultilevel and single-phase H-bridge structure. The voltage source of the traditional single-phase H-bridge is replaced with the proposed cascaded submultilevel. Cascading two basic units forms the submultilevel unit. The basic and submultilevel units generate positive voltage only hence the need for an H-bridge to generate both polarities of load voltage. Five algorithms of source voltage are proposed and the optimal algorithm selected to generate the peak load voltage and output levels. The proposed three-phase cascaded multilevel inverter generates 31-level of load voltage. The per-phase component distribution of the proffered inverter are twelve power switches, four dc sources and twelve driver circuits accordingly. Principal merits of the proposed 31-level inverter are high quality load waveforms, production of high levels of load voltage utilizing reduced component quantity, simple cascaded layout, decreased inverter area, minimal inverter cost, minimum inverter losses and utilizing lower rated switches. Also, the proposed topology is highly suited for employment in PV-DVR and other power systems. To validate these advantages of the proposed multilevel inverter, contrastive analysis of the proposed inverter and existing topologies are studied. Finally, the functionality of the proposed inverter is substantiated by simulation in PSCAD/ EMTDC software.

Keywords: cascaded multilevel inverter; asymmetrical multilevel inverter; submultilevel; three-phase multilevel inverter

1. Introduction

Electric power system comprising generation, transmission, distribution, protective devices and loads are dynamic. Therefore, an effective dynamic power conditioning device is required to appropriately synchronise power between these sectors of the power system. Power electronic converter; categorised into rectifiers, inverters, cycloconverters and dc-dc choppers is the most useful and appropriate power conditioning device. Among the family of inverters is the multilevel inverter which provides superior advantages. The popularity and usefulness of multilevel inverters (MLI) is not diminishing anytime soon because MLI continue to attract noteworthy attention in industry and academia. This remarkable attention can be attributed to its' excellent advantages such as reduced dv/dt stress, reduced switching losses, high quality output waveforms, lower EMI interference, high efficiency, medium and high power applications [1–3]. Multilevel inverters are conveniently utilized in power systems such as FACTS and HVDC, electric vehicles, renewable energy generation and grid integration, DVRs (dynamic voltage restorer) and energy storage systems [4–6]. Traditional MLI topologies are categorised into three classes namely CHB (Cascaded H-bridge), FC (Flying capacitor) and NPC (Neutral-point clamped) multilevel inverters. These conventional topologies have seen

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wide-range of improvements. They however suffer from few limitations such as increased switch and dc source count in CHB topology, increased capacitor count in FC topology, increased diode count in NPC topology and structural and control complexities in higher levels for NPC and FC topologies [7,8].

The focus of researchers currently is to refine the structure of MLI topologies by placing prominence on higher efficiency, minimising THD and general component quantity mostly power switches, driver circuits and dc sources whiles maximizing the levels of load voltages [9–12]. An optimal asymmetrical three-phase multilevel inverter is presented in [13] which generates 19-level of load voltage per-phase. The device count of the presented topology per phase is 13 switches, 3 dc-sources and 13 driver circuit. The presented topology boast of reduced component quantity and reduced THD. 31-level single phase MLI topology based on cascaded H-bridge structure is presented by [14] utilizing four asymmetric electrolytic capacitors dc sources, the presented topology amalgamates the merits of chain-cell converter and the concept of static phase-shifter. A modified cascaded 31-level inverter is investigated with respect to reduced dc input, less switches etc. by the authors in [15], the presented topology is controlled by SIC-PWM to minimize the THD content. A novel topology of single-phase multilevel inverter is presented by the authors in [16] generates 31-level of load voltage. The topology is derived by modifying the conventional H-bridge structure by incorporating extra switches and dc sources.

A switched capacitor based cascaded single-phase multilevel inverter capable of generating higher levels of load voltage utilizing lower number of components is presented by [17], the 31-level topology is controlled by nearest level control technique. A high step-up single-phase multilevel composed of unidirectional switches, two dc inputs, power diodes and multiple capacitors is presented in [18] where the voltage gain is dependent on the quantity of capacitors used and is also easily scalable. Another voltage boosting topology based on switched capacitor network and cross-switched configurations is presented by the authors in [19]. The dc source count is one but the switches and diodes count are high. A novel hybrid clamped 7-level inverter composed of reduced component quantity and competitive performance is presented in [20], this topology is an improvement of the traditional diode-clamped and provides floating capacitor voltage balancing at switching frequencies thus provide low voltage ripples. This work propounds a new cascaded three-phase multilevel inverter founded on a cascaded submultilevel and single-phase H-bridge structures comprising minimum component quantities such as dc sources, power switches and driver circuits. Contrastive analysis of the proffered inverter and some selected publicized topologies shows the proffered topology exhibits superior advantages. The remainder of this research is subdivided into the ensuing parts: section II encapsulates the proffered topology made-up of basic and cascaded submultilevel units. Contrastive analysis of the proffered topology and existing topologies is set forth in section III. Simulation of the proffered topology is presented in section IV and conclusion is presented in section V.

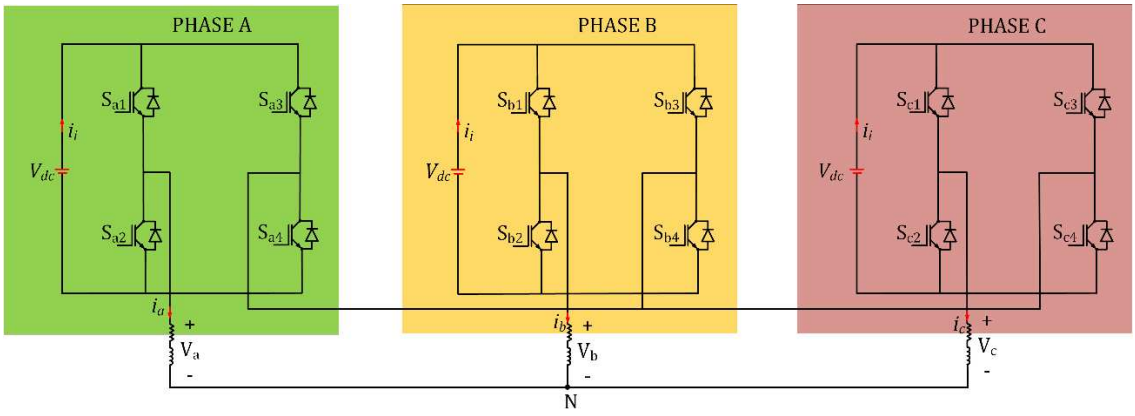

Figure 1. Three-phase multilevel inverter grounded on three single-phase H-bridge inverters.

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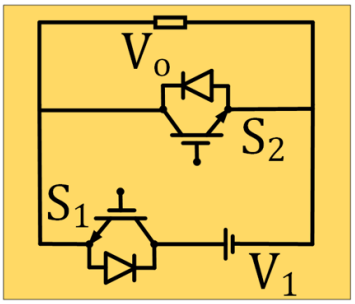

Figure 2. Basic unit.

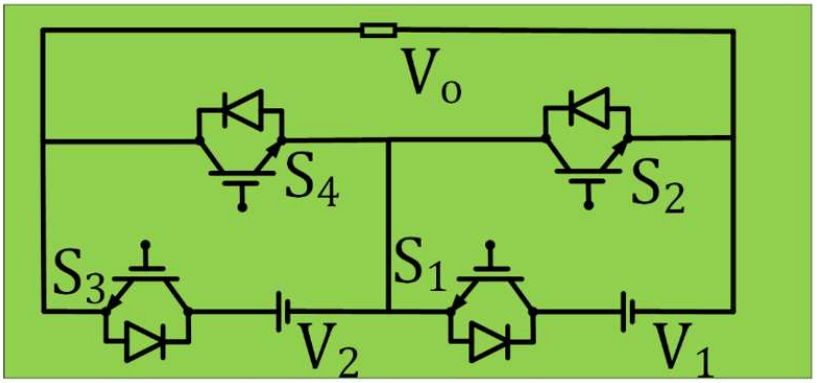

Figure 3. Submultilevel unit.

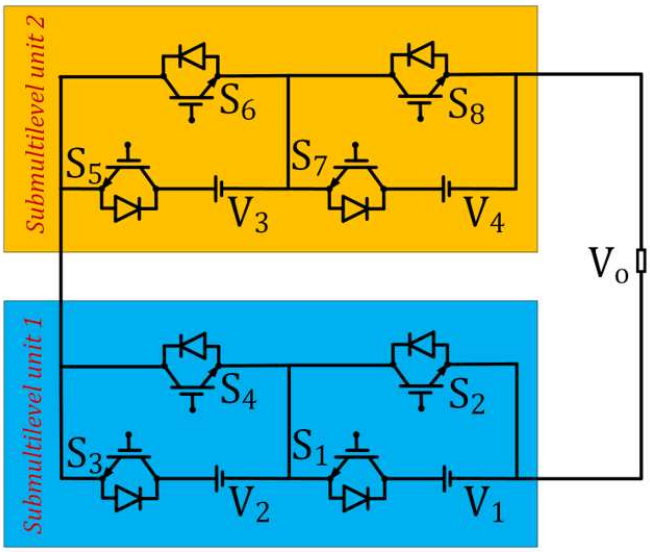

Figure 4. Cascaded submultilevel structure.

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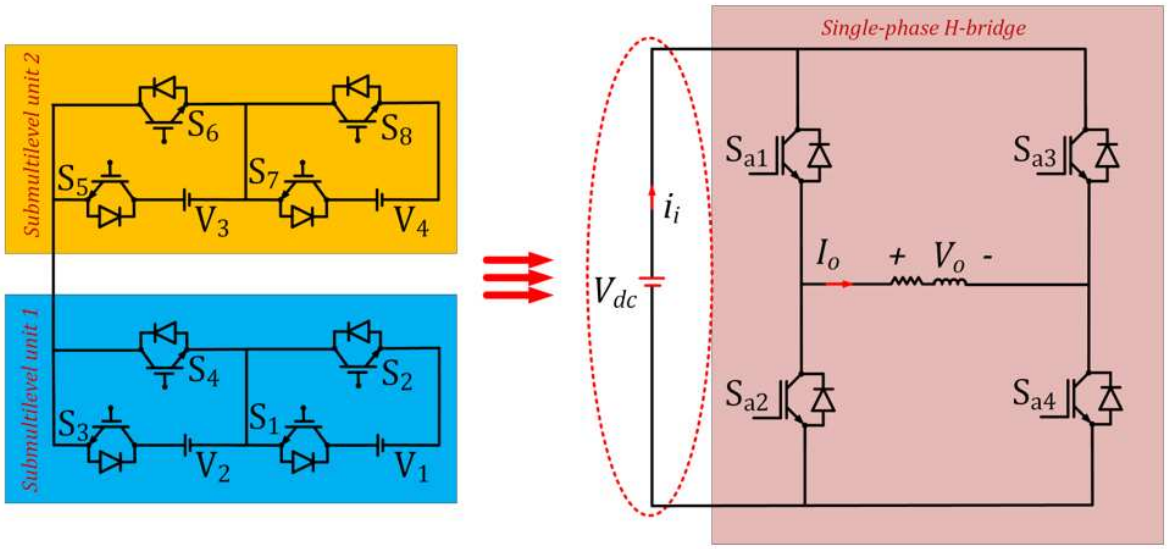

Figure 5. Deriving the proposed cascaded three-phase topology.

2. Materials and Methods

2.1. Proposed Topology

Figure 1 shows the power circuit of a three-phase multilevel inverter based on three conventional single-phase H-bridge inverters. The proposed three-phase multilevel inverter is derived by modifying the power circuit of the conventional three-phase multilevel inverter of Figure 1. The input/source voltage section of each phase of Figure 1 is replaced with a cascaded submultilevel structure shown by Figure 4. The submultilevel structure shown by Figure 3 is derived by cascading two basic units. Figure 2. shows the basic unit of the proffered three-phase multilevel inverter built by two switches and one dc source. Therefore, the submultilevel structure entails four unidirectional switches and two dc sources. Only positive output voltages are generated by the basic unit (Figure 2) and the submultilevel (Figure 3), consequently, an H-bridge structure is needed to produce both polarities load voltage. Figure 5 shows the derivation of the proffered cascaded three-phase multilevel inverter by replacing the voltage source of each phase of Figure 1 with a cascaded submultilevel structure. The proffered three-phase multilevel inverter is a cascaded structure based on the submultilevel units. Figure 6 shows the proffered three-phase multilevel inverter based on the cascaded submultilevel structure. The cascaded structure for each phase of the proffered three-phase multilevel inverter of Figure 6 is composed of eight voltage unidirectional power switches and four dc sources. The cascaded three-phase structure is composed of twenty-four voltage unidirectional switches and twelve dc sources. The overall component count of the proposed three-phase multilevel inverter will have to include the H-bridge structure in each phase, each H-bridge structure contains four unidirectional switches. Therefore, the proposed cascaded three-phase multilevel inverter of Figure 6 comprises thirty-six voltage unidirectional switches and twelve dc sources. Component distribution of the proffered multilevel inverter are computed by equation (1) where $N_{DC\text{-}Sources}$, N_{Driver}, $N_{switches}$, N_{Level}, and N_{IGBT} denotes dc source, driver circuit, switch, output voltage level, and IGBT count accordingly. The switch, IGBT and driver circuit count are equal because no bidirectional switches are used. Also, n denotes the number of basic unit in the cascaded structure.

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$$
\begin{aligned}
N_{switches} &= 3(2n+4) \\
N_{IGBT} &= 3(2n+4) \\
N_{Level} &= 2n^2 - 1 \\
N_{Driver} &= 3(2n+4) \\
N_{DC-Source} &= 3n \\
V_{o,\max} &= 15V_{dc}
\end{aligned} \tag{1}
$$

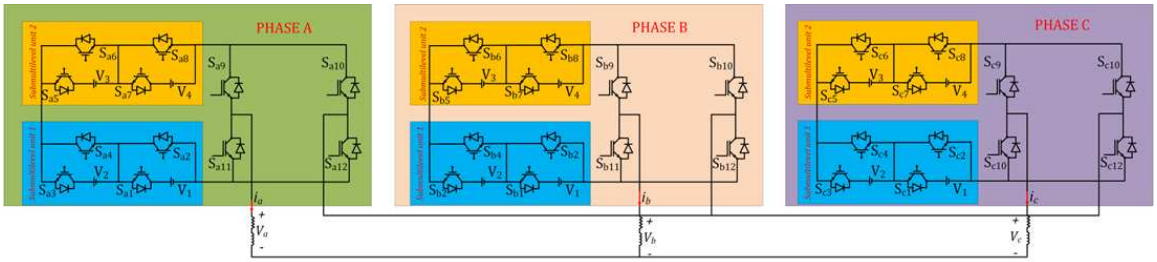

Figure 6. Proposed cascaded three-phase multilevel inverter.

2.2. Input Voltage Characteristics

Based on the value of input dc sources, multilevel inverters are grouped into symmetric or asymmetric topologies. In symmetric topologies, the magnitude of all input dc sources are equivalent. If the magnitude of input dc sources varies, the topology is classified as asymmetric; which is further categorised into binary and trinary topologies. Asymmetric topologies generate much more levels of output voltage juxtaposed to symmetric topologies. However, the rate of depletion of the input sources in asymmetric topologies is variable. Based on symmetric and asymmetric characteristics of the input dc sources, 5 algorithms of voltage permutations are presented in Table 1 to select the optimal source voltage. In Table 1, the second column indicates the type of input voltage, the third column indicates the level of generated output voltage N_{level}, the fourth column indicates the maximum voltage $V_{o,\max}$. n denotes the number of basic unit in the cascaded structure. The first algorithm is symmetric while the remaining algorithms (2nd to 5th) are a variety of asymmetric.

Table 1. Proposed Voltage Algorithms.

Algorithm	DC Voltage Magnitude	Output Voltage Level (N_{Level})	Maximum Output Voltage ($V_{o,max}$)
First Algorithm	$V_1 = V_{dc}$, $V_2 = V_{dc}$ $V_3 = V_{dc}$, $V_4 = V_{dc}$	$2n + 1$	$4nV_{dc}$
Second Algorithm	$V_1 = V_{dc}$, $V_2 = 2V_{dc}$ $V_3 = 3V_{dc}$, $V_4 = 4V_{dc}$	$5n + 1$	$5nV_{dc}$
Third Algorithm	$V_1 = 0.5V_{dc}$, $V_2 = V_{dc}$ $V_3 = 1.5V_{dc}$, $V_4 = 2V_{dc}$	$5n + 1$	$(2n + 1)V_{dc}$
Fourth Algorithm	$V_1 = V_{dc}$, $V_2 = 2V_{dc}$ $V_3 = 4V_{dc}$, $V_4 = 6V_{dc}$	$5n^3 + 2$	$(6n + 1)V_{dc}$

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Fifth Algorithm	$V_1 = V_{dc}$, $V_2 = 2V_{dc}$ $V_3 = 4V_{dc}$, $V_4 = 8V_{dc}$	$4n^3 - 1$	$(3n^2 + 2)V_{dc}$

Using the first algorithm as the input voltage, Figure 2 and Figure 3 generates 1-level and 2-level of positive output voltages respectively. Figure 4 and Figure 6 generates 5-level ($+4V_{dc}, 0$) and 9-level ($\pm 4V_{dc}, 0$) of output voltages respectively. Using the fifth algorithm, Figure 2 and Figure 3 generates 1-level ($V_{dc},$) and 3-level ($3V_{dc},$) of positive output voltages respectively. Figure 4 and Figure 6 generates 16-level ($+15V_{dc}, 0$) and 31-level ($\pm 15V_{dc}, 0$) of output voltages respectively. Therefore, from the 5 proposed algorithms of Table 1, the fifth algorithm yields the maximum output voltage ($V_{o,\max}$) and the maximum output levels ($N_{Level,\max}$). The theoretical output waveform of the proposed 31-level inverter (Figure 6) and the corresponding switching states of the power switches is illustrated by Figure 7. The switching pattern of the proposed 31-level inverter is given in Table 2, only active switches in one phase per state is provided, the corresponding switches in the other phases are active for the same state. All other switches are in the off-state or voltage blocking state.

2.3. Inverter Power Loss

Power loss of the proposed topology is determined by two parameters: switching power loss and conduction power loss. Switching losses occur during switching states of the inverter whiles conduction losses occur during active states of switches. Blocking voltage power losses are present but are ignored because IGBT off-state leakage currents are negligible.

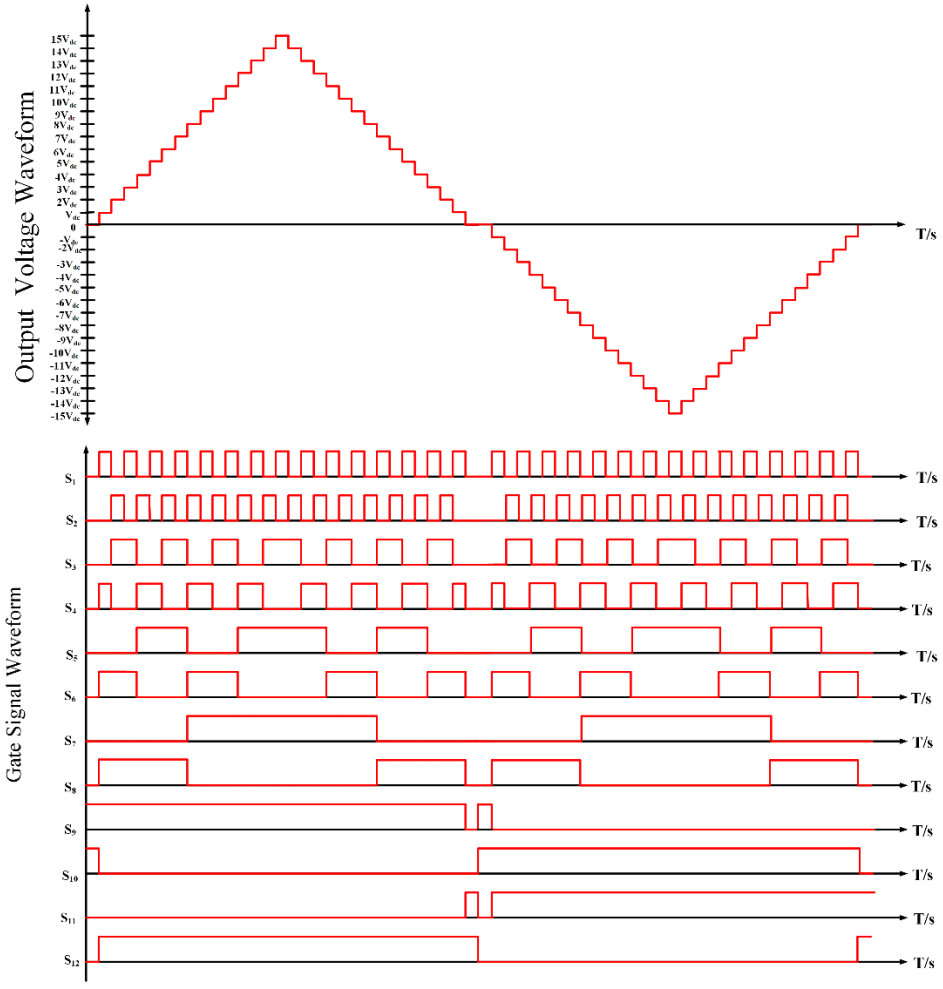

Figure 7. Theoretical output voltage and switching states.

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Table 2. Switching Pattern.

State	Switches	DC Sources	Output Voltage
1	S_{a1}, S_{a3}, S_{a5}, S_{a7}, S_{a9}, S_{a12}	$V_1 + V_2 + V_3 + V_4$	$15V_{dc}$
2	S_{a2}, S_{a3}, S_{a5}, S_{a7}, S_{a9}, S_{a12}	$V_2 + V_3 + V_4$	$14V_{dc}$
3	S_{a1}, S_{a4}, S_{a5}, S_{a7}, S_{a9}, S_{a12}	$V_1 + V_3 + V_4$	$13V_{dc}$
4	S_{a2}, S_{a4}, S_{a5}, S_{a7}, S_{a9}, S_{a12}	$V_3 + V_4$	$12V_{dc}$
5	S_{a1}, S_{a3}, S_{a6}, S_{a7}, S_{a9}, S_{a12}	$V_1 + V_2 + V_4$	$11V_{dc}$
6	S_{a2}, S_{a3}, S_{a6}, S_{a7}, S_{a9}, S_{a12}	$V_2 + V_4$	$10V_{dc}$
7	S_{a1}, S_{a4}, S_{a6}, S_{a7}, S_{a9}, S_{a12}	$V_1 + V_4$	$9V_{dc}$
8	S_{a2}, S_{a4}, S_{a6}, S_{a7}, S_{a9}, S_{a12}	V_4	$8V_{dc}$
9	S_{a1}, S_{a3}, S_{a5}, S_{a8}, S_{a9}, S_{a12}	$V_1 + V_2 + V_3$	$7V_{dc}$
10	S_{a2}, S_{a3}, S_{a5}, S_{a8}, S_{a9}, S_{a12}	$V_2 + V_3$	$6V_{dc}$
11	S_{a1}, S_{a4}, S_{a5}, S_{a8}, S_{a9}, S_{a12}	$V_1 + V_3$	$5V_{dc}$
12	S_{a2}, S_{a4}, S_{a5}, S_{a8}, S_{a9}, S_{a12}	V_3	$4V_{dc}$
13	S_{a1}, S_{a3}, S_{a6}, S_{a8}, S_{a9}, S_{a12}	$V_1 + V_2$	$3V_{dc}$
14	S_{a2}, S_{a3}, S_{a6}, S_{a8}, S_{a9}, S_{a12}	V_2	$2V_{dc}$
15	S_{a1}, S_{a4}, S_{a6}, S_{a8}, S_{a9}, S_{a12}	V_1	V_{dc}
16	S_{a2}, S_{a4}, S_{a6}, S_{a8}, S_{a9}, S_{a10}	-	0

2.3.1. Switching losses

Switching losses of the proposed multilevel inverter occurs during the gating action of on/off of the power switches. These losses are computed as energy losses during on/off gating. Hence E_{on} and E_{off} constitute the on/off gating states accordingly. Overall switching energy losses P_{SW} is computed by equation (4) where V_{sw} is the off-mode switch voltage, I and I' are the on/off switch currents accordingly. t_{on} and t_{off} are the time in seconds for turn-on and turn-off accordingly.

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}} t \right) \left(-\frac{V_{sw,k}}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw,k} I' t_{on} \quad (2)$$

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(\frac{V_{sw,k}}{t_{off}} \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw,k} I t_{off} \quad (3)$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left(\sum_{i-1}^{N_{on,k}} Eon,k + \sum_{i=1}^{N_{off,k}} E_{off},k \right) \quad (4)$$

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2.3.2. Conduction losses

Conduction losses of the proposed multilevel inverter occurs when the power switches are conducting. Each power comprises one transistor fitted with an antiparallel diode. Therefore, conduction power losses P_C is computed by summing the transistor $P_{C,T}$ and diode $P_{C,D}$ power losses. The magnitude of β is constant and depends on the kind of power switch used. The diode and transistor resistance are denoted by R_D and R_T accordingly, also V_T denotes the transistor voltage whiles and V_D denotes the diode voltage accordingly. Integrating equation (5) for a period will yield transistor average conduction power loss equation expressed by equation (7), also integrating equation (6) for a period will yield diode average conduction power loss equation expressed by equation (8). The conduction cycle alternates when the control methods and load characteristics are taken into account. Therefore, the overall inverter power loss P_L is computed by equation (9) and the converter efficiency is computed by equation (10).

$$P_{C,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \quad (5)$$

$$P_{C,D}(t) = [V_D + R_D i(t)]i(t) \quad (6)$$

$$P_{C,T} = \frac{1}{2\pi}\int_0^{2\pi} n_T(t)[V_T + R_T i^{\beta}(t))i(t)]d(\omega t) \quad (7)$$

$$P_{C,D} = \frac{1}{2\pi}\int_0^{2\pi} n_D(t)[(V_T + R_D i(t))i(t)]d(\omega t) \quad (8)$$

$$P_L = P_C + P_{SW} \quad (9)$$

Therefore, inverter efficiency (η) is computed by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{Loss}}{P_{in}} \quad (10)$$

2.4. Standing/Blocking Voltage

Overall standing voltage of the proffered inverter is determined by computing and summing the blocking voltage of each switch during the off-state or mode. Because of the symmetric relationship between the phases, it enough to determine the standing voltage of one phase then multiple by three to achieve the overall standing voltage of the inverter. There are twelve unidirectional switches per-phase. Eight switches are in the cascaded topology; switches in individual basic units are equivalent with respect to the blocking voltage, this is expressed by equation (11). Four are in the H-bridge and are all equivalent with respect to the blocking voltage, this is expressed by equation (12). Therefore, the total standing voltage is computed by equation (13).

$$\begin{aligned} V_{dc} &= V_{S_{1a}} = V_{S_{2a}} \\ 2V_{dc} &= V_{S_{3a}} = V_{S_{4a}} \\ 4V_{dc} &= V_{S_{5a}} = V_{S_{6a}} \\ 8V_{dc} &= V_{S_{7a}} = V_{S_{8a}} \end{aligned} \quad (11)$$

$$15V_{dc} = V_{S_{9a}} = V_{S_{10a}} = V_{S_{11a}} = V_{S_{12a}} \quad (12)$$

$$\begin{aligned} V_{\text{Standing}_{1\phi}} &= 2(15V_{dc}) + 4(15V_{dc}) = 90V_{dc} \\ V_{\text{Standing}_{3\phi}} &= 3*90V_{dc} = 270V_{dc} \end{aligned} \quad (13)$$

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3. Results

3.1. Comparative Analysis

Comparative investigation of the proposed cascaded multilevel topology and selected published multilevel inverters are analysed in this section with respect to component quantity and output voltage levels. Multilevel inverters with higher number of components i.e. switches, driver circuits, dc sources etc. have increased volume and weight, increased cost, high losses and reduced efficiency. Therefore, it's imperative to design a topology having reduced component count and higher output voltage levels. Based on Table 3, a phase of the proposed topology is juxtaposed with selected single-phase multilevel inverter topologies. Each phase of the proposed topology comprises 12 switches, 4 dc sources and 12 driver circuit. Evidently, it's clear the proposed topology contains less components juxtaposed with the selected topologies. There are no fictitious dc sources such as capacitors as existing in [17–19], all switches in the proposed topology are unidirectional thus less complex compared to bidirectional switches which are complex structurally, also there are no clamping diodes and capacitors as in NPC and FC topologies. Figure 8 shows a bar chart representation of the comparative analysis of Table 3. Table 4 shows comparative evaluation of the proffered topology and selected three-phase multilevel inverter topologies with respect to the quantity of switches, sources, driver circuit, clamping diodes and capacitors, output voltage levels and source capacitors. It evident that the proposed topology provides the optimal cost benefit analysis when component quantity is juxtaposed with the levels of output voltage.

Table 3. Comparative analysis (single-phase topologies).

Components	**[13]**	**[14]**	**NPC**	**FC**	**CHB**	**[15]**	**[16]**	**[17]**	**[18]**	**[19]**	**[P]**
Levels	19	31	31	31	31	31	31	31	31	31	31
Switches	13	16	60	60	60	8	14	18	14	16	12
Sources	3	4	1	1	15	4	4	2	2	2	4
Driver Circuits	13	16	60	60	60	8	14	18	14	16	12
Diodes	0	0	56	0	0	4	0	0	0	2	0
Capacitors	0	0	0	28	0	0	0	4	4	4	0

[P]: Proposed Topology.

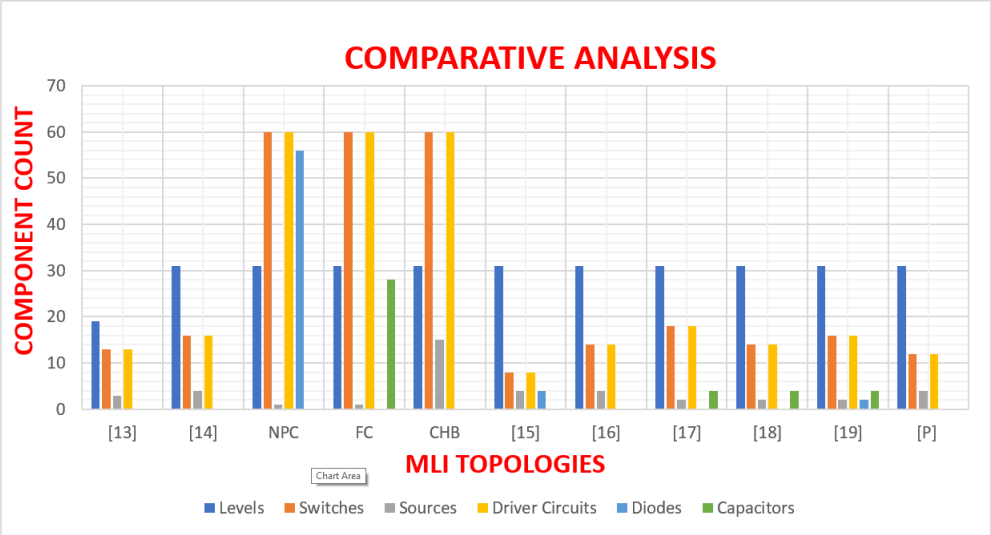

Figure 8. Comparative analysis illustration of the proposed and selected topologies.

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Table 4. Comparative analysis (three-phase topologies).

Components	NPC	FC	CHB	[1]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[P]
Switches	36	36	36	39	36	36	42	24	27	24	18	36
Levels	7	7	7	19	7	7	11	7	7	9	7	31
Sources	1	1	9	9	1	2	15	2	6	6	6	4
Driver Circuits	36	36	36	39	36	36	42	24	27	36	18	36
Clamping Diodes	90	0	0	0	0	0	0	0	0	0	0	0
Clamping Capacitors	0	45	0	0	0	0	0	0	0	0	0	0
Capacitors	6	6	0	0	6	9	0	0	0	0	0	0

[P]: Proposed Topology.

3.2. Simulation Results

Simulation results of the proffered cascaded three-phase multilevel inverter of Figure 6 is provided in this section. Using fundamental frequency control technique and an appropriate switching sequence, the required output waveforms are generated by developing and simulating the power circuit of the proffered multilevel inverter in PSCAD/EMTDC software. High switching frequencies provide high quality output waveforms, however, switching losses are increased. Compared to PWM control techniques, fundamental frequency control provides minimum switching losses [27,28]. Table 5 shows the variables used for simulation.

Table 5. Simulation Variables.

Variables	Magnitude
Switching Frequency f_s	50kHz
Load frequency f_o	50Hz
DC Sources V_{dc}	$V_1 = 16V,\ V_2 = 32V$ $V_3 = 64V,\ V_4 = 128V$
Load Inductance L	55mH
Modulation Index	1
Load Resistance R	50Ω

Simulation results of the proposed three-phase cascaded multilevel inverter are illustrated by the waveforms of by Figure 9 to Figure 18. Three cases of the cascaded topology are investigated for the proposed multilevel inverter. The first case consists of one submultilevel unit (or two cascaded basic unit), the second case consist of a cascaded topology of three basic units (i.e. one submultilevel and one basic unit). Finally, the third case consist of a cascaded topology of two submultilevel units (i.e. four basic units). The phase voltage waveforms are composed of the step output voltages (V_A, V_B and V_C) and corresponding reference voltages (Refa, Refb and Refc) which perfectly align together. The generated output waveforms of the first case are illustrated by Figure 9 to Figure 11. The phase voltage waveforms with peak value of $\pm 240V$ are depicted by Figure 9. The phase current waveforms with peak value of $\pm 8.1A$ are depicted by Figure 10. The line voltage waveforms are shown by Figure 11 having peak value of $\pm 415V$. The first case has two dc sources with maximum output voltage of $240V$. Therefore, the magnitude of input voltage is expressed by equation (14):

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$$V_1 = V_{dc} = 80V$$
$$V_2 = 2V_{dc} = 160V \quad (14)$$
$$V_{o,\max} = 3V_{dc} = 240V$$

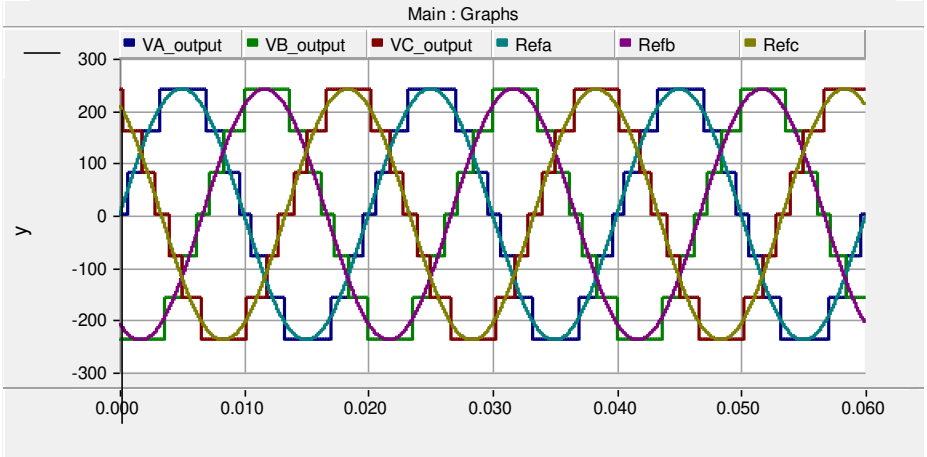

Figure 9. Phase voltage waveforms of the 1st case.

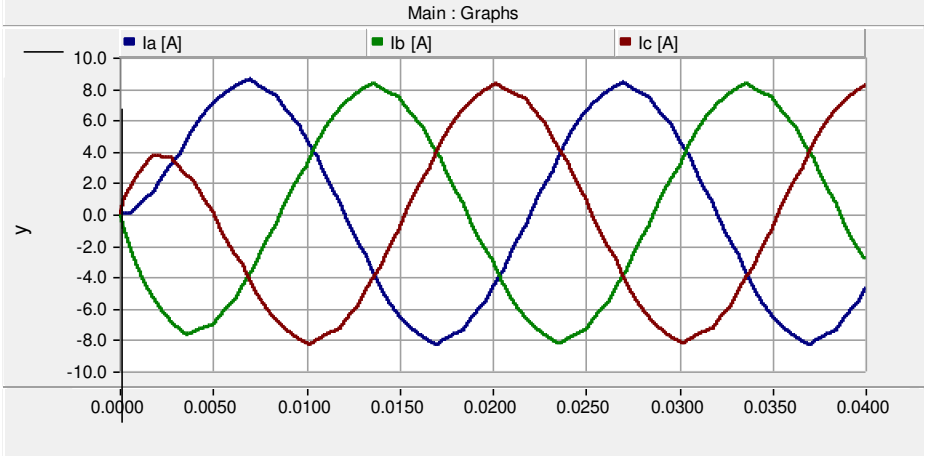

Figure 10. Phase current waveforms of the 1st case.

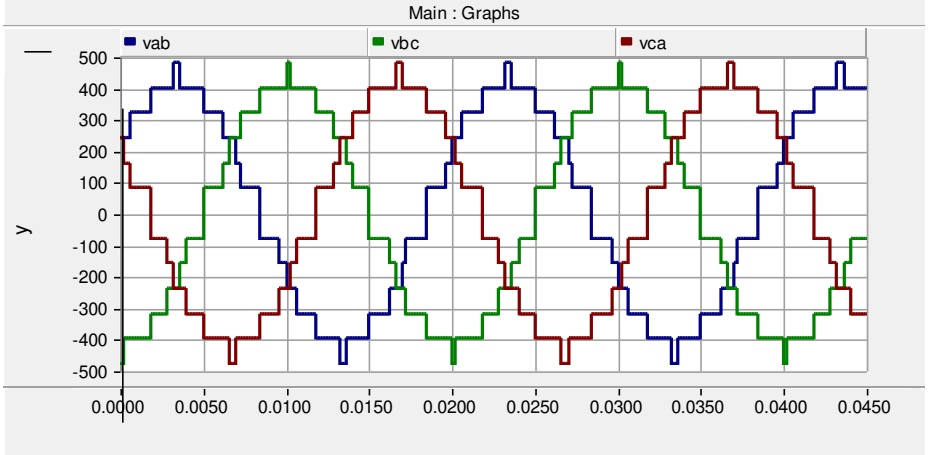

Figure 11. Line voltage waveform of the 1st case.

The output waveforms of the second case are illustrated by Figure 12 to Figure 14. The phase voltage waveforms with peak value of $\pm 240V$ are depicted by Figure 12. The line voltage waveforms

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are shown by Figure 13 having peak value of $\pm 415V$. The phase current waveforms with peak value of $\pm 8.1A$ are depicted by Figure 14. The second case has three dc sources with maximum output voltage of $240V$. Therefore, the magnitude of input voltage is expressed by equation (15):

$$\begin{aligned} V_1 &= V_{dc} = 40V \\ V_2 &= 2V_{dc} = 80V \\ V_3 &= 3V_{dc} = 120V \\ V_{o,\max} &= 6V_{dc} = 240V \end{aligned} \tag{15}$$

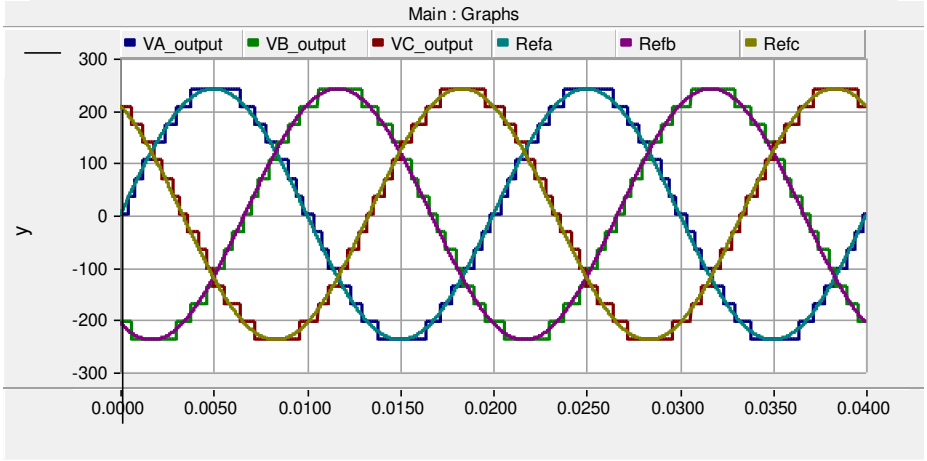

Figure 12. Phase voltage waveforms of the 2nd case.

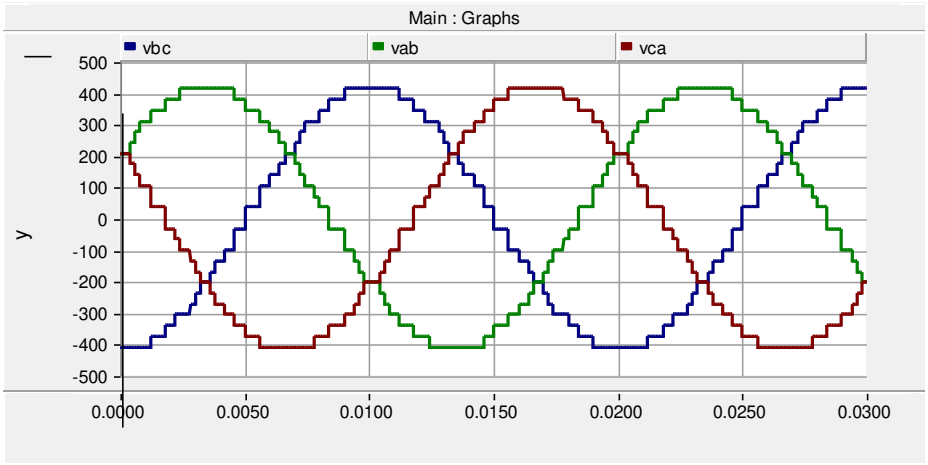

Figure 13. Line voltage waveform of the 2nd case.

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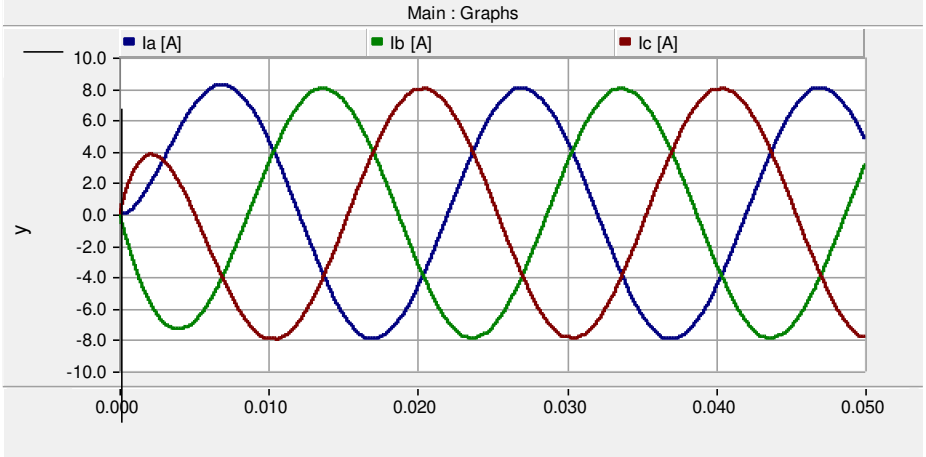

Figure 14. Phase current waveforms of the 2nd case.

The output waveforms of the third case are illustrated by Figure 15 to Figure 18. The phase voltage waveforms with peak value of $\pm 240V$ are depicted by Figure 15. The line voltage waveforms are shown by Figure 17 having peak value of $\pm 415V$. The phase current waveforms with peak value of $\pm 8.1A$ are depicted by Figure 16. The blocking voltage waveforms are illustrated by Figure 18, where switches in individual basic unit have equal blocking voltage and switches in the H-bridge have equal blocking voltage. The third case has four dc sources with maximum output voltage of $240V$. Therefore, the magnitude of input voltage is expressed by equation (16):

$$\begin{aligned} V_1 &= V_{dc} = 40V \\ V_2 &= 2V_{dc} = 80V \\ V_3 &= 4V_{dc} = 120V \\ V_4 &= 8V_{dc} = 120V \\ V_{o,\max} &= 15V_{dc} = 240V \end{aligned} \tag{16}$$

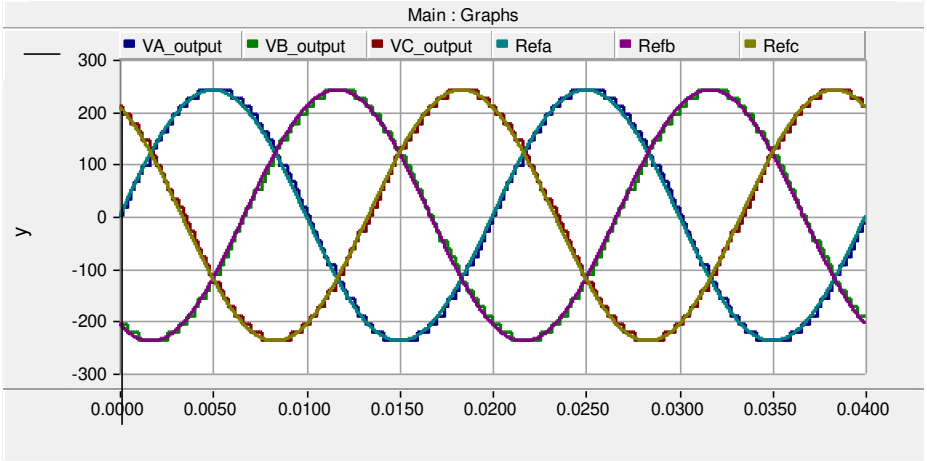

Figure 15. Phase voltage waveforms of the 3rd case.

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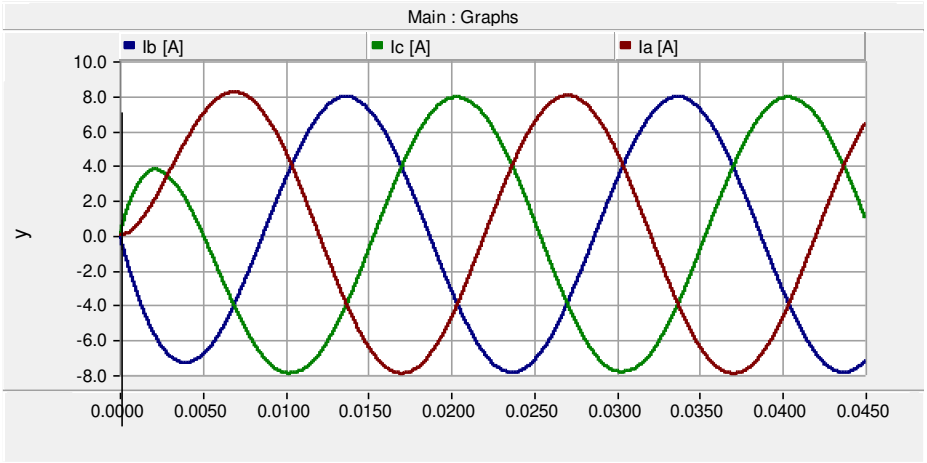

Figure 16. Phase current waveforms of the 3rd case.

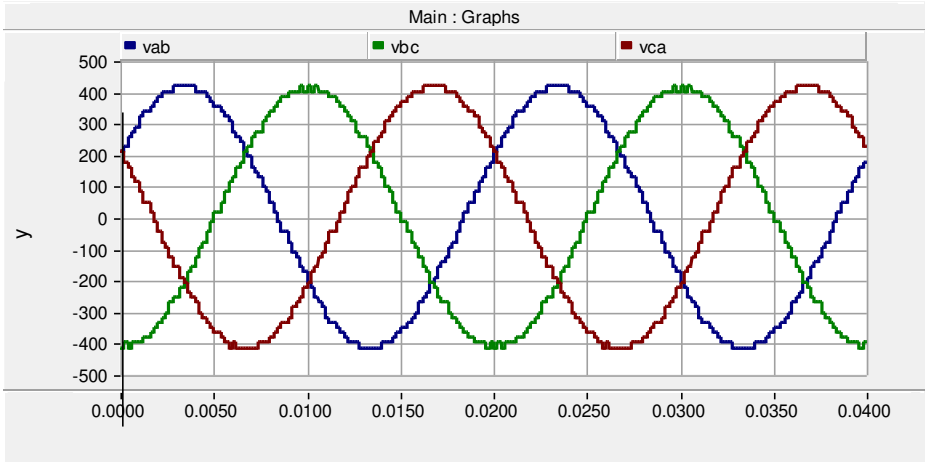

Figure 17. Line voltage waveforms of the 3rd case.

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Figure 18. Blocking voltage waveforms of the switches in 3rd case.

5. Conclusions

This work proffered a new cascaded three-phase multilevel inverter gounded on a cascaded submultilevel and single-phase H-bridge structures. The per-phase component distribution of the proposed topology are twelve unidirectional power switches, four dc sources and twelve driver circuits. Five algorithms of source voltage are proposed and the optimal algorithm selected to generate the peak load voltage and output levels. The proposed MLI is switched with high switching frequencies which provide high quality output waveforms, however, switching losses are increased. Contrastive evaluation of the proposed inverter and existing topologies shows the superb merits of the proffered MLI. Functionality of the proffered MLI is substantiated by simulation where three cases of the cascaded topology are investigated for the proposed multilevel inverter. The results of the simulated topologies where the first case is a submultilevel unit (or two cascaded basic units), the second case is three basic units (i.e. one submultilevel and one basic unit) and the third case is two submultilevel units (i.e. four basic units) shows that the phase voltage waveforms composed of step load voltages (V_A, V_B and V_C) and corresponding reference voltages (Refa, Refb and Refc) perfectly align together.

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