Superior High Transistor's Effective Mobility of 325 cm2/V-s by 5-nm Quasi-Two-Dimensional SnON nFET

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Article

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Abstract: This work reports the first nanocrystalline SnON (7.6 % Nitrogen content) nanosheet n-type Field-Effect Transistor (nFET) with transistor's effective mobility (μ_{eff}) as high as 357 and 325 cm²/V-s at electron density (Q_e) of 5×10^{12} cm^{-2} and ultra-thin body thickness (T_{body}) of 7 nm and 5 nm respectively. At the same T_{body} and Q_e, these μ_{eff} values are significantly higher than single crystalline Si, InGaAs, thin-body Si-on-Insulator (SOI), two-dimensional (2D) MoS_2 and WS_2. New discovery of slower μ_{eff} decay rate at high Q_e than SiO_2/bulk-Si universal curve was found, owing to one order of magnitude lower effective field (E_{eff}) by more than 10 times higher dielectric constant (κ) in channel material, which keeps the electron wave-function away from the gate-oxide/semiconductor interface and lowers the gate-oxide surface scattering. In addition, the high μ_{eff} is also due to the overlapped large radius s-orbitals, low 0.29 m_o effective mass (m_e^*) and low polar optical phonon scattering. SnON nFETs with record-breaking μ_{eff} and quasi-2D thickness enable potential monolithic three-dimensional (3D) integrated circuit (IC) and embedded memory for 3D biological brain-mimicking structures.

Keywords: high mobility; thin film transistors; SnON; SnO_2; density functional theory

1. Introduction

Modern processors, with over 100 billion transistors, are among the most complex systems. To meet the ever-changing demand for small and high-performance devices, processor transistor density and performance must be increased. Therefore, Moore's law must be preserved, i.e., transistor must be kept shrinking in size. Fin Field Effect Transistor (FinFET) technology is a game changer in enabling 22 to 3 nm technology nodes [1,2]. However, at sub-3 nm technology nodes in the near future, FinFET technology will face critical challenges of limited area scaling and performance degradation. The Fin width can no longer be scaled down due to increased threshold voltage (V_{th}) shift and lowered transistor's effective mobility (μ_{eff}) [3]. Gate length is also difficult to reduce due to transistor's quantum-mechanical (QM) tunneling from source to drain [4], resulting in high leakage current even when the transistor is off. Nanosheet (NS) transistors are the best solution to overcome these challenges of FinFET scaling, enabling higher drive currents [5,6]. NS-FETs are suitable for high computing needs due to their compatibility with various materials such as InGaAs, two-dimensional (2D) MoS_2 and WS_2, among others.

The downscaling of Si NS complementary FET is planned to 1 nm node, but further shrinking device is limited by the 2D material and hyper numerical-aperture (NA) extreme-ultraviolet (EUV) lithography. Unfortunately, there is no known solution to form defect-free and uniform monolayer 2D material over the 12-inch wafer. The rapidly increasing cost and huge power consumption are the major bottlenecks to realize hyper-EUV lithography system. Those downscaling barriers may be overcome by the monolithic three-dimensional (3D) structure [4,7,8] that mimic the bio-brain. In addition, monolithic 3D integrated circuits (ICs) can provide better performance of higher operating frequencies and lower power consumption than their 2D counterparts [7]. Yet the poor μ_{eff} for transistor made on backend dielectric of an IC is the basic challenge. Peviously, we reported high field-effect mobility (μ_{FE}) of SnO_2 [4,9,10] and SnON FET [11], but the effective mobility (μ_{eff}) is the required important

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data for transistors. The μ_{eff} can give crucial information on electron scattering mechanisms over the wide range of inversion charge (Q_e). The Q_e or gate voltage (V_G) dependent μ_{eff} is also essential for device modeling used for IC design. In this report, we measure the transistor output current over a wide range of V_G, equivalent to a Q_e close to 1×10^{13} cm^{-2}, to analyze the device scaling mechanism. Such high Q_e is critical to deliver a high transistor's output current and drive the IC speed quickly. The μ_{eff} degrades monotonically with increasing charge density is the physical limitation of a Metal-Oxide-Semiconductor FET (MOSFET). However, the MOSFET must be biased at high charge density to deliver a high output current. For the first time, this fundamental restriction is overcome by using a higher dielectric constant (κ) and high μ_{eff} channel. The nanocrystalline SnON n-type FET (nFET) has μ_{eff} as high as 325 $cm^2/V\text{-}s$ at 5×10^{12} cm^{-2} electron density (Q_e) and 5 nm nanosheet body thickness (T_{body}). At the same T_{body}, this μ_{eff} is significantly higher than single-crystalline Si, InGaAs, 2D MoS_2, 2D WS_2 and 2D WSe_2. The high μ_{eff} is also due to small 0.29 m_o effective mass (m_e*), overlapped large radius s-orbital, signifincatly lower effective field (E_{eff}) by >10× higher κ value than Si, GaAs, InP, GaN and SiC. The N^{3-} anions having higher p orbital energy can move up valance band (E_V) from first principle QM calculation and the Oxygen vacancy levels (V_o) residing in the channel layer are reduced to improve the μ_{eff}. The 3D 400°C process of SnON does not require a single crystal substrate; thus, the energy consumption is many orders of magnitude lower than today's single crystal Si wafer. The record-high μ_{eff} and quasi-2D thickness SnON nFET suggest potential monolithic three-dimensional (3D) and embedded dynamic random access memory (DRAM), to mimic the 3D bio-brain structure.

2. Materials and Methods

The bottom-metal-gate/high-κ/[SnON or SnO_2] nFETs were made by depositing a 50 nm TaN as bottom gate using reactive sputtering. Then, a 45-nm high-κ HfO_2 and 3-nm SiO_2 were deposited as a gate dielectric using electron-beam evaporator and annealed at 400°C under oxygen environment for 30 minutes using furnace. Further, SnON or SnO_2 channel layer were deposited by reactive sputtering using Sn target (purity 99.99%) followed by post-annealing at 400°C. The Sn sputter power, argon flow rate and process pressure is fixed at 30 W, 24 sccm and 7.6×10^{-3} torr respectively. O_2 flow rate is fixed at 20 sccm for SnO_2 channel layer. 7.6 % Nitrogen content (30 sccm of Nitrogen) are used for deposition of SnON channel layer. The source-drain electrodes of 80 nm thick Al was deposited and patterned using thermal coater. The fabricated nFET has channel length of 50 μm and width of 500 μm, respectively. The material properties of SnON and SnO_2 were studied using first principle QM calculations [12]. The Broyden-Fletcher-Goldfarb-Shanno (BFGS) minimization technique has been used to optimize the crystal structure [13]. It was done using the self-consistent field approach, which has a convergence precision of 1×10^{-8} eV/atom. This study made use of the generalized gradient approximation (GGA) with local density approximation plus U (LDA+U) approach. The energy cutoff for enlarging the plane wave basis set was set at 430 eV, and the Brillouin zone was sampled using the Monkhorst-Pack k-point approach with the k-points (6 ×6×5) [14].

3. Results

Using first principle calculations based on density functional theory, the density of state (DOS) for SnO_2 and SnON were examined as shown in Figure 1 (a) and (b), respectively. For convenience of analysis, the valence band maximum (VBM) was adjusted to zero. The lower conduction states close to the conduction band minimum (CBM) in SnO_2 and SnON were primarily produced from Sn 5s orbitals [15], while the localized states immediately above the VBM in SnON had a predominance of N 2p character. The N states in the valence band, principally N 2p character, are the main cause of the bandgap reduction in SnON. SnO_2 and N_2 doped SnO_2 have effective electron masses (m_e*) of 0.41 m_o and 0.29 m_o, respectively, where m_o is the free electron mass which is reported in our previous work [11]. The m_e* for SnON is evidently smaller than SnO_2, which could result in a larger μ_{eff}.

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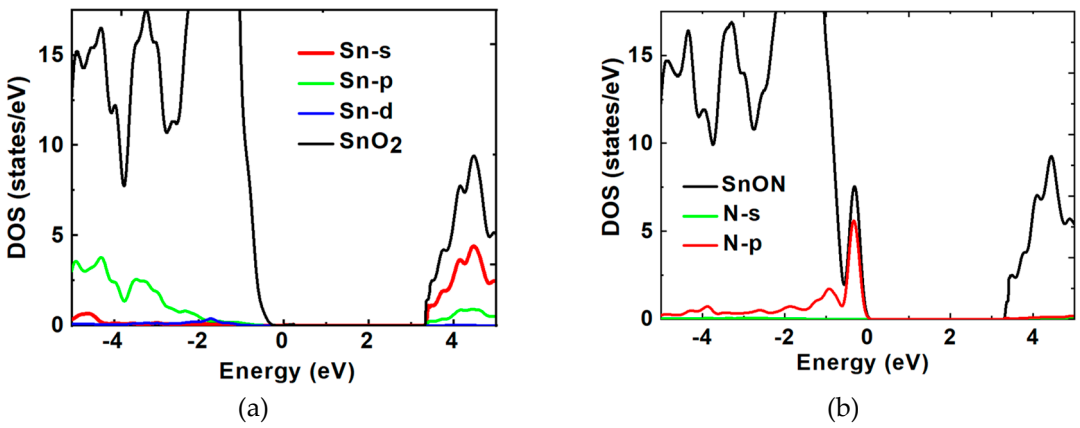

Figure 1. (a) DOS of Sn in SnO_2 and (b) DOS of N in SnON calculated using first principle density functional theory.

Figure 2 (a)-(c) depicts the transistor's drain-current versus drain-voltage (I_D-V_D) characteristics at various V_G for SnO_2 and SnON nFETs with T_{body} of 5 nm and 7 nm. A clear pinch-off and good current saturation were measured. The SnON nFETs displayed higher I_D compared to control SnO_2 device. Because the metal-gate/high-κ was made at the same run with identical gate oxide capacitance, the only reason to cause significantly higher I_D at the same V_G-V_T of SnON nFET is due to the higher μ_{eff}.

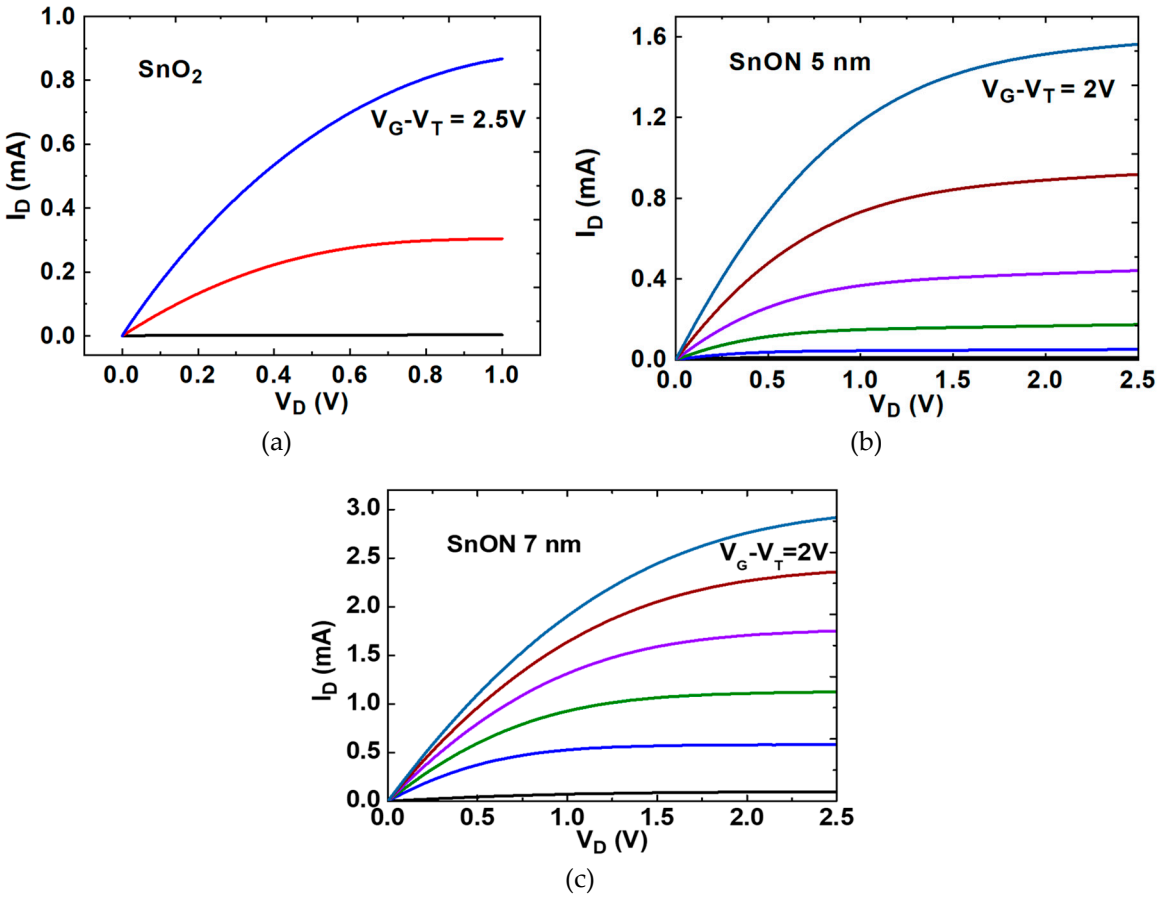

Figure 2. I_D-V_D output characteristics for (a) TaN/HfO_2/*5-nm*-SnO_2 nFET (b) TaN/HfO_2/*5-nm*-SnON nFET and (c) TaN/HfO_2/*7-nm*-SnON nFET.

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Figure 3 (a) and (b) display gate-current versus gate-voltage (I_G-V_G) and I_D-V_G transfer characteristics at a V_D=0.1 V for SnON nFETs with T_{body} of 5 and 7 nm. Large on-current/off-current (I_{ON}/I_{OFF}) is achieved in 5 nm T_{body} thickness that is important for IC application. The FET's scattering mechanism is further analyzed by the μ_{eff} as a function of Q_e. As shown in Figure 3 (c), at low to medium Q_e, the nFET's μ_{eff} of SnO_2 is significantly lower than SnON one. The SnO_2 nFET shows much faster μ_{eff} degradation with increasing Q_e. Although the oxide charges in high-κ dielectric is responsible for lower μ_{eff} than conventional SiO_2 gate dielectric [16–19], such μ_{eff} reduction is most significant at high Q_e rather than at low Q_e. It is reported that the μ_{eff} at low E_{eff} or Q_e is due to coulomb scattering from charged impurities [20]. The potential reason for such larger μ_{eff} of SnON nFET than that of SnO_2 may be related to the lower charged V_o. By injecting non-oxide nitrogen anions, SnON can lower the defect trap densities. This allows for the removal or passivation of Vo through substitutional alloying with N^{3-} to improve the μ_{eff} as seen in Figure 4. Similar observations were also found with ZnON [21]. It is well-known that the transition SiO_x between Si and SiO_2 gives a positive fixed oxide charge, primarily due to structural V_o defects in the oxide layer. Such positive V_o charge close to valence band in SnON may be lowered by extra N-band as shown in DOS of Figure 1(b).

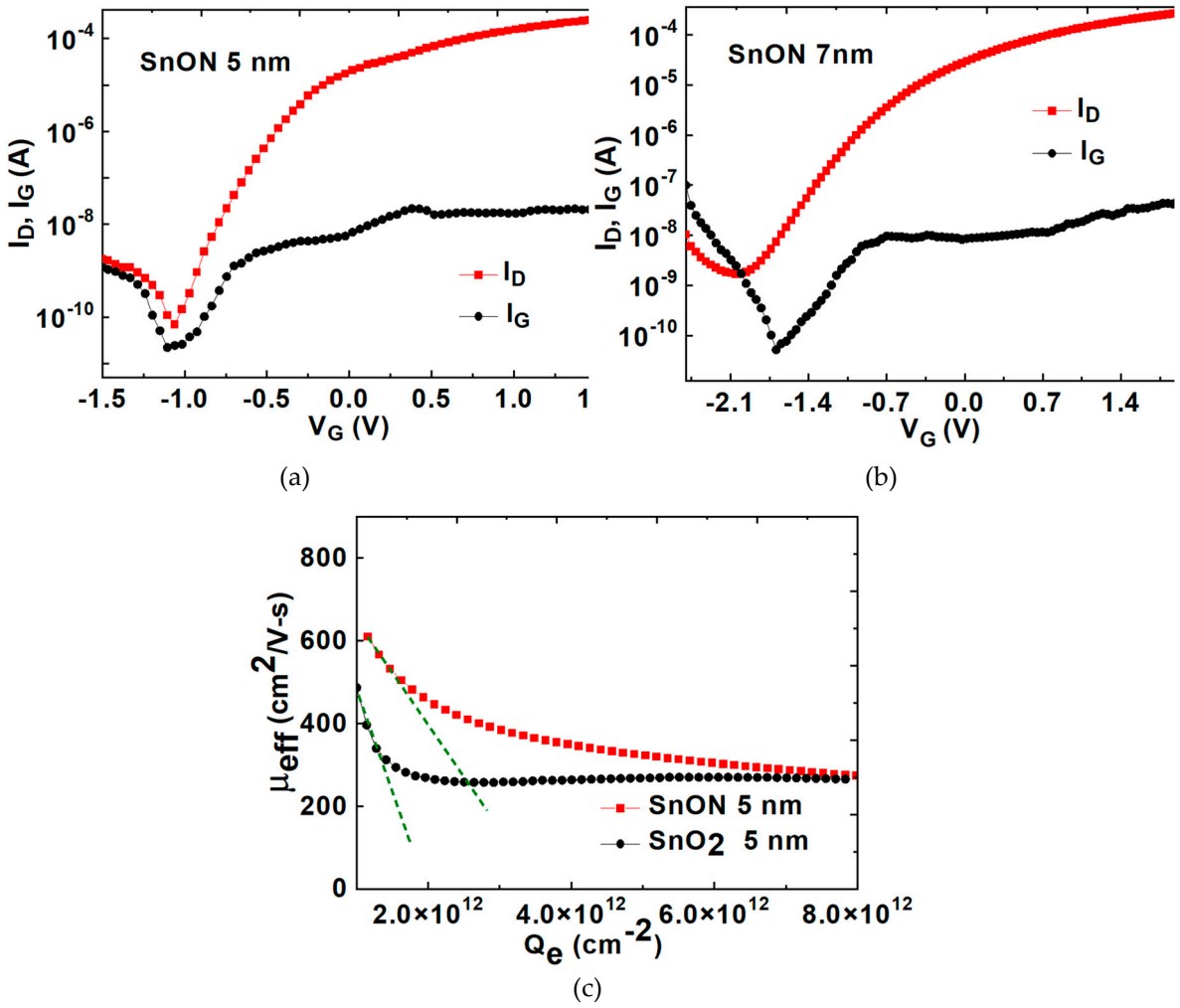

Figure 3. I_G-V_G and I_D-V_G transfer characteristics for (a) TaN/HfO_2/5-*nm*-SnON nFET and (b) TaN/HfO_2/7-*nm*-SnON nFET; and (c) μ_{eff} versus Q_e for 5-nm SnO_2 and SnON nFETs.

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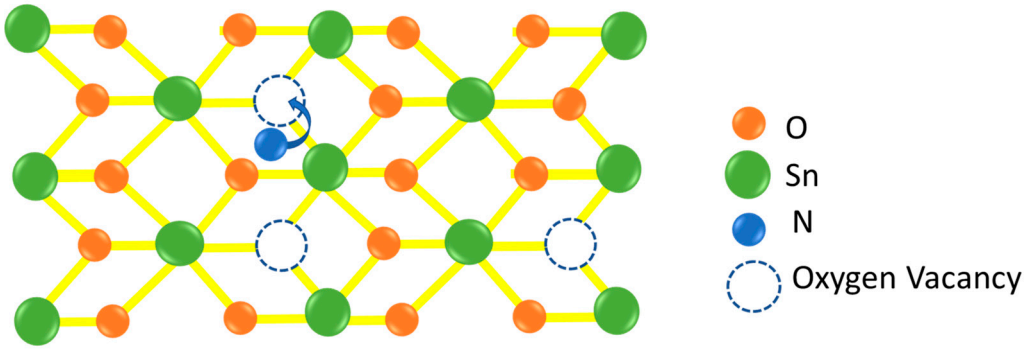

Figure 4. Diagrammatic sketch of substitutional alloying of Oxygen vacancy with Nitrogen atom

Figure 5 (a) further plots $1/\mu_{eff}$ vs. Q_e, and the large slope in the low Q_e is related to charged V_o scattering in SnO_2 that is lowered by adding N^{3-} anions. We further compare the μ_{eff}-Q_e dependence for universal SiO_2/bulk-Si, SiO_2/Si-on-Insulator (SOI), high-κ/SnO_2, and high-κ/SnON nFETs. As shown in Figure 5 (b), the μ_{eff} as high as 357 and 325 cm^2/V-s are achieved at Q_e of 5×10^{12} cm^{-2} and T_{body} of 7 and 5 nm, respectively. At 1×10^{13} cm^{-2} Q_e, an ultra-thin 5 and 7 nm thickness, the μeff of high-κ/SnON nFET is 85% and 95% of universal SiO_2/bulk-Si nFET. The μ_{eff} scattering mechanism of SiO_2/bulk-Si nFET at low, medium, and high E_{eff} is due to coulomb, phonon, and surface scattering, respectively. The universal μeff of SiO_2/bulk-Si nFET depends on standard $Q_e^{-0.3}$ in medium Q_e, which becomes $Q_e^{-0.6}$ dependence at high Q_e to 1×10^{13} cm^{-2}. However, the μ_{eff} decay rate of high-κ/SnO_2 and high-κ/SnON nFETs at high Q_e is much slower than universal SiO_2/bulk-Si and thin-body SOI nFETs [22]. To understand such abnormal slow μ_{eff} dependence on Q_e, we further measured the dielectric constant, κ of 5 nm SnO_2. Figure 6 shows the measured capacitance under various voltage at 1 kHz. The SnO_2 has a κ of 123 that is >10× larger than major semiconductors of Si, GaAs, InP, GaN, SiC etc [23–27]. This high κ value is also close to the reported data in literature [28]. The novel discovery μ_{eff} dependence on $Q_e^{-0.30}$ at high Q_e range is due to the >10× higher κ value to keep high-κ/SnON nFET at medium E_{eff} range. Here the E_{eff} is proportional to Q_e:

$$E_{eff} = \frac{1}{\varepsilon_{semi}}\left(\frac{|Q_e|}{n} + |N_{dep}|\right) \approx \frac{1}{\varepsilon_{semi}}\left(\frac{|Q_e|}{n}\right) @ \text{high } Q_e \quad (1)$$

The ε_{semi} equals $\varepsilon_0\kappa$, where ε_{semi} and ε_0 are permittivity of semiconductor and free space respectively. N_{dep} is the depletion charge of charged impurities in doped Si or charged V_o in major oxide semiconductors. The n factor in SiO_2/bulk-Si equals to 2 and 3 for nMOSFET and pMOSFET, respectively. The significantly much higher κ value than most of the commercial semiconductors of Si, GaAs, InP, GaN and SiC allow the channel electrons to keep a low E_{eff}. This in turn keeps the electron wave-functions in the conduction channel [29] away from the gate-oxide/semiconductor interface and decreases the gate-oxide surface scattering.

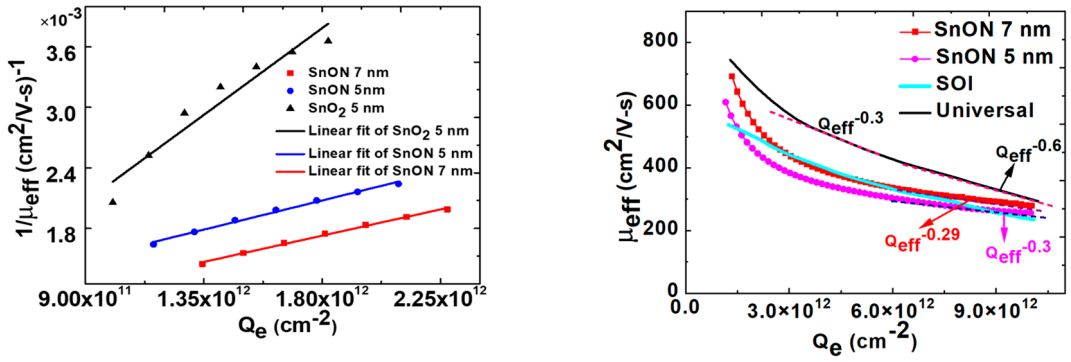

Figure 5. (a) $1/\mu_{eff}$ versus Q_e plot for 5-nm SnO_2, 5-nm SnON and 7-nm SnON nTFTs and (b) μ_{eff} versus Q_e with different channel thickness of SnON nFET and comparison with SOI [22] and universal nFETs.

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It is important to notice that the μ_{eff} of SnON nFET are the highest values among all the oxide-based semiconductors. This is due to the smaller m_e^* and larger phonon energy (E_{op}) [30] to give high μ_{eff}:

$$\mu_{op}\ \alpha\ \frac{1}{(\frac{m_e^*}{m_0})^{\frac{3}{2}}}\ \frac{\exp\left(\frac{E_{op}}{kT}\right)-1}{(\frac{E_{op}}{kT})^{\frac{1}{2}}} \quad (2)$$

The E_{op} is higher than ZnO, GaN, and SiC [31–34].

The total μ_{eff} can be expressed as:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{V_o}} + \frac{1}{\mu_{op}} \quad (3)$$

Here the μ_{Vo} is the FET's mobility that is limited by charged V_o. This μ_{Vo} is extremely important at low to medium Q_e shown in Figure 3 (c). The radius of s-orbital increases with increasing principle quantum number n with n^2 dependence, so the overlapping s-orbitals are stronger for SnO_2 than ZnO [15]. This explains why the mobility of SnON nFET is significantly larger than that of ZnO.

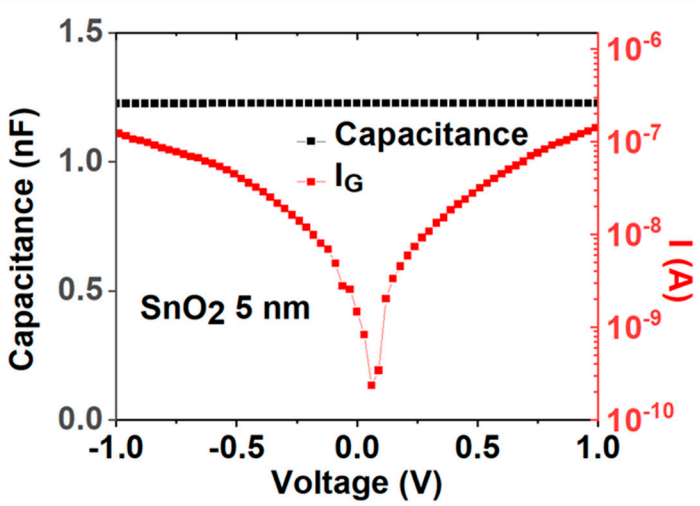

Figure 6. C-V and I-V plot for Ni/SnO_2/Ni capacitor.

Table 1 compares device performance. The wide energy bandgap (E_G) nanocrystalline SnON nFET has the highest μ_{eff} among single crystal Si, InGaAs, 2D MoS_2, and 2D WS_2. It is noticed that the next 2 nm node commercial NS nFET will use single crystalline Si with a T_{body} of 7 nm, since the μ_{eff} decreases with decreasing T_{body} with a T_{body}^6 dependence [3]. The μ_{eff} of high-κ/SnON nFETs is 2.7 times higher than that of Si nFET at the same 5 nm T_{body}, which could be used for downscaling the NS T_{body}. The wide-E_G SnON also leads to large I_{ON}/I_{OFF} as shown in Figure 3 (a).

Table 1. Comparisons of 2D semiconductor performances with our present work at Q_e of 5×10^{12} cm^{-2}.

Semiconductor Material	E_G (eV)	m_{eff} (m_o)	Dielectric Const. κ	μ_{eff} (cm^2/V-s) @5 nm
SnON (This work)	~3.3	~0.29	123	325
Si [5]	1.12	1.08	11.7	120
MoS_2 [5]	1.8	~0.5	4~8 (2~5 layers)	184
WS_2 [5]	1.4	0.33	-	234
InGaAs [5]	0.75	0.042	12.9	200

4. Conclusions

In this work, we demonstrated record high μ_{eff} 5-nm T_{body} nFETs, made on IC's backend for monolithic 3D usage. For the first time, the μ_{eff} of 325 $cm^2/V\text{-}s$ at 5×10^{12} cm^{-2} Q_e is 2.7 times higher than that of Si nFET at the same T_{body} of 5 nm. This was achieved using wide-E_G 5 nm quasi-2D SnON channel at 400°C process. Such high FET's μ_{eff} is due to the smaller 0.29 m_o, overlapped large-radius s-orbitals, and low polar optical phonon scattering. In addition, smaller μ_{eff} decay rate than SiO_2/bulk-Si nFET at high Q_e was found, owing to <10× E_{eff} by >10× higher κ value. Record high μ_{eff} SnON nFETs formed on IC's backend is the empowering technology for monolithic 3D ICs.

Supplementary Materials:

Author Contributions: Pheiroijam Pooja did the simulation and writing, Chun Che Chien did the experiments; Albert Chin is the principal investigator (PI) to monitor the project. All authors reviewed the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to privacy

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Conflicts of Interest: The authors declare no conflict of interest.

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