Design Analysis of a Modified Current Reuse Low Power Wideband Single-Ended CMOS LNA

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Article

Design Analysis of a Modified Current Reuse Low Power Wideband Single-Ended CMOS LNA

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Abstract: This paper presents the design analysis of a low power wideband single-ended CMOS low-noise amplifier (LNA). The proposed topology is based on the modified current reuse circuit to achieve good performance and low power consumption. Two stage current source (CS) amplifiers consume the same DC current which are isolated with large MIMCAPs. The proposed circuit has 2.5 GHz bandwidth which can cover several wireless communication standards (GSM, WLAN and Bluetooth). In first stage a current reuse circuit with shunt feedback is used to satisfy input impedance matching and amplify the signal with minimal noise injection. A common source (CS) with a source follower circuit forms the second stage to improve NF, harmonic distortion and also output impedance matching. The proposed LNA is designed in 65-nm CMOS technology with 2.51 GHz bandwidth that covers frequency range of 0.17-2.68 GHz. The post-layout simulation results show a maximum S_{21} of 17.24 dB, minimum NF of 2.67 dB, maximum IIP3 of -14.9 dBm, input and output return losses less (S_{11}, S_{22}) than -10 dB while power consumption is 3.52 mW from 1 V power supply. Excluding pads, the proposed circuit occupies 0.45 mm^2 silicon die area.

Keywords: CMOS LNA; wideband LNA; noise cancellation technique; linearity improvement; low power circuit

1. Introduction

Wideband low-noise amplifiers (LNAs) cover more wireless communication and should amplify with a flat response the weak signal received by the antenna with minimal noise injection. Input impedance matching and linearity with flat response are also two important parameters of a wideband LNA to prevent signal reflections and produce harmonic distortion whole bandwidth [1]. There is a trade-off between mentioned parameters with power consumption [2]. These days the low power designs have received a lot of attention, as most of systems are powered by only a single lithium battery which must work for several days (mobile phone) or even a year (medical devices) that is why designing low-power circuits has become a major challenge for RF designers [3]. LNAs can be designed in two modes of single-ended and differential. Although single-ended LNAs have lower gain and linearity, they are designed easily with good stability and low-noise performance whereas differential LNAs are excellent to achieve high gain and better linearity [4]. Common gate (CG) and common source (CS) circuits are used individually or a combination of both in differential and single-ended LNAs [5]. Although CG topology shows the best performance for a wideband LNA because of the low input impedance of independent of frequency, it needs high power to satisfy input impedance matching and NF, that is why it is not used alone for low power circuits. The CS with shunt feedback is another choice to design a wideband LNA which needs to consume high power to achieve high gain and low NF, that is why it is often used with current reuse technique [6].

The noise cancellation technique is another method for reducing thermal noise with low power consumption which was reported in 2004 [7]. Figure 1a shows conventional current reuse with shunt

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feedback [2] and Figure 1b noise cancellation LNA [7]. In [9] by using CS and CG a differential LNA has been reported which by using a cross-couple amplifier structure between positive and negative outputs linearity has been improved whole band width without decreasing gain. Although the reported results are excellent, an external RF chock has been used, power consumption is around 12 mW and it is also required a buffer circuit to measure. Authors in [10] has reported a differential LNA by combination of CG and CS in 65 nm CMOS. Although they have obtained high gain, the reported circuit consume 19.8 mW that is very high for low power devices, also the circuit needs an external RF chock. Reference of [11] has presented a differential LNA by using CG and CS. The reported results are reasonable with a 5.7 mw power that cover frequency range of 0.05 to 1.3 GHz; however, an external RF chock has been used. In [12] a differential LNA for sub-GHz applications has been provided which by using a CG and current reuse positive and negative outputs has been formed, respectively. Although the reported power is 3 mW, minimum NF is 3.6 dB that may not be acceptable for some sensitive applications. Kishore and Venkataramani in [13] has presented an inductor less wideband LNA that cover 0.18 to 2 GHz. The presented circuit has used combination of CG and CS, transconductance (gm) is also boosted by using a cross-couple structure between differential nodes. The results were reported in an unmatched output impedance condition, if the buffer current is calculated, the results will become poor. In [14] a shunt-feedback and feedforward technique has been used to design a single-ended wideband LNA which it cancels out noise and distortion simultaneously with ultra-low power of under 1 mW. Although the reported circuit consumes ultra-low power, it needs buffer network to measure and minimum NF of 4.45 dB has been reported which may not be suitable for some applications which need high sensitivity. Yunyou Pu and Wei Li have reported a differential wideband LNA from 0.2 to 3.2 GHz by using CS and CG and noise cancellation technique [15]. Although they have achieved to high gain and minimum NF of 1.4 dB, power dissipation is 17.4 mW that is very high for low power applications. Reference of [16] has presented a single-ended LNA by combination CG, current reuse and noise cancellation circuits for low voltage and low power applications. Although the reported results are acceptable, the area and power of buffer circuit has not been calculated. In [17] a differential wideband LNA by using noise and distortion cancellation technique with 1.6 GHz bandwidth has been provided. The minimum NF of 1.1 dB has been reported, however the power consumption is little high 9.1 mW that is not reasonable for low power systems.

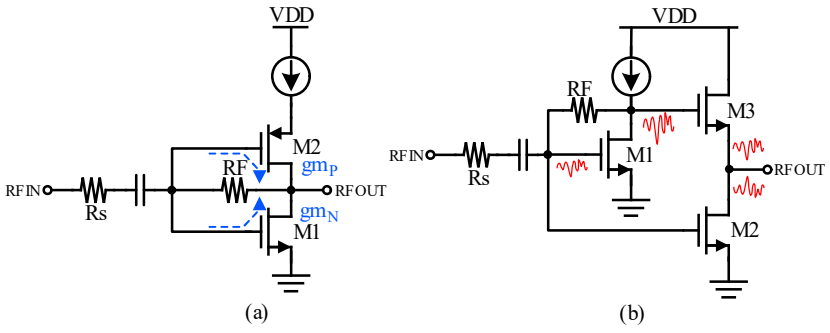

Figure 1. (a) Conventional current reuse LNA and (b) noise cancellation technique LNA.

This paper presents a single-ended wideband LNA for low-power applications with an operating frequency in the range of 0.17 to 2.68 GHz. The proposed circuit consists of two stages, a current reuse with shunt feedback and a series inductor peaking technique in the first stage, and a CG and CS form second stage. Both stages consume the same DC current which are isolated from each other by using large metal-insulator-metal capacitor (MIMCAP). By this method power consumption is reduced significantly. Output impedance is also matched to 50 Ω load which does not require an extra buffer network for measurement. The paper is organized as follows. Section 2 analyze the proposed LNA structure in details. Section 3 presents the post-layout simulation results and finally, Section 4 provides the conclusion.

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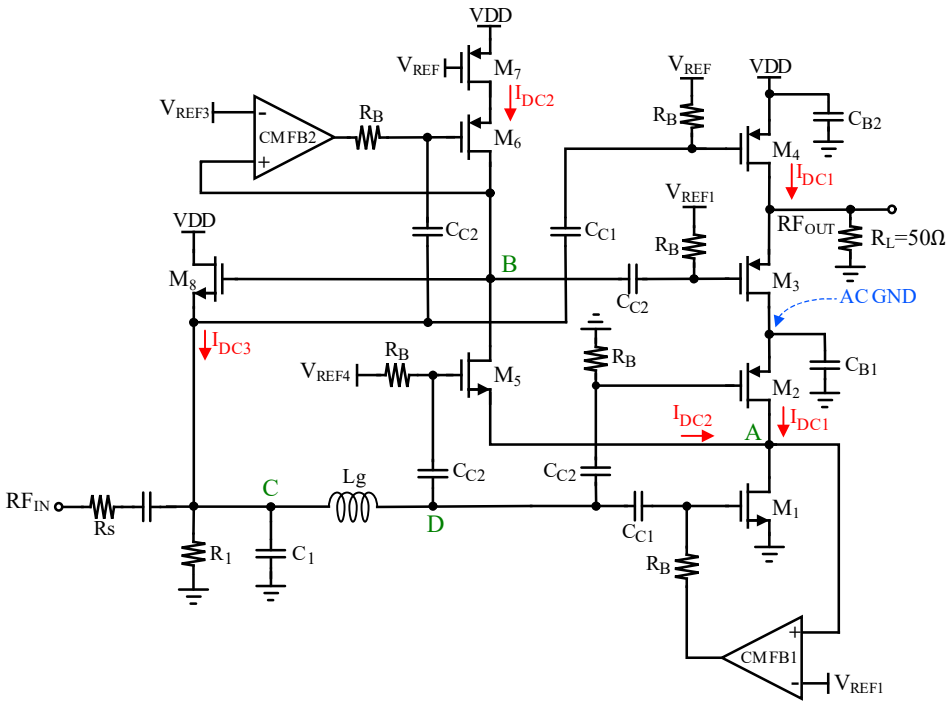
2. Analysis of the Proposed LNA

The proposed wideband LNA with value of elements is shown in Figure 2. The proposed LNA consists of two stages. Transistors of M_1, M_2 form first stage as a current reuse circuit which DC point in A node is set by a common mode feedback (CMFB) circuit. The length of transistors M_1 and M_2 is chosen to be slightly longer than the minimum length of the technology used (60 nm) to increase the intrinsic impedance between source and drain (1/gds), which slightly increases the voltage gain at node A [8]. M_1, M_2 also act as a gm boosting for M_5, as a result the signal of A node with again amplification appears in B node. DC point of B node is also set by CMFB2. M_8 acts as a shunt- series feedback to meet a wideband input impedance matching and also linearity improvement, this transistor is biased in sub-threshold region to decrease power, besides because gain in B node is high, input impedance matching is satisfied very well without increasing the feedback network coefficient (gm_8). Transistors of M_3 and M_4 form second stage of the proposed LNA which consumes the same DC current as first stage and are isolated from first stage by capacitor of C_{B1}. M_3, M_4 act as a buffer stage which are used for output impedance matching. Gate terminal of the M_4 is also connected to input (node of C) and acts as noise and distortion cancellation technique to improve slightly gain, NF linearity. It means that the noise and harmonic distortion returned by the feedback network is slightly amplified by this transistor with a 180° phase difference and summed with the output, which reduces distortion and noise.



	M × W/L
M_1	32 × 2.3 µm/70 nm
M_2	32 × 2.1 µm/70 nm
M_3	32 × 3.7 µm/60 nm
M_4	32 × 2.9 µm/70 nm
M_5	20 × 1.1 µm/70 nm
M_6	10 × 1.1 µm/80 nm
M_7	32 × 2 µm/60 nm
M_8	4 × 1.2 µm/60 nm

L_g	5.7 nH with Q ≈ 12.8 @1.5 GHz
C_1	MIMCAP 372 fF
C_{C1}	MIMCAP 4.1 pF
C_{C2}	MIMCAP 1.8 pF
C_{B1}	4 × MIMCAP 12 pF
C_{B2}	MIMCAP 3.65 pF
R_B	R-POLY 12 KΩ
R_1	R-POLY 4.1 KΩ

Figure 2. Schematic of the proposed wideband LNA with values of its elements.

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Inductor Lg is used to help flat gain, input impedance matching and slightly bandwidth. The details of the input impedance matching, voltage gain, NF, and linearity of the proposed balun-LNA are presented in the following.

2.1. Input Impedance Matching

Figure 3 shows the small-signal model of input of the proposed wideband LNA to calculate the input impedance. The inductor Lg more or less compensates parasitic capacitors (C_P) for frequencies of above 1.5 GHz to satisfy input impedance matching whole desired bandwidth (0.17 to 2.68 GHz).

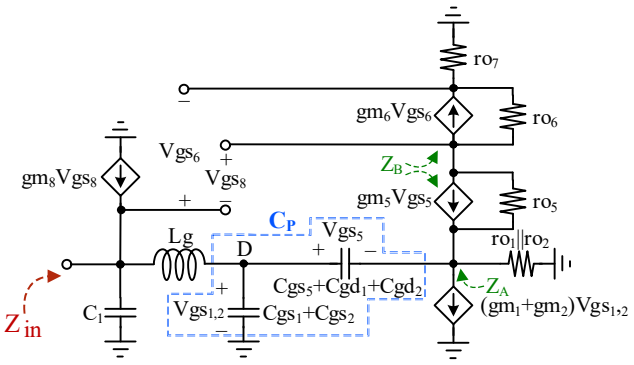

Figure 3. Small signal model of first stage for input impedance calculation.

According to the Figure 3, the input impedance of the proposed LNA is approximately calculated as follows:

$$Zin \approx \frac{1}{SC_1}\left\| \left(\frac{S^2 LgC_P + 1}{SC_P + gm_8 Z_B \left(S^2 LgC_P + 1\right) \times \left(\frac{gm_6}{1 + gm_6 ro_7} + \frac{gm_5}{S^2 LgC_P + 1} - \frac{gm_5 Z_A \left(gm_5 - \left(gm_1 + gm_2\right)\right)}{\left(1 + gm_5 Z_A\right)\left(S^2 LgC_P + 1\right)} + 1 \right)} \right) \right. \quad (1)$$

where $Z_A \approx ro_1 \| ro_2$, $Z_B \approx \left(gm_6 ro_6 ro_7\right) \| \left(gm_5 ro_5 \left(ro_1 \| ro_2\right)\right)$ and C_P is parasitic capacitors of D node that approximately equals:

$$C_P \approx \left(Cgs_1 + Cgs_2\right) + \left(Cgd_1 + Cgd_2 + Cgs_5\right)\left(1 + \left(gm_1 + gm_2\right)\left(ro_1 \| ro_2\right)\right) \quad (2)$$

Based on the Equation (1), when Lg and C_P are resonated, the input impedance tends towards zero which causes S_{11} to be spoiled, however the amount of the resonance frequency is around 6 GHz that is much more than desired bandwidth (0.17 - 2.68 GHz).

2.2. Voltage Gain

Figure 4 shows AC model of the proposed circuit. As is clear, first stage is formed by M_1, M_2 M_5, M_6 and feedback of M_8. Transistors M_3 and M_4 form second stage.

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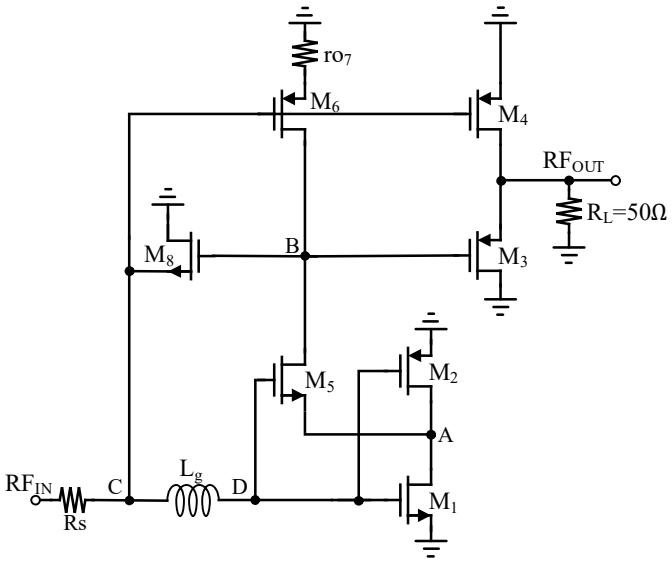

Figure 4. AC model of the proposed LNA.

By considering an output load of R_L of 50 Ω, voltage gain can be approximately calculated as follows:

$$\frac{V_O}{V_S} \approx \frac{\left(gm_3 Z_B\left(1+gm_6 ro_7\right)\left(-\left(gm_1+gm_2\right)\left(1+gm_6 ro_7\right)-gm_6\right)-gm_4\left(1+gm_6 ro_7\right)\right)R_L}{\left(1+gm_3 R_L\right)\left(1+gm_6 ro_7\right)\left(1+gm_8 R_S\left(\left(gm_1+gm_2\right)Z_B+1\right)\right)+gm_8 R_S gm_6 Z_B} \quad (3)$$

where $Z_B \approx \left(gm_6 ro_6 ro_7\right)\left\|\left(gm_5 ro_5\left(ro_1\left\|ro_2\right.\right)\right)\right.$. Inductor Lg and parasitic capacitors are not considered in Equation (3) to simplify calculation and better understanding, however the effect of Lg on the gain is explained below.

The inductor Lg acts as a series inductive peaking to compensate parasitic capacitors of D node. Figure 5 shows effect of Lg on the gain, as shown, it is clear that before the current reuse stage, a passive gain is created by the inductor Lg at D node, which contributes to increase the 3_{dB} bandwidth.

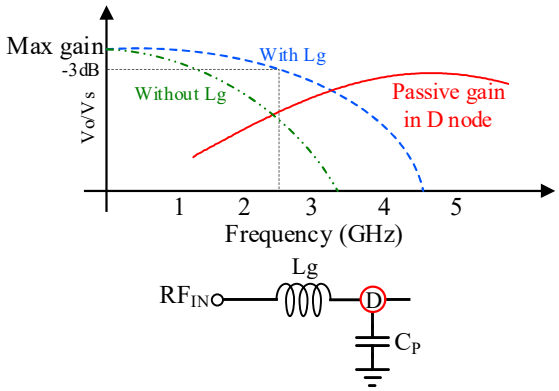

Figure 5. Increasing 3dB bandwidth by using inductor Lg as series inductive peaking.

2.3. Noise Analysis

Considering the proposed circuit consists of two stages, according to the Friis equation, it is clear that the first stage has the main effect on NF [2]. Although M_4 is connected between the input and output as a CS and can play the role of noise cancellation technique [7], the conditions for complete cancellation cannot be met due to the low-power design and also the connection of a 50 Ω load to the output. In other words, the noise sampling coefficient by the M_8 feedback is much lower than its amplification by M_4 with R_L of 50 Ω that is why it has low effect on NF improvement. In first stage, thermal noise of M_5 and M_6 can be ignored because they have a degenerated impedance in their

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source terminals [2]. Transistor M_8 is biased in sub-threshold region and low current by a large resistor of R_1 to decrease power dissipation, although shot noise is comparable to thermal noise in this regime [18], as a result it can also be ignored because seen impedance in this node (node of C) is too small by around Rs. As a result, main noise depends on current reuse stage, so NF is calculated as following:

$$NF = 1 + \frac{\left(ro_1 \| ro_2\right)^2 \left(1 + gm_8 Rs\right)^2 \gamma \left(gm_1 + gm_2\right)}{\left(1 + \left(gm_1 + gm_2\right)\left(ro_1 \| ro_2\right)\right)^2 Rs} \quad (4)$$

where γ is the correction factor which is assumed to be the same for NMOS (M_1) and PMOS (M_2) for simplicity. According to Equation (4), because the value of $\left(gm_1 + gm_2\right)\left(ro_1 \| ro_2\right)$ is much higher than one, the (4) is simplified to (5).

$$NF \approx 1 + \frac{\left(1 + gm_8 Rs\right)^2 \gamma}{\left(gm_1 + gm_2\right) Rs} \quad (5)$$

According to Equation (5), obviously, the greater the effect of the feedback network of M_8 $\left(gm_8 R_S\right)$, the worse the NF will be.

2.4. Linearity Analysis

Usually, both types of LNAs (single-ended and differential) are designed in one stage to achieve good linearity [2]. In a non-ideal amplifier signal is approximately amplified as [2]:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \quad (6)$$

where α_1 is as the small-signal gain. In differential LNAs due to the output differential signal, second term of (6) can be decreased significantly [2], but third order harmonic is still problematic [9].

Figure 6 illustrates the mechanism of linearity improvement of the proposed circuit. If two interferer signals of ω_1, ω_2 is applied to input, a third order harmonic of $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ is produced in output of first stage of current reuse (A node). The produced harmonic node of A comes to node of B through M_5 and is also brought to input (node of C) through feedback of M_8 then it is amplified with 180° phase different by M_4 that can decrease the distortion of output and improve linearity [7]. Based on the Figure 6, in the proposed circuit the conditions for complete harmonic cancellation are not provided, because the harmonic appeared in node B reaches node C with a large attenuation coefficient which transistor M_4 cannot fully compensate this attenuation in output due to low power design and consequently low gm_4, which is why linearity of the proposed LNA is improved by slightly less than 2 dB.

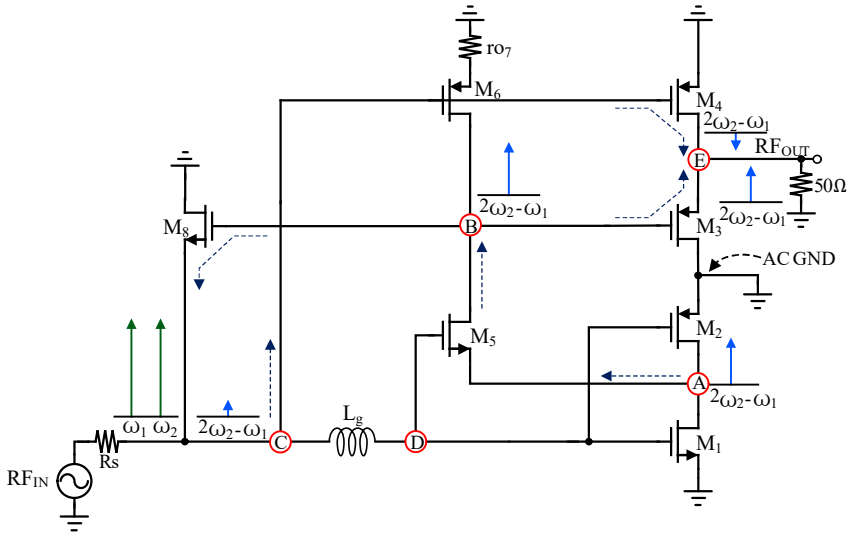

Figure 6. The mechanism of the linearity improvement.

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3. Simulation Results

The proposed low power single-ended wideband LNA is suitable for low power Mult-standards receivers which cover the frequency range of 0.17-2.68 GHz such as (GSM, WLAN and Bluetooth). The proposed LNA is designed in 65 nm CMOS technology with 1 V supply voltage and a reference current (IREF) of 50μA for bias network to improve circuit stabilization under process, supply and temperature (PVT) variations. Figure 7 shows the layout of the proposed LNA with a core area of 0.45 mm^2. The results of the proposed wideband LNA across PVT and corner variations are presented in Figures 8 and 9, respectively. As shown, S_{11} and S_{22} have a value of less than -10 dB over the entire desired bandwidth, also the power gain (S_{21}) and NF have an amount of more than 15 dB and less than 3.24 dB over the desired bandwidth, respectively. Figure 10 shows stability factor (Kf) that has an amount of more than 1 from 0.1 to 12 GHz which means the proposed circuit is unconditionally stable.

To ensure the value of the inductance and quality factor (Q) of the Lg, electromagnetic (EM) simulation has been performed. Figures 11 and 12a demonstrate substrate stack map of 65 nm CMOS technology and inductor Lg for EM simulation. Figure 12b illustrates EM simulation of Lg which values of inductance and Q-Factor at 2 GHz are obtained 5.9 nH and 13.9, respectively. The Self-resonant frequency (SRF) is also around 9 GHz that is a reasonable value for the desired bandwidth (0.17 to 2.68 GHz).

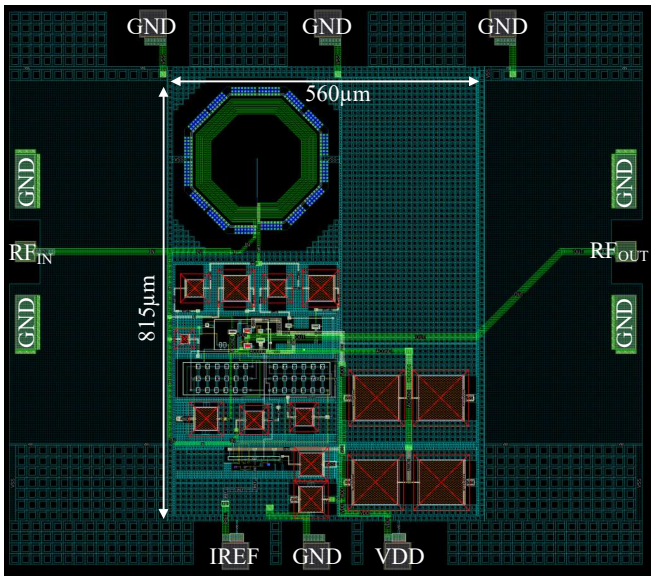

Figure 7. The layout of the proposed wideband LNA with DC and signal PADs.

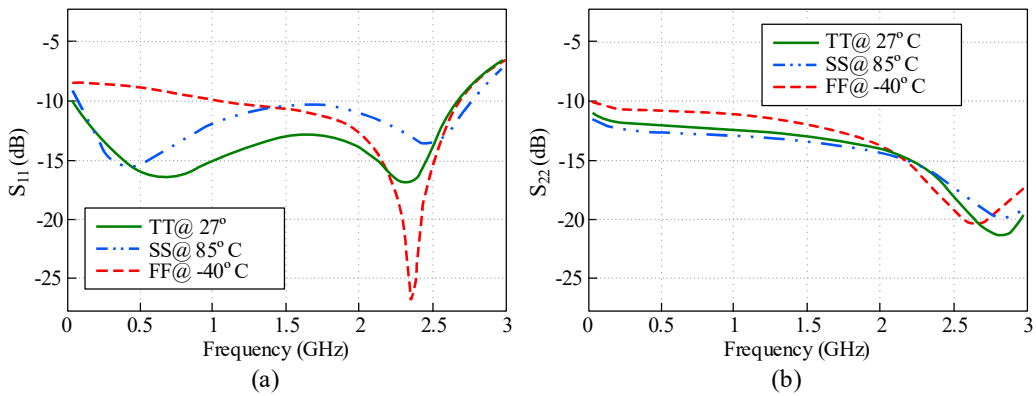

Figure 8. (a) The post layout simulation of input and (b) output return losses in temperature and corner variations.

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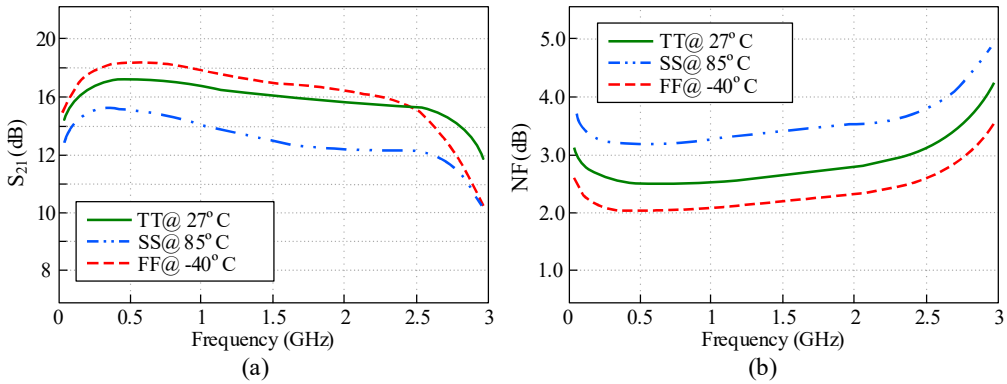

Figure 9. (a) The post layout simulation of power gain and (b) NF in temperature and corner variations.

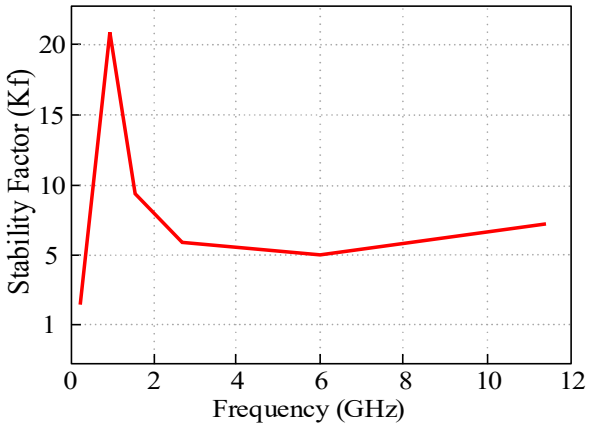

Figure 10. Stability factor (Kf) from 0.1 to 12 GHz.

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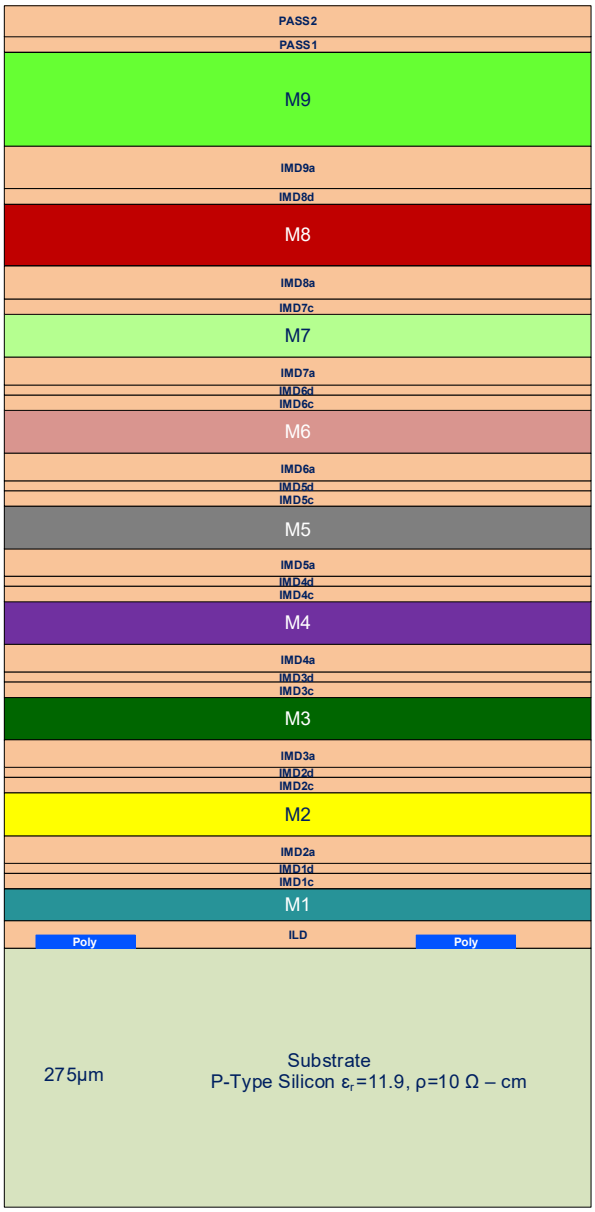
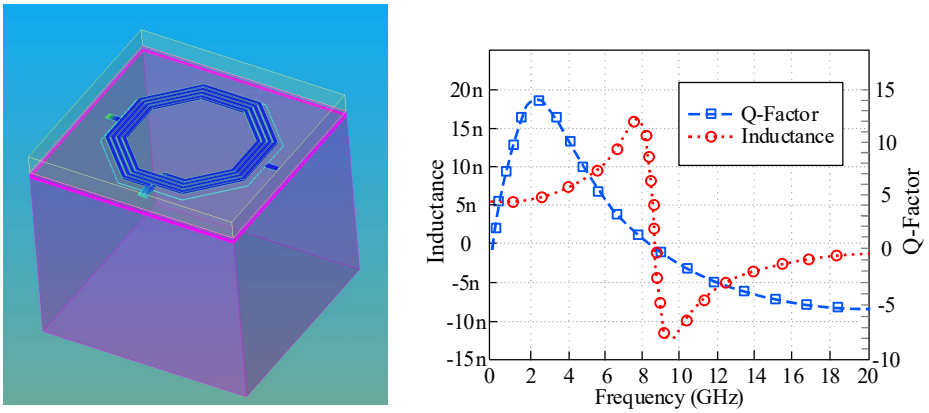


Figure 11. Substrate map of 65 nm CMOS technology for EM simulation.



(a) (b)

Figure 12. (a) The inductor of Lg in ADS environment (b) inductance and Q-Factor of Lg by EM simulation.

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As mentioned in the linearity analysis section, M_4 improves linearity. To prove it, IIP3 is simulated in two cases that is shown in Figure 13a,b. Once when the terminal gate of M_4 is connected to the input and M_4 acts as a CS which the mechanism of distortion improvement is carried out and once when M_4 acts only as a current source for second stage. Figure 14a,b show intercept point three (IIP3) at 2.4 GHz and IIP3 versus input frequency, respectively. As shown in Figure 14a, by simulation of two-tone tests with 10 MHz spacing at 2.4 GHz when M_4 is as CS, an IIP3 of -14.9 dBm is achieved. Figure 15b, shows both curves of IIP3 at entire desired bandwidth when M_4 acts as CS and current source, respectively. As shown the IIP3 is improved when M_4 acts as a CS. Table 1 summarizes the results of the proposed wideband LNA in different corners and temperatures. Although the proposed LNA show a small variation in different corners, it is robust against corner and temperature variations. Table 2 represents a comparison to state-of-the art work between the proposed LNA and some similar recent works. Figer of merit (FoM) are calculated as follow [16]:

$$FOM = 20\log_{10}\left(\frac{S_{21}[abs]\,.\,BW_{-3dB}[GHz]}{P_{DC}[mW]\,.\,(F_{\min}-1)}\right) \quad (7)$$

Table 1. Corners and Temperature Simulation Results.

Parameter	TT @ 27˚C	SS @ 85˚C	FF @ -40˚C
BW-3dB (GHz)	0.17-2.68	0.17-2.2	0.17-2.54
S21 (dB)	15-17.24	13.58-15.58	15.2-18.2
NFmin (dB)	2.67	3.35	1.99
IIP3 (dBm)	-14.9	-13	-12.6
Power (mW)	3.52	3.64	2.87

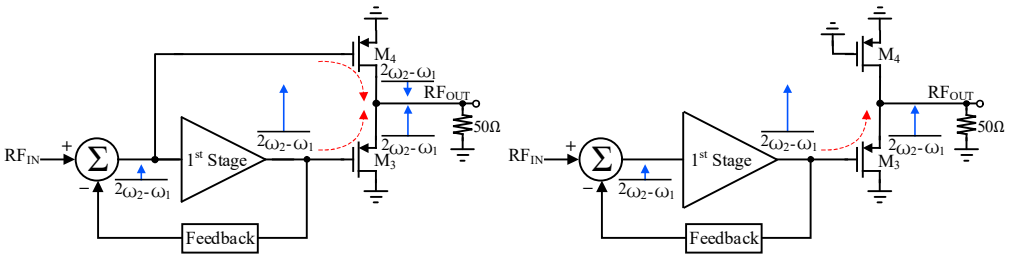

Figure 13. (a) M_4 as CS (b) M_4 as a current source.

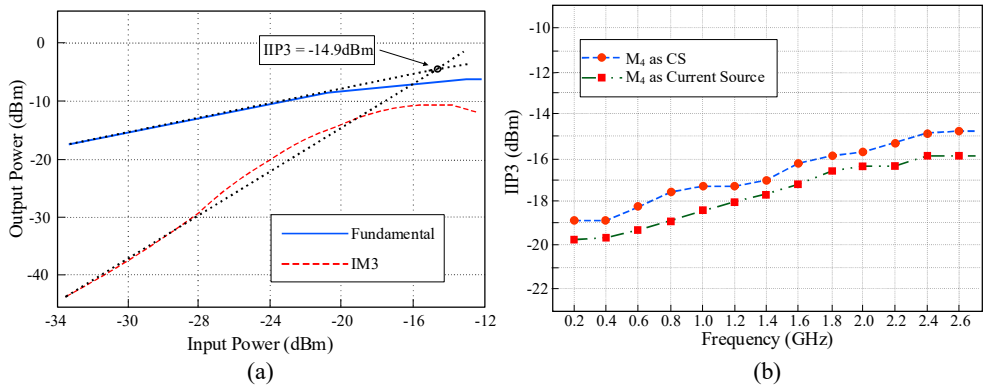

Figure 14. (a) Amount of IIP3 at 2.4 GHz (b) IIP3 versus the input signal frequency with 10 MHz spacing.

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Table 2. Performance Comparison with Several Recent Similar Works.

Reference	CMOS Process	VDD (V)	Frequency (GHz)	S_{21} (dB)	NF (dB)	S11 (dB)	IIP3 (dBm)	Symmetric load	Power (mW)	Area (mm^2)	FoM (dB)
TCAS-II'22*[b] [9]	65 nm	1.5	0.47-3.3	19.45-22	2.57-3.5	<-10	+2.81	Yes	12.5	0.057	11.02
TCAS-I'19[b] [10]	65 nm	2.2	0.05-1	24-30	2.3-3.3	<-12	-4.1	Yes	19.8	0.045	6.84
TCAS-I'20[b] [11]	65 nm	1	0.05-1.3	24-27.5	2.3-3	<-12	-2.2	Yes	5.7	0.046	17.73
TCAS-II'21[b] [12]	180 nm	1.8	0.13-0.93	16.6-19.6	3.6-5	<-10	-8.5	Yes	3	0.18	6.52
AEUE'19*[b] [13]	180 nm	1.2	0.18-2	15-20.8	2.65-3.8	<-8	-4.91	Yes	4.9	0.04	13.7
TCAS-I'24[b] [14]	65 nm	0.78	0.1-4.2	15.6	4.45-6.9	<-10	-14.5	No	0.96	0.011	23.19
MWT'25 [15]	28 nm	1.1	0.2-3.2	24.4-26	1.4-2.18	<-15	-3.6	Yes	17.4	0.018	19.13
TCAS-I'24[b] [16]	28 nm	0.6	0.2-2.85	20	2.9-3.6	<-13	-12.3	No	1.74	0.0048	24.19
TCAS-II'25[b] [17]	130 nm	1.3	0.01-1.7	21.5	1.1-1.9	<-10	-2.3	Yes	9.1	0.18	17.45
This work*	**65 nm**	**1**	**0.17-2.68**	**15-17.24**	**2.67-3.24**	**<-10**	**-14.9**	**No**	**3.52**	**0.45**	15.7

* Post-layout simulation results. [b] needs buffer to measure.

Excluding [15] which has a fully output impedance matching, other cited references only have reported the LNA core power, that is why some of them has a FoM of higher than the proposed circuit. Only [12] has mentioned the output buffer power of 9 mW, which would make its FoM much lower if it were included. The results of the proposed LNA are reported without using extra output buffer and under conditions of fully output impedance matching. One of the advantages of the proposed topology used is to perform output impedance matching without high power consumption.

4. Conclusions

In this paper, a low power wideband single-ended LNA is analyzed and presented which cover 0.17 to 2.68 GHz and is suitable for low power multi-standards wireless applications. By using two stages of amplifier with same DC current and noise and distortion cancellation method all parameters of a wideband LNA have been satisfied plus output impedance matching in a low power design. One of the advantages of the proposed LNA is a fully output impedance matching with low power consumption so no additional buffer is required for measurement.

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