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Gamma Radiation Effects on n-MOSFET I–V Performance

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Abstract

In this work, we investigate n-channel Si MOSFETs commonly used in radiation-hardened electronics for space and nuclear applications. Radiation-induced defects degrade the transistor electrical characteristics, particularly the current–voltage behavior. Experimental results reveal a negative shift in the threshold voltage with increasing gamma-ray doses up to 348 krad, mainly attributed to the trapping of positive charges in the gate oxide. In the proposed model, these trapped charges are represented through an effective acceptor concentration N_A^{eff}, introduced as a phenomenological parameter to describe their electrostatic influence on the inversion layer, without implying any physical modification of the silicon doping. Static (DC) and small-signal (AC) current models are developed to describe the post-irradiation electrical behavior. Empirical relationships linking device parameters to the total ionizing dose are extracted from experimental I–V measurements. The proposed approach provides a compact framework suitable for low-frequency circuit-level simulations under radiation environments.

Keywords: SOI n-MOSFET; gamma radiations; I-V characteristics; total ionizing dose; in-situ thermal annealing; electron traps

I. Introduction and Related Works

During the last decades, significant progress has been achieved in epitaxial growth and technological design for both bipolar-junction and metal-oxide semiconductor FETs [1–4]. The challenge has been how to reduce the detrimentaleffects of imperfections. However, impurities and defects are always present in the host lattices, thus inducing localized extrinsic states in the active layers. Most process-induced traps behave as trapping centers, leading to deposited positive charges. The origin of these active traps, and especially their locations, has been characterized using various techniques, but explanations remain controversial. It is worth noting that defects may be intrinsic or arise from extrinsic origins.

For MOSFET transistors operating in hostile environments, exposure to gamma radiation can cause significant disturbances in their characteristics and functionality [5–7].The dose rate of gamma radiation is an important parameter influencing the degradation mechanisms in MOSFETs, as highlighted in previous studies **[8–10]**. In thiswork, as ample of 1µm SOI-PD nMOSFETs from xfab, were irradiated using a Co-60 gamma source with a controlled dose rate of 1.2 krad(Si)/h. The total ionizing dose (TID) applied was up to 348 Krad. The chip were packaged in a Dual-In-Line ceramic package and connected to a load board for bias application and I-V measurements during Irradiation.

The investigated devices are commercial n-channel silicon MOSFETs fabricated using a conventional CMOS process on p-type substrates. Gamma irradiation experiments were carried out at room temperature using a calibrated Co-60 source. The total ionizing dose (TID) was progressively increased up to 348 krad(SiO2) under unbiased conditions. After irradiation, the devices were subjected to a thermal annealing step performed in ambient atmosphere at 120°C for 30 minutes. Electrical I–V measurements were performed before irradiation, after irradiation, and after annealing.

 doi:10.20944/preprints202505.1056.v2

Measurements were conducted on multiple nominally identical devices for each dose level. The reported results correspond to average values, showing good reproducibility and limited dispersion. The TID induce permanent and cumulative degradation of the transistor's electrical properties during gamma radiation. These degradations are mainly attributed to an accumulation of trapped holes in the oxide layer and at the oxide–channel interface [11]. It is important to mention that the density of trapped charges strongly depends on device architecture and the technological process [12].As a first approach to mitigate trapped charge effects, irradiated transistors were subjected to annealing at relatively high temperatures over prolonged heating periods [13,14]. However, the major drawback of this procedure is the high thermal energy consumption. In recent works, advanced recovery methods have been developed using micro-integrated hot plates, which offer rapid response, low power consumption, and in-situ electro-thermal annealing [13,15].From a technological perspective, it has also been demonstrated that the immunity to transient gamma radiation effects can been hanced by including buried-oxide (BOX) epilayers [12], which separate the thin silicon active layer from the substrate. This novel technique has proven successful in partially or completely recovering degradation over a wide range of TIDs [16,17].

The understanding of radiation-induced defect dynamics has been expanded through recent studies, highlighting the role of interface states and oxide traps on device degradation mechanisms [18,19]. Moreover, the dose rate and energy spectrum of the gamma source critically influence the extent of degradation, as shown in various experimental investigations [20.21]. The aim of the present to investigate the effects of gamma radiation on electron transport in a Si-based n-MOSFET with a 1 μm channel length. I-V output measurements were performed before and after thermal annealing. From these I-V characteristics, we extracted threshold voltage, transconductance, and conductance parameters.

This work focuses on compact and phenomenological modeling for post-irradiation electrical characterization and circuit-level analysis. It does not aim to introduce new fundamental radiation damage mechanisms nor to propose RF-validated transistor models. The modeling framework is intentionally based on classical MOSFET analytical formulations, with radiation effects incorporated through effective electrostatic parameters. In particular, the effective acceptor concentration N_A^{eff} introduced in this study does not represent a physical modification of the silicon doping profile. It is defined as a phenomenological parameter that captures the electrostatic influence of radiation-induced oxide and interface trapped charges on the channel potential. This approach enables the integration of total ionizing dose effects into standard MOSFET models while preserving intrinsic material and technological parameters.

The paper is organized as follows: after this introduction, section II presents the DC and small-signal models, section III discusses the results, and section IV summarizes the conclusions.

II. DC and Small-Signal Models for an n-MOSFET

This section recalls only the **minimum set of standard MOSFET expressions** required to interpret the experimental results. Textbook-level derivations are omitted for brevity. **Radiation effects** are introduced through **effective electrostatic parameters** that capture the influence of oxide- and interface-trapped charges.

II.1.The Direct-Current Model

In the proposed modeling approach, radiation effects are incorporated through effective electrostatic parameters. In particular, the parameter N_A^{eff} is introduced to phenomenologically capture the electrostatic impact of oxide- and interface-trapped charges on the inversion layer. This parameter should not be interpreted as a real change in substrate doping.

Assuming a quasi-static transport regime and a constant carrier mobility along the channel, the local drain current density at a position y can be written as:

$$\mathbf{i_y = -W\mu_n Q_N(y)\frac{dV(y)}{dy}} \quad \textbf{(1)}$$

 doi:10.20944/preprints202505.1056.v2

Where $Q_N(y)$ is the local inversion charge density per unit area.The drain–source current I_{DS} is a global quantity and is obtained by integrating the local current density along the entire channel length:

$$: \mathbf{I_{DS}(y) = W\mu_n \int_0^L Q_N(y) \frac{dV(y)}{dy} dy}$$

By changing the integration variable from y to the channel potential V, the expression becomes:

$$\mathbf{I_{DS}(y) = W\mu_n \int_{V_S}^{V_D} Q_N(V) dV}$$

Although the local current density is expressed as a function of the channel position y, the drain current IDS is obtained after integration along the full channel length and is therefore independent of y.

The **inversion charge density is expressed as:**

$$\mathbf{Q_N(y) = -\frac{\varepsilon_0 \varepsilon_{ox}}{d}[V_{GS} - 2\phi_{Fi} - V(y)] + \sqrt{2e\varepsilon_0 \varepsilon_{si} N_A}[V(y) + 2\phi_{Fi}]} \quad (2)$$

Where , ϕ_{Fi} is the Fermi potential , and d is the gate oxide thickness. The effective acceptor concentration N_A^{eff} captures the effect of oxide-trapped charges.

From I_{DS}, the key DC parameters are derived :

Transconductance:

$$\mathbf{g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)_{V_{DS}}}$$

Conductance

$$\mathbf{g_d = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)_{V_{GS}}}$$

II.2. Drain Current in Linear and Saturation Regimes

II.2.1. Linear Regime

For $\mathbf{V_{DS} \ll 2\phi_{Fi}}$ and $\mathbf{\frac{V_{DS}^2}{2} \ll (V_{GS} - 2\phi_{Fi})V_{DS}}$, the drain current reduces to:

$$\mathbf{I_{DS}(V_{GS}, V_{DS}) = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_{Th})\, V_{DS}} \quad (3)$$

with $\mathbf{C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d}}$ is the oxide capacitance per unit area

and $\mathbf{V_{Th} = 2\phi_{Fi} + \frac{2}{C_{ox}}\sqrt{\varepsilon_0 \varepsilon_{si} e N_A \phi_{Fi}}}$ is the threshold voltage

In this regime, the drain current varies linearly with V_{DS} and V_{GS} (for $V_{GS} > V_{th}$). The transconductance and conductance are given by:

$$\mathbf{g_m(V_{GS}, V_{DS}) = \frac{W\mu_n C_{ox}}{L} V_{DS}} \quad (4)$$

$$\mathbf{g_d = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_{Th})}$$

As can also be noticed from **Eq. (4)**, both g_m and g_d show a linear variation as a function of the V_{DS} and V_{GS} bias potentials.

II.2.2 Saturation regime-Effect of the channel modulation

When V_{DS} exceeds the linear regime, the electron density $Q_N(y)$ decreases near the drain, and the current tends toward saturation. Saturation occurs when the channel pinch reaches the drain :

 doi:10.20944/preprints202505.1056.v2

$$\mathbf{V_{DS,SAT}(V_{GS}) = (V_{GS} - V_{Th})} \quad (5)$$

and $\mathbf{I_{DS,SAT}(V_{GS}) = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{Th})^2}$

For a V_{DS} supper than $V_{DS,SAT}$, the excess voltage $\Delta V_{DS} = V_{DS}\text{-}V_{DS,SAT}$ drops across a depleted region of width ΔL, and the channel conductance increases:.

$$\mathbf{I_{DS,SAT}(V_{GS}, V_{DS}) = \frac{W\mu C_{ox}}{2L}\left[1 + \frac{1}{L}\sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{eN_A}(V_{DS} - V_{DS,SAT})}\right](V_{GS} - V_{Th})^2}$$

$$\mathbf{g_m = \frac{W\mu_n C_{ox}}{L}\left[1 + \frac{1}{L}\sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_A}(V_{DS} - V_{DS,SAT})}\right](V_{GS} - V_{Th})} \quad (6)$$

$$\mathbf{g_d = \frac{W\mu_n C_{ox}}{4L^2}\sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_A(V_{DS} - V_{DS,SAT})}}(V_{GS} - V_{Th})^2}$$

As revealed from Eq.6, the I_{DS}–V_{DS} characteristics of an n-MOSFET exhibit an increase with V_{DS}, thus affecting the parameters g_m and g_d.

II.3.Small-Signal Model

II-3-1 Resistive Operating

In the linear regime, the n-MOSFET behaves as a resistance controlled by V_{GS}

$$\mathbf{R_{DS}(V_{GS}) = \frac{L}{w\mu_n C_{ox}(V_{GS} - V_{Th})}} \quad (7)$$

In technological applications, the n-MOSFET in linear regime can be used as an on-off switch.

II-3-2 Operation as an amplifier

In saturation, the n-MOSFET behaves as an ideal current sour

$$\mathbf{I_0 = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_{Th})^2} \quad (8)$$

Channel modulation for $V_{DS} > V_{DS,SAT}$ is described by Eq.6. The output resistance is:

$$\mathbf{R_o(V_{GS}, V_{DS}) = \frac{4L^2}{W\mu_n C_{ox}}\sqrt{\frac{eN_A(V_{DS} - V_{DS,SAT})}{2\varepsilon_0\varepsilon_{si}}}(V_{GS} - V_{Th})^2} \quad (9)$$

The **parallel combination of** I0 **and** _Ro forms the low-frequency small-signal equivalent. At higher frequencies, capacitances must be included as in **Figure 1**.

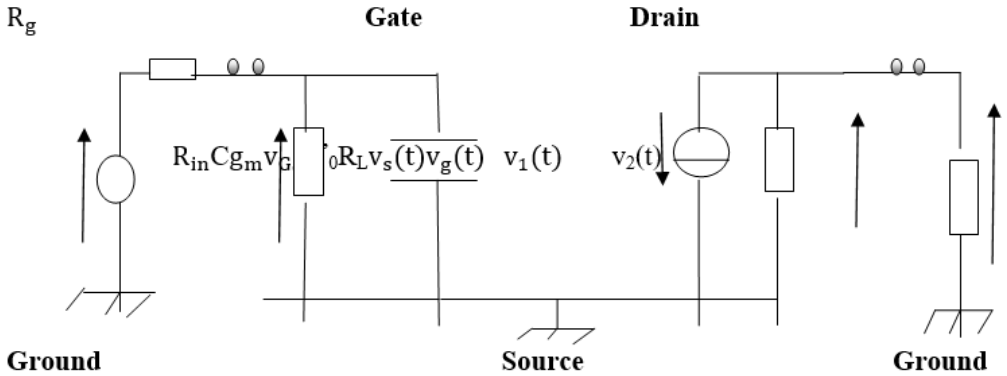

Figure 1. Equivalent circuit at high frequencies of an n-MOSFET amplifier with: $\mathbf{R_{in} = R_{G1}//R_{G2}}$. $\mathbf{C = \frac{1}{2}(2 + g_m R_0')WLC_{ox}}$ and $\mathbf{R_0' = R_0//R_D}$.

The small-signal hybrid parameters are:

$$\mathbf{h_{11} = \frac{R_{in}}{1 + jR_{in}\,c\omega}}$$

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$$h_{12} = 0$$

$$h_{21} = \frac{-g_m R_{in}}{R_g + R_{in}\, c\omega} \quad (10)$$

$$h_{22} = \frac{1}{R_0'}$$

The small-signal hybrid parameters are:

$$Z_{in} = h_{11}$$

$$A_v(\omega) = \frac{h_{21}}{h_{11}\left(h_{21} + \frac{1}{R_L}\right)} \quad (11)$$

$$A_i = \frac{h_{21}}{1 + h_{22} R_L}$$

$$Z_{out} = \frac{1}{h_{22}}$$

For $h_{22}R_L \ll 1$, simplified formulas are:

$$Z_{in} = h_{11} \quad ; \quad A_v = -\frac{h_{21} R_L}{h_{11}} \; ; \quad A_i = h_{21}; \; Z_{out} = \frac{1}{h_{22}} \quad (12)$$

The cut off frequency is:

$$\omega_c = \frac{1}{R_{in} C} \quad (13)$$

III. Static and Dynamic Characteristics of an Irradiated n-MOSFET

III-1 Static Parameters

The n-MOSFET under investigation was fabricated using a 1 µm partially depleted SOI technology. The device is implemented within a 600 µm-diameter circular membrane located near an integrated micro-heater used for *in-situ* thermal annealing. Two auxiliary PIN diodes are placed on the membrane to monitor the temperature during operation. A detailed description of the fabrication process and the annealing procedure is available in Ref. [12]. Electrical characterization was carried out by measuring the drain current as a function of the gate-to-source voltageV_{GS} in both linear and saturation regimes, with the drain-to-source voltage V_{DS} fixed at 50 mV and 3 V, respectively. Measurements were performed before and after gamma irradiation. The gate dielectric of the investigated n-MOSFET consists of a 25 nm-thick thermally grown silicon dioxide (SiO_2) layer formed by dry thermal oxidation. The quality of this gate oxide, including its defect density and interface trap concentration, plays a critical role in the device response to gamma radiation exposure. Radiation-induced degradation primarily results from charge trapping within the oxide and from interface state generation at the Si–SiO_2 interface. Consequently, the parameters employed in the proposed modeling approach, such as the effective trapped charge density and equivalent doping variations, are directly related to these gate oxide properties and the fabrication technology.

Gamma irradiation experiments were performed at room temperature using a calibrated Co-60 source with a dose rate of 1.2 krad(Si)/h. The total ionizing dose was increased up to 348 krad(Si). Electrical measurements were conducted on several nominally identical devices in order to assess reproducibility. All devices exhibited consistent trends with limited sample-to-sample dispersion, and the results presented in this work correspond to averaged values representative of the technology. After irradiation, thermal annealing was performed at 120 °C for 30 minutes in ambient atmosphere using the integrated micro-heater.

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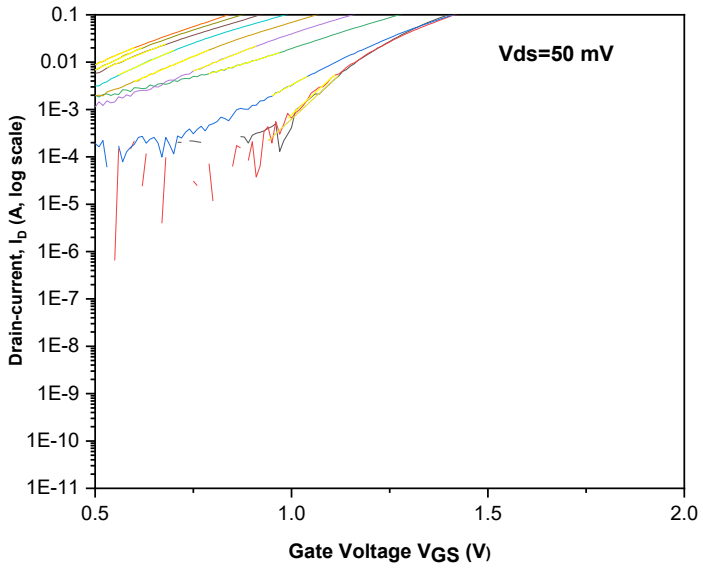

Figure 2. Threshold voltage V_{th} extraction by linear extrapolation in the subthreshold region from the I_{DS}–V_{GS} characteristics plotted on a logarithmic scale.

The threshold voltage V_{th} was extracted using the conventional subthreshold extrapolation method. The drain current I_{DS} was plotted on a logarithmic scale as a function of the gate voltage V_{GS} , and a linear fit was performed in the subthreshold region, where the current exhibits an exponential dependence on V_{GS}. The threshold voltage was determined from the intersection of the extrapolated linear fit with the reference threshold current. This extraction procedure, illustrated in Fig. 2, follows the methodology reported in *Applied Physics Letters* **48**, 133–135 (1986).

The same extracted V_{th} values are consistently used in the determination $Q_{ox\text{-}eff}$ and N_A^{eff} in order to avoid any artificial trend inversion and to ensure physical consistency.

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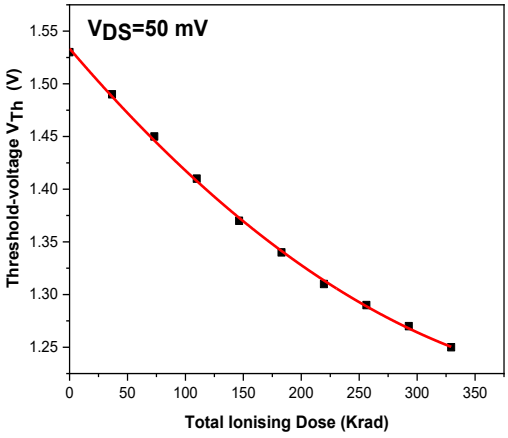

Figure 3. a . The threshold-voltage as a function of Total Ionising Dose in the linear regime

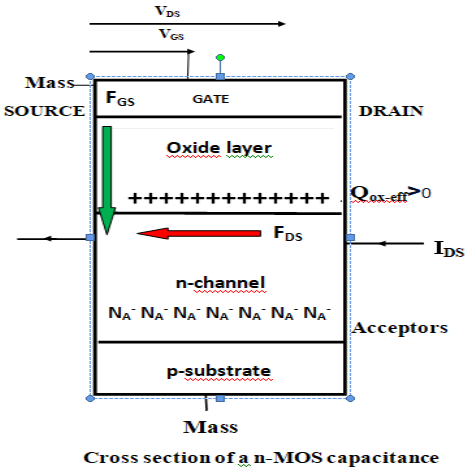

Figure3 b. Cross-Sectional schematic of n-MOSFET.

oxide layer, trapped oxide charges, and the effective acceptor concentration in the channel region of a n-MOS capacitance

It clearly appears that the threshold-potential V_{th}shows a decreasing tendency as TID increases. Using a linear fit, the threshold potential V_{th}(TID) reads in the linear-regime as:

$$\mathbf{Vth(TID)[V]} = \mathbf{1.53 - 129 \times 10^{-5} \times TID + 1.30 \times 10^{-6} \times TID^2} \quad [\mathrm{rad(SiO2)}] \qquad \textbf{(14)}$$

As reported in Ref.**[12]**, the threshold voltage shift $\Delta V_{th}$is expectedto result from a trapping of positive charges inside the oxide layer and at oxide n-channel. Let Q_{ox-eFF} be the total density of oxide-and interface-trapped holes per unit area, $\Delta V_{th}$is related to Q_{ox-eff}using the model **(12)**:

$$\mathbf{Q_{ox} = -C_{ox}\Delta V_{th}} \quad [\mathrm{C/cm}] \textbf{(15)}$$

Q_{ox-eff} represents a charge density per unit area and is therefore expressed in C/cm^2

with $\mathbf{\Delta V_{th} = V_{th}(TID) - V_{th}(TID = 0)}$

From V_{th}=V_{th}(TID), we have deduced the interfacial gate-oxide density Q_{ox-eFF} versus TID. Obtained results are shown in **Fig.4**.

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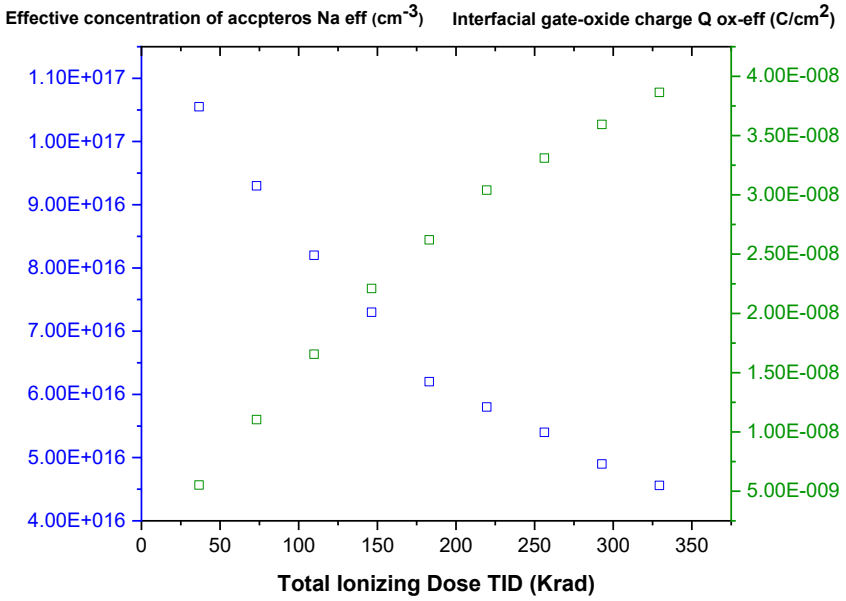

Figure 4. Effective concentration of acceptors and interface gate-oxide density as a function of Total Ionizing Dose.

As it is found, $Q_{ox\text{-}eff}$ shows an amount with increased gamma radiation dose. In terms of an analytical fitting, its expression is as follows:

$$\mathbf{Q_{ox-eFF}(TID) = -1.46\ 10^{-9} + 1.86\ 10^{-10} \times TID - 2.009\ 10^{-13} \times TID^2} \quad [\mathrm{C/cm^2}] \quad \mathbf{(16)}$$

As an illustrative picture, we report in the **Fig.3.b** the cross section of the MOS capacitance for a n-MOSFET under bias potentials V_{GS} and V_{DS}. The inset clearly shows the deposited interfacial holes under the effect of F_{GS} electric field. On the other hand, radiation hardening technologies reveal that thin gate oxide designs have a large capacitance which leads to a reduced threshold voltage shift. In terms of quantum tunneling, thin gate-oxide transistors favour the recombination of trapped holes with electrons initially located in the channel [22,23]. This can efficiently help MOSFET devices with thin gate-oxide thicknesses to become more hardened against hostile radiating environments. From the inset of Fig3, it is seen that the n-channel is located between ionized acceptors in Si-substrate and trapped holes. Physically, this implies that free electrons in the conductive channel are jointly subjected to a double electrostatic interaction. In terms of equilibrium charge balance, acceptors can be considered as partially compensated by equivalent donor centers. This leads to define an effective density of the doped acceptors as $N_A^{eff.} = \alpha N_A$ where α represents the centesimal percent of compensation. According to this relation, the threshold voltage shift can be expressed as a function of $N_A^{eff.}$ using the new model:

$$\mathbf{\Delta V_{Th}(TID) = K[-1 + \sqrt{\frac{N_A^{eFF.}}{N_A}})]} \quad \mathbf{(17)}$$

with $\mathbf{K = \frac{2}{C_{ox}}\sqrt{\varepsilon_0 \varepsilon_r e N_A \phi_{Fi}}}$

In establishing this relation, we have assumed that K does not vary significantly with TID. For the parameters N_A, n_i and C_{ox}, we have taken the corresponding values $1.17 10^{17} cm^{-3}$, $1,510^{10}$ $cm^{-3}$and 1.3810^{-3} Fm^{-2} respectively. From the measurements of V_{th} versus TID in the linear regime, we have deduced $N_A^{eff.}$ and results are summarized in **Fig.5**. As clearly shown, $N_A^{eff.}$ (cm^{-3}) exhibits a decreasing trend as the gamma radiation dose increases. Analytically, the effective doping concentration of acceptors is fitted by a quadratic law according to:

$$\mathbf{N_A^{eFF.}(TID) = 1.19 - 3.9910^{-3} \times TID + 5.41\ 10^{-6} \times TID^2} \quad \mathbf{in} \quad \mathbf{10^{-17}}\ \mathbf{cm^{-3}}$$

(18)

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So that, the choice of N_A^{eff} seems to being physically meaningful as $Q_{ox\text{-}eff}$ to analyze the electron transport in an irradiated n-MOSFET. From $I_{DS}=I_{DS}(V_{GS})$ measurements in the linear regime, we have also extracted the transconductance. The relevant results are depicted in **Fig.5**.

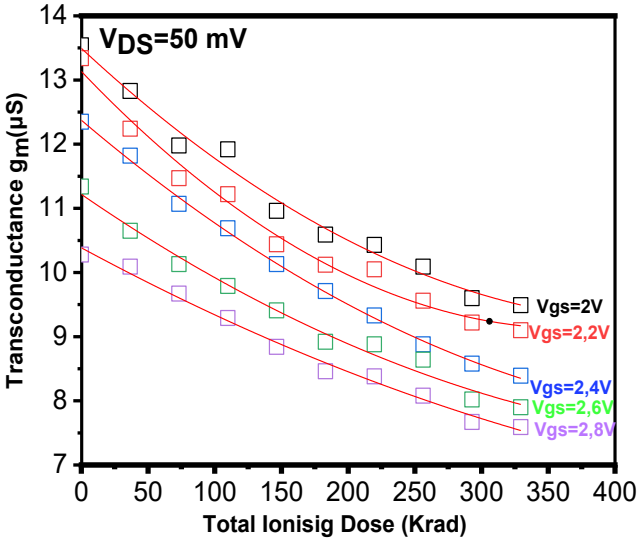

Figure 5. The transconductance as measured versus Total Ionizing Dose in the linear regime.

Two peculiar features were revealed:**(i)** For a fixe V_{GS} the transconductance decreases with increased TID, **(ii)** Under a gamma radiation dose, the transconductance decreases as the gate-to-source voltage increases. On the other hand, the transconductance can be fitted by the TID-dependent expression:

$$g_{mLR}(TID) = a_0 + a_1 \times TID + a_2 \times TID^2 \quad (19)$$

$$a_0(V_{GS}) = 21.92 - 4.085 \times V_{GS}$$

$$a_1(V_{GS}) = 0.0412 - 0.104 \times V_{GS}$$

$$a_2(V_{GS}) = 5.88\,10^{-5} + 1.79\,10^{-5} \times V_{GS}$$

In the saturation regime, however, measurements of the drain current have been carried out as follows. **Fig.6** depicts the relevant I_{DS} versus TID for different applied V_{GS} ranging from 1V to 3V.

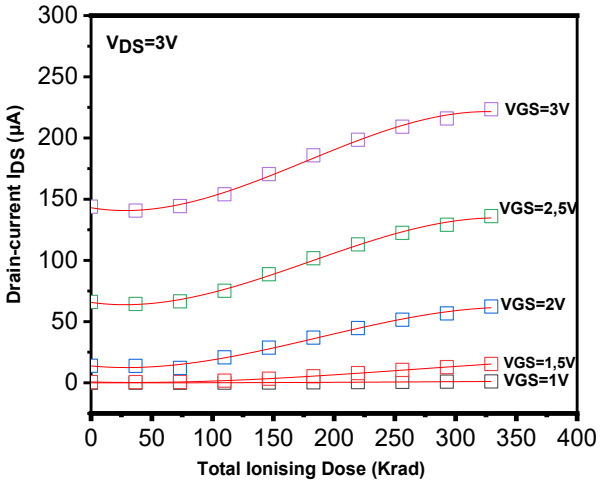

Figure 6. The drain-current versus Total ionizing Dose in the saturation regime.

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The drain is subjected to a fixed bias voltage V_{DS}=3V. The plots reveal that:**(i)** for a V_{GS} lower than 1.5V which corresponds to the threshold potential, the drain current does not show a significant change as the TID varies, **(ii)** Beyond this value, I-V at output exhibits, in contrary, an increasing tendency as TID increases. As it is also noted, the increasing of I_{DS} is more noticeable with increased V_{GS}. Similarly to I_{DS} in the linear regime, saturated I-V characteristics are found to be fitted as a function of TID by a polynomial law with V_{GS}-dependent coefficients.

$$\mathbf{I_{DS,sat}(TID) = a_0 + a_1 \times TID + a_2 \times TID^2 + a_3 \times TID^3}$$

$$\mathbf{a_0(V_{GS}) = 87.37 - 138.59 \times V_{GS} + 52.27 \times V_{GS}{}^2} \quad (20)$$

$$\mathbf{a_1(V_{GS}) = a_1(\mu A \times Krad^{-1})}$$

$$\mathbf{= 0.114 - 0.120 \times V_{GS} + 8.2510^{-3} \times V_{GS}{}^2}$$

$$\mathbf{a_2(V_{GS}) = 2.8810^{-3} + 2.2910^{-3} \times V_{GS} - 1.5410^{-4} \times V_{GS}{}^2}$$

$$\mathbf{a_3(V_{GS}) = 3.48\,10^{-6} - 3.4610^{-6} \times V_{GS} + 7.28\,10^{-8} \times V_{GS}{}^2}$$

An attempt to explain the latter results will be subsequently proposed. The first feature is predictable since the conductive channel is not yet formed below the threshold potential. While the increase in I_{DS} as observed for V_{GS} greater than V_{th} is due presumably to the flow of an excess of free electrons originating from hole-electron pairs created at the vicinity of the channel in Si-substrate, In n-MOSFET transistors exposed to high TIDs, it is worth noting that this dysfunction can lead to a derivation of the operating point. From I-V measurements performed in the saturation regime, we have deduced as well the transconductance versus TID and V_{GS}, see **Fig.7.**

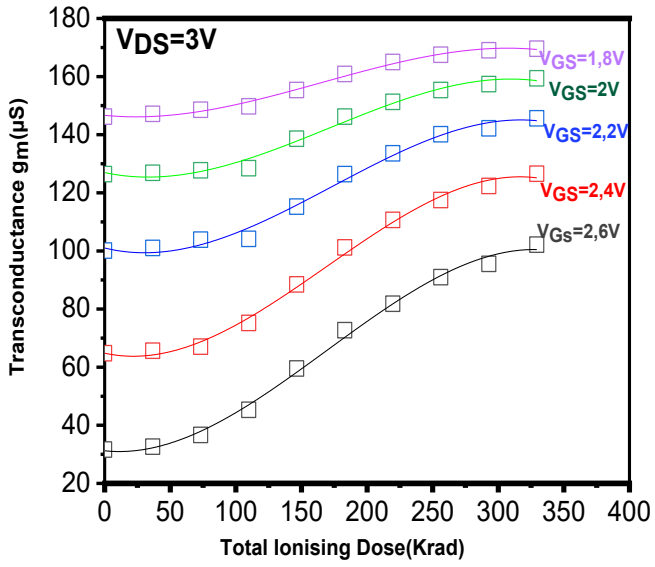

Figure 7. The transconductance as measured versus TID in the saturation regime.

As a main observation, the transconductance shows an increasing trend with increased TID. From a polynomial fitting, it was found that the transconductance can be written under the form:

$$\mathbf{g_{mSR}(TID) = a_0(V_{GS}) + a_1(V_{GS}) \times TID + a_2(V_{GS}) \times TID^2 + a_3(V_{GS}) \times TID^3}$$

$$\mathbf{a_0(V_{GS}) = -288.2 + 146.52 \times V_{GS}} \quad (21)$$

$$\mathbf{a_1(V_{GS}) = 0.149 - 0.117 \times V_{GS}}$$

$$\mathbf{a_2(V_{GS}) = 4.32\,10^{-3} - 1.13\,10^{-5} \times V_{GS}}$$

$$\mathbf{a_3(V_{GS}) = 7.98\,10^{-6} + 1.99\,10^{-6} \times V_{GS}}$$

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The latter static parameter to being deduced is the conductance. As an experimental support, the drain current I_{DS} has been measured versus V_{DS} only for TID=0 Krad and TID=348 Krad. The gate voltage is fixed at V_{GS}=3V. From the relevant I-V characteristics, we have determined the conductance versus V_{DS}. . Results are shown in **Fig.8**.

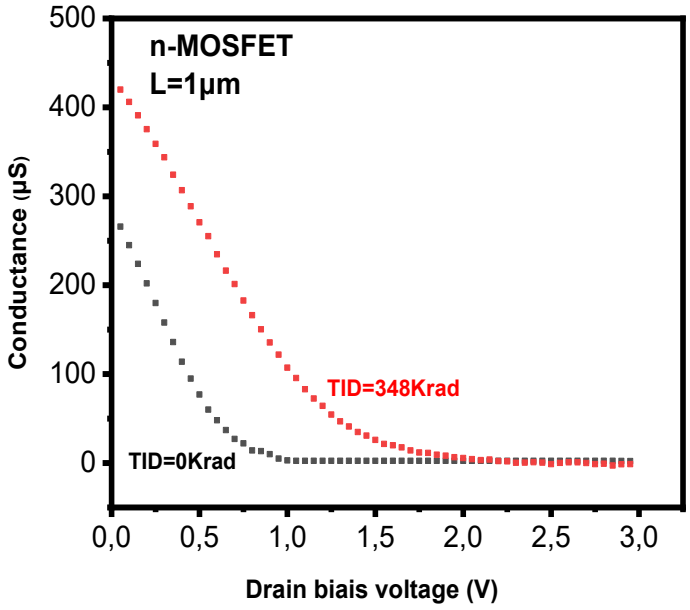

Figure 8. The VDS-dependent conductance as obtained for TID=0 Krad and TID=348 Krad.

It is thus found that the conductance shows a large amount with respect to that at TID=0 Krad for V_{GS} inferior to 2 V, which corresponds to $V_{DS,SAT}$. In the saturation regime, however, the conductance does not exhibit a significant change under the impact of gamma radiations. Note that, in the absence of experimental data for intermediate TIDs, it has not been possible to achieve a direct fitting. But the TID-dependence of this parameter can be derived from the transconductance by using the relationships

$$\mathbf{g_{DLR}(TID) = g_{mLR}(TID) = \frac{V_{GS}-V_{th}}{V_{DS}}} \quad \mathbf{for V_{DS}<V_{DS,SAT}} \quad \mathbf{(22)}$$

$$\mathbf{g_{DSR}(TID)=g_{mSR}(TID)\frac{g_{mSR}^2}{4W\mu_n C_{ox}}\sqrt{\frac{2\varepsilon_0\varepsilon_{rsc}}{eN_A V_{DS}-V_{GS}+V_{th}}}} \quad \mathbf{for} \quad V_{DS}>V_{DS,SAT}$$

The threshold-potential $\mathbf{V_{Th}}$ and the transconductance in both regimes $\mathbf{g_{mLR}}$ and $\mathbf{g_{mSR}}$ have been calculated as a function of **TID** above.

III-2Hybrid and Dynamic Parameters

A deal of interest has also been paid to the dynamic characteristics under the impact of gamma radiations. In section **II**, the hybrid parameters of the non- irradiated n MOSFET are defined by **Eq. (10)**. As it is seen, they are related to the transconductance g_m, the total capacitance C and the resistance R_O at output. Note that these static parameters are affected by the TID. From **Eq. (10),** we can deduce the modulasof the hybrid parameters as a function of TID.

$$\mathbf{h_{11}(TID) = \frac{R_{in}}{\sqrt{1+R_{in}^2 C^2(TID)\omega^2}}} \quad \mathbf{(24)}$$

$$\mathbf{h_{12} = 0}$$

$$\mathbf{h_{21}(TID) = g_m(TID) * h_{11}(TID)}$$

$$\mathbf{h_{22}(TID)=\frac{1}{R_D} * \frac{1}{R_O(TID)}}$$

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The TID-dependence of the dynamic parameters can be established as well using the set of relations:

$$\mathbf{Z_{in}(TID) = h_{11}(TID)} \quad \textbf{(25)}$$

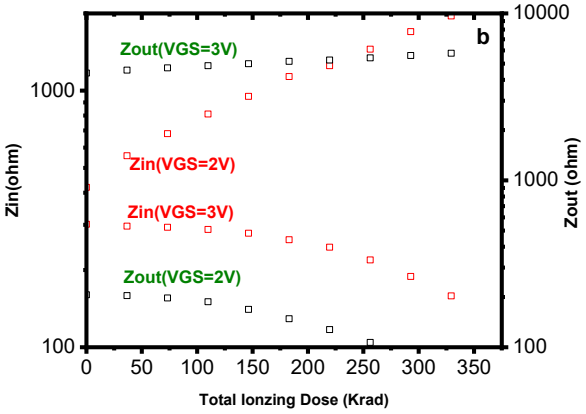
$$\mathbf{A_v(TID) = \frac{h_{21}(TID)R_L}{h_{11}(TID)}}$$

$$\mathbf{A_i(TID) = h_{21}(TID)}$$

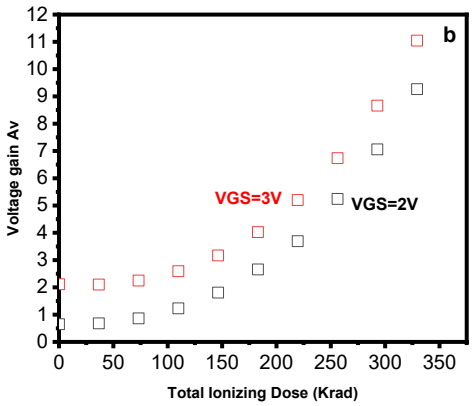
$$\mathbf{Z_{out}(TID) = \frac{1}{h_{22}(TID)}}$$

$$\mathbf{\omega_c(TID) = \frac{1}{C(TID)R'_{in}}}$$

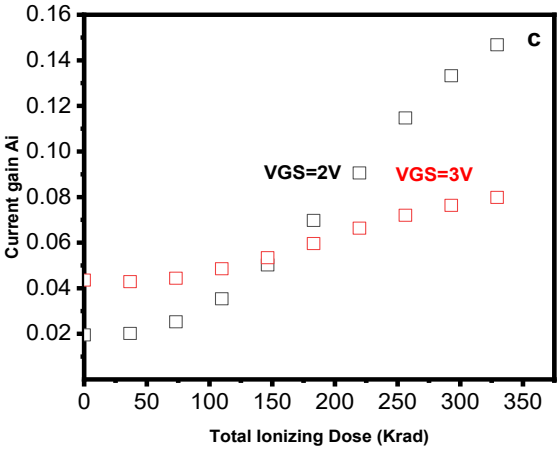
The small-signal model developed in this work is purely analytical and derived from the static I–V characteristics under quasi-static, low-frequency assumptions. Its purpose is to analyze qualitatively the evolution of AC parameters as a function of total ionizing dose. This model is not intended for RF or high-frequency operation, and all previous references to unrealistic frequencies have been removed. The gate-to-source voltage V_{GS} is treated as an adjustable variable. Using **Eqs (24)** and **(25)**, we have computed the hybrid parameters and their related dynamic characteristics for the n-MOSFET investigated versus TID and V_{GS}. **Fig.9** depicts the plots as obtained in the TID range 36.66 Krad-329.6Krad and for V_{GS} fixed at 2V and3V respectively which correspond to the amplifier operating regime. As has been found: **(i)** For V_{GS} =2V, both the hybrid and dynamic parameters show a significant change under the effect of gamma radiations particularly at high gamma-ray doses, **(ii)** They, however, seem to be less impacted under the same TIDs at V_{GS}=3V.

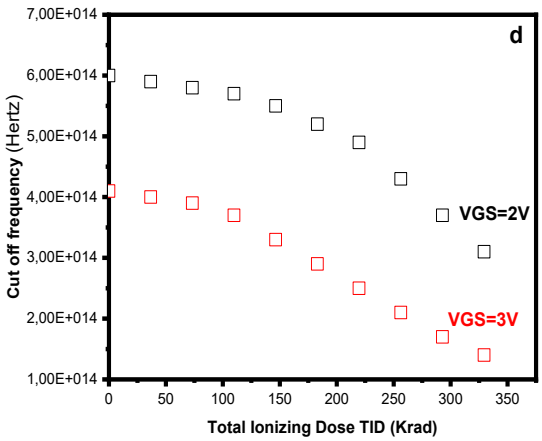


(a)



(b)





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(**c**) (**d**)

Figure 9. input/output Impedances **(a)**; Current/Voltage Gains **(b-c)** and Cutoff Frequency **(d)** versus TID for V_{GS}=2V and 3V respectively.

III-3 Novel Insights Compared to Existing Literature

To highlight the originality and relevance of the present results, we compare our observations with key findings from previous studies on radiation-induced degradation in MOSFETs. The experimental results reveal a clear degradation of the electrical characteristics of the n-channel MOSFETs as a function of the total ionizing dose, consistent with charge trapping in the gate oxide and interface state generation. These observations align well with the mechanisms described in previous studies [21,23], where oxide trapped charges induce threshold voltage shifts and increased leakage currents in MOS devices. Furthermore, the combined effect of gamma irradiation and electrical stress on the current mirrors shows a complex interplay between static and dynamic device parameters. The small-signal modeling results indicate that radiation not only affects the DC operating point but also significantly alters the transistor transconductance and output conductance, which is in agreement with the physics-based approaches developed by Zebrev et al. [22].It is important to note that the dose rate and irradiation procedure also influence the device degradation, as discussed in [21–23]. Although our experiments were conducted under controlled dose rates, the observed trends suggest that recombination and annealing effects could modify the extent of radiation-induced damage. This underscores the necessity of considering both total dose and dose rate when interpreting the reliability of MOSFETs in radiation environments. Overall, our combined DC and AC analyses is provides new insights into the electron transport degradation mechanisms in irradiated MOSFET current mirrors, extending the existing knowledge base by integrating static and dynamic perspectives.

IV. Summary and Conclusions

This work investigated the effects of gamma-ray-induced total ionizing dose on the electrical behavior of n-channel silicon MOSFETs. Experimental results demonstrated a progressive negative shift of the threshold voltage and degradation of both static and small-signal parameters with increasing radiation dose. An analytical modeling approach was proposed in which radiation-induced oxide trapped charges are treated as effective acceptor-like charge centers modifying the electrostatic conditions of the channel. This formulation preserves the classical MOSFET analytical structure while enabling a direct relationship between total ionizing dose and device parameters. The developed DC and low-frequency AC models provide a compact and physically consistent framework suitable for radiation reliability analysis and circuit-level simulations. Although the radiation-induced threshold voltage shift is a well-known phenomenon, the proposed equivalent modeling approach offers a practical analytical tool for linking experimental data to compact device models.

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