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Abstract: Lowpass filters with bandwidths larger than several GHz are required in many applications, such as anti-aliasing filters in high-speed ADCs and pulse-shaping filters in high-speed DACs. In highly integrated applications, low area occupation and power consumption are key specifications, so that inductor-less implementations are to be preferred. Furthermore, full CMOS implementations provide an advantage in terms of technology availability and cost. In this paper we present an inductor-less CMOS biquad stage based on the super source follower topology, that provides 8GHz cut-off frequency and a low power consumption of 0.42mW per pole, showing remarkable performance also in terms of bandwidth and dynamic range. The availability of two separate current sources allows independent tuning of natural frequency and quality factor. The stage can be implemented in two complementary ways, exploiting NMOS and PMOS input devices respectively, thus simplifying cascadability. The two complementary biquads have been implemented in the STMicroelectronics FDSOI 28nm CMOS process and extensively simulated, and provide stable performance under PVT variations and mismatches. The area occupation is about 387.5mm^2 per biquad, one of the lowest in the literature. The figures-of-merit are remarkable, as the filters achieve excellent power efficiency, very low area occupation, and good dynamic range.

Keywords: CMOS integrated circuits; analog filters; lowpass filters; inductor-less filters; anti-aliasing filters

1. Introduction

The recent diffusion of wideband communication systems [1–3] and high frequency measurement systems [4] drives the development of analog-to-digital (ADC) [3,5,6] and digital-to-analog (DAC) converters [7] operating with sampling frequencies of tens of GHz. Such converters usually require lowpass filters (LPFs) with bandwidth ranging from DC to GHz frequencies, to be used as anti-aliasing filters in ADCs and shaping filters in DACs. To allow processing very wide signal bandwidths, digitizer architectures based on the multiply-filter-processing (MFP) paradigm have been proposed [4,8,9], and they also require LPFs with GHz bandwidths. All these applications usually require high-order filters, to achieve a large out-of-band suppression, and they can be implemented by cascading biquad stages with suitable resonance frequencies and quality factors. Technology limitations pose constraints on the maximum quality factor that can be achieved, and this can be coped with by a suitable system design of the overall filter [10]. Noise and distortions, that determine the dynamic range of the filter, are the main design specifications; the high level of integration of the systems adds further requirements on the minimization of power consumption and area footprint.

Active filters are usually designed according to the gyrator synthesis method starting from an LC-ladder prototype [11,12], to the leapfrog LC-ladder simulation technique [13] or as a cascade of biquadratic sections (biquad) [10,14–16]. In the GHz frequency range, the traditional approach to

design filters involves the use of real inductors in such active structures or in passive networks [17,18]. The use of inductors however is in contrast with the requirements of high integration, since on-chip inductors require a huge amount of area and are prone to electromagnetic interferences. Moreover, the constraints on practically realizable inductance values could lead to high power consumption, and the low quality factor and the large parasitic effects could limit the design space to achieve the desired frequency response.

The design of multi-GHz filters that do not use physical inductors is therefore an active field of research, and several lowpass and bandpass filters have been proposed in the literature. The most common approaches are the Gm-C architecture in the few-GHz range [11–14] and the use of RLC reference structures with active inductors [16,19–22] for frequencies around 10GHz. Low-frequency approaches such as the Sallen-Key [15,23,24] and Tow-Thomas biquads [25] have also been reported, and availability of deep sub-micron CMOS and SiGe BiCMOS technologies with f_T of hundreds of GHz [26,27] has allowed applying the Sallen-Key architecture up to 17GHz [28].

While BiCMOS technologies surely allow very high frequencies using such low-frequency approaches, the trend towards the use of CMOS technologies for ever higher frequencies leads to exploring the design of inductor-less biquads operating at 10GHz in CMOS. In this context, open-loop architectures, such as Gm-C and the use of active inductors, seem preferable to closed-loop ones to achieve high frequencies. For low frequency applications, open-loop active-C biquad structures based on the flipped voltage follower (FVF) and super source follower (SSF) topologies have been proposed, and they appear to be a good candidate to achieve CMOS biquads with GHz-range frequencies and low power consumption [29–33]. A 7.5GHz biquad based on the FVF-C approach was proposed in [34] using a 28nm CMOS technology. It extends to high frequencies the approach used in [32], but the availability of a single control terminal makes it impossible to separate the control of the resonance pulsation ω_o and of the quality factor Q. Tuning of ω_o and Q would instead be useful both to compensate process variations and to allow the tunability of the filter, to adapt it to different applications.

In this paper we propose a biquad architecture based on the use of the SSF that allows achieving a 3dB bandwidth of 8GHz in a 28nm FDSOI CMOS technology with a power consumption below 1mW. The architecture can be implemented in two complementary forms (NMOS input and PMOS input), thus allowing an easy cascadability overcoming the different input and output voltage levels in the SSF topology. The SSF topology allows separate (and ideally orthogonal) tuning of ω_o and Q of the biquad, thus improving with respect to the filter in [34].

This paper is organized as follows. Section 2 introduces the proposed topology, discussing its nonideal effects, that cannot be neglected at high frequency. Section 3 summarizes the simulation results and provides a comparison with the literature, and Section 4 concludes.

2. Analysis of the Topology

This Section analyzes the proposed biquad topology in terms of frequency response, impact of parasitic effects, and large-signal performance.

2.1. Analysis of the SSF-Based Biquad

Inductor-less biquads usually are based either on closed-loop architectures (Sallen-Key, Tow-Thomas) or on open-loop structures such as Gm-C, active-C or RLC equivalents exploiting active inductors. With the goal of maximizing the resonance frequency for a given power level, open-loop architectures have a net advantage, and in particular the simpler topology creates fewer extra poles and zeros that affect the high frequency behavior of the biquad, limiting the maximum cut-off frequency.

As a consequence, the source-follower-C (SF-C) filter class is a good candidate to design biquads with very high cut-off frequency and good overall performance, since they use a limited number of devices, and hence of internal nodes that add extra poles that are desired to be out of band. In particular, biquads based on the flipped voltage follower (FVF) and on the super source follower

(SSF) topologies have been proposed in the literature, aimed at low frequency biomedical applications [29–33].

Figure 1 shows the topology of FVF and SSF stages: by an analysis of the schematics, it is clear that their small-signal behavior is identical, since the SSF can be interpreted as the folded version of the FVF. They both form a unitary-gain loop with the same input and output impedances and voltage and current gains. However, the folded nature of the SSF yields more flexibility in accommodating voltage swings at the internal high impedance node: thus we select it to design a multi-GHz lowpass biquad. The structure can be considered as a current-mode circuit [35–38]: M_1 is an inverting second-generation current conveyor (CCII) [36], whereas M_2 is a transconductance. The combination of the two yields a CFOA (current-feedback operational amplifier) [37] without the output low-impedance stage.
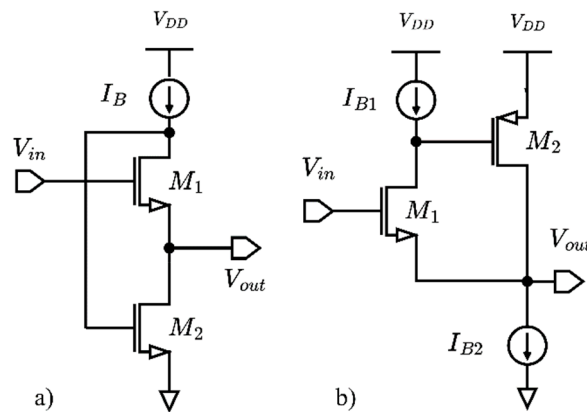
Figure 1. FVF (a) and SSF (b) stages.

It has to be noted that source follower structures provide a DC level shift between input and output equal to a gate-source voltage. While this is not an issue for a single biquad, it can impair the cascading of stages to achieve higher-order filters with a limited supply voltage range. However, the complementary nature of CMOS technology allows overcoming this issue, by alternating stages based on NMOS and PMOS input devices (N-type and P-type biquads in the following), as shown in Figure 2.
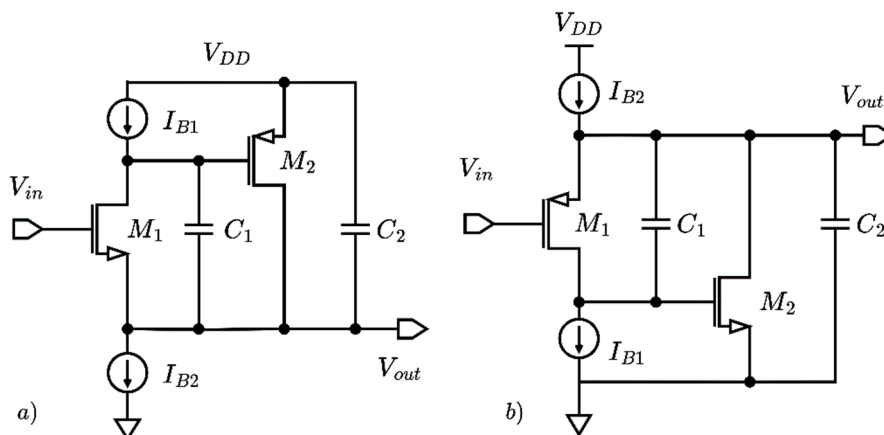
Figure 2. SSF-C biquads with NMOS (a) and PMOS (b) input devices.

2.2. Ideal Frequency Response

The proposed biquad, shown in Figure 2 in the N-type and P-type configurations, is composed of a super source follower with two additional capacitors, one between the output node and the

internal high-impedance node, and the other between the output node and ground. In practice, transistor M_1 acts as a current conveyor with the gate as Y terminal, the source as X terminal and the drain as Z terminal; the high-impedance load at the Z terminal and the common-source amplifier (M_2) close the feedback loop. The current generator I_{B1} sets the bias current of M_1, whereas current generator I_{B2} draws the sum of the currents of M_1 and M_2: having two current sources allows easier tuning of biquad parameters than in the FVF case [34], as we will show in the following.

Figure 3 shows the small-signal equivalent circuit of the proposed topology: transistors M_1 and M_2 are modeled by their transconductance $g_{m1,2}$, their output conductance $G_{1,2} = g_{m1,2}/A_{1,2}$, where $A_{1,2} = g_{m1,2}/g_{ds1,2}$ is the intrinsic gain of the device, and their gate-source capacitance is $C_{gs1,2}$. Current sources are modeled by their output conductances $G_{B1,2}$. Gate-drain capacitances are neglected.
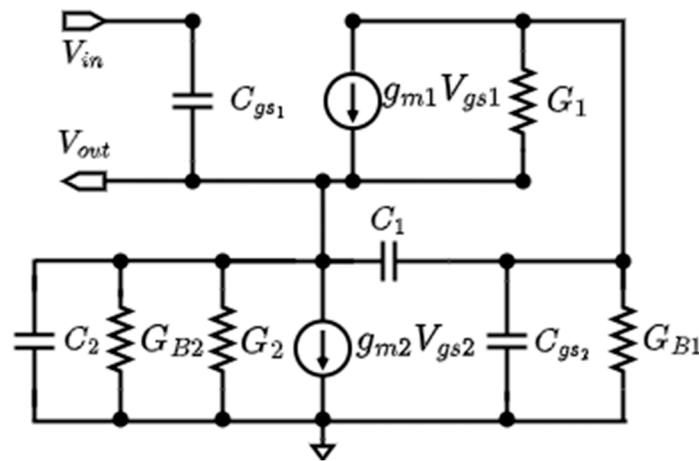

Figure 3. Small-signal circuit of the proposed biquad.

Neglecting the capacitances and the output conductances of the transistors, the ideal transfer function can be easily calculated as

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}}{g_{m1}g_{m2} + sC_1g_{m2} + s^2C_1C_2} = \frac{1}{1 + \dfrac{s}{\omega_0 Q} + \dfrac{s^2}{\omega_0^2}} \qquad (1)$$

where

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} = \omega_{0id} \qquad (2)$$

$$Q = \sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}} = Q_{id} \qquad (3)$$

Because g_{m1} and g_{m2} are functions of the biasing currents of the corresponding transistors, it is possible to tune the frequency response to compensate the variations of both Q and ω_0. Scaling the two currents by the same amount leaves the g_m ratio roughly unchanged and ideally affects only ω_0. On the other hand, changing the two currents in opposite directions has a larger impact on Q and ideally no impact on ω_0. The control could therefore independently set the ratio and product of the g_m's to set the two parameters separately, because they will impact the two parameters differently. Because the filter is in unity feedback configuration, the low-frequency gain is always close to 0dB at DC and cannot be tuned.

In the following subsections, we will analyze the impact of parasitic elements of the transistors on the transfer function (1).

2.3. Effect of Parasitic Capacitances

The two main parasitic capacitances in Figure 3 are the C_{gs} of the two transistors M_1 and M_2. We assume for simplicity that $C_{gs} = g_m/\omega_T$ for both transistors, with $\omega_T \gg g_{mi}/C_i$, $i = 1,2$. The frequency response of the biquad, including these capacitances, can be calculated from the circuit in Figure 3, neglecting the conductances G_i, as:

$$\frac{V_{out}}{V_{in}} \approx \frac{1 + \dfrac{s}{\omega_T} + \dfrac{C_1}{g_{m2}\omega_T}\left(1 + \dfrac{g_{m2}}{C_1\omega_T}\right)s^2}{1 + \dfrac{C_1}{g_{m1}}\left(1 + \dfrac{g_{m1}}{C_1\omega_T}\right)s + \dfrac{C_1C_2}{g_{m1}g_{m2}}\left(1 + \dfrac{C_1g_{m1} + C_1g_{m2} + C_2g_{m2}}{C_1C_2\omega_T}\right)s^2}. \tag{4}$$

The impact on the poles is limited if $\omega_T \gg \omega_0, \omega_0 Q$, but two negative zeros appear. Unfortunately, the second-order term at the numerator is large with respect to the first-order term, so that the zeros will be complex conjugated with large quality factor:

$$\omega_{0Z} \approx \sqrt{\frac{g_{m2}\omega_T}{C_1}} \tag{5}$$

$$Q_Z \approx \sqrt{\frac{\omega_T C_1}{g_{m2}}} \tag{6}$$

Because the number of zeros is equal to the number of poles, the gain at infinity is finite:

$$F(j\infty) \approx \frac{g_{m1}}{\omega_T C_2} \tag{7}$$

However, the asymptotic gain is low if $\omega_T \gg g_{m1}/C_2$. It has to be noted that the zeros set a limit to the maximum bandwidth that can be achieved for a given level of out-of-band attenuation.

For what concerns the poles of the biquad, the expressions for the resonance frequency and the quality factor are reported below:

$$\omega_0 \approx \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \frac{1}{\sqrt{1 + \dfrac{C_1g_{m1} + C_1g_{m2} + C_2g_{m2}}{C_1C_2\omega_T}}} = \frac{\omega_{0id}}{\sqrt{1 + \dfrac{C_1g_{m1} + C_1g_{m2} + C_2g_{m2}}{C_1C_2\omega_T}}} \tag{8}$$

$$Q \approx \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}} \frac{\sqrt{1 + \dfrac{C_1g_{m1} + C_1g_{m2} + C_2g_{m2}}{C_1C_2\omega_T}}}{1 + \dfrac{g_{m1}}{C_1\omega_T}} \approx$$
$$\approx Q_{id}\left(1 + \frac{C_1g_{m1} + C_1g_{m2} + C_2g_{m2} - 2C_2g_{m1}}{2C_1C_2\omega_T}\right) \tag{9}$$

Equations show that the resonance frequency is slightly reduced by the additional capacitances, whereas the impact on the quality factor can be positive or negative.

2.4. Effect of Parasitic Resistances

There are two nodes in the circuit where the parasitic resistances of the current generators and of M_1 and M_2 are present. M_1 adds a parasitic resistance in parallel with C_1, the other devices add parasitic resistances from one of the two nodes (output and high-impedance internal node) toward ground.

To make this analysis more meaningful, we assume that all output conductances are proportional to the respective transconductances as

$$G_i = g_{mi}/A_v \tag{10}$$

where $A_v = A_i$ (the intrinsic gain of the transistor) in case of simple transistors (i.e. $G_i = g_{dsi}$) and $A_v \approx A_i^2$ in case of cascodes. Moreover, we assume $G_{B1} = G_1$ and $G_{B2} = G_1 + G_2$, i.e. the output

conductances of the current sources are proportional to their currents, and devices implementing them are sized with the same overdrive voltage as M_1 and M_2.

With these assumptions, the frequency response is:

$$\frac{V_{out}}{V_{in}} \approx \frac{1 + \frac{g_{m1}}{g_{m2}A_v}}{\left[1 + \frac{1}{A_v}\left(\frac{g_{m1}}{g_{m2}} + \frac{g_{m2}}{g_{m1}}\right)\right] + \left[\frac{C_1}{g_{m1}}\left(1 + \frac{2}{A_v}\left(1 + \frac{g_{m1}}{g_{m2}}\right)\right) + \frac{2C_2}{A_v g_{m2}}\right]s + \frac{C_1 C_2}{g_{m1}g_{m2}}s^2} \tag{11}$$

Eq. (11) shows that parasitic resistances reduce the DC gain, slightly increase the resonance frequency, and reduce the quality factor. No additional poles or zeros are created.

The most interesting effect of the parasitic resistances is that they result in a maximum quality factor that can be achieved by using this biquad topology. Defining the capacitive ratio $R_C \equiv C_2/C_1$ and the resistive ratio $R_R \equiv g_{m1}/g_{m2}$, the quality factor can be calculated as:

$$Q = \frac{\sqrt{R_C R_R\left[1 + \frac{1}{A_v}\left(R_R + \frac{1}{R_R}\right)\right]}}{1 + 2\frac{2(R_R + 1)}{A_v} + R_C\frac{2R_R}{A_v}} \leq \frac{\sqrt{A_v}}{2\sqrt{2}} \tag{12}$$

Eq. (12) shows that the quality factor cannot go to infinity, and to achieve $Q = 2.5$, it is necessary to have $A_v > 50$. This cannot be obtained in advanced CMOS processes using simple minimum length devices, so that the devices must be cascoded to obtain a higher gain A_v, hence a higher resistance.

2.5. Impact of Cascoding

The output resistances can be removed (improved by a factor $A_i = g_{mi}/g_{dsi}$) by cascoding, and each transistor in the actual circuit (including the current generators) is in fact cascoded. However, cascoding adds a pole to the transconductances, at the frequency of the cascoding device, i.e., $\omega_T \approx g_m/C_{gs}$, and these poles modify the frequency response of the filter, adding two poles at high frequency. The resulting transfer function is:

$$\frac{V_{out}}{V_{in}} \approx \frac{1}{1 + \frac{C_1}{g_{m1}}s + \left(\frac{C_1 C_2}{g_{m1}g_{m2}} + \frac{C_1}{g_{m1}\omega_T}\right)s^2 + \frac{2C_1 C_2}{g_{m1}g_{m2}\omega_T}s^2 + \frac{C_1 C_2}{g_{m1}g_{m2}\omega_T^2}s^4} \tag{13}$$

With a fourth-order polynomial it is hard to find an interesting expression for the poles; assuming the first two poles to be dominant with respect to the parasitic poles, however, provides a simple separation:

$$\frac{V_{out}}{V_{in}} \approx \frac{1}{\left[1 + \left(\frac{C_1}{g_{m1}} - \frac{2}{\omega_T}\right)s + \left(\frac{C_1 C_2}{g_{m1}g_{m2}} - \frac{C_1}{g_{m1}\omega_T}\right)s^2\right]\left(1 + \frac{s}{\omega_T}\right)^2} \tag{14}$$

The first two terms will be affected by the terms in ω_T, but the effect is limited as long as $\omega_T \gg \omega_0, \omega_0 Q$. However, both ω_0 and Q tend to increase with the additional poles, which will be at much higher frequency. All these effects are usually negligible, but can become significant when this topology is exploited to design very high frequency biquads.

2.6. Noise Analysis

Noise of the biquad is analyzed in the ideal case, neglecting the effect of parasitic resistors and capacitors. The schematic in Figure 4 shows the corresponding small-signal circuit including noise sources: I_{n1} and I_{n2} are the noise sources related to devices M_1 and M_2, and in the schematic are in parallel to the controlled sources $g_{mi}V_{gsi}$ (i=1,2), whereas I_{nB1} and I_{nB2} are the noise sources associated to the current generators. It has to be noted that noise sources I_{n2} and I_{nB2} result in parallel between the output node and ground. Each noise source has a power spectral density

$$S_{ni} = \frac{K_F g_{mi}^2}{f C_{ox} WL} + 4K_B T\gamma g_{mi} \tag{15}$$

where K_B is the Boltzmann constant, T is the absolute temperature, C_{ox} the oxide capacitance per unit area, W and L are the channel width and length, and γ and K_F are process-dependent coefficients. The flicker component is neglected in the following due to the wide filter bandwidth.
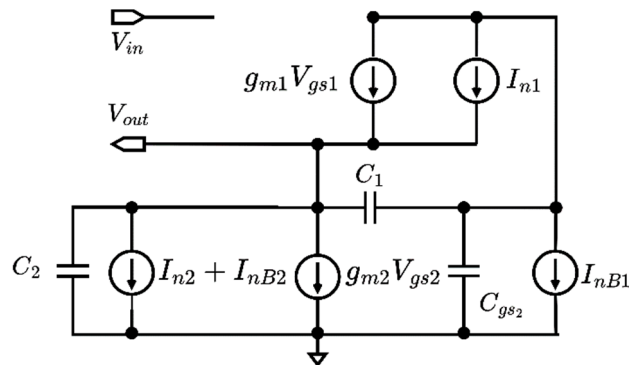
Figure 4. Small-signal equivalent circuit for noise analysis.

Analysis of the schematic in Figure 4 provides the output voltage due to the noise sources in the form

$$V_{out} = \frac{\dfrac{I_{n1}}{g_{m1}} - sC_1 \dfrac{I_{n2} + I_{nB2}}{g_{m1}g_{m2}} + \left(1 - s\dfrac{C_1}{g_{m2}}\right)\dfrac{I_{nB1}}{g_{m1}}}{1 + s\dfrac{C_1}{g_{m1}} + s^2\dfrac{C_1 C_2}{g_{m1}g_{m2}}} \tag{16}$$

that shows that the different noise sources go through different frequency behavior. Considering the corresponding power spectral density, and substituting equations (2) and (3), the output noise power spectral density can be expressed highlighting lowpass and bandpass components:

$$S_{no} = \frac{1}{g_{m1}^2} \frac{S_{n1} + \left(\dfrac{\omega C_1}{\omega_0 C_2}Q\right)^2 (S_{n2} + S_{nB2}) + \left[1 + \left(\dfrac{\omega C_1}{\omega_0 C_2}Q\right)^2\right]S_{nB1}}{\left(1 - \dfrac{\omega^2}{\omega_0^2}\right)^2 + \dfrac{\omega^2}{\omega_0^2 Q^2}} \tag{17}$$

and integrating over frequency the total equivalent output noise power is obtained:

$$P_{no} = \frac{\pi Q \omega_0}{2 g_{m1}^2}\left[S_{n1} + \left(\frac{C_1}{C_2}Q\right)^2 (S_{n2} + S_{nB2}) + \left[1 + \left(\frac{C_1}{C_2}Q\right)^2\right]S_{nB1}\right] \tag{18}$$

2.7. Cascadability of Biquads

The cascading of an N-type and of a P-type biquad, shown in Figure 5, allows input and output biasing voltages of the overall 4-th order filter to be the same, but constraints the output voltage at the intermediate node. For simplicity, we assume $V_{GS} = V_{SG}$ for all NMOS and PMOS devices, and the same threshold voltage V_T (and hence overdrive voltage V_{ov}). We assume that the lowpass outputs have unity gain and the bandpass outputs[1] negligible gains: these hypotheses are realistic at low frequencies. According to the previous discussion, all devices have been cascoded.

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[1] It can be shown that the transfer function from V_{in} to the drain of M_1 has a bandpass behavior in the ideal case.
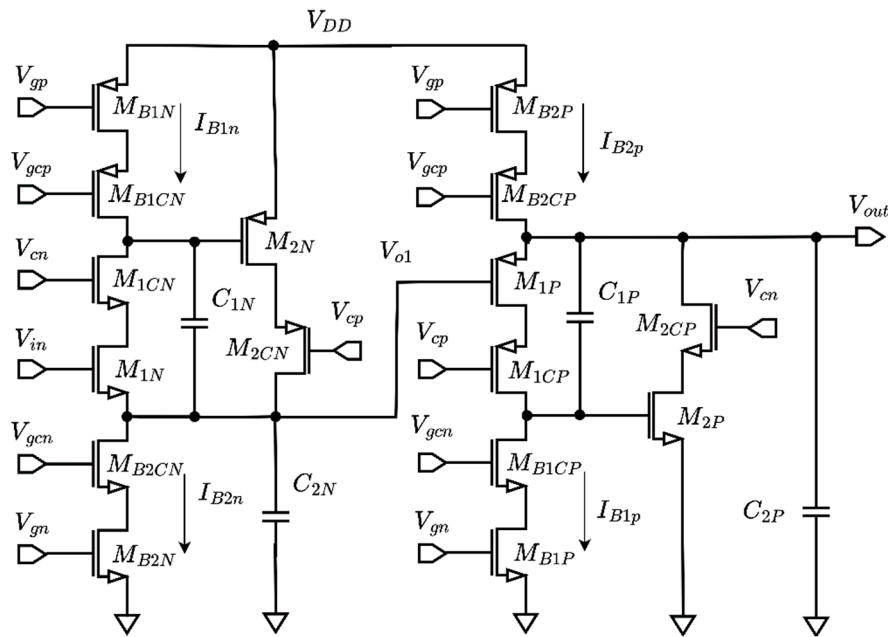
Figure 5. 4-th order filter with cascaded N-type and P-type biquads.

The condition to have M_{B2N}, M_{1N}, M_{1P} and M_{B2P} (and the respective cascoding devices) all operating in the saturation region is:

$$V_{GS} + 2V_{ov} < V_{in} < V_{DD} - 2V_{ov} \tag{19}$$

whereas M_{2N} and M_{2P}'s constraints are not binding because other devices enter the triode regions before. We have assumed that the cascoded devices are biased at the minimum required V_{DS} voltage. From the above equations, the minimum supply voltage to have proper biasing is:

$$V_{DD} > V_{GS} + 4V_{ov} \tag{20}$$

3. Simulation Results

The N-type and P-type biquads in Figure 5 have been designed and simulated in the 28nm CMOS FDSOI (fully-depleted Silicon-on-Insulator) technology by STMicroelectronics [27]. Both biquads have been designed to achieve a resonance frequency of 5.8GHz and a quality factor Q=2. Table 1 reports the sizing of all devices, that have been designed with minimum gate length to maximize the transition frequency. Supply voltage is 1.2V. Forward body bias has been exploited to reduce the threshold voltage and further increase device speed. The use of an FDSOI process allows setting the voltage on the body terminal without the risk of the body-channel junction turning on, thus voltages outside the supply rails have been exploited to bias the body terminals of M_1 and M_2 (including cascode devices). Chosen values are 1V and -0.6V for NMOS and PMOS devices. Reported values of the capacitors refer to the explicit capacitors that have been implemented; device and layout parasitics add to these values, and the effect is particularly significant for C_2.

Table 1. Device sizing.

	N-type biquad	P-type biquad	Units
W_{M1}, W_{M1C}	4.4	11.2	μm
W_{M2}, W_{M2C}	7.6	3.2	μm
W_{MB1}, W_{MB1C}	5.5	5	μm
W_{MB2}, W_{MB2C}	10	12	μm
I_{B1}	300	350	μA
I_{B2}	700	700	μA

C_1	50	40	fF
C_2	90	80	fF

Figure 6 shows the layout of the N-type and P-type biquads, whose size is 15.5x25μm². The filters thus result very compact, minimizing parasitic effects of layout and routing lines.


a)
b)
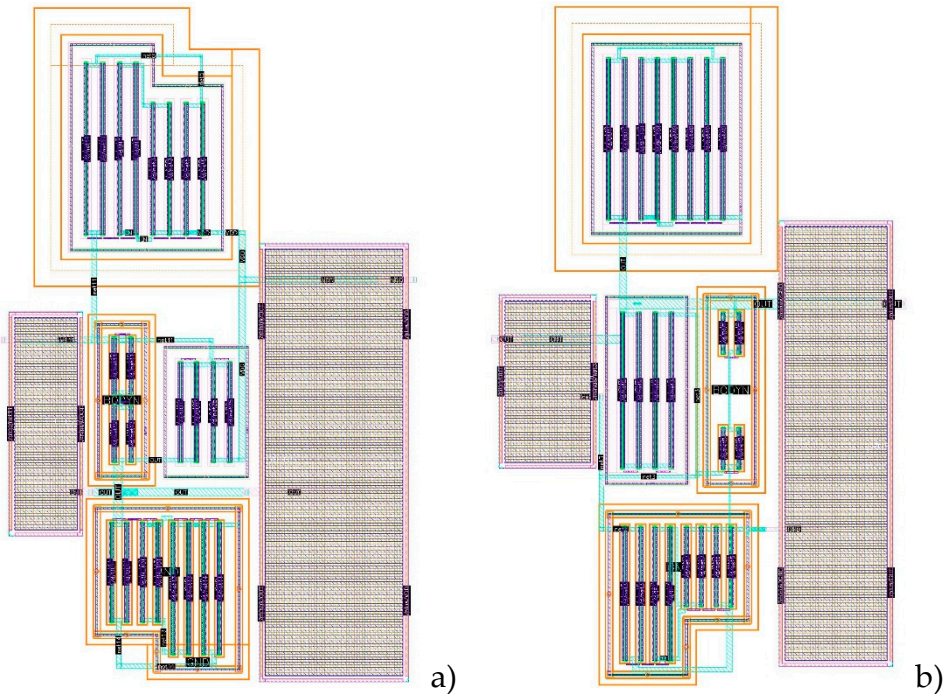
Figure 6. Layout of (a) N-type, and (b) P-type biquads.

3.1. Performance in Nominal Conditions

Post-layout simulations in nominal conditions (typical process corner, 27°C, 1.2V supply voltage) have been performed to assess the performance of the designed biquads. Power dissipation is 820μW and 670μW for the N-type and P-type biquad respectively.

Figure 7 shows the frequency response of the N-type, P-type and cascaded (N + P) filters: resonance frequency and quality factor are 5.4GHz (5.5GHz) and 6.6dB (7.2dB) for the N-type (P-type) biquad, and the cut-off frequency is about 8GHz for both biquads. Out-of-band gain saturates to -30dB because of the complex zeros in (4); obviously out-of-band gain drops to -60dB for the cascade of the two biquads, making the suppression of out-of-band components not an issue in practical cases.

Simulations have been performed to verify the tunability of filter parameters through the bias currents I_{B1} and I_{B2}. As discussed in Section 2, the resonance frequency and the quality factor can be adjusted separately, by a suitable control of the bias currents. Figure 8 shows the case of tuning of the resonance frequency with an (ideally) constant quality factor, achieved by keeping the ratio of g_{m1} and g_{m2} constant, so that I_{B2} scales by the same factor K as I_{B1}. Second-order effects result in some variation of the quality factor, and the resonance frequency shows about a 50% tuning range. More specifically, the resonance frequency goes from 3.5GHz to 5.9GHz (3.3GHz to 5.7GHz) for K varying between 0.45 and 1.3 (0.3 and 1.1) for the N-type (P-type) biquad, with about 1dB variation of the quality factor.
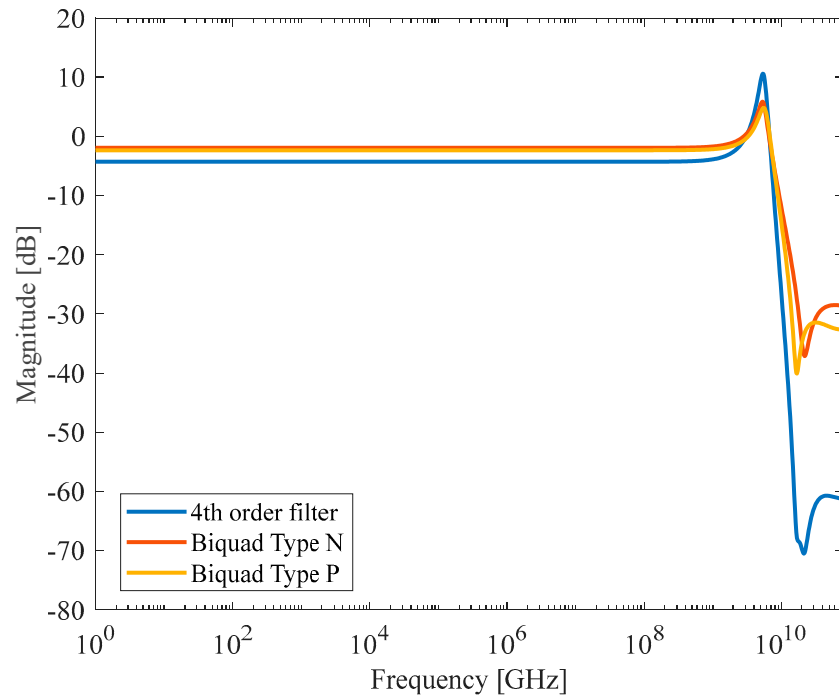
Figure 7. Frequency response of the N-type, P-type and cascaded (N + P) filters.
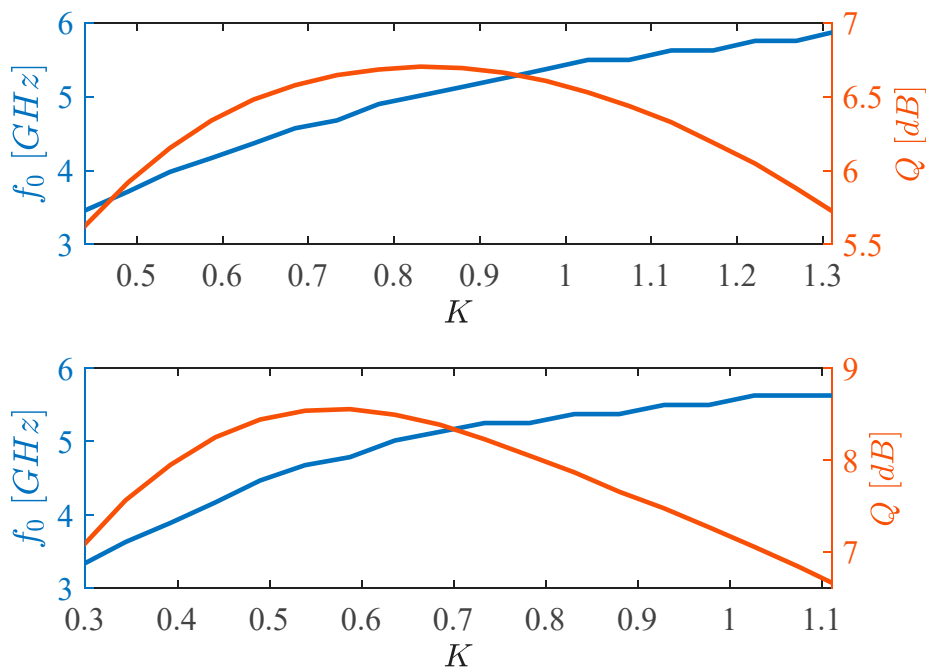
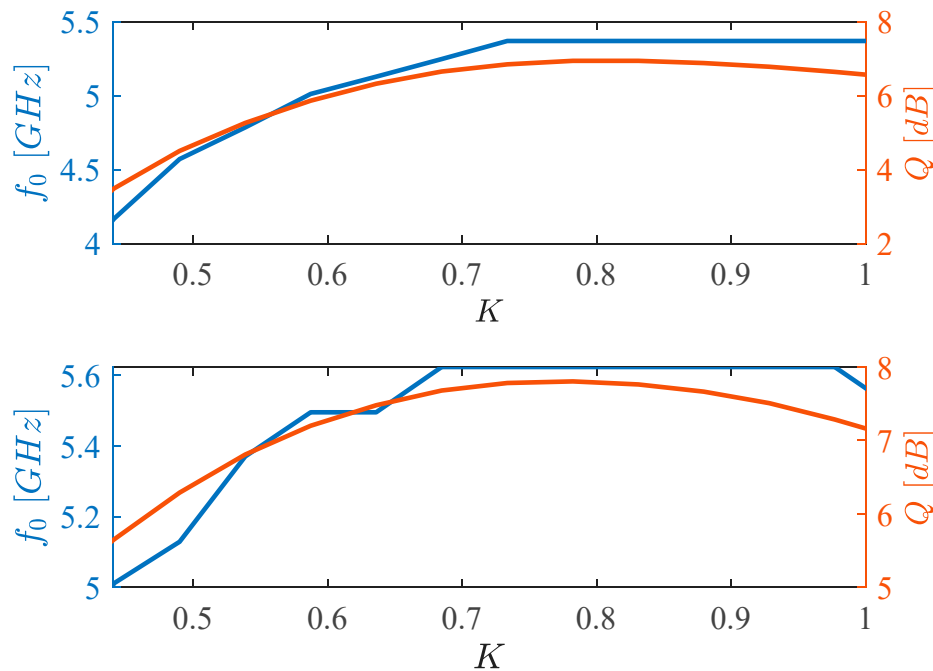**Figure 8.** Tuning of resonance frequency for (a) N-type and (b) P-type biquads.

Figure 9 shows the case of changing the quality factor while keeping the resonance frequency constant. In this case, the ratio of g_{m1} and g_{m2} needs to be varied, while keeping their product constant, hence the currents of M_1 and M_2 have to be varied in opposite directions. Currents are defined as

$$I_1 = I_{B1} = KI_0 \tag{21}$$

$$I_2 = I_0/K \tag{22}$$

hence

$$I_{B2} = I_0 \left(K + \frac{1}{K} \right) \tag{23}$$

Figure 9. Tuning of quality factor for (a) N-type and (b) P-type biquads.

Simulations show a good range of tunability for the quality factor (about 3dB) with a limited variation of the resonance frequency. The quality factor changes from 3.5dB to 7dB for N-type biquad with K ranging from 0.4 to 1, and from about 5.6dB to 7.8dB for P-type biquad; the corresponding variation in resonance frequency is about 1GHz for the N-type biquad (4.2GHz to 5.2GHz) and 600MHz (5GHz to 5.6GHz) for the P-type one. Controls on resonance frequency and quality factor result non-orthogonal due to the effect of secondary poles and zeros, that are not negligible at such high frequencies, but anyway the resulting control ranges allow to counteract the effect of process variations, as will be shown in the next subsection.

Figure 10 shows the output noise spectrum for both biquads, resulting in a noise corner frequency of about 2MHz and an in-band integrated output noise of 1.44mVrms for the N-type biquad and 1.5mVrms for the P-type biquad.
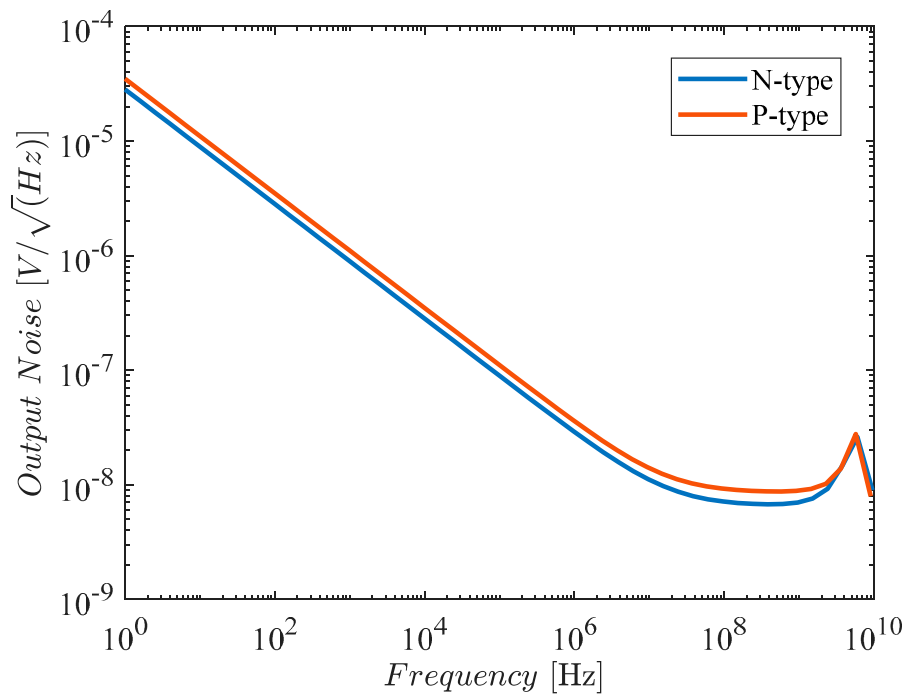
Figure 10. Output noise spectra for N-type and P-type biquads.

Figure 11 reports the DC transcharacteristic, that shows the input-output level shift and a linear range of about 400mVpp. This is further confirmed by Figure 12 which shows the output spectrum for a two-tone test with 200mVpp sinusoidal signals at 900MHz and 1GHz. Third-order intermodulation distortion (IMD3) is -49.7dB and -52.9dB for the N-type and P-type biquads respectively. The spectrum also shows a second-harmonic distortion (HD2) of about -33.13dB (-33.44dB), due to the single-ended nature of the biquad, and a third-harmonic distortion (HD3) of -44dB (-46.8dB) for the N-type (P-type) biquad.
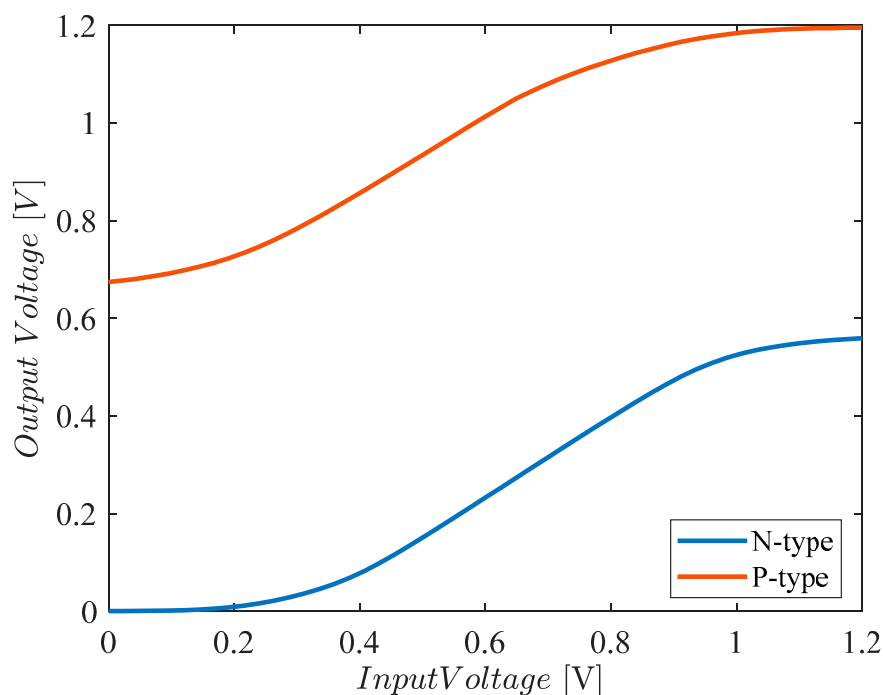
Figure 11. DC transcharacteristic for N-type and P-type biquads.
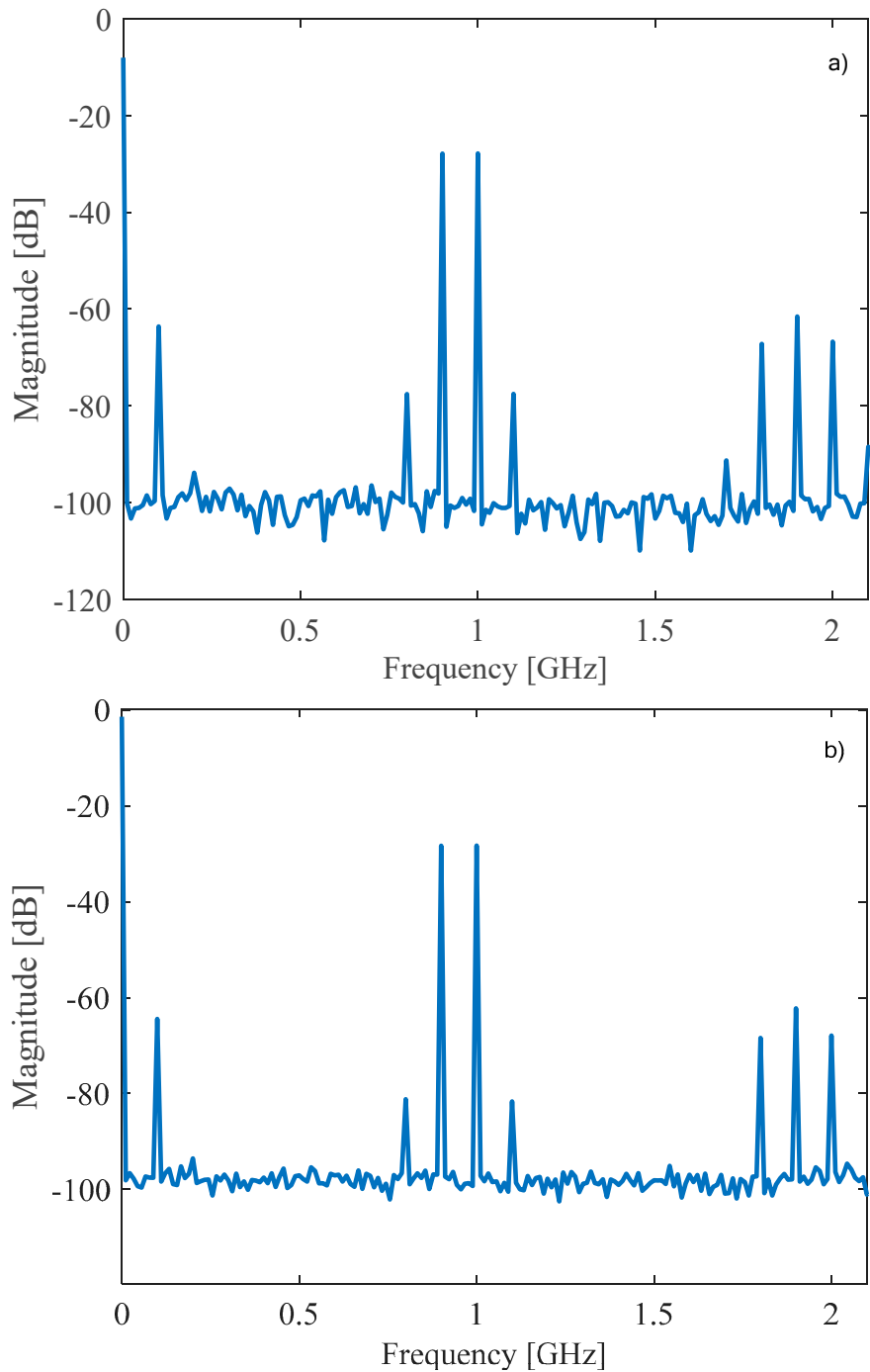
Figure 12. Two-tone spectra of the (a) N-type and (b) P-type biquads for 900MHz and 1GHz 200mVpp inputs.

3.2. Robustness to PVT Variations and Mismatches

To assess the robustness of the biquads to supply voltage and temperature variations, simulations have been carried out considering ±10% supply voltage variations and 0°C and 80°C temperatures. Tables 2 and 3 synthesize the results for N-type and P-type biquads, together with the nominal performance.

Table 2. Performance of N-type biquad under supply and temperature variations.

Performance	Nominal	$V_{DD} + 10\%$	$V_{DD} - 10\%$	0°C	80°C
f_0 [GHz]	5.4	5.2	5.4	5.6	5
f_{3dB} [GHz]	8.1	7.9	8.1	8.3	7.5
Q [dB]	6.6	5.6	6.5	6.7	6

A_0 [dB]	-1.9	-2	-1.9	-1.9	-2
P_{diss} [mW]	0.82	0.82	0.82	0.81	0.83

Table 3. Performance of P-type biquad under supply and temperature variations.

Performance	Nominal	V_{DD} + 10%	V_{DD} - 10%	0°C	80°C
f_0 [GHz]	5.5	4.9	5.9	5.6	5.3
f_{3dB} [GHz]	7.9	7.1	8.3	8	7.5
Q [dB]	7.2	5.6	8.1	7.3	6.6
A_0 [dB]	-2.3	-2.3	-2.3	-2.3	-2.4
P_{diss} [mW]	0.67	0.57	0.74	0.66	0.70

It is interesting to note that variation of the resonance frequency is less than the range that can be covered by a variation of bias currents, shown in Figure 8, thus allowing to compensate the effect.

Joint process and mismatch Monte Carlo simulations have been carried out to verify the effect of process variations (both of MOS transistors and capacitors) and mismatches. Table 4 reports the results after 200 Monte Carlo iterations, showing a good robustness of both resonance frequency f_0 and quality factor Q, with standard-deviation-to-mean ratios below 3.5% (for f_0) and 7.5% (for Q).

Table 4. Monte Carlo process and mismatch simulations.

Performance	N-type biquad		P-type biquad	
	Mean	Std	Mean	Std
f_0 [GHz]	5.6	0.186	5.5	0.177
f_{3dB} [GHz]	8	0.223	7.8	0.224
Q [dB]	6.5	0.48	7	0.58

3.3. Comparison with the Literature

In this subsection we compare the performance of the proposed biquads with other multi-GHz inductor-less lowpass filter implementations from the literature. Figures of merit (FOMs) are typically used to allow a fair comparison and highlight the trade-offs in the designs. In particular, the following figures of merit commonly used in filter literature have been exploited:

$$FOM_1 = \frac{P_{diss}}{N_{pole}} \tag{24}$$

$$FOM_2 = \frac{FOM_1}{f_{3dB}} \tag{25}$$

$$FOM_3 = \frac{FOM_2}{D_R^{pow}} \tag{26}$$

Figure of merit FOM_1 simply normalizes the power dissipation P_{diss} to the number of poles N_{pole}, to allow a comparison between filters of different order. Figure of merit FOM_2 takes also into account the 3dB-bandwidth of the filter f_{3dB}, highlighting the trade-off between power and frequency. Figure of merit FOM_3 includes also the dynamic range D_R, expressed in linear scale:

$$D_R^{pow} = 10^{D_R/10} \tag{27}$$

(D_R in (21) is the dynamic range in decibel). The dynamic range D_R is defined as the difference (in dB) between the signal level that corresponds to maximum signal-to-noise-and-distortion ratio (SNDR) and the noise level (i.e. SNR=0).

Table 5 shows a comparison with the literature. Some reported filters are implemented using BiCMOS, others use CMOS. CMOS implementations are expected to require lower power, but bandwidth and dynamic range can be limited, so that the two latter FOMs may be challenging.

The proposed biquads have the lowest consumption in the literature, and the only CMOS implementation with a larger bandwidth has more than 150 time the power dissipation. The very low power consumption increases the SNR, and thus limits the dynamic range of the filter. Hence, while the proposed biquads have remarkable FOM_1 and FOM_2 performance (consumption per pole and consumption per pole and bandwidth), the FOM_3 (which also includes the dynamic range) is good but two BiCMOS implementations are more efficient because of higher linearity and lower noise. The proposed biquads also have the lowest area occupation in the literature, almost one order of magnitude lower than comparable filters.

Table 5. Comparison with the literature.

Performance	This work		[34]		[28]	[39]	[16]	[40]	[23]	[13]	[12]
	N-type	P-type	N-type	P-type							
Tech. [nm]	CMOS 28 FDSOI		CMOS 28 FDSOI		BICMOS	CMOS 22	BICMOS	CMOS 90	BICMOS	CMOS 28	CMOS 22
N_{pole}	2	2	2	2	2	5	6	4	2	5	3
V_{DD} [V]	1.2	1.2	1.2	1.2	2.7	0.8	3	1	3	1.1	1.4
P_{diss} [mW]	0.82	0.67	1.08	1.6	15.75	19.9	43	3.7	18	30	140
f_{3dB} [GHz]	8.1	7.9	7.57	7.2	17.1	4.9	10.3	1	9.55	3.3	10
A_0 [dB]	-1.9	-2.3	-1.6	-1.8	3.8	0.5	-0.2	0	-0.5	-1	1.3
P_{inoise} [dBm]	-44.7	-45.4	-43.5	-39.4	-50.4	-56.8	-45.9	-46	-46.8	-56	-55.6
P_{in}^{Q} [dBm]	-10	-10	-10	-10	-2.9		-1	-13	-1	-17	-10.6
THD [dB] @ P_{in}^{Q}	-33.1	-33.4	-46.8	-42.4	-51.7		-42.6	-41.77	-64	-40	-45
IIP3 [dBm]					17.25	5.5					
DR [dB]	33.9	34.4	40.2	35.9	47.9	41.7	43.1	34.9	50.9	38.4	44
Area [mm²]	0.00038	0.00038	0.000246	0.000193	0.0025	0.05	0.02	0.000092	0.0027	0.09	0.01
Area/pole [mm²]	0.00019	0.00019	0.000123	0.000096	0.00125	0.01	0.003	0.000023	0.00135	0.018	0.003
FOM1 [mW]	0.41	0.33	0.54	0.3	7.87	3.98	7.2	0.925	9	6	46.7
FOM2 [pW/Hz]	0.051	0.042	0.071	0.042	0.461	0.812	0.696	0.925	0.942	1.818	4.667
FOM3 [aW/Hz]	20.52	15.31.	6.82	10.78	7.48	54.88	33.84	297.46	7.65	267.08	185.93
Sin. /Meas.	S	S	S	S	S	M	S	S	S	M	M

4. Conclusions

Two complementary single-ended CMOS high-speed lowpass filters have been developed and extensively simulated, showing remarkable performance, good tunability, and good stability to PVT and Monte Carlo simulations. The two filters have excellent figures of merit, proving that CMOS technologies can be used for filters from DC up to 10GHz of cut-off frequency.

The complementary nature of the two biquad stages make them easily cascadable to obtain higher-order filters with steeper response in the transition band. The inductor-less architecture, and the limited active and passive component count, allow an extremely low-area design, an order of magnitude lower than the best alternatives in the literature. Tunability can be obtained for both bandwidth and quality factor controlling the two bias currents separately: the tunability range is larger than the effect of PVT variations and mismatches, thus allowing their compensation. Power consumption, also normalized for number of poles (FOM1) and bandwidth (FOM2) is excellent with respect to the literature, including CMOS and BiCMOS solutions.

Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-digital converter
CMOS	Complementary metal-oxide-semiconductor
DAC	Digital-to-analog converter
FDSOI	Fully depleted silicon on insulator
FOM	Figure of merit
FVF	Flipped voltage follower
LPF	Lowpass filter
MFP	Multiply-filter-processing
SF	Source follower
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SSF	Super source follower

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