On the Realization of “Dead Time” in a Synchronous Step-Down Converter

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Article

On the Realization of "Dead Time" in a Synchronous Step-Down Converter

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Abstract: The article proposes a synchronous step-down converter implemented with P-channel and N-channel transistors. The transistors are controlled by a single driver, and "dead time" is implemented with external circuits. When an initial problem occurs with ensuring this time in practical implementation, the influence of the Schottky diode capacitance on "dead time" is considered. Mathematical expressions were derived, showing the ratio of the value of this capacitance and the input capacitance of the transistor, and the influence of this ratio on the shape of the leading edge of the pulse for switching on the transistor. Results of computer simulation are given for different ratios of the two capacitances. The results of the mathematical description and computer simulation were used to select a suitable transistor and Schottky diode and are applied in the subsequent practical implementation. Conclusions and recommendations were done, for the synchronous step-down converter, as well as for other cases of implementing dead time in the manner considered.

Keywords: synchronous step-down converter; dead time; P-channel MOSFET; N-channel MOSFET; Schottky diode; junction capacitance

1. Introduction

The main issues in the design of DC/DC converters are presented in [1]. The difference between continuous and discontinuous current mode through the inductance is discussed for example in [2]. Typically, the synchronous step-down converter is implemented with two N-channel MOSFETs [3]. Issues related to the efficiency of such a converter are considered, for example, in [4–7]. The requirements for controlling MOSFETs are considered in many scientific works, such as [8–13]. In cases where the supply voltage does not exceed the maximum allowable gate-source voltage of a P-channel MOSFET, the upper N-channel transistor in the synchronous buck converter can be replaced by a P-channel transistor. This provides certain advantages in terms of controlling both transistors. It can be implemented by a single driver with push-pull output as shown in Figure 1. In this way, some additional elements are avoided to provide the control voltage of the upper transistor in case it is also N-channel – capacitor, diode and additional circuits [14]. However, it should be noted that in the proposed control in Figure 1, one of the two transistors is always on, while in the case of two N-channel transistors, both can be turned off under certain circumstances. This is a known disadvantage of the variant considered in this study, which is suitable, for example, when charging low-power energy storage elements - batteries, ultracapacitors. In this case, the constant current regulation and voltage limitation can be carried out, and when the maximum charging voltage is reached, the electronic regulator for this voltage remains to work, i.e. both transistors can be switched. Issues related to regulation and the rest of the control system are not the subject of consideration in this research. The charging circuits of the input capacitances of the two transistors is presented on Figure

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1 (red lines) and the discharge circuits (blue lines). The additional elements to the gates of the transistors (the two resistors and the Schottky diode) are known and often recommended. Through these circuits, the so-called "dead time" is implemented when controlling the transistors. The goal is to turn one transistor on with a certain delay compared to turning the other off. This problem is known and also exists in other converters using phase leg transistors [15]. Different methods for realization "dead time" are known [16–20]. For the circuit of a synchronous converter using two N-channel MOSFETs, controllers in an integrated circuit are proposed, containing different methods for "dead time" realization [21,22]. The present work focuses on the realization with the circuits shown in Figure 1. The operating principle is as follows:

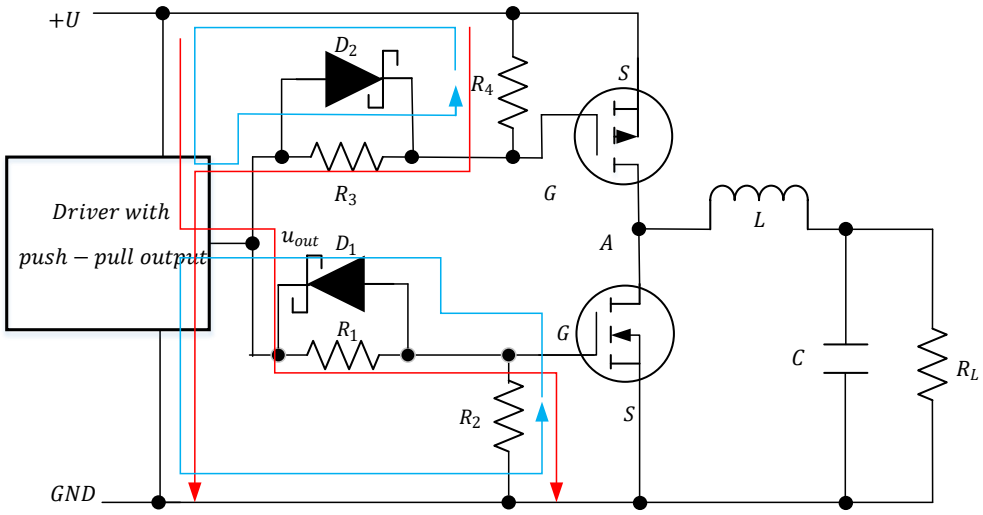

Figure 1. Implementation with P-channel and N-channel MOSFET and control with a driver with push-pull output

At a low level at the driver output (the lower transistor at its output is turned on), the input capacitance of the lower N-channel transistor is discharged through the diode D_1 and the driver output. At the same time, the input capacitance of the upper P-channel transistor is charged through the resistor R_3 to a voltage approximately equal to the supply +U (the difference is due to the voltage on the transistor at the driver output). At a high level at the driver output (the upper transistor at its output is turned on), the input capacitance of the upper P-channel transistor is discharged through the diode D_2 and the driver output. At the same time, the input capacitance of the lower N-channel transistor is charged through the resistor R_1 to a voltage approximately equal to the supply +U (the difference is due to the voltage on the transistor at the driver output). Since the charging of the input capacitances occurs through a resistor, the idea is to change its value and the charging time constant to change the turn-on delay time. It can be larger than that during turn-off, because the capacitance discharge occurs through the low-resistance Schottky diode [23].

In the literature known to the authors no methodology for sizing these circuits is described, especially with regard to the problem described below. This problem may occur in low-power converters, where the input power sources are small photovoltaics, piezoelectric elements, etc. In these cases, the transistors used are low-power. Characteristic features of low-power MOSFETs are the low threshold voltage U_{th} (usually 0.7 – 1.5V) and the small value of the input capacitance C_{iss} (usually tens to hundreds of pF). When controlling power MOSFETs, the described problem could not arise, since their threshold voltage is high (usually above 4.5V), and their input capacitance is larger (up to several tens of nF).

Description of the problem: When controlling the transistors in the manner shown in Figure 1, the authors observed the oscillograms shown in Figure 2 and Figure 3. The supply voltage of the converter is 3.3V. In Figure 2 - CH2, a steep trailing front is observed in the voltage of the drains of both transistors (point A – Figure 1), i.e. the lower transistor turns on very quickly. At the same

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moment, a sharp decrease is observed in the supply voltage on CH1. These are signs of simultaneous conduction of both transistors, i.e. a single-arm short circuit. From CH1 in Figure 3, it can be seen that at the same moment in time, the gate-source voltage of the lower transistor increases steeply, and it has been established that the rate of increase is not affected by a change in the value of the resistor R1 from Figure 1. This prompted a more detailed study of these circuits, described below.

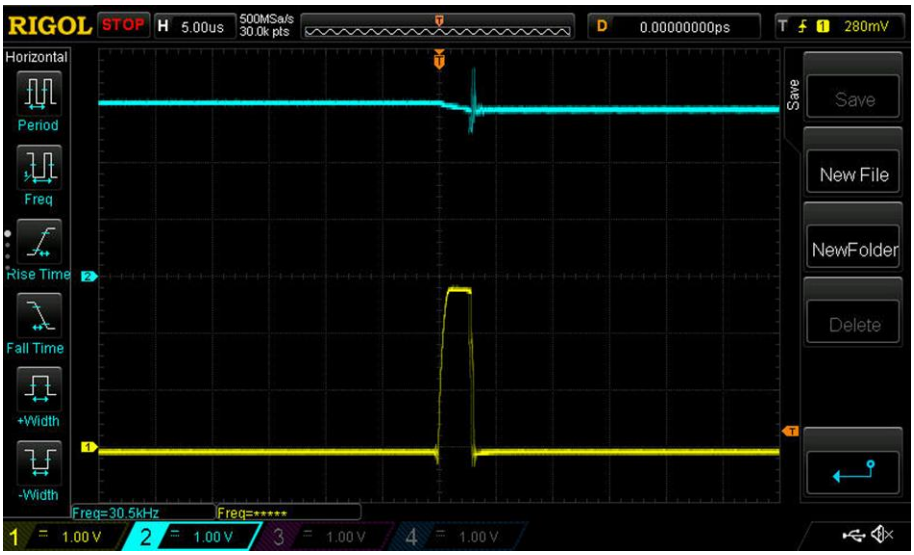

Figure 2. CH1 – supply voltage 3.3V, CH2 – voltage at point A.

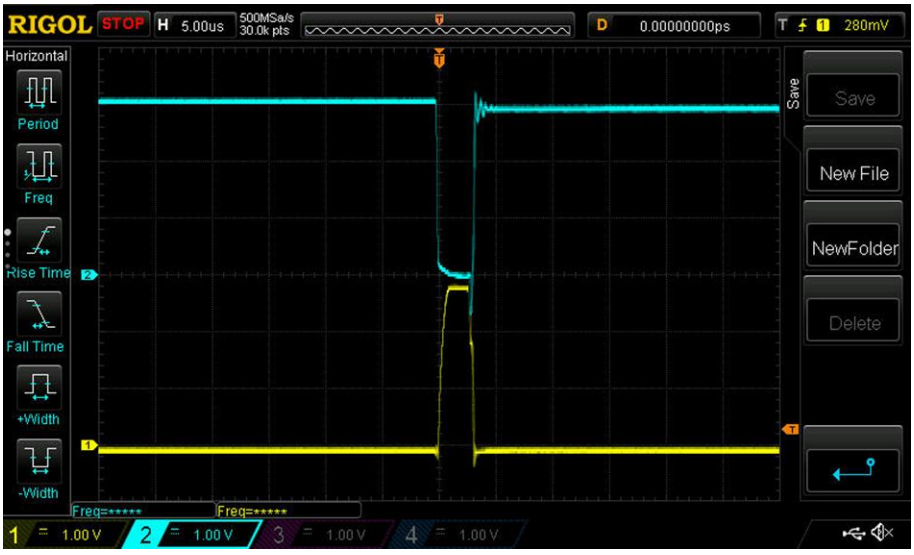

Figure 3. CH1 – the impulse of the lower transistor, CH2 – the voltage at point A.

2. Mathematical Descriptions and Study

Essential to the solution of the described question is the consideration of the influence of the Schottky diode capacitance when applying a signal to turn on the transistor. The study was carried out using the circuit shown in Figure 4, where the Schottky diode capacitance C_j and the input capacitance of the transistor C_{iss} are added to the elements D_1, R_1, R_2 existing in Figure 1. The equivalent circuit for mathematical description is presented in Figure 5.

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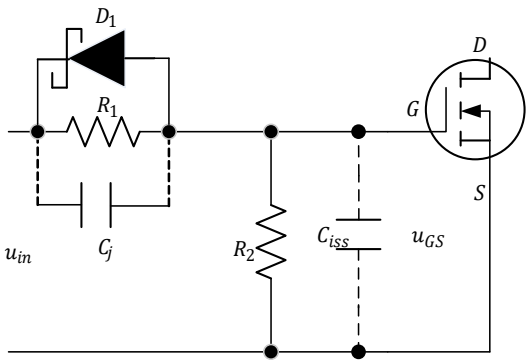

Figure 4. Scheme for studying the influence of the Schottky diode capacitance when applying a signal to turn on the transistor.

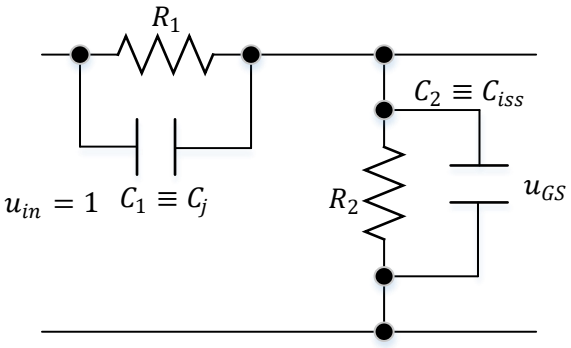

Figure 5. Mathematical description scheme -$C_1 \equiv C_j$; $C_2 \equiv C_{iss}$.

It is assumed that the input voltage is increased stepwise to a value of 1 (single input pulse) $u_{in} = 1$ and the change in the output voltage u_{GS}, which is the gate-source voltage of the transistor, is examined.

The expressions for the impedances from the circuit on Figure 5 in operator form are:

$$Z_1(s) = \frac{R_1}{1+s.R_1.C_1};\ Z_2(s) = \frac{R_2}{1+s.R_2.C_2} \quad (1)$$

For a single input, the output voltage has the form:

$$u_{GS}(s) = \frac{1}{s}.\frac{Z_2(s)}{Z_1(s)+Z_2(s)} \quad (2)$$

It can be represented also:

$$u_{GS}(s) = \frac{A}{a+s} + \frac{B}{s(a+s)} \quad (3)$$

where,

$$A = \frac{C_1}{C_1+C_2} \quad (4)$$

$$B = \frac{R_2}{R_1+R_2}$$

$$a = \frac{1}{\tau}$$

$$\tau = \frac{R_1.R_2.(C_1+C_2)}{R_1+R_2}$$

When switching from Laplace form to the original, the change in output voltage over time is obtained:

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$$u_{GS}(t) = A.e^{-\frac{t}{\tau}} + B.\left(1 - e^{-\frac{t}{\tau}}\right) \quad (5)$$

Figure 5 presents the two terms of expression (5) – the first with a blue line, the second – with a green line, and their sum – with a red line.

From Figure 6 it can be seen that the output voltage u_{GS}, which is the gate-source voltage of the transistor, has a sharp increase at the initial moment, which depends on the ratio of the two capacitances C_1 (the capacitance of the Schottky diode) and C_2 (the input capacitance of the MOSFET). For example, if $C_2 \gg C_1$ the value of the initial increase will be of a negligible value. If the two capacitances are equal, this value will be equal to half the value of the input voltage. However, if, $C_1 \gg C_2$ the initial increase may be close to the value of the input voltage. This is the effect that is observed in the upper oscillogram of Figure 3. The problem is that depending on the ratio of the two capacitances, the value of the initial increase may be greater than the value of the threshold voltage U_{th} of the transistor. In such a situation, "dead time" is not realized and the effect described in the introduction is observed.

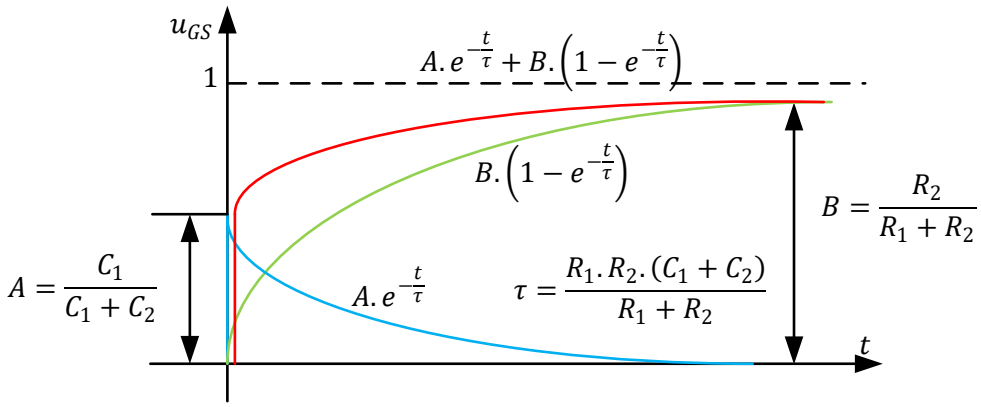

Figure 6. Variation of the output voltage over time - the red line.

Formula (5) can be used to determine the value of the "dead time" depending on the value of the resistor R_1 at known other values. For this purpose, it is presented in the form:

$$u_{GS}(t) = (A - B)e^{-\frac{t}{\tau}} + B \quad (6)$$

When replacing $\boldsymbol{t = t_d}$ and $\boldsymbol{u_{GS}(t_d) = U_{th}}$ the expression is obtained:

$$\boldsymbol{t_d = \tau . ln\frac{A-B}{U_{th}-B}} \quad (7)$$

By substituting in (7) the quantities from formula (4) we get:

$$t_d = \frac{R_1.R_2.(C_1+C_2)}{R_1+R_2} . ln\frac{\frac{C_1}{C_1+C_2} - \frac{R_2}{R_1+R_2}}{U_{th} - \frac{R_2}{R_1+R_2}} \quad (8)$$

Because dependencies were derived at unit input, then the value of U_{th} should be set in units relative to the maximum value of the driver's output voltage. So, for example, if it is 3V and the threshold voltage is 1.8V, in formula (8) for U_{th} value 0.6 should be substituted.

In formula (8), the capacitance values are known from the reference data for the selected elements – Schottky diode, MOSFET and Zener diode parallel to the gate-source transition. The value of resistor R_2 is usually 10K. It remains for different values of R_1 to calculate the value of t_d and choose the appropriate value of the resistor.

So, for example, for variant 4 of table 1 considered below, the values are as follows: $C_1 = 140pF$; $C_2 = 365pF$; $R_2 = 10K$. With a minimum threshold voltage of 1V for the MOSFET and an output voltage from the driver of 3V in formula (8) is placed $U_{th} = \frac{1}{3} \approx 0.33$. After calculation at resistor value $R_1 = 500\Omega$ a value is obtained for t_d 111 ns.

A computer simulation was performed using models of real diodes and transistors. The results are shown and commented below.

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Variant 1 – Schottky diode 1N5819 with a capacitance of 150 pF [24], input capacitance of the transistor 150 pF. The input signal has a maximum value of 5V. The simulation scheme and the results are shown on Figure 7.

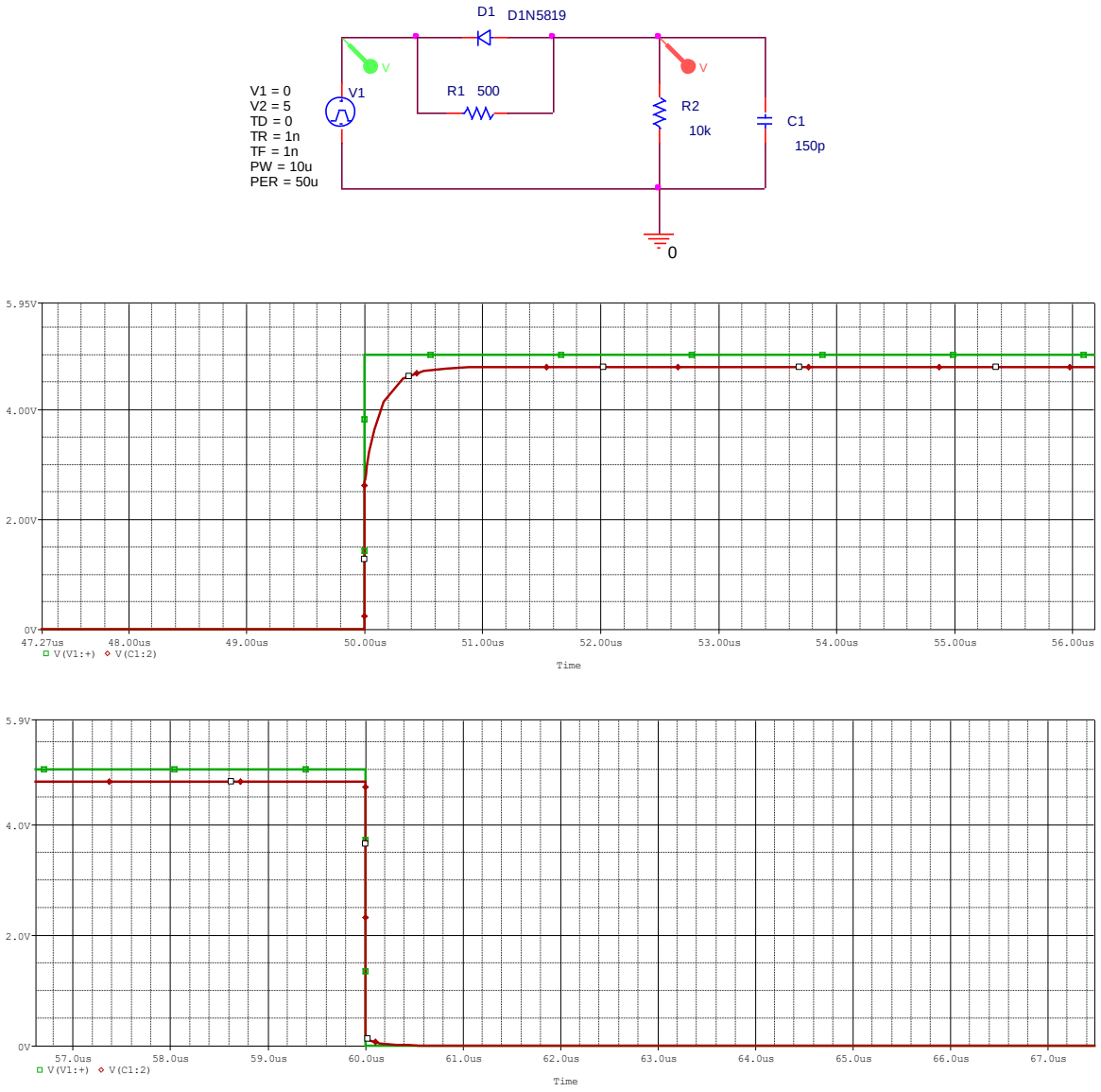

Figure 7. Simulation scheme and results for variant 1.

It can be seen that when a signal is applied to turn on, the initial peak of the output voltage is 2.5 V in accordance with the coefficient A from Figure 6. When switched off, an initial retention of about 0.3 V (the voltage across the switched-on Schottky diode) is observed. It is clear that with such a combination, the realization of dead time will not be obtained for transistors with a threshold voltage below 2.5 V.

Variant 2 - Schottky diode 1N5819 with a capacitance of 150 pF [24], input capacitance of the transistor 500 pF. The input signal has a maximum value of 5V. The simulation scheme and the results are shown on Figure 8.

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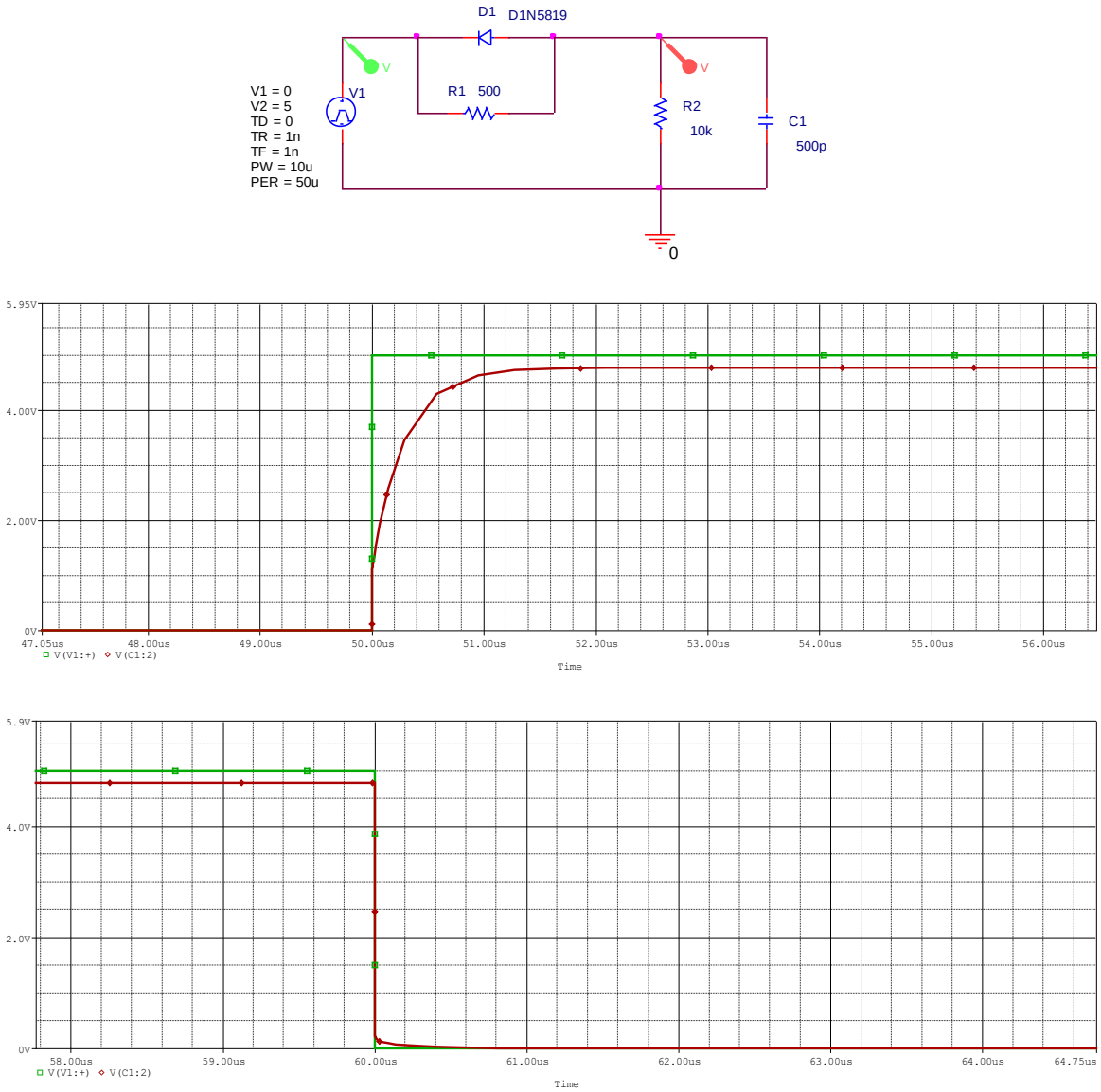

Figure 8. Simulation scheme and results for variant 2.

It can be seen, when a signal is applied to turn on, the initial peak of the output voltage is approximately 1V in accordance with the coefficient A from Figure 6. When switched off, an initial retention of about 0.3 V (the voltage across the switched-on Schottky diode) is observed. It is clear that with such a combination, the realization of "dead time" will not be obtained for transistors with a threshold voltage below 1V. When the input capacitance of the transistor increases, the initial jump of the gate-source voltage decreases.

Variant 3 – Silicon diode 1N4148 with a capacitance of 3 pF [25], input capacitance of the transistor 500 pF. The input signal has a maximum value of 5V. The simulation scheme and the results are presented on Figure 9. This option was chosen because pulse diodes with a PN junction are characterized by significantly smaller capacitance values.

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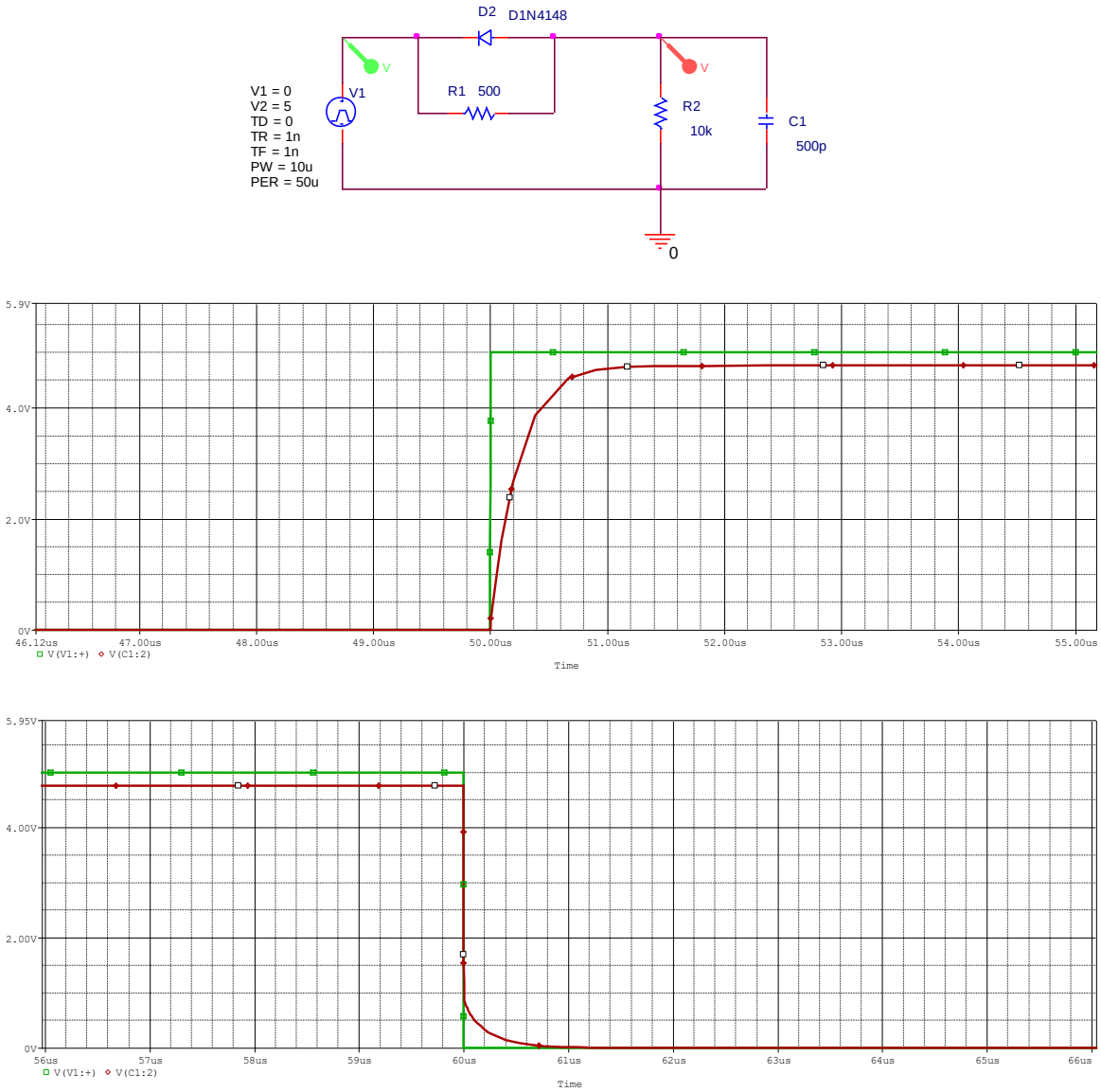

Figure 9. Simulation scheme and results for variant 3.

This variant corresponds to the condition $C_2 \gg C_1$

It can be seen that when a signal is applied to turn on, the initial peak of the output voltage is negligibly small in accordance with the coefficient A - Figure 6. It is clear that with such a combination the implementation of "dead time" when turning on the lower transistor will be the easiest even at low threshold voltages. When turning off, an initial hold of a value of about 0.7 V (the voltage on the switched-on diode) is observed. However, this is unpleasant, since at the same moment a signal is applied to turn on the upper transistor of the synchronous converter and at threshold voltages of the lower one about 0.7 V the latter may remain on for a short time. This would make it difficult to implement "dead time" when turning on the upper transistor. For this reason, the authors recommend using Schottky diodes, as in the scheme on Figure 1.

Variant 4 – Connecting a zener diode in parallel with the gate-source junction of the transistor. The diode has protective functions and are described in the literature [8,9]. The schematic diagram together with the capacitances is shown on Figure 10. - Schottky diode 1N5819 with a capacitance of 150 pF [24], input capacitance of the transistor 500 pF, zener diode BZX84C5V6 SMD with a capacitance of 200 pF [26]. The input signal has a maximum value of 5V. The simulation scheme and the results are shown on Figure 11.

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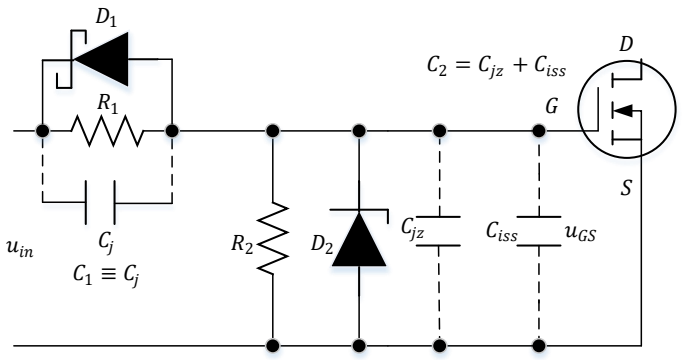

Figure 10. Connecting a zener diode in parallel with the gate-source junction of the transistor.

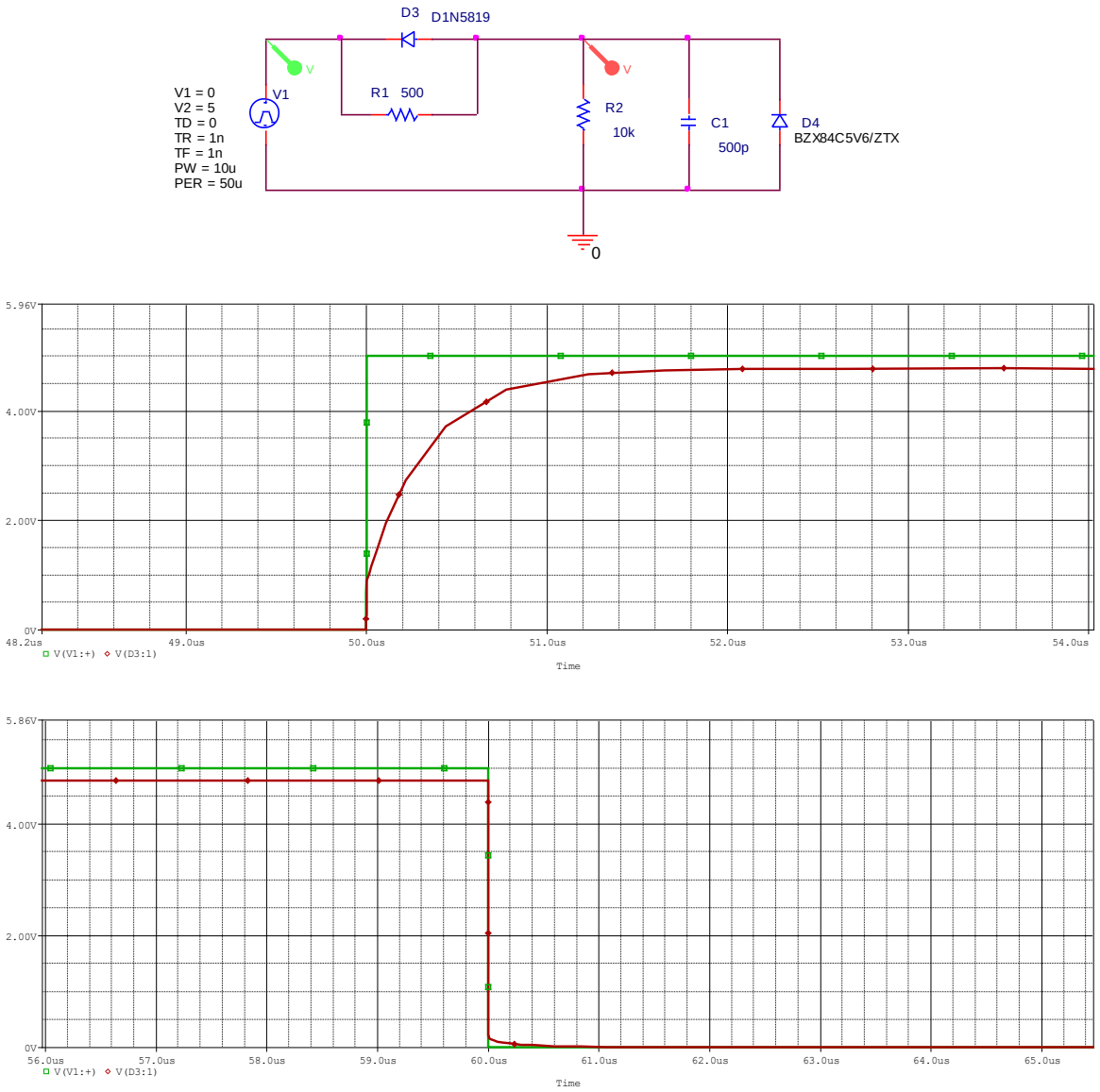

Figure 11. Simulation scheme and results for variant 4.

This variant differs from variant 2 only in the inclusion of the zener diode. From the comparison of the timing diagrams on Figure 11 with those on Figure 8, it is seen that the initial peak is reduced to about 0.9 V, which would facilitate the implementation of "dead time" for transistors with a threshold voltage above 1V. In addition to the protective function, the authors recommend placing a zener diode also from the point of view of the issue considered in this article.

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3. Experimental

The initially implemented variant for the lower transistor on Figure 1 is the following: transistor BSS214N with capacitance $C_{iss} = 107pF$ and threshold voltage $U_{th} = 0.7V$ [27] and Schottky diode SS34 with capacitance $C_j = 1nF \div 500pF$ [28]. The oscillograms shown on Figure 2 and Figure 3 correspond to this variant. From the previous consideration, it is clear that this variant is unsuitable. Table 1 shows various possible variants for implementation - combinations of Schottky diodes and transistors with or without a zener diode. Those shown in red are unsuitable, the one in yellow is not preferable, since the results are close to the limit. From the point of view of "dead time", variants 4, 5 and 6 are suitable - shown in green. Variants 5 and 6 are not preferred due to the considerations expressed when commenting on the results in Figure 9. The preferred implementation variant is 4, shown in blue in the first column of Table 1. It uses a Schottky diode SS14 with a significantly smaller capacitance than SS34 [29].

Table 1. Variants for providing "dead time" for a signal to turn on the lower transistor.

	Schottky diode (Diode) Capacitance, pF	**Transistor, Zener diode Capacitance, pF**	**Value of A, Starting voltage G-S at 3V from the driver, V**	**Transistor $U_{GS(th)}$, min. value, V**
Variant 1	SS34,$C_j = 500pF$	BSS214N, $C_{iss} = 107pF$	0.837, 2,51V	0.7
Variant 2	SS34, $C_j = 500pF$	UT6402G, $C_{iss} = 265pF$	0.654, 1.962V	1.0
Variant 3	SS14, $C_j = 140pF$	UT6402G, $C_{iss} = 265pF$	0.345, 1.035V	1.0
Variant 4	SS14, $C_j = 140pF$	UT6402G, $C_{iss} = 265pF$, BZM55C5V1, $C_{jz} = 100pF$	0.277, 0.831V	1.0
Variant 5	1N4148W-G, $C_j = 2pF$	UT6402G, $C_{iss} = 265pF$	0.0075, 0.0225V	1.0
Variant 6	1N4148W-G, $C_j = 2pF$	UT6402G, $C_{iss} = 265pF$, BZM55C5V1, $C_{jz} = 100pF$	0.00544, 0.0163V	1.0

The last three variants from Table 1 were evaluated from the following point of view: When turning on the upper transistor from Figure 1 and increasing the voltage in point A, through the feedback capacitance C_{rss} of the lower transistor, its gate-source capacitance is charged (Miller effect) [30]. Shortly before this (to ensure the "dead time") there is a low level at the driver output. In this situation, due to the feedback, the input capacitance would be charged to a voltage equal to the sum of the drop on the Schottky diode (or the pulse diode with a PN junction) and the voltage on the lower transistor of the driver. This sum of voltages must remain less than the threshold voltage of the lower transistor, otherwise it is possible to turn it on as well. With a sharp increase in the voltage at point A, the consideration made in the previous part can be applied. The results from Table 2 show that from such a point of view, variants 5 and 6 are borderline (shown in yellow). Variant 4 (in green) is also suitable for this consideration.

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Table 2. Ensuring the off state of the lower transistor through the feedback capacitance when the upper transistor is turned on.

	Schottky diode (Diode), forward voltage, V Driver output low voltage, V	**UT6402G, $C_{Rss} = 56pF$**	**Value of s**tarting voltage G-S at 3V from D-S,V	**Transistor $U_{GS(th)}$, min. value, V**
Variant 4	SS14, *0.3V*, LPV7215, $V_{oL} =$ *0.3V* Total 0.6V<1V	UT6402G, $C_{iss} = 265pF$, BZM55C5V1, $C_{jz} =$ *100pF*	0.4V	1.0
Variant 5	1N4148W-G, *0.75V* LPV7215, $V_{oL} =$ *0.3V* Total 1.05V>1V	UT6402G, $C_{iss} = 265pF$	0.523V	1.0
Variant 6	1N4148W-G, *0.75V* LPV7215, $V_{oL} =$ *0.3V* Total 1.05V>1V	UT6402G, $C_{iss} = 265pF$, BZM55C5V1, $C_{jz} = 100pF$	0.4V	1.0

After the implementation assessment, variant 4 was chosen, and the part of the board corresponding to the scheme under consideration is shown in Figure 12. All electronic elements correspond to this variant 4.

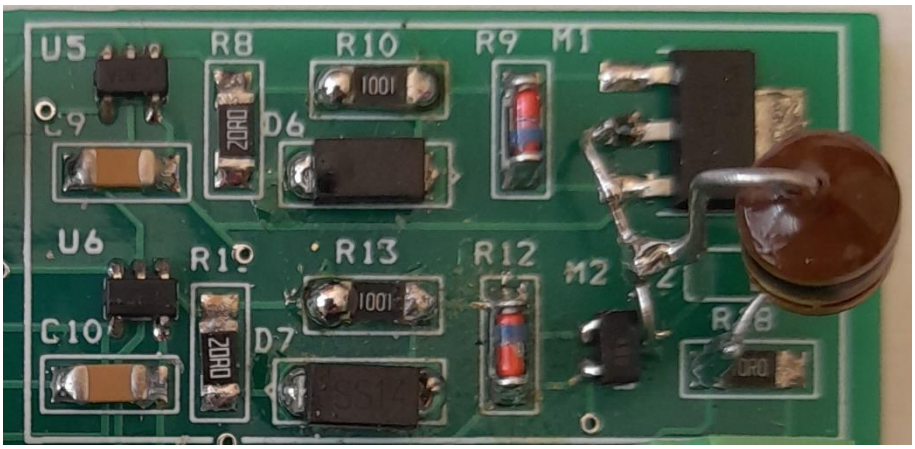

Figure 12. A picture of the power schematic part.

Schottky diodes $\boldsymbol{D_6}$ and $\boldsymbol{D_7}$ are SS14 and correspond to $\boldsymbol{D_2}$ and $\boldsymbol{D_1}$ in Figure 1. Resistors $\boldsymbol{R_{10}}$ and $\boldsymbol{R_{13}}$ consist of two parallel-connected resistors with a value of 1K and correspond to $\boldsymbol{R_3}$ and $\boldsymbol{R_1}$ in Figure 1. Resistors $\boldsymbol{R_9}$ and $\boldsymbol{R_{10}}$ have a value of 10K and correspond to $\boldsymbol{R_4}$ and $\boldsymbol{R_2}$ in Figure 1. zener diodes BZM55C5V1 are soldered to these resistors. The transistor M1 (P-channel) is BSP250. The transistor M2 (N-channel) is UT6402G. The two drains pins are connected externally together with the left terminal of the inductance in the diagram of Figure 1 (point A – Fig.1).

Figure 13 and Figure 14 show the recorded oscillograms. The operating frequency of the converter is 17 kHz, and the supply voltage is 3.3 V.

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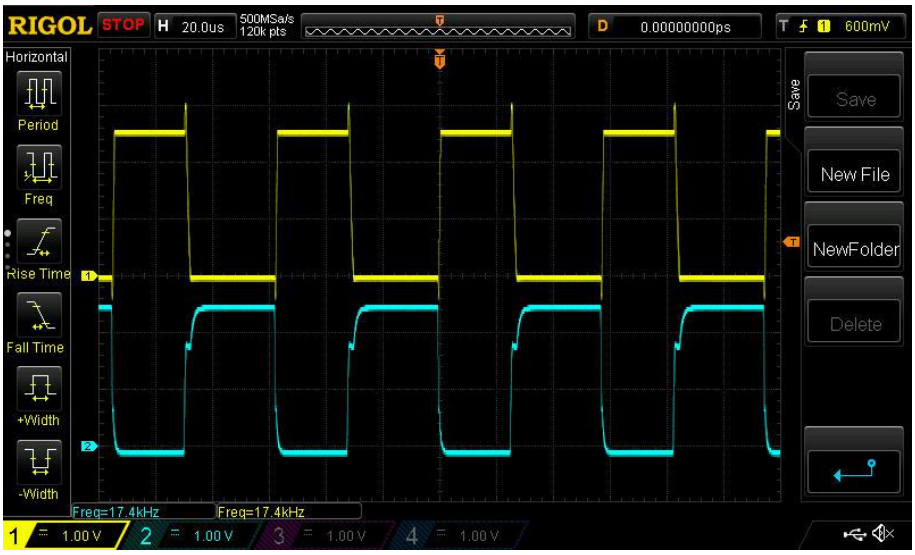

Figure 13. CH1 - the voltage in point A; below it CH2 - pulses to control the lower transistor.

From CN2 on Figure 13, the gradual increase in the gate-emitter voltage of the N-channel transistor when turned on (to realize "dead time" when turning off the P-channel transistor) and a rapid decrease (to realize "dead time" when turning on the P-channel transistor) are observed.

Figure 14. CH1 - the control pulses of the lower transistor, below them CN2 - the supply voltage.

From CN2 in Fig.14, it can be seen that there are no short-term dips in the supply voltage both during switching on and during switching off of the N-channel transistor. The measured current, consumed by the power source in this case is significantly less than that in the case of Figure 2. These are proofs of correct implementation of dead time according to the scheme of Figure 10 for the two transistors of the synchronous step-down converter.

4. Conclusions

The article presents the results of the study of a synchronous step-down converter implemented with P-channel and N-channel MOSFET. The realization of "dead time" with external elements when controlled by a driver with push-pull output is considered. Main attention is paid to the influence of the Schottky diode capacitance. The main conclusions are as follows:

1. It is recommended to implement the external circuits to the gate of the transistor according to the scheme in Figure 10.

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2. When designing "dead time' circuits, it is necessary that the Schottky diode capacitance be significantly smaller than the input capacitance of the transistor.
3. Based on formula (5) and Fig.6, the compliance with the threshold voltage of the MOSFET must also be checked.
4. It is not recommended to use a pulse diode with a PN junction instead of a Schottky diode due to possible parasitic charging of the input capacitance of the transistor through the feedback capacitance when the upper transistor is turned off and possible reaching the threshold voltage of the lower.
5. It is recommended to include zener diodes in parallel with the gate-source junction of the transistors with the lowest possible reference voltage, but greater than the maximum threshold (zener diodes with lower reference voltage have greater capacitance). In addition to their protective function, these diodes also facilitate the realization of "dead time".
6. Formula (8) can be used to determine the value of the dead time t_d at different values of the resistor R_1 and known values of the other quantities as described above.

The considerations and conclusions presented in this article refer not only to the diagram in Fig.1. They can be applied in all cases of implementation of dead time according to the scheme of Figure 10.

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