Modelling, Design, and Application of Analog Pre-Distortion for the Linearity and Efficiency Enhancement of a K-Band Power Amplifier

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Article

Modelling, Design, and Application of Analog Pre-Distortion for the Linearity and Efficiency Enhancement of a K-Band Power Amplifier

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Abstract: This paper presents the theory, design, and application of a dual-branch series-diode analog pre-distortion (APD) linearizer to improve the linearity and efficiency of a K-band high power amplifier (HPA). A first-of-its-kind, frequency-dependent large-signal APD model is presented. This model is used to evaluate different phase relationships between the linear and nonlinear branches, suggesting independent gain, and phase expansion characteristics with this topology. This model is used to assess the impact of diode resistance, capacitance, and ideality factor on the APD characteristics. This feature is showcased with two similar GaAs diodes to find the best fit for the considered HPA. The selected diode is characterized and modeled between 1-26.5 GHz. A comprehensive APD design and simulation workflow is reported. Before fabrication, the simulated APD is evaluated with the measured HPA to verify linearity improvements. The APD prototype achieves a large signal bandwidth of 6 GHz with 3 dB gain expansion and 8° phase rotation. This linearizer is demonstrated with a 17-21 GHz GaN HPA with 41 dBm output power and 35 % efficiency. Using a wideband 750 MHz signal, this APD improves the noise power ratio (NPR) by 6.5-8.2 dB over the whole HPA bandwidth. Next, the HPA output power is swept to compare APD vs. power back off for the same NPR. APD improves the HPA output power by 1-2 W and efficiency by approximately 5-9 % at 19 GHz. This efficiency improvement decreases by only 1-2 % when including the APD post-amplifier consumption, thus suggesting overall efficiency and output power improvements with APD at K-band frequencies.

Keywords: analog pre-distortion (APD); backhaul; efficiency; digital pre-distortion (DPD); gallium-nitride (GaN); high power amplifier (HPA); linearization; noise power ratio (NPR)

1. Introduction

Attaining amplification with high power, efficiency, and linearity on a wide frequency range poses a formidable challenge, particularly when operating at higher frequencies. Pre-distortion linearization is an effective technique that can be introduced before the high power amplifier (HPA) to compensate for the HPA nonlinear characteristics in both amplitude and phase over its bandwidth [1]. This can be easily achieved at baseband with digital pre-distortion (DPD), thanks to the high flexibility of digital algorithms. However, DPD requires the use of digital signal processors such as FPGAs or ASICs whose cost and power consumption increase with the clock frequency [2]. DPD also requires the use of at least five times the signal bandwidth, thus significantly increasing the power demand of the digital baseband [2].

Analog pre-distortion (APD) linearization has a fundamental advantage over DPD by directly implementing the APD circuit in the RF/microwave front-end with minimal addition of hardware, cost, and power consumption while enabling very wide bandwidths. It is therefore an ideal technique for many fields, such as wideband RF transmitters, radio-over-fiber-optic, satellite communications,

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radar, and electronic warfare systems. The linearizer module is typically composed of an APD circuit, including a nonlinearity or inter-modulation generator, and a post-amplifier that compensates for the losses of the analog linearizer.

The degree of improvement attainable with APD depends on the HPA compression point [1]. At deep compression, the HPA is clipping and both DPD and APD cannot recover from this. When instead the HPA is in back-off, APD linearization is unnecessary and may even degrade HPA linearity [1]. When instead the HPA is operated 3-4 dB into compression, to maximize its output power and efficiency, APD linearization is an effective technique that can increase the HPA linearity.

APD is particularly suitable with HPAs realized with Gallium-Nitride (GaN) as they can provide wide bandwidths that are difficult to cover with DPD. GaN is also a well-suited technology for space and satellite applications given its radiation hardness and temperature handling capabilities. Today, commercial mm-wave GaN HPAs can achieve 10 W output power with up to 35 % efficiencies and bandwidths exceeding 4 GHz at K-band, e.g. [3]. However, such efficiencies rapidly decrease when the HPA is operated in back-off to improve linearity.

APD linearizer architectures can be divided into 1) single-branch linearizers and 2) dual-branch linearizers [4]. Both 1) and 2) rely on a nonlinearity generator, either an amplifier or a diode. For best performance, this nonlinearity needs to closely match the HPA compression shaping in amplitude and phase.

Single-branch linearizers can be based on a shunt diode [5,6], on a series diode [7], or on a FET [8] and have shown adjacent channel power ratio (ACPR) improvements between 5 and 7 dB. Important design parameters of single-branch APDs are the diode parallel capacitor and the bias point. By tuning the diode bias and parallel capacitor value, it is possible to improve the HPA linearity but with ACPR improvements below 4 dB [4]. A single-branch shunt diode linearizer at 2.4 GHz achieves improvements of the ACPR of 5 dB and improvement of the HPA efficiency by 8.5% [5]. This concept is extended in [6] by using two shunt diodes separated by a transmission line to achieve higher suppression at 2.2-2.3 GHz. At Ku-band frequencies (14-15 GHz), a single-branch linearizer based on a branch-line hybrid has been demonstrated to achieve up to 11 dB gain expansion and 180° phase rotation [9]. At V band frequencies, a single-branch linearizer is realized with a 3 dB waveguide coupler and a pair of Schottky diodes in [10]. This linearizer provides up to 7.8 dB amplitude expansion and 28° phase expansion between 59 and 61 GHz.

Dual-branch linearizers provide higher performance as compared to single-branch linearizers thanks to the extra degree of flexibility introduced by the added branch [10–15]. Recently, a dual-branch linearizer with independently tunable gain and phase at Ka-band frequencies has been proposed in [13]. This linearizer achieves 4.5 dB gain expansion and 23.4° phase variation at 29-31 GHz [13]. At lower frequencies, a triple-diode linearizer for narrowband HPAs at 2.14 GHz is proposed in [15] and it is used to reduce dual inflection in the gain characteristic typical of high-efficiency HPA modes. This linearizer can reduce the gain expansion by 0.4 dB while maintaining the same P_{1dB} and improving the IMD3 by 10 dB. Another example is the one discussed in [14] in which two diodes connected to a hybrid coupler are used to obtain a purer cubic nonlinearity. This linearizer achieves between 11.5 and 22.6 dB improvement of the IMD3 between 27 and 31 GHz.

This work advances the associated conference paper [16] by introducing a first-of-its-kind APD model of the proposed dual-branch series-diode linearizer [17]. This model is used to investigate the impact of the phase offset between the linear and nonlinear branches, highlighting the possibility of achieving negative or positive phase rotation while maintaining the same gain expansion. This model is used to compare two similar diodes to find the best fit for the inverted HPA characteristics. The selected diode is characterized between 1-26.5 GHz. A detailed simulation and design workflow are reported for this APD. Simulation results predict a large signal bandwidth of 16-25 GHz with gain expansion of 4-5 dB and phase rotation of 10°. The simulated APD is verified with the HPA-in-the-loop to evaluate linearity improvements before APD fabrication. Next, the APD circuit is experimentally characterized at small- and large-signal, with results used to validate the APD model. The APD circuit

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archives 3 dB gain expansion and 8° phase increase between 15-21 GHz. This APD is able to increase the average output power and efficiency, including post-amplifier consumption, across the whole bandwidth of a K-band GaN HPA.

2. Wideband Large-Signal APD Model

The block diagram of the APD linearizer is shown in Figure 1. This linearizer uses a 3 dB splitter to feed a linear and a nonlinear branch. The linear branch is realized with a transmission line of electrical length $\phi_{LIN}(f)$. The nonlinear branch contains a line of electrical length $\phi_{NL}(f)$, a series diode, and two bias-Ts providing a bias voltage V_{D0}. The output of the two branches is summed by a 3 dB combiner.

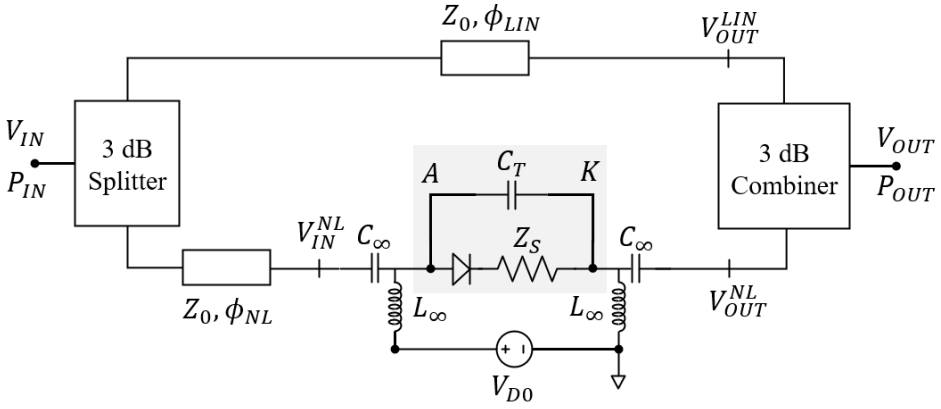

Figure 1. Schematic of the dual-branch APD with series diode, phase delay lines, bias-Ts (ideal RF choke L_∞ and an ideal DC block C_∞), and 3 dB splitters and combiners.

Let's assume a power $P_{IN} = V_{IN}^2/2Z_0$ at the APD input, where V_{IN} is the peak RF voltage and Z_0 is the characteristic impedance. This signal is split by a loss-less perfectly-matched 3 dB splitter that generates two in-phase signals $V_{IN}/\sqrt{2}$ at the input of the linear and nonlinear branches. The linear branch is modeled with an ideal loss-less transmission line described by

$$V_{OUT}^{LIN}(f) = \frac{V_{IN}}{\sqrt{2}} e^{j\phi_{LIN}(f)} \tag{1}$$

The nonlinear branch uses an ideal lossless transmission line to connect to the diode and bias-Ts, which is described by

$$V_{IN}^{NL}(f) = \frac{V_{IN}}{\sqrt{2}} e^{j\phi_{NL}(f)} \tag{2}$$

Let's now define the phase difference $\Delta\phi$ between the two lines (frequency dependency is suppressed for brevity)

$$\Delta\phi = \phi_{LIN} - \phi_{NL} \tag{3}$$

For a given diode nonlinearity, the phase difference $\Delta\phi$ sets the APD amplitude response, while ϕ_{LIN} controls the APD phase response (as described later). Let's now consider a diode with cut-off frequency f_C much higher than the carrier frequency f_0

$$f_C = \frac{1}{2\pi R_S C_T} >> f_0 \tag{4}$$

Here, R_S is the series resistance and C_T is the total capacitance at the diode extrinsic terminals (A-K) defined in Figure 1. We note that the Schottky diode used for this APD has a cut-off frequency of 663 GHz which is much higher than the HPA upper cut-off frequency of 21 GHz.

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The AC equivalent circuit of the series diode is shown in Figure 2. The current balance at the output node is

$$I_D + \frac{V_{IN}^{NL} - V_{OUT}^{NL}}{Z_{C_T}} = \frac{V_{OUT}^{NL}}{Z_0} \tag{5}$$

where $Z_{C_T} = 1/j\omega C_T$. Thus, the output voltage is

$$V_{OUT}^{NL} = \frac{Z_0}{Z_0 + Z_{C_T}} V_{IN}^{NL} + \frac{Z_0 Z_{C_T}}{Z_0 + Z_{C_T}} I_D \tag{6}$$

The diode is described using the exponential model

$$I_D = I_S(e^{\alpha V_D} - 1) \tag{7}$$

Here, I_S is the diode saturation current, α is q/nkT, where q is the electron charge, n is the ideality factor, k is the Boltzmann's constant, and T is the temperature in Kelvin. No junction capacitance is included for simplicity (only the A-K linear capacitance is considered).

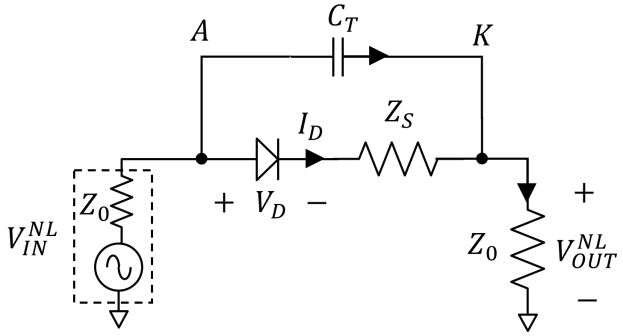

Figure 2. AC equivalent circuit of the nonlinearity in the APD circuit. Highlighted on the circuit are the diode series impedance Z_S and total capacitance C_T between the A-K terminals.

By substituting (7) in (6), we obtain

$$V_{OUT}^{NL} = \frac{Z_0}{Z_0 + Z_{C_T}} V_{IN}^{NL} + \frac{Z_0 Z_{C_T}}{Z_0 + Z_{C_T}} I_S(e^{\alpha V_D} - 1) \tag{8}$$

The diode voltage V_D depends on the DC bias V_{D0} and on the AC voltages and current at its terminals

$$V_D = V_{D0} + V_{IN}^{NL} - V_{OUT}^{NL} - Z_S I_D \tag{9}$$

where $Z_S = R_S + j\omega L_S$. By substituting (5) in (9), we have

$$V_D = V_{D0} + V_{IN}^{NL}\left(1 + \frac{Z_S}{Z_{C_T}}\right) - V_{OUT}^{NL}\left(1 + \frac{Z_S}{Z_0} + \frac{Z_S}{Z_{C_T}}\right) \tag{10}$$

Finally, the linear and nonlinear branches are combined using a perfectly matched, lossless combiner described by

$$V_{OUT} = \frac{V_{OUT}^{LIN}}{\sqrt{2}} + \frac{V_{OUT}^{NL}}{\sqrt{2}} \tag{11}$$

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In summary, the dual-branch series-diode APD model of input V_{IN} and output V_{OUT} can be formulated as follows

$$\begin{cases} V_{OUT}^{LIN} = \dfrac{V_{IN}}{\sqrt{2}} e^{j\phi_{LIN}}, \\ V_{IN}^{NL} = \dfrac{V_{IN}}{\sqrt{2}} e^{j\phi_{NL}}, \\ V_{OUT}^{NL} = \dfrac{Z_0}{Z_0 + Z_{C_T}} V_{IN}^{NL} + \dfrac{Z_0 Z_{C_T}}{Z_0 + Z_{C_T}} I_S (e^{\alpha V_D} - 1), \\ V_D = V_{D0} + \left(1 + \dfrac{Z_S}{Z_{C_T}}\right) V_{IN}^{NL} - \left(1 + \dfrac{Z_S}{Z_0} + \dfrac{Z_S}{Z_{C_T}}\right) V_{OUT}^{NL}, \\ V_{OUT} = \dfrac{V_{OUT}^{LIN}}{\sqrt{2}} + \dfrac{V_{OUT}^{NL}}{\sqrt{2}}. \end{cases} \tag{12}$$

This APD model has been solved numerically considering a maximum input power $P_{IN,MAX} = 20$ dBm at the frequency $f_0 = 19$ GHz (unless specified otherwise). The considered diode parameters are $I_S = 0.2$ pA, $C_T = 40$ fF, $R_S = 6\,\Omega$, $n = 1.2$, and $T = 300$ K (thus $\alpha = 32.2\,V^{-1}$).

2.1. APD Amplitude Range

The theoretical gain characteristics of the proposed APD are shown in Figure 3(a). Indicated on the diagram is the small-signal gain G_{SS}, the large signal gain G_{LS}, and the maximum gain range $\Delta G_{MAX} = G_{LS} - G_{SS}$. Note that for high input powers, the diode generates harmonics that reduce the gain expansion at the fundamental (APD compression).

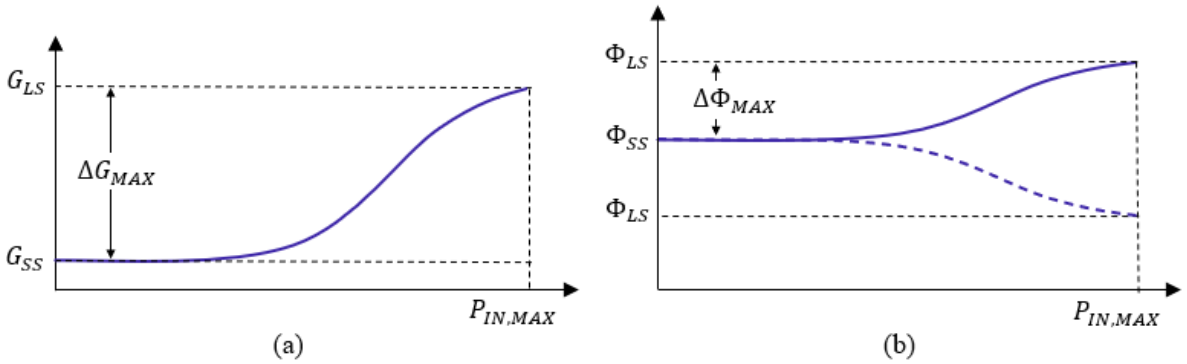

Figure 3. Ideal APD gain (a) and phase (b) vs. input power. Highlighted on the characteristics are the small-signal gain and phase (G_{SS} and ϕ_{SS}), the large-signal gain and phase (G_{LS} and ϕ_{LS}), maximum gain and phase variations (ΔG_{MAX} and $\Delta\Phi_{MAX}$) at the maximum input power $P_{IN,MAX}$.

As anticipated previously, the phase difference $\Delta\phi$ determines the APD gain range and this is demonstrated analytically as follows. Let's assume $C_T = 0$ fF and $Z_S = 0\,\Omega$, the nonlinear branch output voltage (8) reduces to

$$V_{OUT}^{NL} = V_{IN}^{NL} + Z_0 I_S (e^{\alpha V_D} - 1) \tag{13}$$

The exponential can be approximated about $V_{D0} = 0$ V with a Taylor series truncated at the first order,

$$e^{\alpha V_D} \cong 1 + \alpha V_D \tag{14}$$

Therefore, the nonlinear branch output voltage becomes

$$V_{OUT}^{NL} \cong V_{IN}^{NL} + Z_0 I_S \alpha V_D \tag{15}$$

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As the diode voltage is $V_D = V_{IN}^{NL} - V_{OUT}^{NL}$, we have

$$V_{OUT}^{NL} \cong V_{IN}^{NL} + Z_0 I_S \alpha (V_{IN}^{NL} - V_{OUT}^{NL}) \cong V_{IN}^{NL} \tag{16}$$

Therefore the APD output voltage is

$$\begin{aligned} V_{OUT} &\cong \frac{V_{IN}}{2} e^{j\phi_{LIN}} + \frac{V_{IN}}{2} e^{j\phi_{NL}} \\ &\cong \frac{V_{IN}}{2} e^{j\phi_{LIN}} + \frac{V_{IN}}{2} e^{j(\phi_{LIN} - \Delta\phi)} \\ &\cong \frac{V_{IN}}{2} e^{j\phi_{LIN}} (1 + e^{-j\Delta\phi}) \end{aligned} \tag{17}$$

The APD voltage gain amplitude can be written as

$$|G_V| = \left| \frac{V_{OUT}}{V_{IN}} \right| \cong \frac{1}{2} \left| 1 + e^{-j\Delta\phi} \right| \tag{18}$$

This last equation shows that the APD gain is only dependent on the phase difference $\Delta\phi$ between the two branches.

For a more precise evaluation of the gain variation with $\Delta\phi$, the diode nonlinearity needs to be included by solving the APD model (12) and this results in Figure 4(Left). The small- and large-signal losses are minimized for $\Delta\phi$ between $-90°$ and $0°$ and their difference is due to the non-linear phase shift introduced by the diode. The gain variation ΔG_{MAX}, usually optimized for maximum APD+HPA improvement, presents a maximum of 4.8 dB for $\Delta\phi = 84° \pm k360°$. If the system requirements mandate minimizing APD large-signal losses instead of range, a choice of $-6°$ is suggested for this diode.

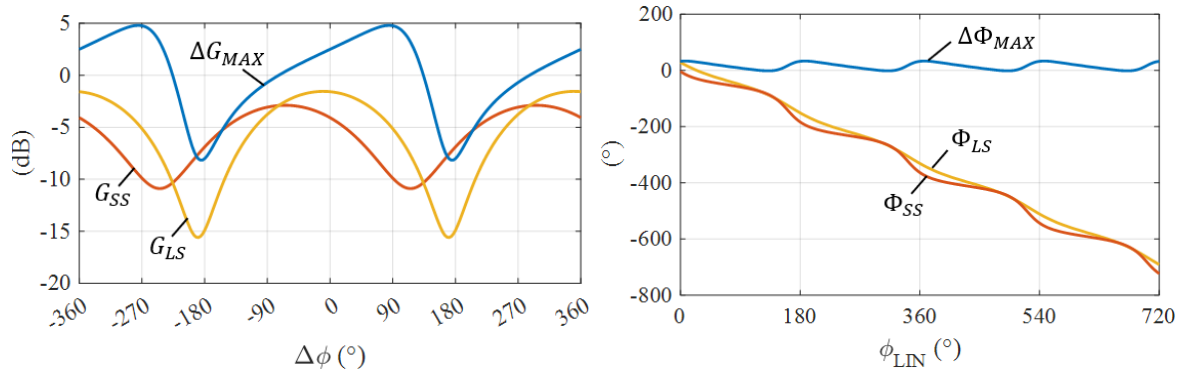

Figure 4. Left: Small-signal gain G_{SS}, large-signal gain G_{LS}, and gain variation ΔG_{MAX} vs. phase difference $\Delta\phi$. Right: Small-signal phase Φ_{SS}, large-signal phase Φ_{LS}, and maximum phase variation $\Delta\Phi_{MAX}$ vs. linear branch phase ϕ_{LIN} for a set $\Delta\phi = 84°$.

2.2. APD Phase Range

The theoretical phase characteristics of the proposed APD are shown in Figure 3(b). Indicated on the diagram are the small-signal phase Φ_{SS}, the large-signal phase Φ_{LS}, and the maximum phase range $\Delta\Phi_{MAX} = \Phi_{LS} - \Phi_{SS}$. Note that for high input powers, the diode generates harmonics that reduce the phase expansion at the fundamental (APD compression). The linear branch phase ϕ_{LIN} can be used to control the APD phase range. This is demonstrated by using (17) to calculate the phase

$$\angle G_V = \angle V_{OUT} - \angle V_{IN} = \phi_{LIN} + \angle (1 + e^{-j\Delta\phi}) \tag{19}$$

Given a fixed $\Delta\phi$ that sets the amplitude range, this equation shows that ϕ_{LIN} can be used to tune the APD phase variation.

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The APD phase at small-signal, large-signal, and overall phase range are evaluated by solving the APD model (12). Figure 4(Right) shows that the phase variation reaches a maximum of 33.2° at $\phi_{LIN} = 9° + k180°$. Periodic multiples of ϕ_{LIN} will lead to a lower APD bandwidth so we recommend keeping it at a minimum to interconnect the components. We also note that most HPAs require a phase rotation of $\pm 10°/15°$, e.g. [18], and so a different ϕ_{LIN} may be chosen to match the APD to a specific HPA phase range.

It is interesting to note that depending on $\Delta\phi$ and ϕ_{LIN} choices, (19) shows that it is possible to generate a negative, neutral, or positive phase rotation depending on the sign of the two terms. This feature is demonstrated by solving the APD model and results in Figure 5 (constant amplitude shape in a dashed line). For all these characteristics, $\Delta\phi = 63°$ and ϕ_{LIN} is varied to achieve a negative, neutral, and positive phase variation, Figure 5(a)-(c).

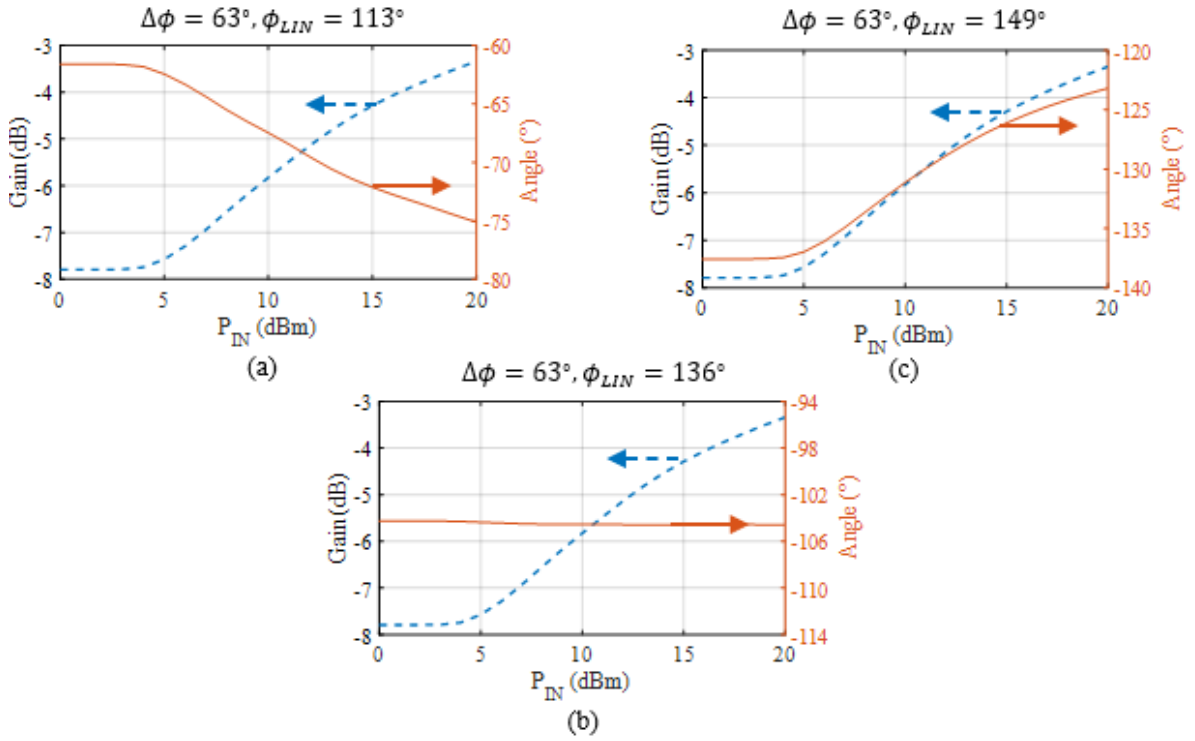

Figure 5. APD gain and phase for a fixed $\Delta\phi$ setting the amplitude variation. Depending on the ϕ_{LIN} choice, this APD can realize a negative (a), neutral (b), and positive (c) phase variation.

2.3. Impact of Diode Capacitance on APD Characteristics

The diode total capacitance C_T has the effect of reducing the APD amplitude (and phase) range. This is demonstrated analytically by simplifying the APD model (12) as follows. In the small-signal region, the diode is off and $I_D = -I_S \cong 0$. So, the nonlinear branch output voltage reduces to

$$V_{OUT}^{NL} = \frac{Z_0}{Z_0 + Z_{C_T}} V_{IN}^{NL} \tag{20}$$

where $Z_{C_T} = 1/j\omega C_T$. The APD output voltage becomes

$$V_{OUT} = \frac{V_{IN}}{2} e^{j\phi_{LIN}} + \frac{Z_0}{Z_0 + Z_{C_T}} \frac{V_{IN}}{2} e^{j(\phi_{LIN} - \Delta\phi)} \tag{21}$$

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Therefore, the APD voltage gain amplitude is

$$|G_V| = \left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{1}{2}\left|1 + \frac{Z_0 e^{-j\Delta\phi}}{Z_0 + 1/j\omega C_T}\right| \tag{22}$$

This last equation captures the fact that for $C_T = 0$ fF, $|1/j\omega C_T| \to \infty$ and $|V_{OUT}| = |V_{IN}|/2$ or $P_{OUT} = P_{IN}/4$, and so the APD loses 6 dB. As C_T increases, more power passes through the nonlinear branch which reduces the APD amplitude (and phase) range. This is demonstrated in Figure 6(Left) by solving numerically the full APD model.

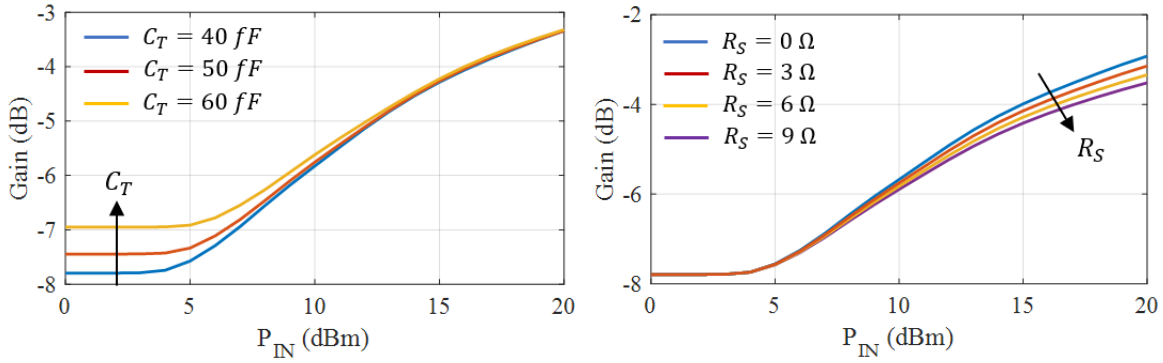

Figure 6. Left: Gain variation vs. P_{IN} for different total capacitances C_T. Right: Gain variation vs. P_{IN} for different series resistance R_S.

2.4. Impact of Diode Series Resistance on APD Characteristics

The diode series resistance R_S has the effect of reducing the diode current as it introduces negative feedback in the exponent of the diode equation. This leads to a reduction in the APD gain (and phase) slope steepness. Assume a diode total capacitance $C_T = 0$ fF and series inductance $L_S = 0$ pH, the diode equation simplifies to

$$\begin{cases} V_{OUT}^{NL} = Z_0 I_S (e^{\alpha V_D} - 1) \\ V_D = V_{D0} + V_{IN}^{NL} - V_{OUT}^{NL}\left(1 + \dfrac{R_S}{Z_0}\right) \end{cases} \tag{23}$$

By calculating the derivative of V_{OUT}^{NL} with respect to R_S, we can study the APD sensitivity to varying R_S as follows

$$\frac{dV_{OUT}^{NL}}{dR_S} = -I_S e^{\alpha V_D} \alpha V_{OUT}^{NL} \tag{24}$$

Noting that the first equation of (23) can be recursively substituted here, we have

$$\begin{aligned} \frac{dV_{OUT}^{NL}}{dR_S} &= -\alpha (V_{OUT}^{NL} + Z_0 I_S)\frac{V_{OUT}^{NL}}{Z_0} \\ &= -\alpha I_S V_{OUT}^{NL} - \frac{\alpha}{Z_0} {V_{OUT}^{NL}}^2 \end{aligned} \tag{25}$$

As I_S is generally in the nA-pA range, the linear term can be neglected. Thus, the nonlinear branch sensitivity to R_S is

$$\frac{dV_{OUT}^{NL}}{dR_S} \cong -\frac{\alpha}{Z_0} {V_{OUT}^{NL}}^2 \tag{26}$$

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Given this negative sign, increasing R_S has the effect of reducing the APD amplitude (and phase) slope steepness, especially at higher voltages given the quadratic dependence. Figure 6(Right) demonstrates numerically this conclusion by solving the APD model.

2.5. Impact of Diode Ideality Factor on APD Characteristics

The diode ideality factor n has the effect of shifting the APD turn-on "knee". This is demonstrated analytically by simplifying (12) as follows. Assume $Z_S = 0\,\Omega$ and $C_T = 0\,$fF, the sensitivity of the nonlinear output voltage to n is the derivative with respect to n of the first equation in (23), namely

$$\frac{dV_{OUT}^{NL}}{dn} = -Z_0 I_S e^{\alpha V_D} \frac{qV_D}{n^2 kT} \tag{27}$$

Noting that the first equation in (23) can be recursively substituted here, we have

$$\frac{dV_{OUT}^{NL}}{dn} = -(V_{OUT}^{NL} + Z_0 I_S) \frac{qV_D}{n^2 kT} \tag{28}$$

As I_S is generally in the nA or pA range, the term $Z_0 I_S$ is neglected. Assuming a lossless diode ($V_D = V_{D0}$), we have

$$\frac{dV_{OUT}^{NL}}{dn} \cong -V_{OUT}^{NL} \frac{qV_{D0}}{n^2 kT} \tag{29}$$

This equation shows that increasing ideality factors n has the effect of "reducing" the APD amplitude characteristic. This concept is also visible in Figure 7 which is obtained by solving numerically the APD model for $n = [1, 1.2, 1.4, 1.6]$.

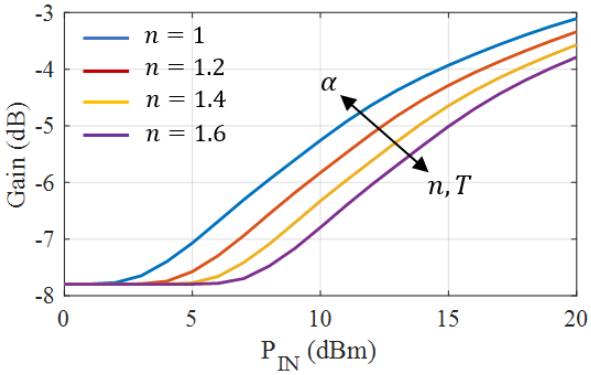

Figure 7. Gain variation vs. P_{IN} for different ideality factor n. Lower ideality factors have the effect of shifting the APD amplitude turn-on "knee".

We note that a similar derivation to (29) can be performed for the temperature T. Temperature drifts have the same effect of changing the ideality factor n.

Equation (29) also suggests the possibility of tuning the diode bias V_{D0} to compensate for temperature effects or to change the turn-on "knee" of the diode.

2.6. Model Validation

In this section, the large-signal measurements of Section 4 are used to validate the APD model (12). Figure 8 shows measured vs. modeled APD gain at 15 and 21 GHz and for the biases $V_{D0} = [-0.5, 0, 0.5]$ V. For this comparison, the diode capacitance and resistance have been slightly varied from the nominal values ($C_T = 40$ fF and $R_S = 6\,\Omega$) to $C_T = 58$ fF and $R_S = 10\,\Omega$, while n and I_S are the same.

An increased diode capacitance can be due to the lack in the APD model of the diode junction capacitance (10 fF at $V_J = 0$ V) and because of the added coupling in the APD board. As for the

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resistance, the diode manufacturer provides a resistance range of 7-9 Ω in the datasheet [19], thus justifying a slight increase in R_S. The additional resistance can be due to the diode pads.

Also, the diode biases have been slightly adjusted (±0.2 V) to match the measurement results, and this is possibly due to mismatches introduced by a real Wilkinson splitter that is not considered in the model. These mismatches will in fact reduce the diode drive and therefore the modeled diode threshold does not correspond to the measured one. Given these adjustments, the APD model well predicts the measured APD characteristics at the two frequency edges (15 and 21 GHz) and for varying diode biases as shown in Figure 8.

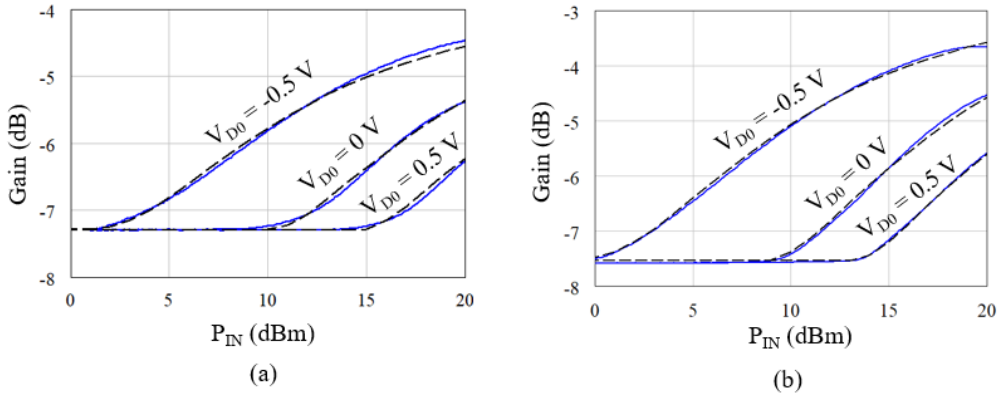

Figure 8. Measured (blue) vs. modeled (dashed) APD gain at 15 GHz (a) and 21 GHz (b) for different diode biases. The APD model fits the measured data on a broad frequency range, for different diode biases and input powers.

2.7. Diode Selection

The APD model can be used to quickly evaluate different diodes before proceeding with the circuit design. Given the K-band operating frequency of the HPA, GaAs Schottky diodes are preferred to other technologies for their lower parasitic. After a component search, two commercial GaAs Schottky diodes have been identified and their parameters are reported in Table 1. Both diodes achieve a 7 V breakdown voltage (BV) and a high cut-off frequency f_C of several hundred GHz. The difference between these diodes is that Diode 1 has a lower n ($n = 1$ is an ideal diode), a higher series resistance R_S, and a lower capacitance C_T.

Table 1. GaAs Diode Comparison

Diode ID	BV	I_S	n	R_S	C_T	f_C
Diode 1	7 V	0.2 pA	1.2	6 Ω	40 fF	663 GHz
Diode 2	7 V	3.0 pA	1.4	4 Ω	50 fF	795 GHz

* Data obtained from the diode manufacturer.

Figure 9 shows the APD model gain and phase response for the two diodes. Diode 1 has a wider amplitude expansion (1 dB more than Diode 2) and a wider phase variation (7° more than Diode 2), mainly because of its lower total capacitance C_T, as discussed in Section 2.3. The lower R_S of Diode 2 provides a small improvement in the amplitude steepness at higher input powers that is insufficient to compensate for the higher C_T.

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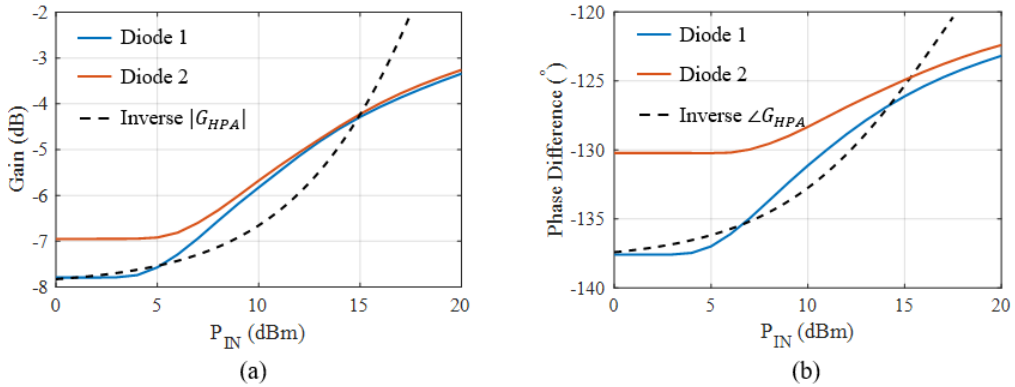

Figure 9. Inverted gain (a) and phase (b) of the HPA at 19 GHz. Superposed is the APD model response for Diode 1 and 2. Diode 1 approximates the HPA characteristics on a wider range than Diode 2 thus suggesting higher linearity and efficiency improvements with this diode.

On the same plot, the inverted characteristics of the HPA are reported. At 19 GHz, the HPA was measured up to 6 dB and 17° into compression. As can be seen, the APD realized with Diode 1 can fit on a wider range of the HPA gain and phase response, thus suggesting higher HPA linearity, output power, and efficiency improvements with this diode.

3. Diode Modelling for APD Design

This section discusses the modeling, extraction procedure, and validation of the APD diode nonlinearity. An accurate model for the nonlinearity plays an important role in the design of the APD circuit, however, not many models capable of operation at high frequencies are available, especially for high-performance GaAs Schottky diodes.

Some academic research in this direction has been recently conducted by [20] for Diode 2 which however resulted in lower performance in our comparison. In [20], the procedure was validated up to 18 GHz and it employs bond-wiring of the diode to the access lines, which is not suitable for this application given the bond-wire inductance that would reduce the APD amplitude and phase range.

3.1. Diode Characterization

The diode is characterized on the same substrate used for fabricating the APD circuit. A Rogers 3003 substrate with a relative dielectric constant $\epsilon_r = 3$, a height of 127 μm, and a copper thickness of 17 μm is used. With this substrate, the 50 Ω line width is 303 μm which is well matched with the diode width of 330 μm. For the characterization, the diode is mounted in a series configuration with 5 mm access lines on each side. A series configuration is preferred to the shunt configuration to avoid performance deterioration due to the via-hole inductance.

An Anritsu 3680K test fixture is utilized to provide 2.92 mm connectors to the diode fixture as shown in Figure 10(a). The diode bias is applied with two bias-Ts (HP 11612A). The anode bias-T provides a positive or negative bias while the cathode bias-T provides a ground connection. These bias-Ts are connected to a 26.5 GHz PNA-X (Keysight N5242A).

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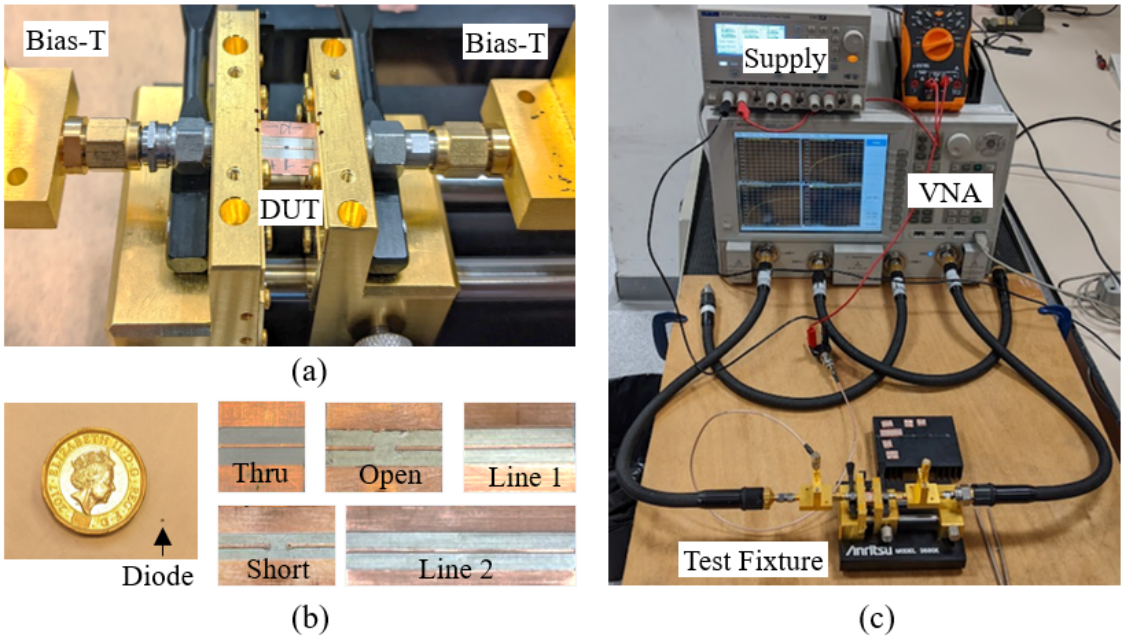

Figure 10. (a) Diode fixture mounted on the test jig with bias-Ts. (b) Two-line TRL calibration kit. (c) Photo of the setup to characterize the diode and APD.

A Thru-Reflect-Line (TRL) calibration kit based on the Rogers 3003 substrate is realized as shown in Figure 10(b). For this kit, the frequency range is 1 to 26.5 GHz (upper-frequency limit of the VNA) and results in the requirements of two 90° lines. The first line is 15.8 mm long and is 90° at 3.07 GHz and covers the frequency range from 1 GHz (29.7°) and 5.15 GHz (152°). The second line is 3.1 mm long and is 90° at 15.8 GHz and covers the frequency range from 5.15 GHz (29.5°) to 26.5 GHz (152°). These lines, therefore, are within the 0-180° limit. A TRL de-embedding algorithm is then used to calibrate at the A-K diode reference planes and remove the effects of the diode pads. Figure 10(c) shows the test setup used for this characterization.

3.2. Diode Modelling

For simplicity's sake, the diode description used for the APD model does not account for the nonlinear junction capacitance as this is typically smaller than the total capacitance C_T (10 fF vs. 40 fF). For the APD design, the diode junction capacitance C_J is described by

$$C_J = C_{J0}\left(1 - \frac{V_D}{V_J}\right)^{-M} \tag{30}$$

The zero-bias junction capacitance is $C_{J0} = 10$ fF and the junction grading coefficient is $M = 0.25$. With these parameters, a Spice diode model is created in AWR.

Figure 11 shows the measured vs. simulated I/V characteristic at room temperature and in static bias conditions. Good agreement is found between the two samples and the model. At higher dissipations, a slight deviation in the current can be caused by self-heating given the high thermal resistance of the diode 0201 die. For these measurements, the cable and bias-T resistances ($2 \cdot 0.5\,\Omega$ for the two HP 11612A bias-Ts) have been de-embedded.

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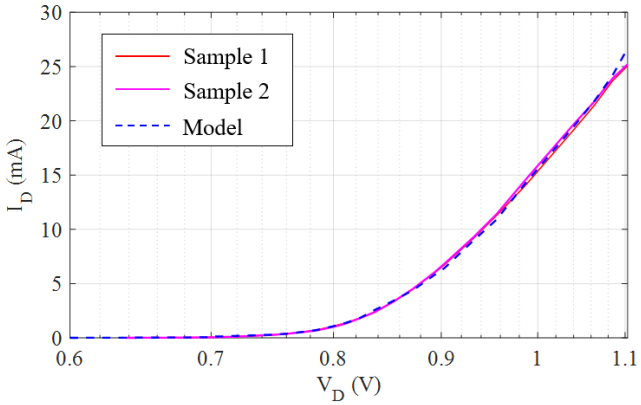

Figure 11. Measured (solid) and modeled (dashed) I/V of two Diode 1 samples.

The diode access lines are also included in the model. As the diode is fabricated on a GaAs substrate of dielectric constant $\epsilon_r = 12.9$, thickness of 203 μm, and $\tan\delta = 0.00056$, the diode access lines are modeled in MWO with MTAPER and MLIN elements with geometries indicated in Figure 12.

The measured vs. simulated S-parameters are shown in Figure 13 for three biases and two samples. To aid the match between simulations and measurements, a shunt capacitor at the pin A and K is placed to simulate the substrate coupling with the diode. We note this coupling will also be present in the APD circuit as it employs the same diode and substrate. As it can be seen in the S-parameter plots, a good agreement is found between the model and measurements from 1 to 26.5 GHz.

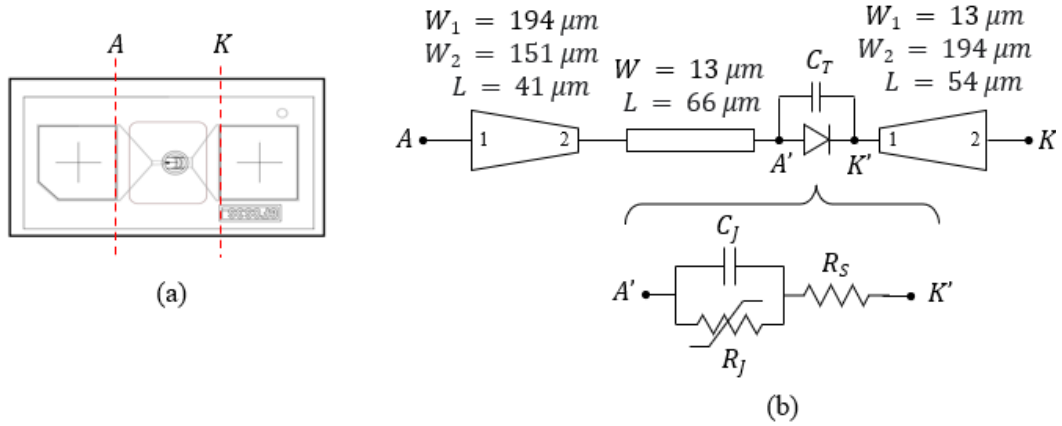

Figure 12. (a) Diode layout [19] with reference planes. (b) Diode equivalent circuit with parasitic network realized with lumped and distributed elements.

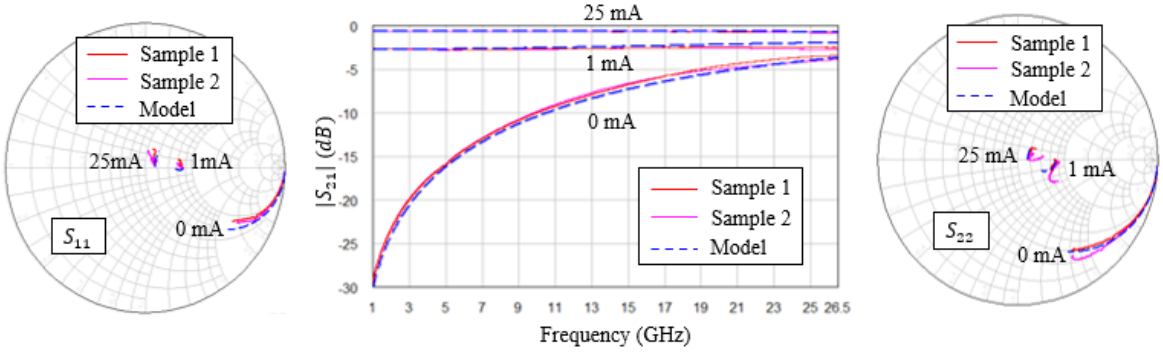

Figure 13. Measured (solid) and modeled (dashed) diode S_{11} and S_{22} (a), and $|S_{21}|$ (b) between 1 GHz and 26.5 GHz and for 0, 1, 25 mA bias current.

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4. Linearizer Design and Characterization

Using the diode model of Section 3, the APD circuit is designed in AWR. The nonlinear branch uses the Schottky diode mounted in a series configuration and connected to a line of 303 μm width. The diode bias is provided by two $\lambda/4$ lines of 200 μm width and 3.64 mm length. The DC bias is removed by two 0201 DC block capacitors of 22 pF (Knowles CSB-140-20x10x4-5-G-220-M) with 50 GHz self-resonance frequency.

The transmission line in the linear branch is 10.3 mm long or $\phi_{LIN} = 363°$ at 19 GHz, while the line in the nonlinear branch is 8.4 mm long or $\phi_{NL} = 283°$ at 19 GHz. Therefore, a phase difference of $\Delta\phi = 80°$ at 19 GHz is introduced. The two branches are connected to a Wilkinson splitter and combiner, with the 100 Ω isolation resistor realized with a 0402 resistor with high self-resonance frequency. The circuit layout is electro-magnetically simulated with AWR Axiem. The diode DC bypass capacitors and bias lines have been optimized to provide a good baseband termination in the video bandwidth of the APD circuit. The layout of the circuit is shown in Figure 14.

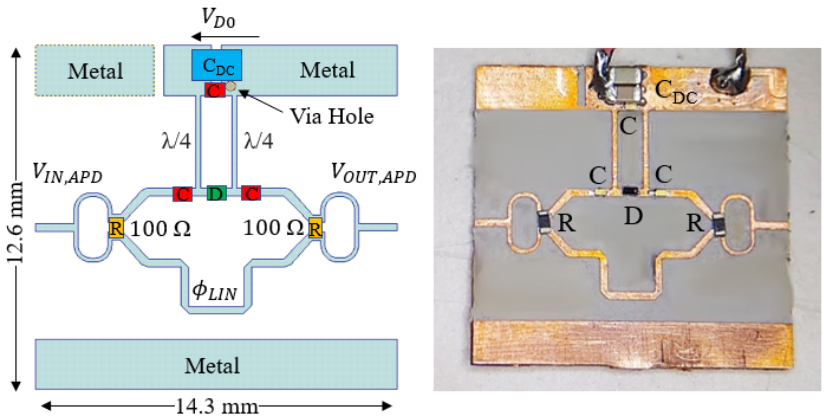

Figure 14. Layout (left) and photo (right) of the APD prototype.

The APD gain is simulated over a large frequency range (10-26 GHz) and for various input powers between -10 and 20 dBm at steps of 2 dB, Figure 15(Left). The designed APD circuit exhibits a large signal bandwidth between 16 and 25 GHz (9 GHz) corresponding to a fractional bandwidth of 44 %. At the lower end, this bandwidth is limited by the bias line resonance. Going towards higher frequencies the gain expansion is reduced by the diode total capacitance C_T, as discussed in Section 2.

The APD gain amplitude and phase tuning range at 19 GHz are evaluated for diode bias voltages between -0.3 and 0.3 V at steps of 0.1 V and the results of these simulations are reported in Figure 15(Right). The diode bias voltage changes the APD small-signal response because of the dependency of $C_J(V_D)$ as in (30). This variation can be easily compensated by the APD post-amplifier. When the diode bias increases, the APD "knee" amplitude and phase move towards higher powers.

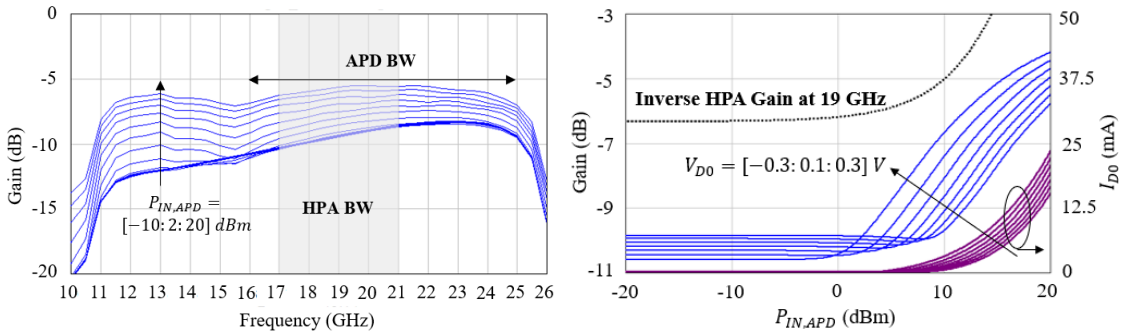

Figure 15. Left: Simulation between 10-26 GHz of the APD circuit for varying input powers and $V_{D0} = 0$ V. The HPA and APD bandwidths are indicated on the plot. Right: Simulated APD gain vs. input power for varying V_{D0}. Superposed are the inverted HPA characteristics and diode DC current.

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Finally, the APD diode voltage is simulated in Figure 16 at the upper-frequency edge of the HPA bandwidth ($f_0 = 21$ GHz) to verify that the diode voltage is not exceeding the 7 V breakdown of Diode 1 [19]. Note that peak voltages are within 75 % voltage derating typically used for space applications [21].

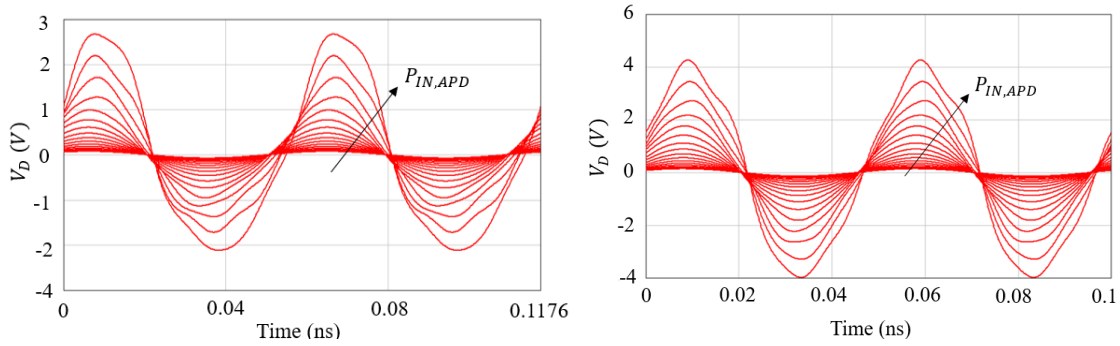

Figure 16. Simulated AC voltage across the diode at 17 GHz (Left) and 20 GHz (Right) for varying input powers. The voltage peaks are below the 7 V diode breakdown voltage.

4.1. Simulated APD with Measured HPA-in-the-Loop

Before proceeding with the fabrication of the APD circuit, the simulated APD linearizer is evaluated with the actual HPA at 19 GHz using the following procedure:

1. A simulation with an amplitude-modulated sine wave at the APD input is performed to generate the pre-distorted signal, Figure 17(a). This simulation is a time-domain harmonic balance (APLAC Transient in MWO);
2. The pre-distorted signal is transferred to the measurement setup and is then applied to the HPA input. An optimal diode bias of $V_{D0} = -0.67$ V is found by iterating between 1) and 2). For $V_D = -0.67$ V, the APD+HPA output amplitude approximates the ideal sine wave amplitude, Figure 17(b).
3. The HPA gain with and without simulated APD is computed and reported in Figure 17(c). As can be seen, the small-signal gain with APD at 19 GHz is reduced by approximately 4 dB while at large signal APD reduces the HPA gain compression (hence less distortion) for the same maximum output power.

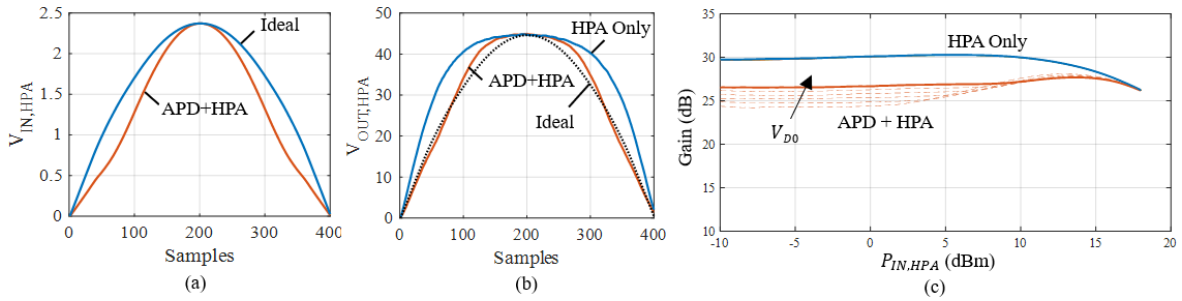

Figure 17. (a) Simulated APD input and output signal. (b) Measured HPA output signal without and with simulated APD. (c) Measured HPA gain with simulated APD for different bias voltages. An optimal bias voltage that ensures maximum gain flatness is found before fabricating the APD circuit.

4.2. Small- and Large-Signal APD Characterization

Using the Keysight PNA-X vector network analyzer N5242A of Figure 10(c), the S-parameters of the APD circuits were first measured for different diode biases and result in Figure 18. A positive diode bias was used to simulate the diode turn-on that is caused by the RF input power and so verify the correct APD operation. As shown by Figure 18, the APD input $|S_{11}|$ improves from about

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-7 to -15 dB as the diode is turned on. Thanks to the input Wilkinson divider, an acceptable input match is maintained even when the diode is off, thus avoiding the need to introduce bulky and bandwidth-limiting isolators.

As for the APD gain, the $|S_{21}|$ reduces for positive diode biases thus providing an expanding gain characteristic. This measurement also confirms the simulation results shown in Figure 15 with good approximation especially when the diode is fully on. From these small-signal measurements, a usable -1 dB bandwidth for this linearizer of 14-24 GHz is observed. As for the APD phase, the $\angle S_{21}$ reduces for increasing input biases, as shown in the zoomed box of Figure 18.

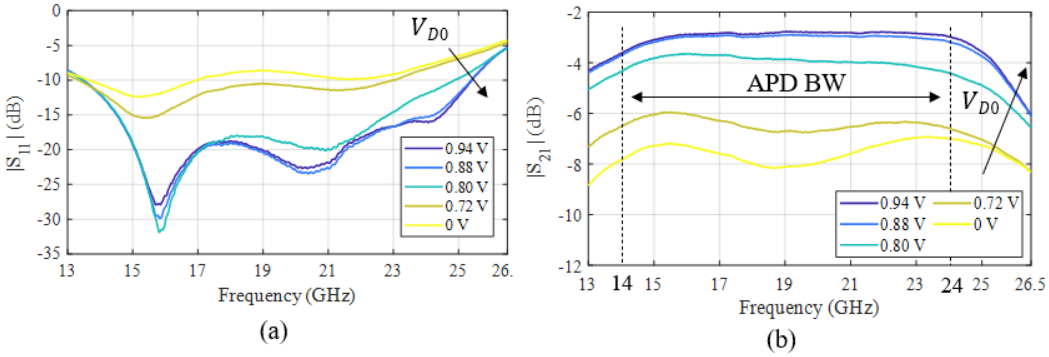

Figure 18. Measured $|S_{11}|$ (left) and $|S_{21}|$ (right) for varying V_{D0} (to simulate the expanding APD characteristic caused by the RF power).

A large-signal setup based on the Keysight PNA-X and booster/driver amplifier (Keysight/HP 83020A) is used to characterize the APD with input powers up to 20 dBm. A bi-directional coupler is placed after the driver to sense the incident and reflected voltage waves at the APD input, and a 30 dB attenuator is used at the APD output to prevent accidental overdrive of the PNA-X receivers. Power calibration is performed at the APD reference planes across the bandwidth. Figure 19 shows the APD characteristics for $V_{D0} = 0$ V. These measurements confirm the simulated large signal bandwidth of 6 GHz. The same large-signal setup is used to measure the APD characteristics at different biases and frequencies of Figure 8 which are used for APD model validation discussed in Section 2.6.

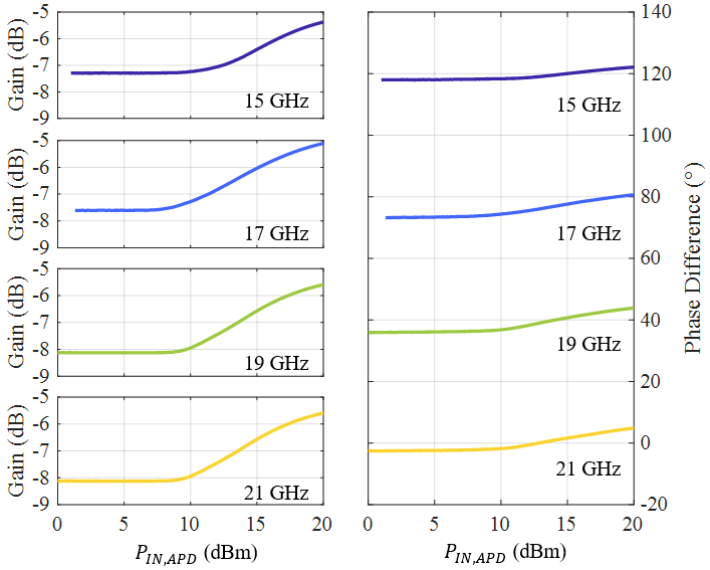

Figure 19. Measured large-signal APD gain (left) and phase (right) between 15 and 21 GHz. For these measurements, the diode bias is $V_{D0} = 0$ V.

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5. APD-HPA Performance Evaluation

The APD circuit is specifically designed to correct the amplitude and phase variation (see Figure 9) of a 3-stage HPA from UMS (CHA8252-99F [3]). This HPA is realized with the UMS 0.15 μm GaN-on-SiC process and can provide ~10 W output power with more than 35 % PAE in the 17-21 GHz band. The three stages of this class-AB HPA are biased at 18 V and 308 mA and provide a small signal gain between 28.5-31.5 dB across the band. The HPA efficiency, however, rapidly decreases when the HPA is backed off. For example, at 10 dB back off, the PAE at 19 GHz is only 10-12 % [3]. The HPA MMIC is mounted on a test fixture providing 2.92 mm connectors and DC bypassing (up to 1 μF).

5.1. Wideband Measurement Setup

The measurement setup of Figure 20 is built to measure the HPA with and without APD. An arbitrary waveform generator (AWG, Keysight M8190A) generates two analog I/Q differential signals that modulate the input of a wideband RF source (Keysight E8267D) capable of 1.2 GHz instantaneous bandwidth. The RF source output signal is amplified by a 13-26.5 GHz driver amplifier (Mini-Circuits ZVM-273HP+) up to 20 dBm necessary to excite the APD nonlinearity.

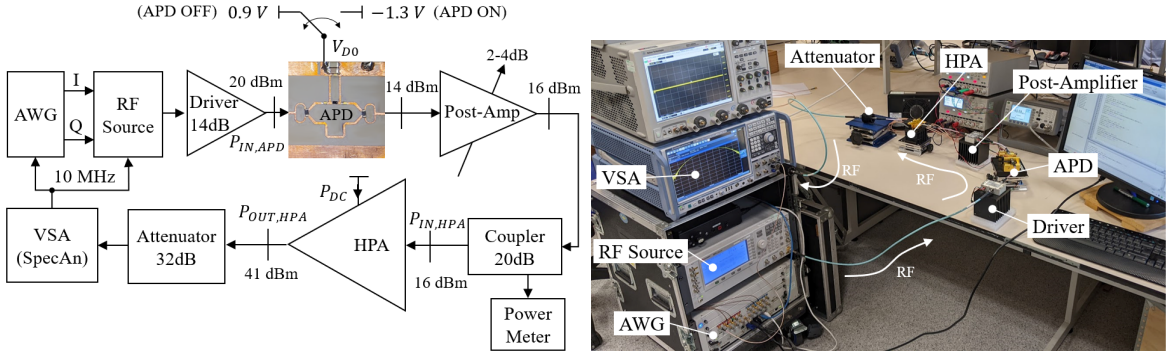

Figure 20. Left: Block diagram of the wideband setup. Right: Photo of the setup.

Depending on the carrier frequency, the APD attenuates by 5-6 dB when the APD input power is 20 dBm, Figure 19. To recover this loss, a post-amplifier (variable attenuator + Mini-Circuits ZVM-273HP+) is introduced to restore the HPA drive of 16 dBm. This power is sensed by a power meter connected to a coupler at the HPA input. The signal is then amplified by the HPA up to 41 dBm. A 32 dB attenuator is connected between the HPA and a vector signal analyzer (VSA, Rohde & Schwartz FSW43) with 1.2 GHz bandwidth.

Scalar calibration of the setup is performed between 17-21 GHz. First, the setup input gain is measured by turning off the APD ($V_{D0} = 0.9$ V) and by measuring the power difference between the HPA input and RF source output. The calibration factors at $f_0 = [17.5, 19.0, 20.5]$ GHz are $\Delta G_{IN}(f) = [0.2, 0.0, 0.9]$ dB. Subsequently, the setup output attenuation is measured by replacing the HPA with a 2.92 mm “thru" connector and then by measuring the power difference between the HPA output and the VSA input. The calibration factors at $f_0 = [17.5, 19.0, 20.5]$ GHz are $\Delta A_{OUT} = [0.3, 0, -0.2]$ dB. For both input and output calibration factors, the gain and attenuation at 19 GHz (central value) have been set as a reference, hence the 0 dB correction. To achieve precise NPR measurements, the DC offset was calibrated by changing the RF source I/Q offset voltages to cancel out the leaking tone.

5.2. Perfomance With APD

The next step is finding the diode bias voltages that ensure maximum gain and phase flatness. This is achieved by sweeping the diode biases with a narrowband Gaussian pulse [22] at 19 GHz as shown in Figure 21. As the diode bias becomes more negative, the APD+HPA combined response starts to flatten in the backoff region and then reaches the compression where APD expansion and HPA compression cancel out thus realizing an extended linear power range. As shown in Figure 21, for $V_{D0} = -1.3$ V

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the APD+HPA presents less than 2 dB compression for the same output power whereas when the APD is not used, the compression is over 6 dB. Similar results can be found for the phase where the APD reduces the variation by 5° (−11° without APD and +6° with APD). This tuning has also been performed for each of the three considered frequencies and results in $V_{D0} = [-1.4, -1.3, -1.4]$ V for $f_0 = [17.5, 19.0, 20.5]$ GHz.

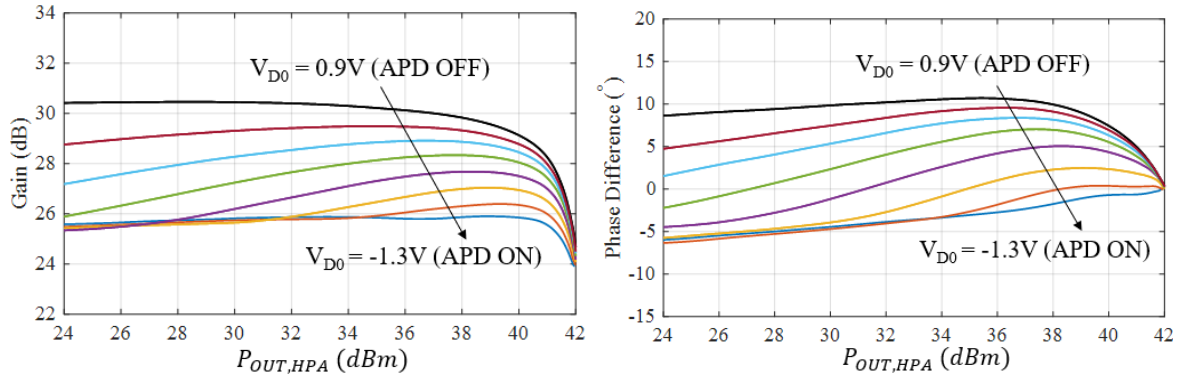

Figure 21. Pulsed gain and phase at 19 GHz for different diode biases.

A noise-like wideband signal is generated using the multi-signal algorithm of [23]. The algorithm has been configured to generate a signal with $B = 750$ MHz bandwidth, a $B_N = 50$ MHz notch bandwidth in the middle for NPR measurements, and a PAPR of 12 dB. In this way, it is possible to simulate a noise-like signal of 140 carriers as needed by the application (DOCSIS 3.0 channel of 5 MHz bandwidth, spaced 5 MHz apart). With this spectrum, the noise-power ratio (NPR) is measured using the following definition

$$\text{NPR (dB)} = -10 \log \frac{\int_{B_N} P_{OUT,HPA}(f)df}{\int_{B} P_{OUT,HPA}(f)df} \tag{31}$$

The NPR has been evaluated without and with APD to evaluate the APD benefit and results are shown in Figure 22. For these measurements, the diode bias has been adjusted to the optimal values of $V_{D0} = [-1.4, -1.3, -1.4]$ V at $f_0 = [17.5, 19.0, 20.5]$ GHz. As APD linearization operates by reducing the backoff gain, the signal average output power changes when APD is introduced. To provide a fair comparison between the HPA-only case (APD disabled) and the APD+HPA case (APD enabled), the average output power has been adjusted to be the same as the HPA-only case. For these measurements, the NPR improves by $[-7.2, -8.2, -6.5]$ dB for the same 750 MHz signal at $f_0 = [17.5, 19.0, 20.5]$ GHz. As for the ACPR, given the large bandwidth of the considered signal (750 MHz) and the setup bandwidth of 1.2 GHz, it was not possible to fully capture the sides of the spectrum. This is also not necessary as the application (cable modem with DOCSIS signal) does not pose ACPR requirements.

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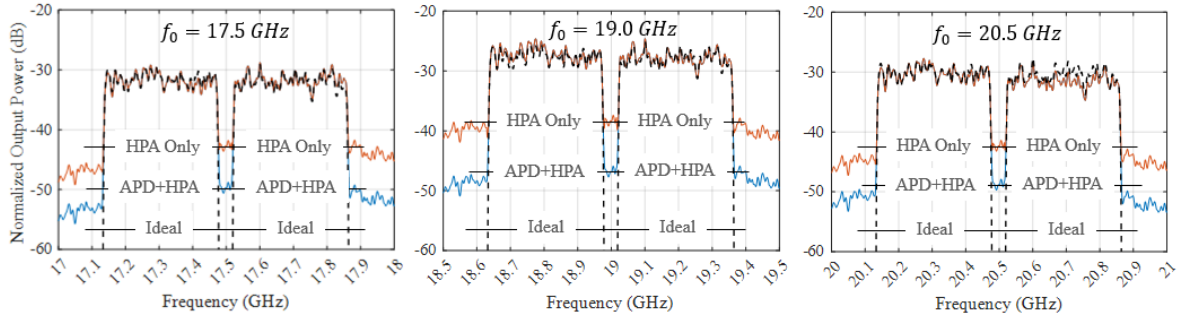

Figure 22. Measured HPA output spectrum for the same 750 MHz signal without APD (brown), with APD (blue), and ideal response (black). NPR improves between 6.5-8.2 dB over the 4 GHz HPA bandwidth while maintaining the same average output power.

Next, the signal average has been swept to compare the case without and with APD over the bandwidth, Figure 23. In this plot, a scale has been added on the top x-axis reporting the measured average HPA efficiency for each average output power. For NPRs around 30 dB, the APD benefit is limited by the noise floor. For NPRs below 15 dB, the APD is limited by the HPA compression. For NPRs between 30 and 15 dB, APD allows for improved HPA output power and efficiency over the whole frequency range. Improvements are the highest for NPR $>$ 30 dB and they decrease for higher output powers as the APD is not able to recover the HPA hard compression.

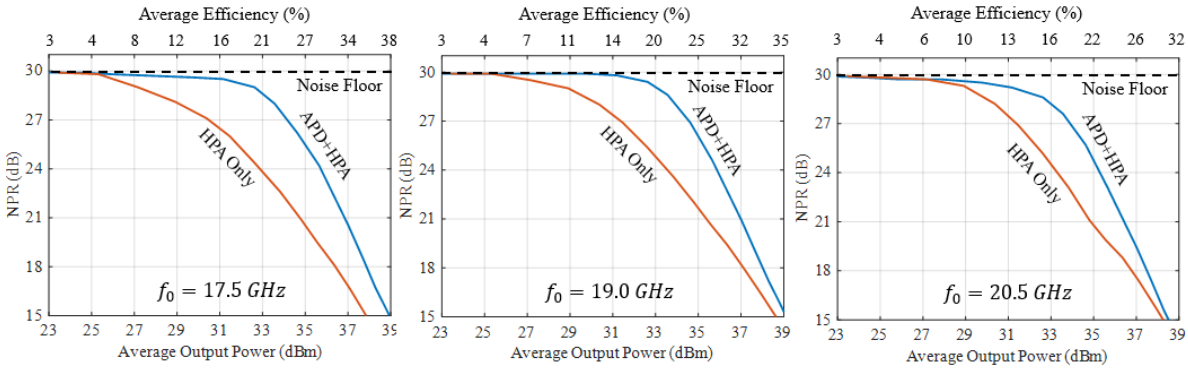

Figure 23. Measured NPR, average output power, and average efficiency for the same 750 MHz signal at different backoff powers. For the same NPR, APD improves the HPA average output power by 1-2 W and the average efficiency by 5-9 %.

5.3. Estimated APD+HPA Efficiency Including Post-Amplifier

In this section, the power consumption due to APD is estimated with the data available on commercial amplifiers compatible with the 17-21 GHz frequency range and power level to drive the HPA (approximately 17 dBm). At these powers and frequencies, GaAs MMICs are commonly used; for example [24–26] present DC power consumptions between 0.7-1 W, and achieve a gain of 23 dB, thus requiring insertion of an attenuator as the APD loss is only 5-6 dB. For 5-6 dB gain at K-band, a single-stage GaAs amplifier should suffice and also result in a lower power consumption.

The overall efficiency improvement obtained with APD can be quantified using the following formula

$$\eta_D = \frac{P_{OUT,HPA}}{P_{DC,HPA} + P_{DC,PostAmp}} \tag{32}$$

As the DC power consumed by the APD block is practically zero (there is a small rectified current by the diode which is however less than a few mA on avarage), the main power consumption caused by APD is due to the post-amplifier, $P_{DC,PostAmp}$. Assuming a driver stage of [25] which achieves 21 dBm output power (OIP3 of 33 dBm) and draws 0.7 W, Table 2 reports the estimated efficiency

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including the driver stage. For NPRs of 28, 24, and 20 dB, the introduction of the post-amplifier reduces the APD+HPA efficiency by only about 1-2 %, thus suggesting the viability of APD for overall efficiency and power increase for this HPA.

Table 2. Efficiency Without and With APD Including Post-Amplifier Consumption

Case	NPR	Frequency	$P_{OUT,HPA}$	$P_{DC,HPA}$	$P_{DC,APD}$	$\eta_{D,HPA}$	$\eta_{D,HPA+APD}$
HPA Only	28 dB	19 GHz	31.0 dBm	9.0 W	-	14 %	14 %
APD + HPA	28 dB	19 GHz	34.2 dBm	11.4 W	0.7 W	23 %	22 %
HPA Only	24 dB	19 GHz	33.5 dBm	10.7 W	-	21 %	21 %
APD + HPA	24 dB	19 GHz	36.0 dBm	13.7 W	0.7 W	29 %	27 %
HPA Only	20 dB	19 GHz	35.8 dBm	14.1 W	-	27 %	27 %
APD + HPA	20 dB	19 GHz	37.1 dBm	15.9 W	0.7 W	32 %	31 %

5.4. Comparison with State-of-the-Art

Table 3 compares the performance achieved by the presented APD linearizer with other relevant APD works. Comparing different APD architectures is a difficult task given the multitude of architectures, technologies, and frequencies. Therefore, we identified the fractional bandwidth, small-signal loss, large-signal gain, and phase expansions as the most suitable metrics for this comparison.

Table 3. Comparison with state-of-the-art APD Linearizers

Ref.	Archi.	Nonlinearity Generator	f_0 (GHz)	BW (GHz)	Fractional BW (%)	Small-Signal Gain $\lvert G_{SS}\rvert$ (dB)	Gain Expansion $\lvert\Delta G_{MAX}\rvert$ (dB)	Phase Expansion $\lvert\Delta\Phi_{MAX}\rvert$ (°)
[6]	Single Branch APD	Two Shunt Schottky Diodes	2	0.1	5%	12	5	25
[9]		Single Shunt Diodes	14	0.75	5%	-	4	30
[10]		Two Shunt Schottky Diodes	60	2	3%	16*	8	28
[25]		Shunt Diodes	6	0.4	7%	17	6	20
[26]		Schottky + Varactor Diodes	5	-	-	20*	4	30
[11]	Dual Branch APD	PIN Diodes	30	2	7%	20*	5	23
[13]		Schottky Diode (MMIC)	29	4	14%	14*	8*	40*
[14]		Shunt Schottky Diode	20	2	10%	27*	4*	9*
[28]		GaN Amplifier	0.8	0.2	25%	-	2*	10*
[29]		GaAs Amp. + Diode (MMIC)	26	2	8%	10	4	40
[30]		Schottky Diode	19	3	16%	-	13	50
This		**GaAs Schottky Diode**	**18**	**6**	**33%**	**8**	**3**	**8**

* Value extracted from a plot.

In the first group of the table, single-branch linearizers are compared [6,9,10,27,28]. Single-branch linearizers present a fractional bandwidth of 3-7 % and introduce significant small-signal losses of 12-20 dB, possibly because of the high isolation achieved when the nonlinearity generator is off. However, the large-signal gain and phase expansion is significant and can be up to 8 dB/28° [10]. Such a wide gain expansion is however not necessary in practice as most HPAs will clip after 4-5 dB of compression.

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Dual-branch linearizers provide comparable small- and large-signal losses to the single-branch APDs but present wider fractional bandwidths of 7-25 %. Such wider bandwidth is due to a less stringent trade-off between nonlinearity isolation and small-signal losses [13,15,29–31]. However, the bandwidth of all these linearizers does not exceed 4 GHz.

Our work provides less nonlinear gain and phase expansion than others but achieves significantly wider fractional bandwidths. Achieving higher gain and phase expansions is most of the time unnecessary as typical HPAs are used 3-4 dB into compression and exhibit $\pm 10 - 20^{\circ}$ phase variation (as also the HPA considered here). As it can also be seen in the NPR measurements vs. HPA efficiency/output power of Figure 23, most of the APD benefit is achieved between 5-15 dB in back-off from the P_{1dB} and therefore very high nonlinear gain expansion is most of the time unnecessary. Additionally, the proposed APD provides a significantly lower loss of only 5-6 dB over the whole APD bandwidth, thus requiring less post-amplifier gain or gain stages for lower cost, less power consumption, and easier system integration.

6. Conclusion

This paper presents the theory, design, and application of a dual-branch series-diode analog pre-distortion (APD) linearizer. A new frequency-dependent large-signal APD model is presented and used to study the APD behavior for different phase lengths between the linear and nonlinear branches. This model is used to investigate the impact of different diode parameters on the APD gain and phase characteristics. The APD model is then used to compare different diode models with reference to the inverted HPA gain and phase trajectory. The selected diode is characterized, modeled between 1 to 26.5 GHz, and used for the design APD circuit. After an extensive simulation workflow, a co-simulation of the APD with the measured HPA suggests a gain compression reduction by 4 dB at 19 GHz. Characterization of the fabricated APD reveals a bandwidth of 6 GHz (15-21 GHz) with a gain expansion of 3 dB and a phase rotation of 6°. This APD improves the HPA efficiency by $\sim$5-9 % while boosting output power by $\sim$1-2 W at 19 GHz for this 10W/35% HPA. This efficiency improvement decreases by only 1-2 % when accounting for the power consumption of the APD post-amplifier, thus suggesting overall efficiency and power improvements with APD at K-band frequencies.

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